A fast and low noise charge sensitive preamplifier in 90 nm CMOS technology

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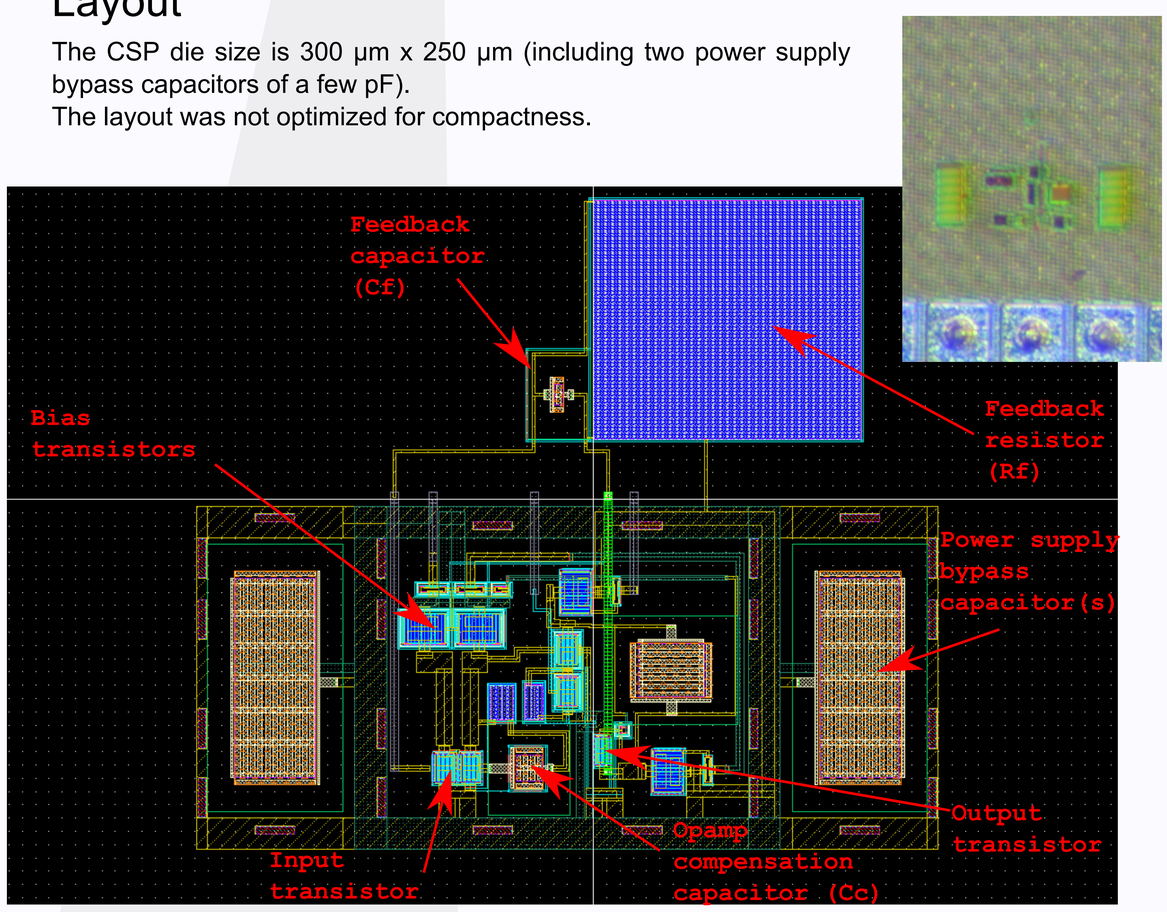
Overview

An integrated charge sensitive preamplifier (CSP) was realized in a TSMC 90 nm CMOS technology. The work is part of the R&D effort towards the read out of pixel sensors in next generation HEP experiments. The CSP was designed to read out pixels of 1 pF capacitance with a signal rise time below 2 ns (requiring a closed loop bandwidth of about 200 MHz) and a noise below 500 electrons RMS. Also larger pixels of up to 5 pF capacitance need to be read out, with a rise time still below 5 ns.

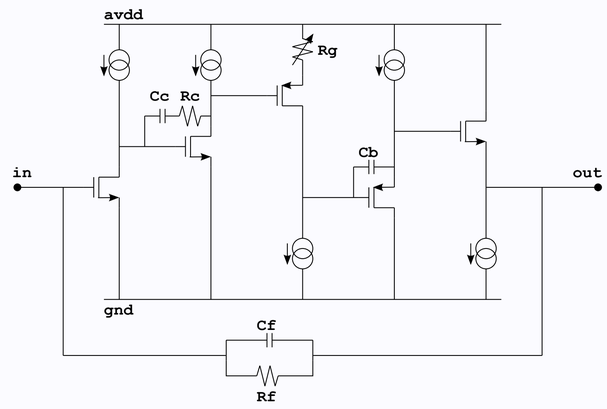
Layout

The CSP die size is 300 µm x 250 µm (including two power supply bypass capacitors of a few pF).
The layout was not optimized for compactness.



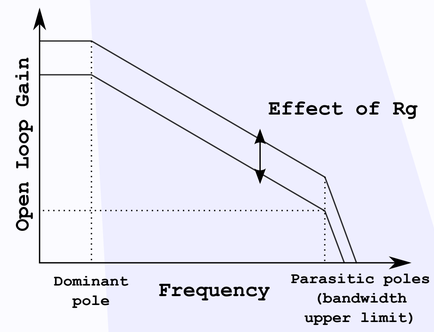
Schematic

The CSP features integrated feedback components Cf = 200 fF and Rf = 500 kΩ.
The single-ended amplifier block has a gain-bandwidth product of about 1 GHz and is stable at a closed loop gain of 5, in order to readout pixels of 1 pF capacitance with a 200 MHz bandwidth.



The charge preamplifier is composed of 5 stages.
The 1st, 2nd and 3rd stages provide gain. The 4th and 5th stages drive the signal to the output.
The 1st and 2nd stages exploit large NMOS transistors to obtain high transconductance (about 10 mA / V).

The 3rd stage is based on a PMOS transistor with a source degeneration resistor Rg. Tuning Rg allows to adjust the gain of the 3rd stage, in order to change the overall open loop gain.
In this way, the gain-bandwidth product can be increased, and detectors of higher capacitance can be read out without the corresponding bandwidth narrowing.

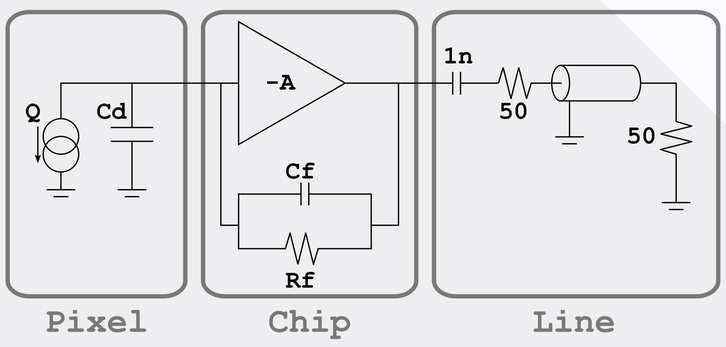


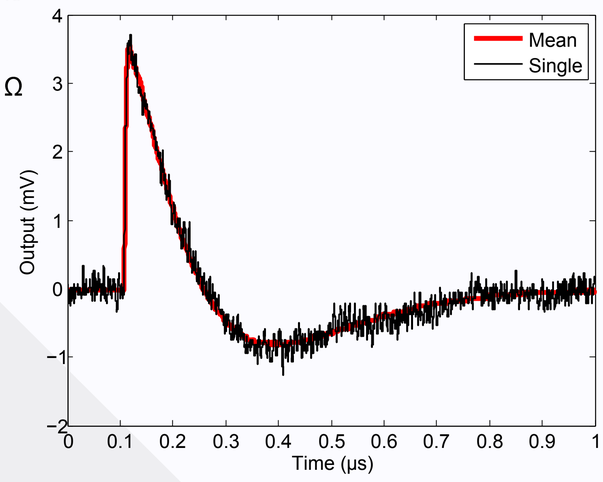
The 4th stage is a DC level shifter: since the PMOS is biased with a very small current, its transconductance is low and all signal passes in the feed-through capacitor Cb.
The 5th stage is a large NMOS, to drive the signal over a 50 Ω transmission line.

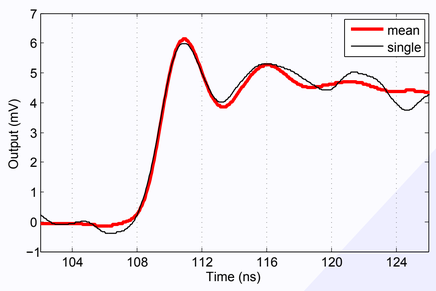
All stages but the 4th are biased with 1 mA. The power supply voltage is 1.2 V.
Power consumption is 5 mW.

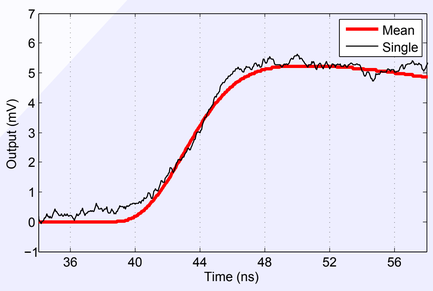
Signals

The response of the prototype to a charge pulse of 15k electrons is shown.
The source simulates a pixel with 1 pF capacitance (Cd).
The signal is acquired at the far end of an AC coupled 50 Ω transmission line.







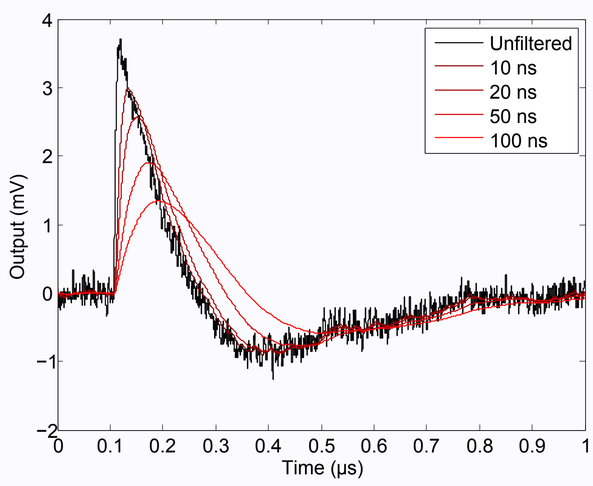


The rise time is limited by bandwidth.
The fastest rise time obtainable is 1.95 ns (10% to 90%), with some ringing, revealing the bandwith limit (up left).
This was obtained with a 1 pF source capacitance.

By tuning Rg to increase the open loop gain, the rise time can still be as fast as 5.5 ns, even with a 5.6 pF source capacitance (up right).

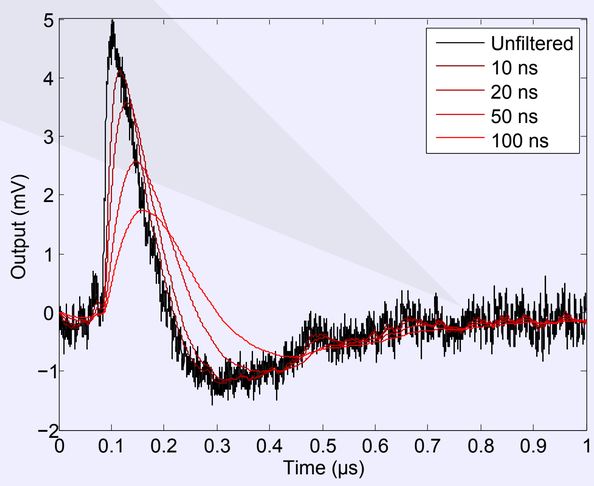
Noise

The equivalent noise charge (ENC) was measured as the RMS baseline fluctuation at the CSP output, divided by the charge gain.
The main source of parallel noise is the feedback resistor, contributing with about 200 electrons RMS, regardless of the pixel capacitance.
The main source of series noise is the the input transistor, with 1 nV / √Hz at high frequency, giving about 100 electrons RMS for pixels of 1 pF capacitance, directly proportional to the pixel capacitance.
To a first order approximation, the 1/f noise components do not contribute, because the signal is AC coupled at the output with a high pass at about 1 MHz.
By applying an offline RC filter with varying filter time constants up to 100 ns the series noise contribution could be reduced.



ENC (electrons RMS) with 1 pF pixels

Unfiltered	377 e
10 ns	226 e
20 ns	206 e
50 ns	196 e
100 ns	186 e



ENC (electrons RMS) with 5.6 pF pixels

Unfiltered	588 e
10 ns	503 e
20 ns	398 e
50 ns	300 e
100 ns	260 e

Conclusions

The chip performs well in terms of bandwidth and noise, meeting the design specifications.
The adopted 90 nm CMOS technology allows to achieve very high transconductance thanks to increased scaling. Low series noise can be obtained, although at the price of fairly high power consumption in the 1st stage. Some power could be saved in the output stage if the 50 Ω line drive capability is not required. The value of the feedback resistor could be increased to reduce the parallel noise.
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