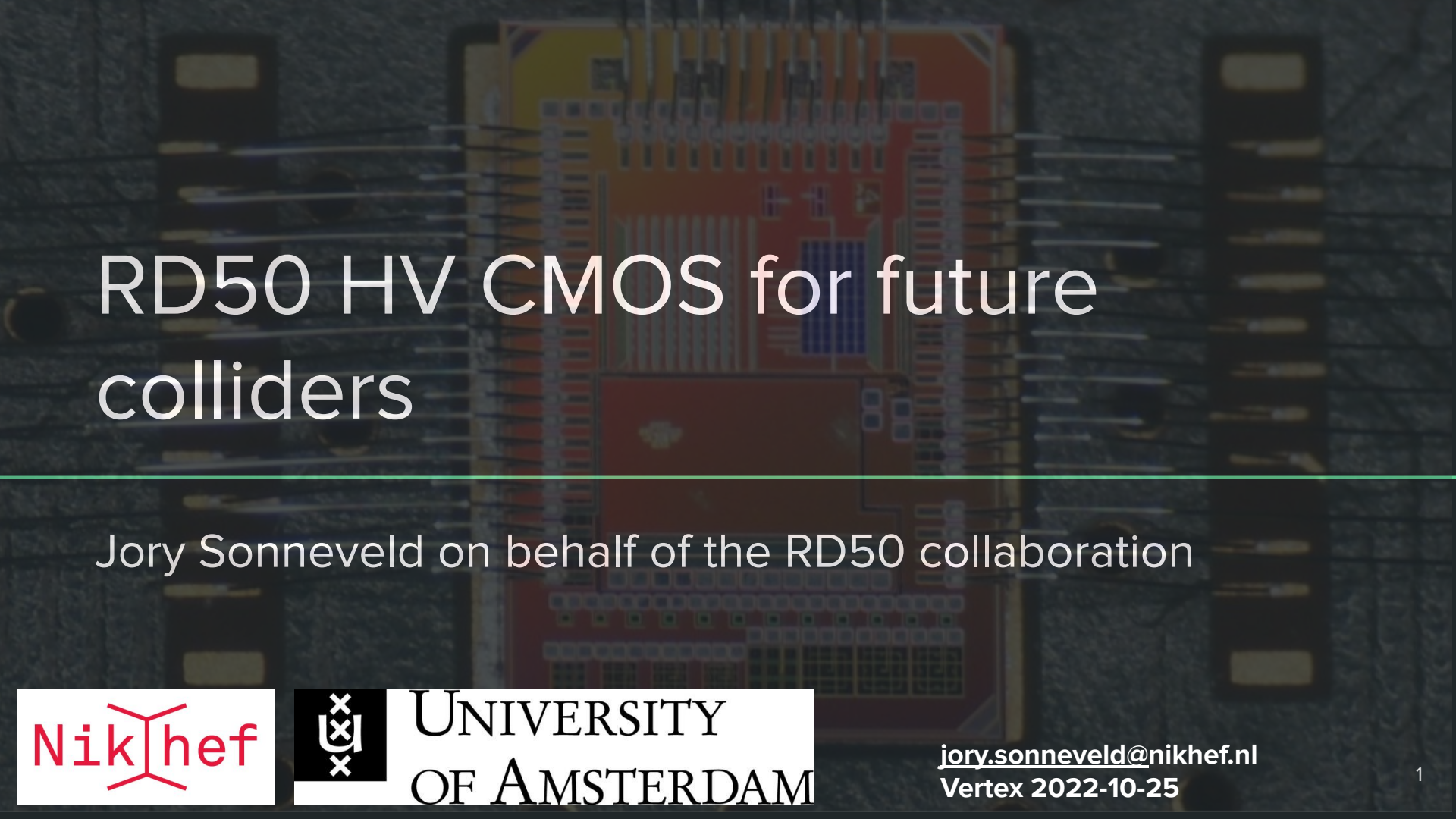


RD50 HV CMOS for future colliders

Jory Sonneveld on behalf of the RD50 collaboration

Nikhef

UNIVERSITY OF AMSTERDAM

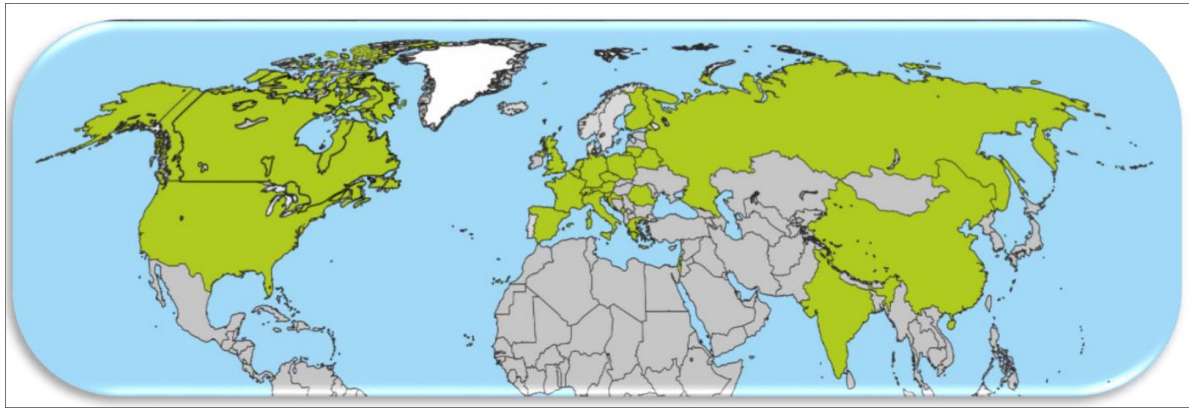
jory.sonneveld@nikhef.nl

Vertex 2022-10-25

RD50 collaboration

https://rd50.web.cern.ch

- Radiation hard semiconductor devices for very high luminosity colliders
- 66 institutes and 430 members (see full list at RD50 website)
- Detectors will face $\Phi_{eq} > 10^{16}/cm^2$ (HL-LHC) and $\Phi_{eq} = 10^{17}/cm^2$ (FCC-hh)



Work program as shown in RD50 status report in LHCC meeting https://indico.cern.ch/event/1192325 :

- Defect and Material Characterization
- Detector Characterization
- New Structures
- Full Detector Systems

New structures: RD50 HV CMOS working group

17 institutes working on:

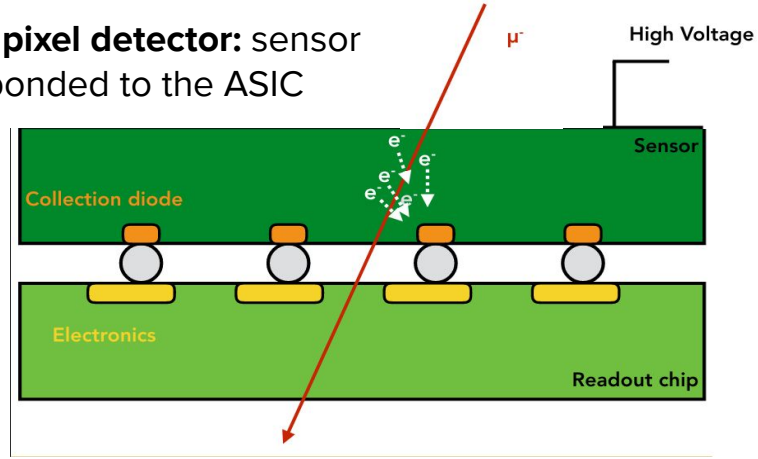
- ASIC design
- TCAD simulations
- DAQ development
- Chip performance evaluation

Why monolithic active pixel sensors?

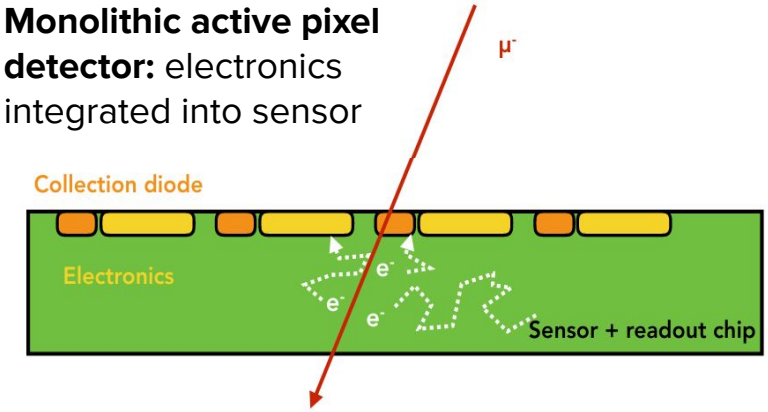
✅ Electronics integrated into the sensor: low mass, no bump bonding
✅ Widely used in digital cameras (like your phone!)

Downside: less room for per pixel functionalities

Hybrid pixel detector: sensor bump bonded to the ASIC



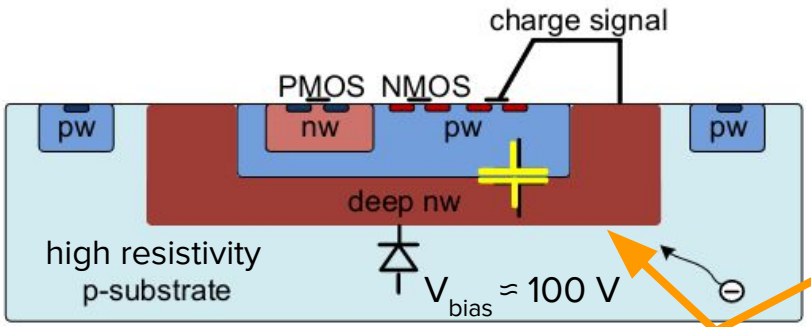
Monolithic active pixel detector: electronics integrated into sensor



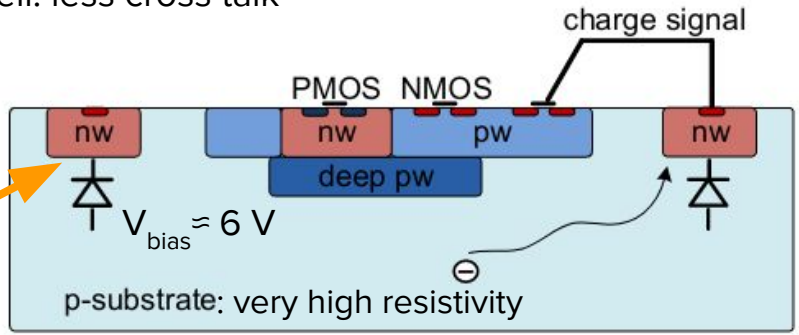
Figures from D. Hynds at CLIC workshop https://indico.cern.ch/event/577810

Depleted MAPS: small and large collection electrodes

✅ High field almost everywhere
✅ Short drift distances
✅ Higher radiation tolerance



✅ Very small sensor capacitance ~5 fF
✅ Reduced noise & power
✅ Readout outside charge collection well: less cross talk



pn-junction

From Norbert Wermes, Trento2020

- Stronger electric field results in less trapping and higher radiation tolerance
- Larger electric field comes at a cost: more capacitance, power and more noise

From E. Vilella, Vertex2018

Radiation hard depleted MAPS

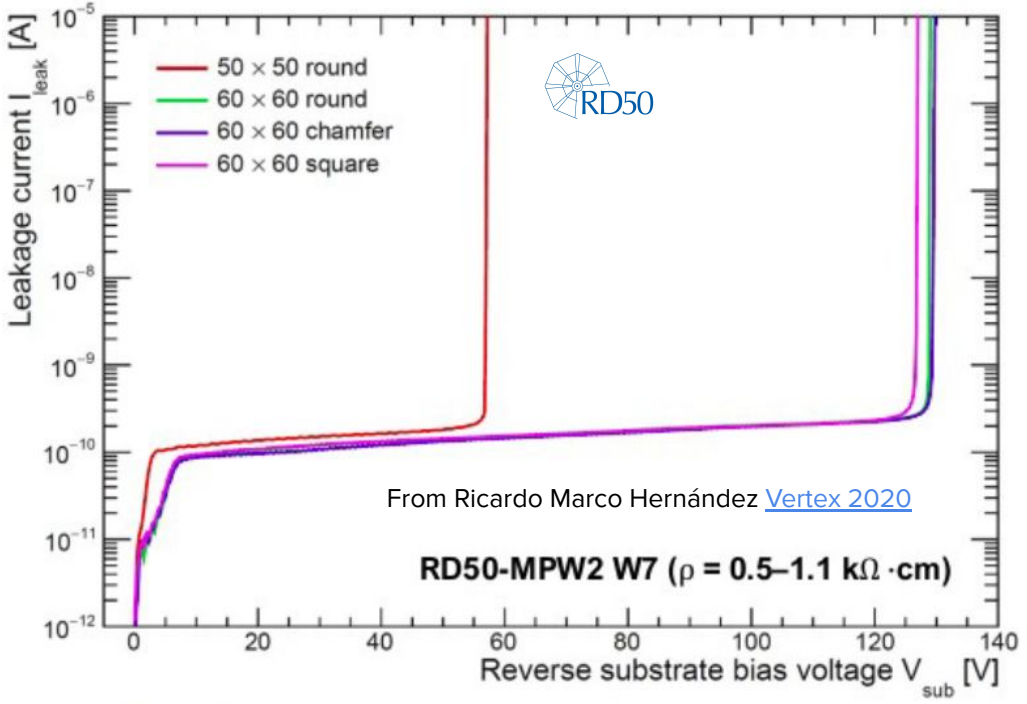
HV CMOS with a **larger collection electrode**:

- **fast collection time**
- **radiation tolerant**
- high breakdown voltage

Ongoing development in HEP

Currently achieved in HV CMOS:

- $\Phi_{eq} = 10^{15}/cm^2$ [1]
- 100 ps time resolution [2] – in HV-HR CMOS even 10s of picoseconds! [3]
- Breakdown voltage only at over 400 V [4]



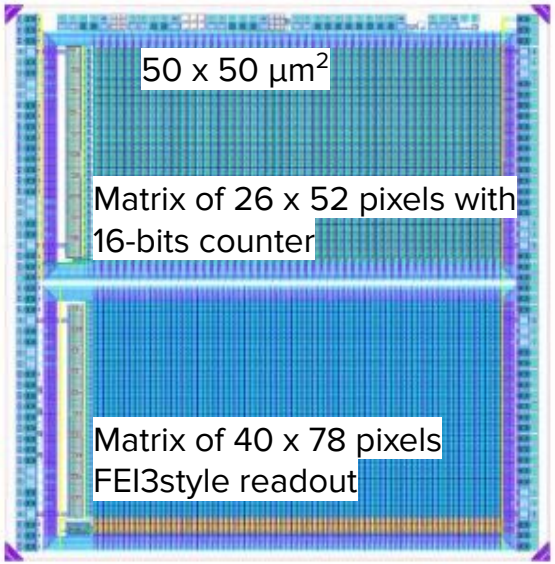
Higher breakdown voltage achieved with

- more electrode spacing
- rounded pixel corners

[1] https://doi.org/10.1016/j.nima.2020.164460
[2] https://doi.org/10.1088/1748-0221/15/06/P06011
[3] https://doi.org/10.48550/arXiv.2208.11019
[4] https://indico.cern.ch/event/1104064/contributions/4786211/

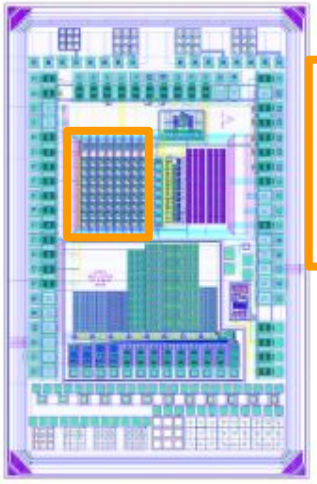
Three submissions of RD50 HV CMOS monolithic sensors

RD50-MPW1
5 x 5 mm² **2017**



Low breakdown V_{bd} ≃ 60 V
High leakage current
I_{leak} ~µA

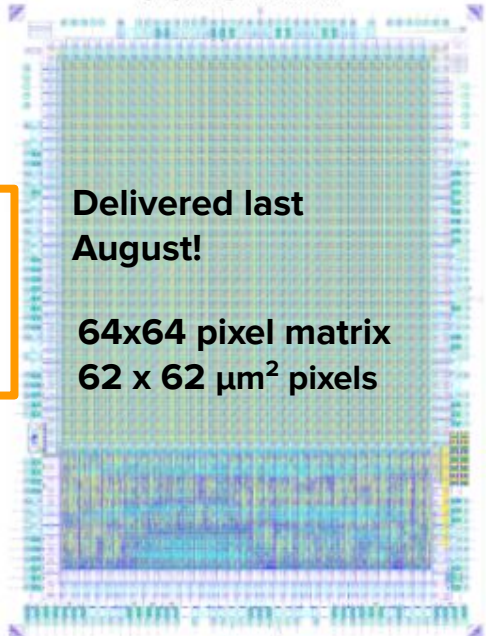
RD50-MPW2
3.2 x 2.1 mm²
2019



Small 8x8 matrix
60 x 60 µm² pixels

High breakdown V_{bd} ≃ 120V
Low leakage current I_{leak} ~nA
Analog readout only

RD50-MPW3
6.6 x 5.1 mm² **2021**



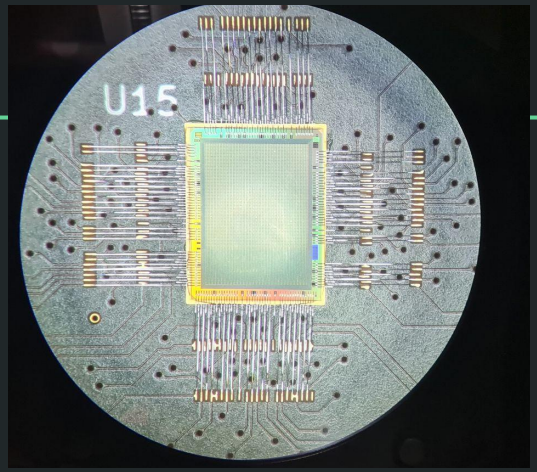
Delivered last August!

64x64 pixel matrix
62 x 62 µm² pixels

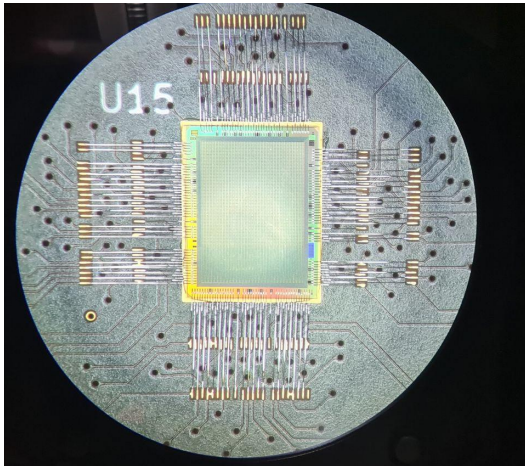
In-pixel digital readout
Advanced peripheral readout

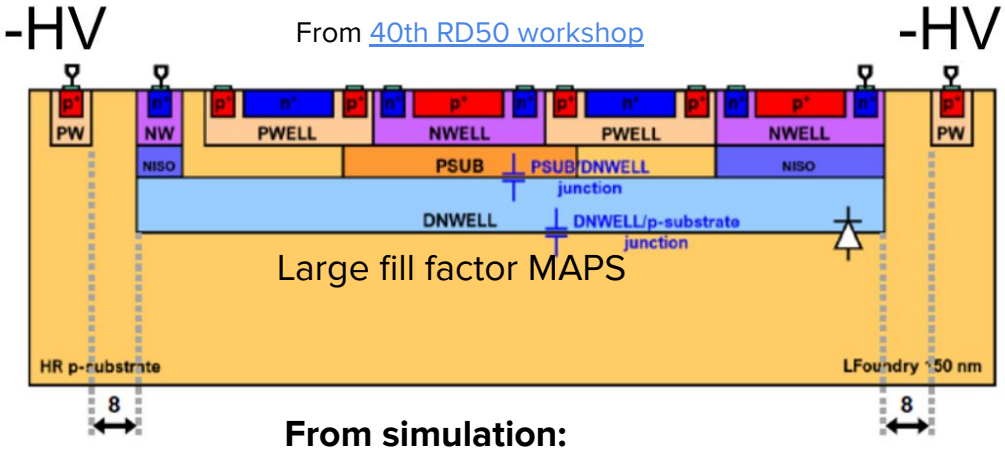
Image from 40th RD50 workshop https://indico.cern.ch/event/1157463

Latest RD50 HV CMOS submission



RD50 HV CMOS monolithic sensors: newest version





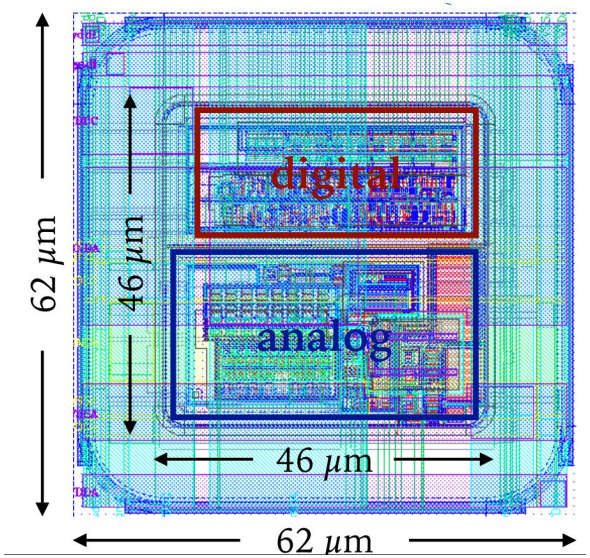
Latest version now in our laboratories:

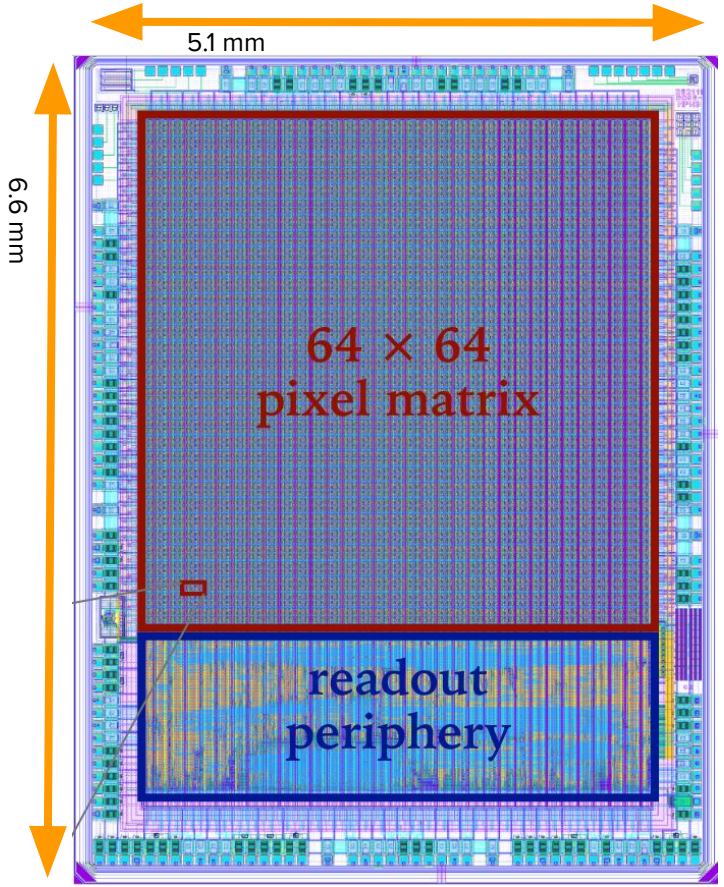
- LF15A process from LFoundry in 150 nm HV-CMOS
- High resistivities: 1.9 kOhm·cm, 3 kOhm·cm (nominal)
- High voltage applied from the top
- Analog and digital electronics inside the collection electrode of 55% pixel area

From simulation:

Pixel size	62 μm × 62 μm
Cd	~ 250 fF
Power	22 μW/pixel (VDD = 1.8 V)
Gain	230 mV (for 5 ke$^-$)
ToT	55 ns (for 5 ke$^-$)
ENC	120 e$^-$
Time walk	9 ns

Layout of latest RD50 HV CMOS



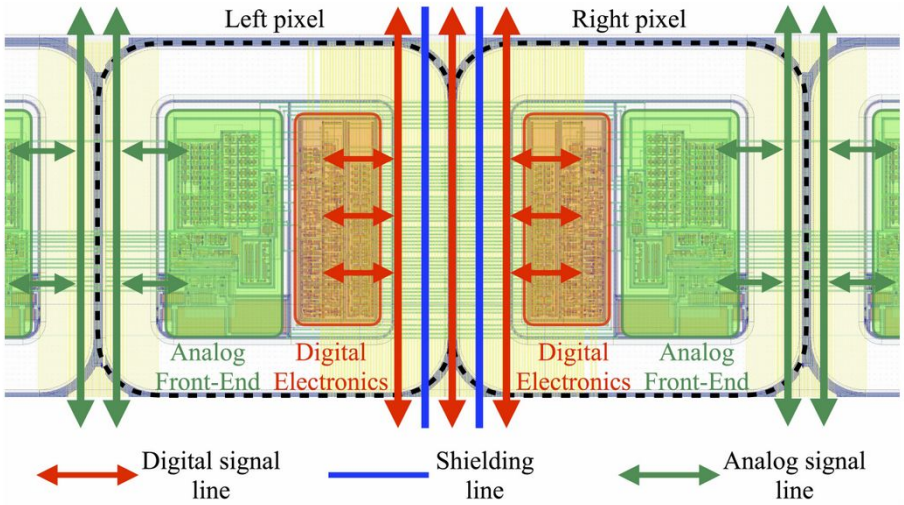


- Analog and digital circuits in separate deep p-wells with different signal lines to minimize crosstalk
- Advanced readout periphery with 640 Mb/s serializer
- FEI3-style readout design

From 40th RD50 workshop

Separation of analog and digital

- Digital signal lines are placed in the middle of each double column
  - Analog lines between double columns
  - Grounded shielding lines between digital signal
- Power grid to minimize voltage drop



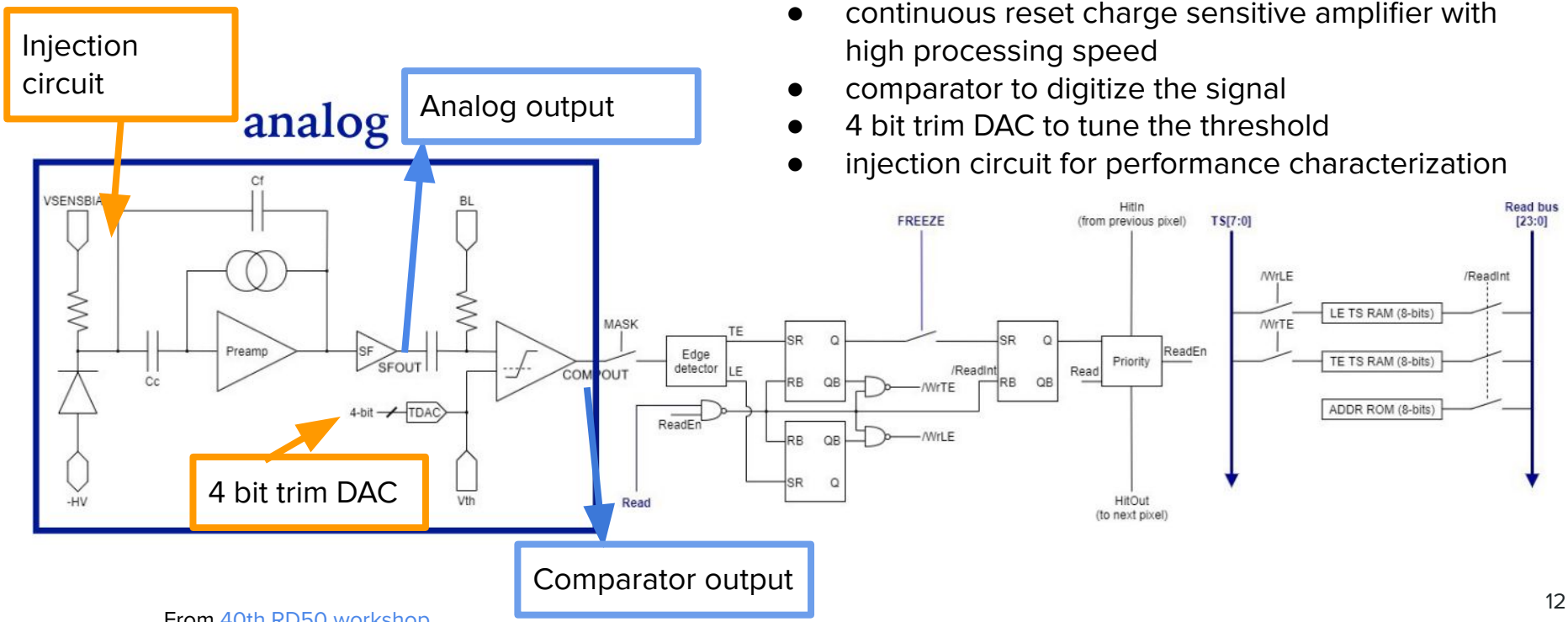
2 pixels

From [40th RD50 workshop]

Analog frontend of the latest HV CMOS sensor

Each pixel has a

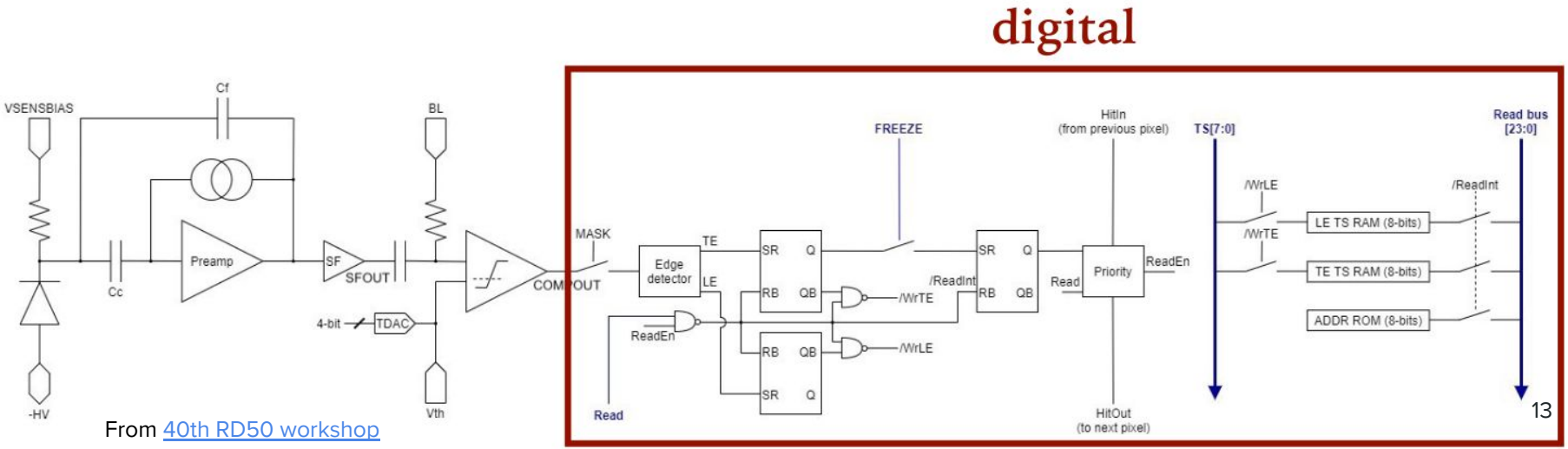
- continuous reset charge sensitive amplifier with high processing speed
- comparator to digitize the signal
- 4 bit trim DAC to tune the threshold
- injection circuit for performance characterization



From [40th RD50 workshop]

Digital frontend of the latest HV CMOS sensor

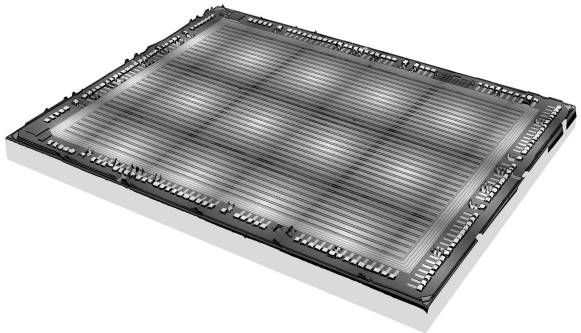
- In-pixel digital readout with double column drain readout and rolling shutter
- Time of arrival and time over threshold are recorded
- Two timestamps in 8-bit RAMs sent out with an 8-bit pixel address via shared readout bus

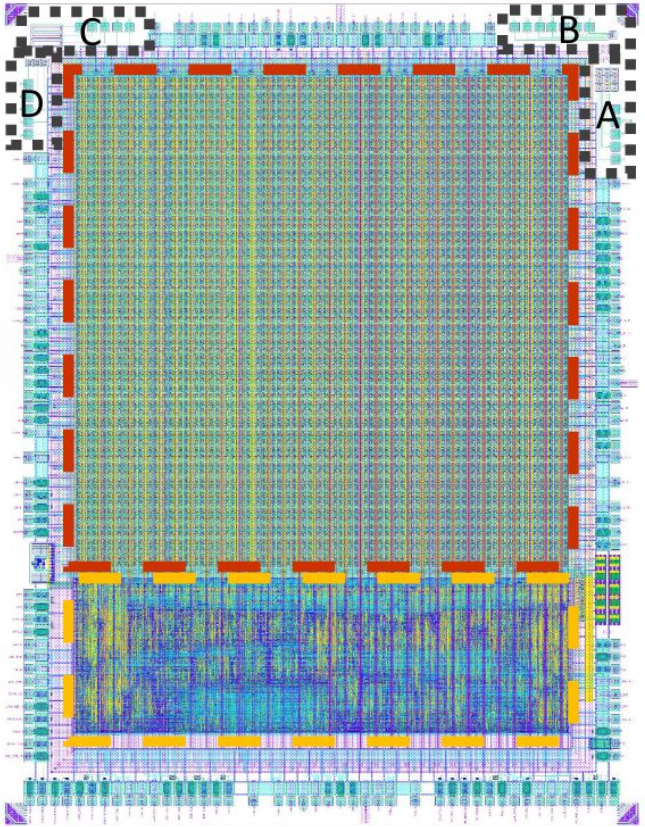


From [40th RD50 workshop]

Advanced test structures for characterization

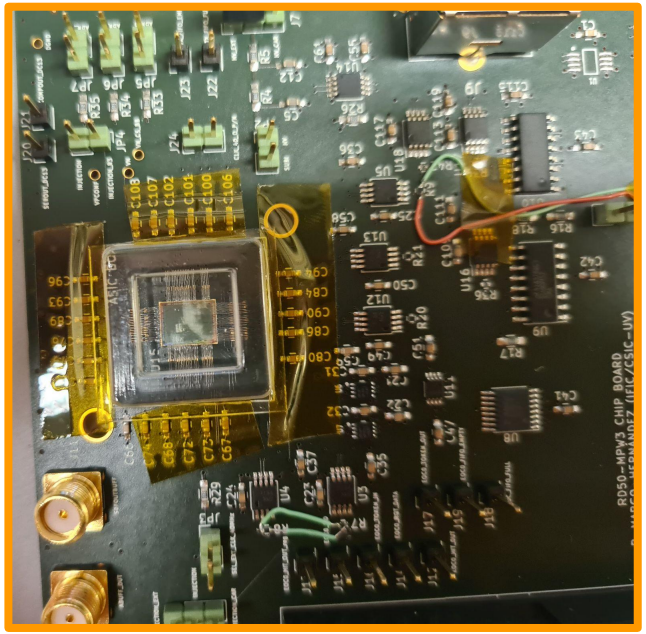
A edge-TCT: 3x3 pixel matrix for timing and charge measurements
B capacitance: single sensing diode for measuring capacitance of a single pixel
C + D thermally stimulated current: for defect characterization



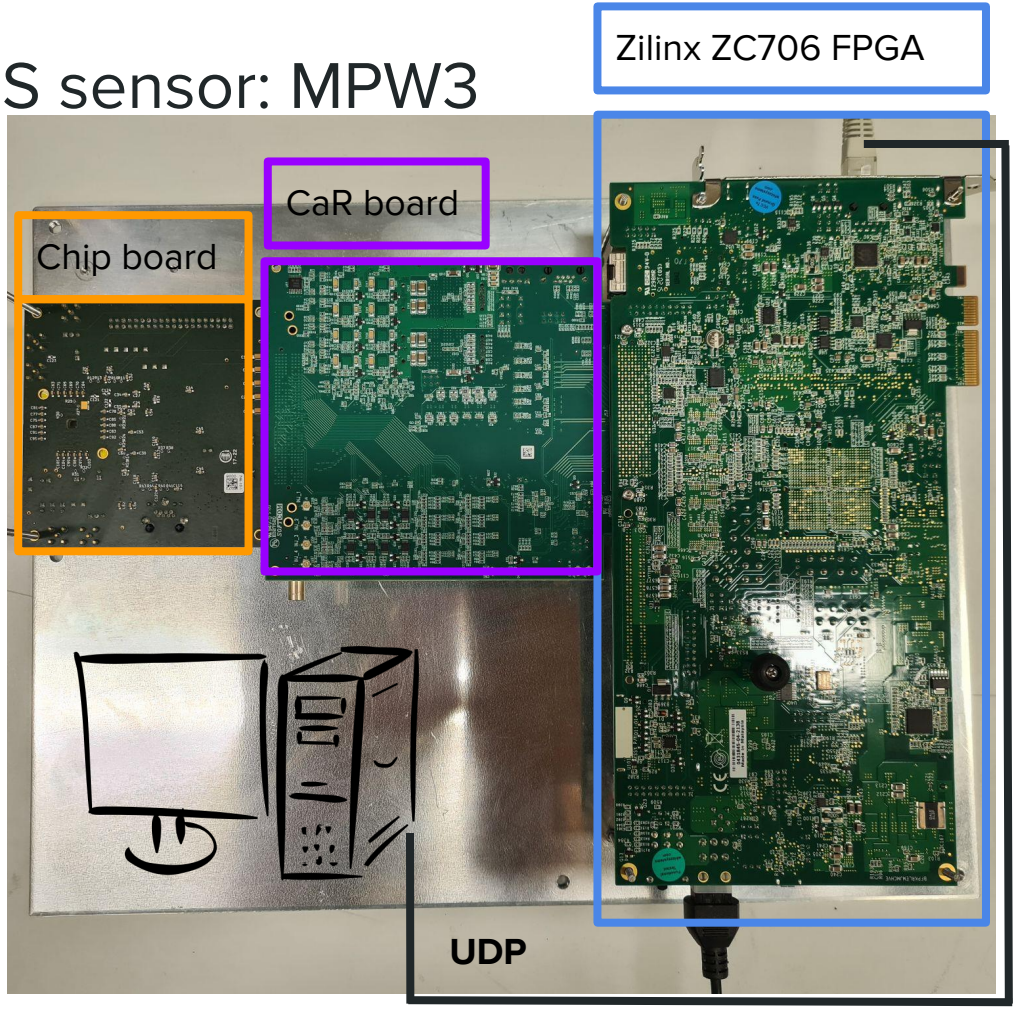


From TWEPP 2022

Setup of RD50 HV CMOS sensor: MPW3



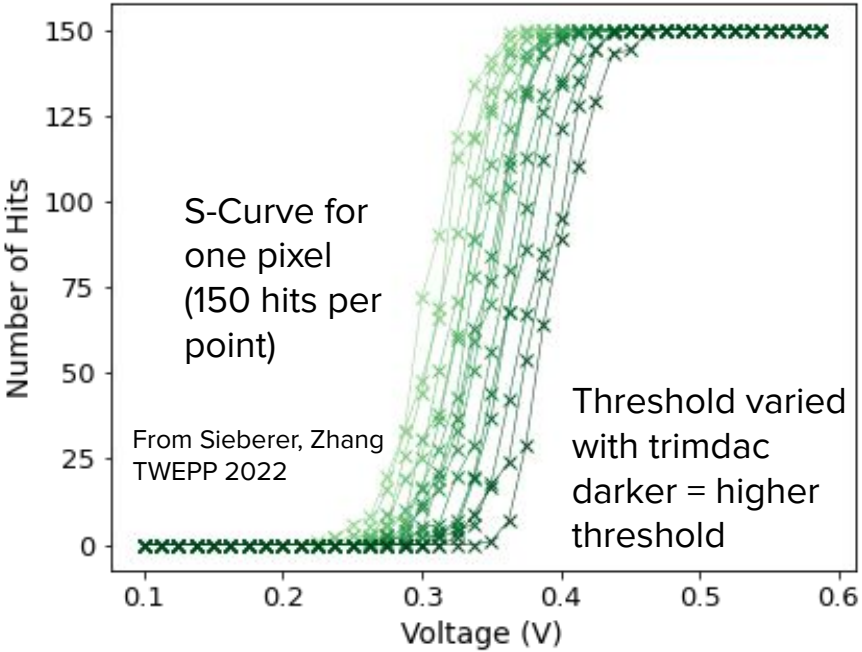
- Caribou used for DAQ
- Can add 2nd chip on top of chip board

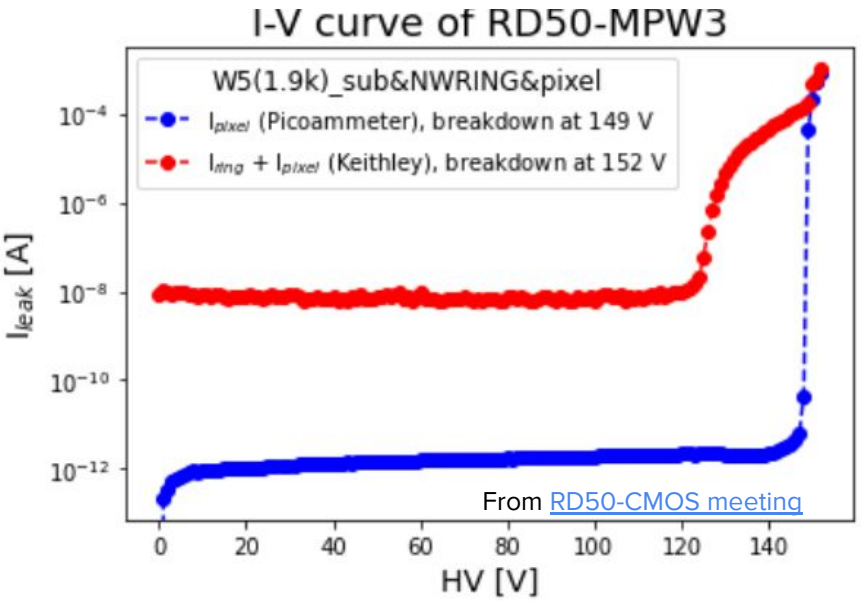


First results of latest RD50 HV CMOS sensor

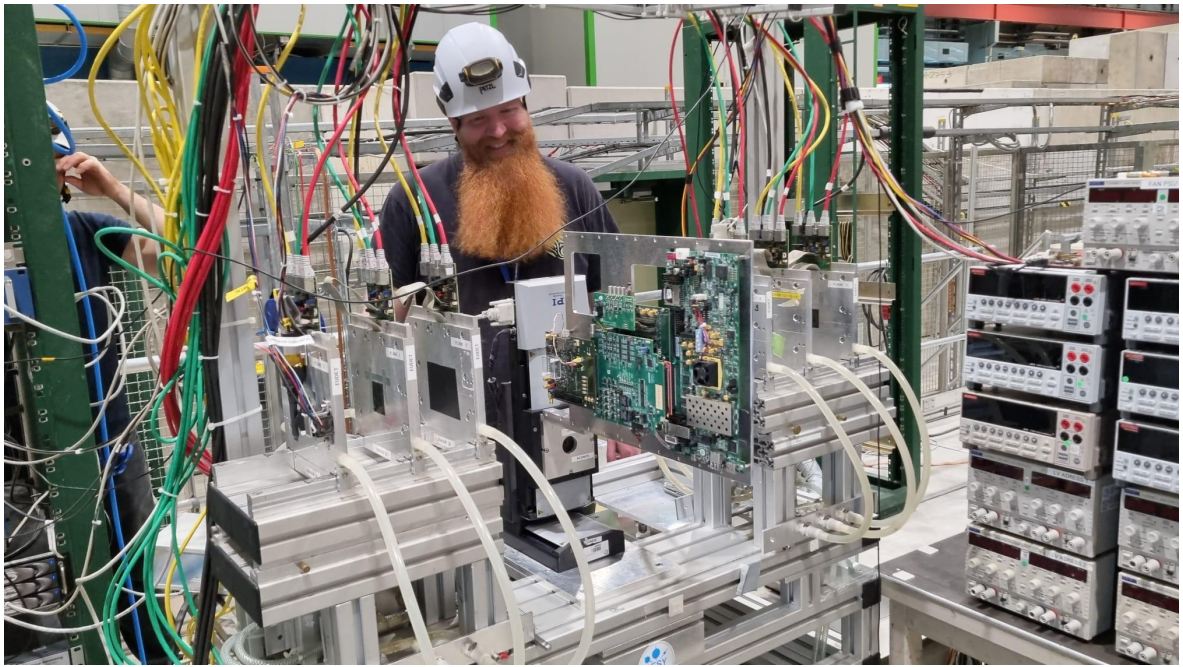
non-irradiated

- Pixel thresholds behave as expected
- Breakdown around 150 V with a per-pixel current of only 1 pA
- N-well ring for routing away most of the pixel leakage current



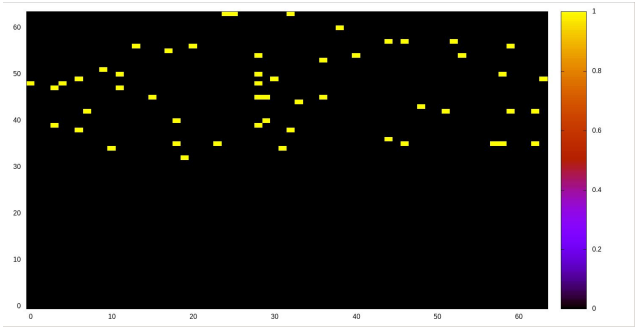


Test beam ongoing **now** at CERN



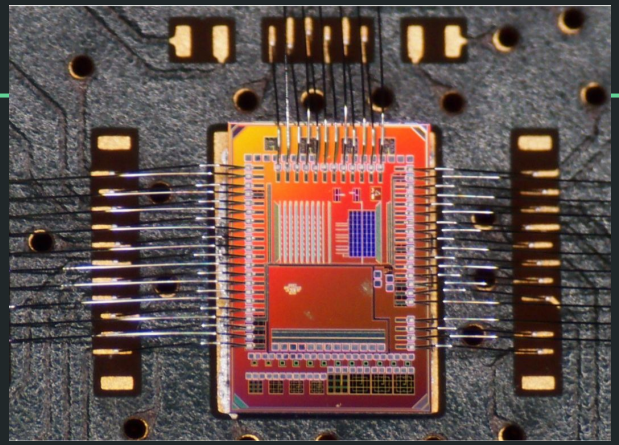
AIDA telescope with AIDA TLU trigger, FEI4 reference plane, and Timepix 3 plane in EUDAQ

CERN SPS:
120 GeV hadrons



- First beam test with large pixel matrix prototype
- Multichannel readout will allow for tracking and efficiency measurements
- Added Timepix 3 plane for measurement of time resolution

Performance of previous RD50 HV CMOS submission



Previous submission of RD50 HV CMOS

Multiproject wafer #2 (MPW2)

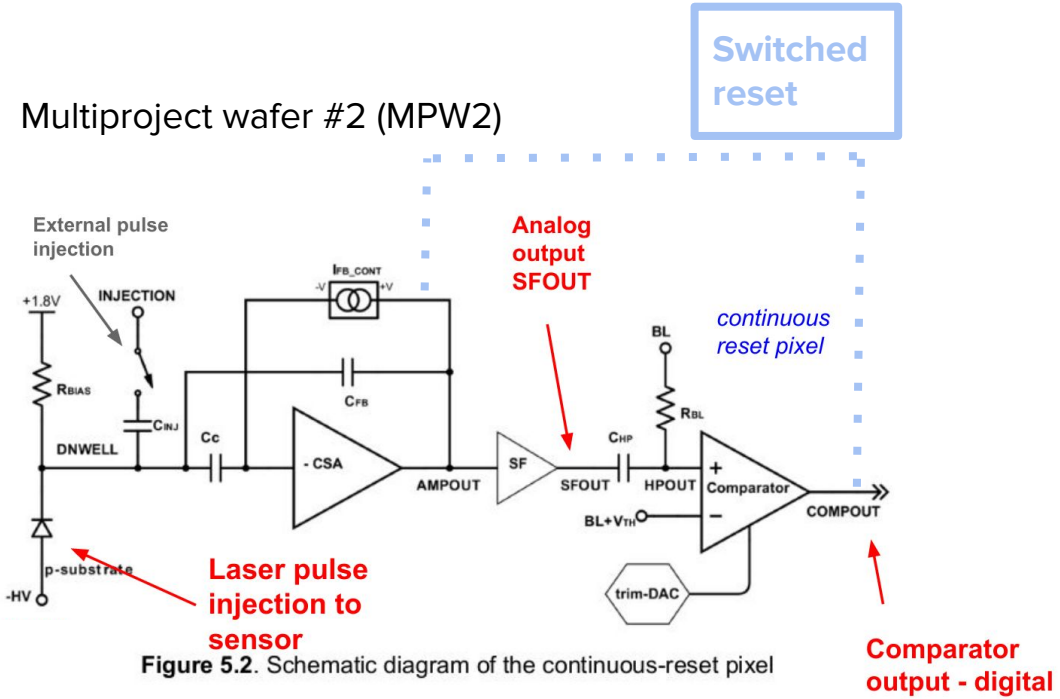
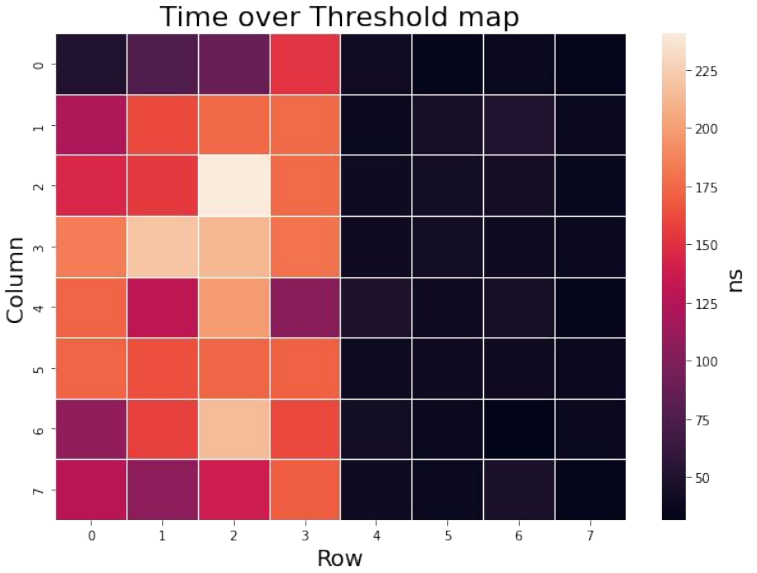


Figure 5.2. Schematic diagram of the continuous-reset pixel



continuous switched

- Continuous reset ToT scales with signal size
- Switched reset much faster reset

Performance of the RD50 depleted CMOS sensors

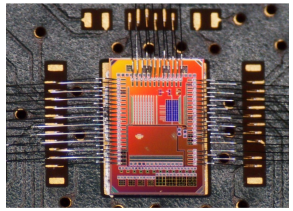
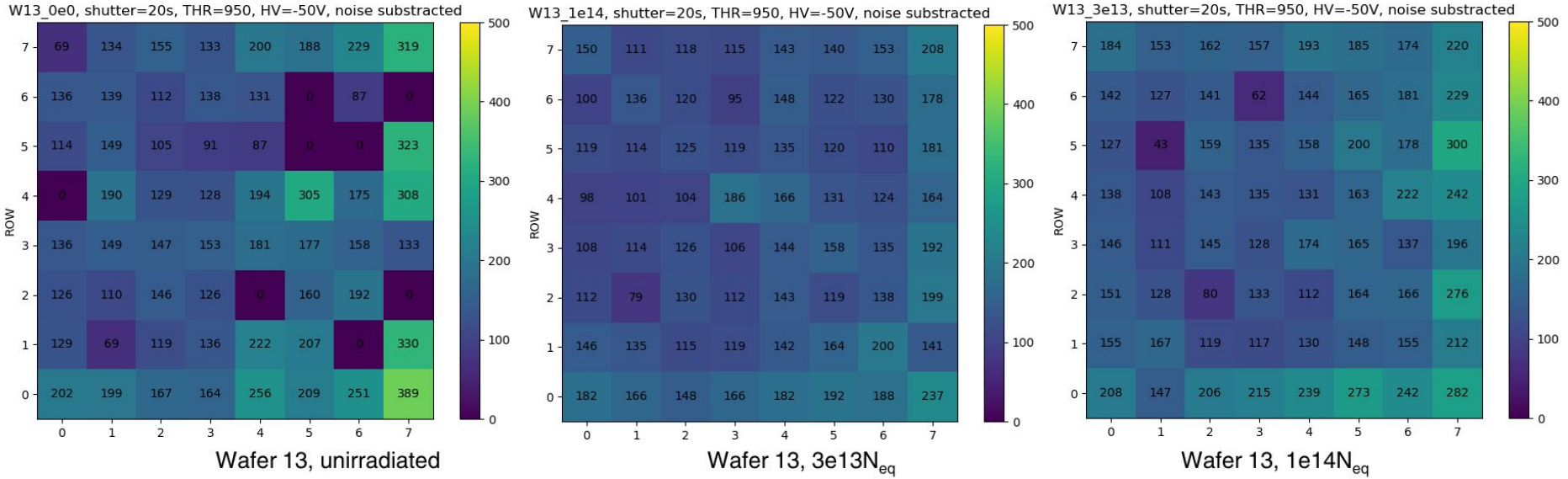


Image from 38th RD50 workshop

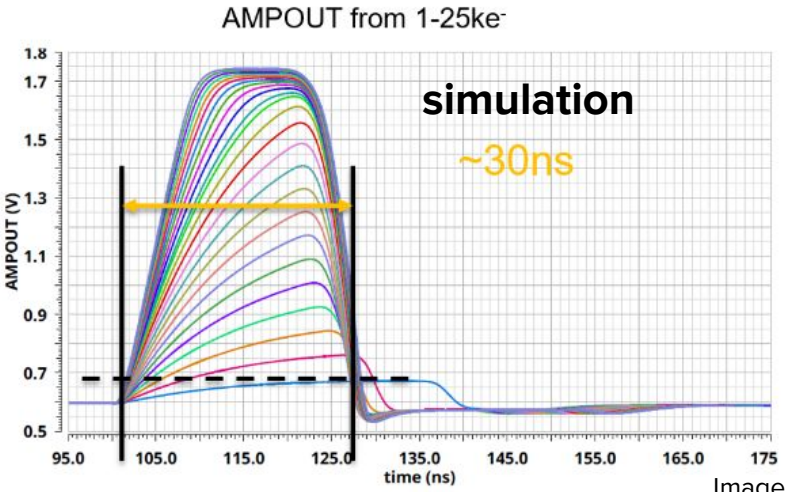


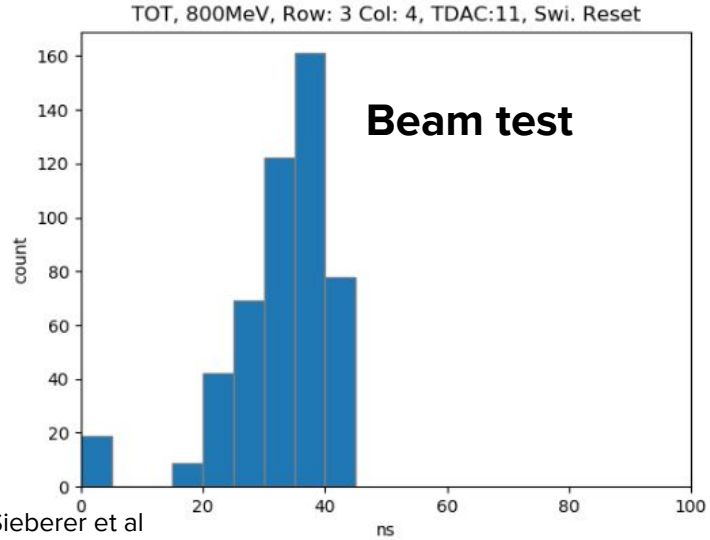
- Measurement with a strontium source: functional after irradiation of $\Phi_{eq}=1{\cdot}10^{14}/cm^2$
- Breakdown voltage over 120 V [1]
- 280 µm thick sensor, at least 100 µm depletion [2] for 100 V bias

[1] Vertex 2020
[2] doi:10.1088/1748-0221/16/12/P12020

Measurement in beam test

- 252.7 MeV proton beam at MedAustron
- 30 kHz event rate
- ToT measurement peaks at 35 ns as expected from simulation
- Readout of 1 pixel at a time: multi-pixel readout in latest chip submission





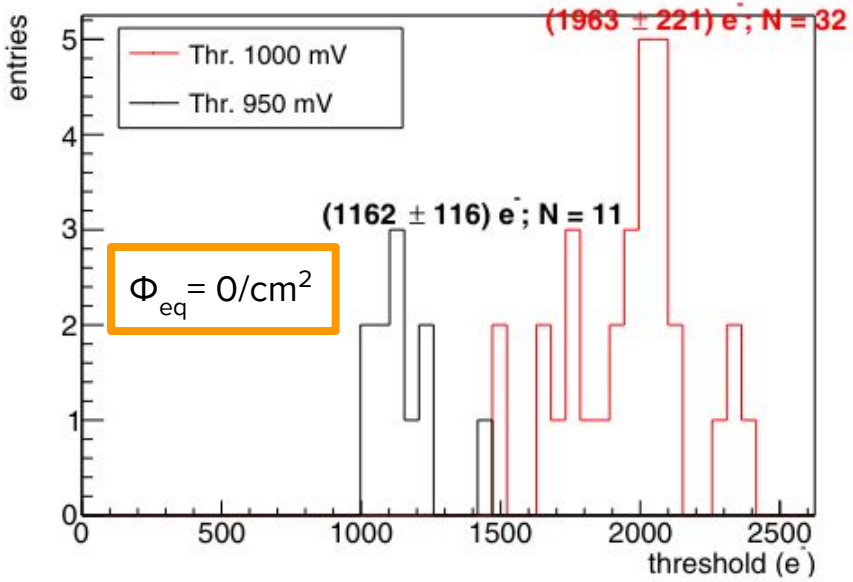
https://doi.org/10.1016/j.nima.2022.167020

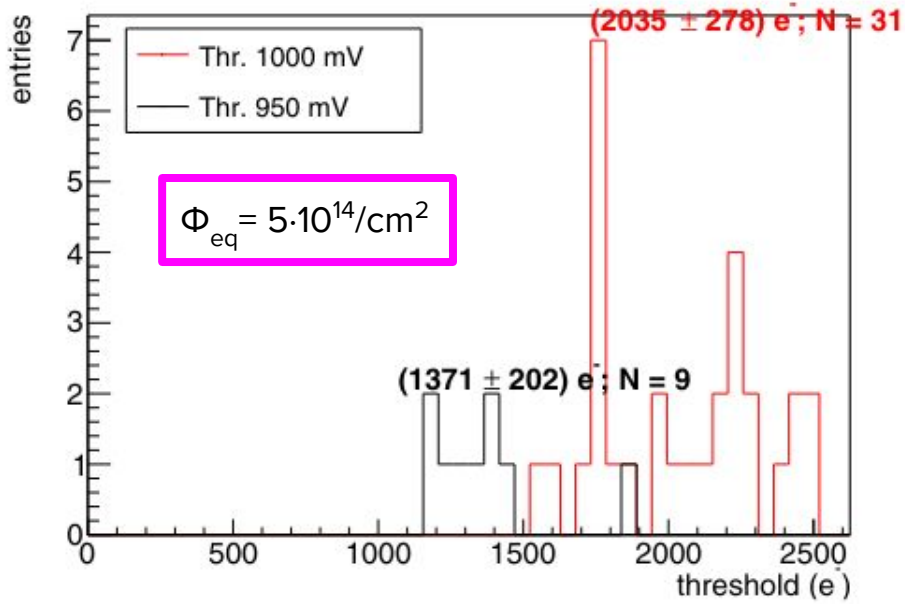
Image from Sieberer et al
https://doi.org/10.48550/arXiv.2201.08585

Performance of previous HV CMOS sensor after irradiation

Threshold for q = $C_{inj}U$ with C_{inj} = 2.8 fF

Total inonizing dose of 5 kGy



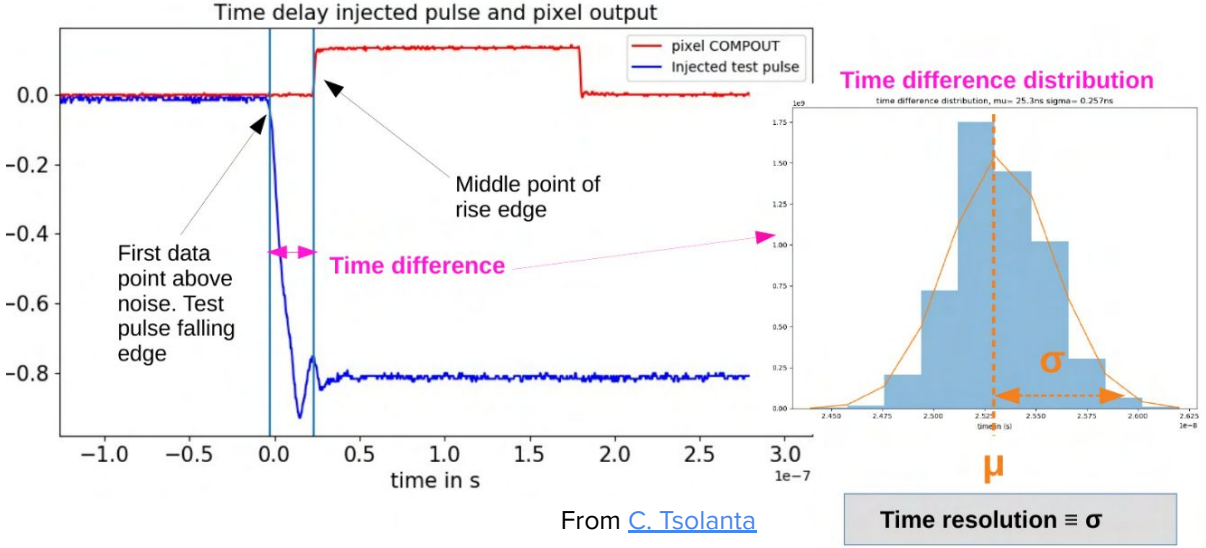


From B. Hiti et. al https://doi.org/10.1088/1748-0221/16/12/P12020

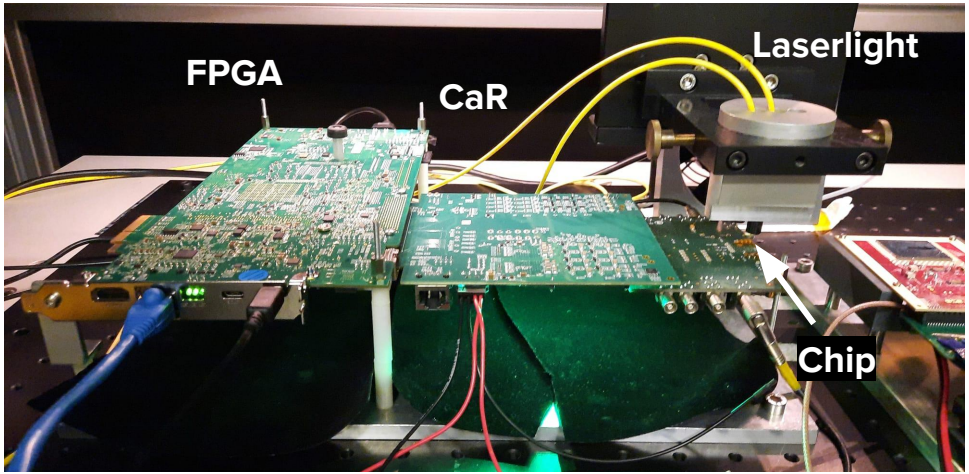
- Threshold change is minimal after irradiation
- Noise similarly does not vary with irradiation and stays under 200 e^-

Time resolution

- With a single photon absorption laser, inject a test pulse with various intensities
- With a radioactive source, measure difference in time of arrival with LGAD



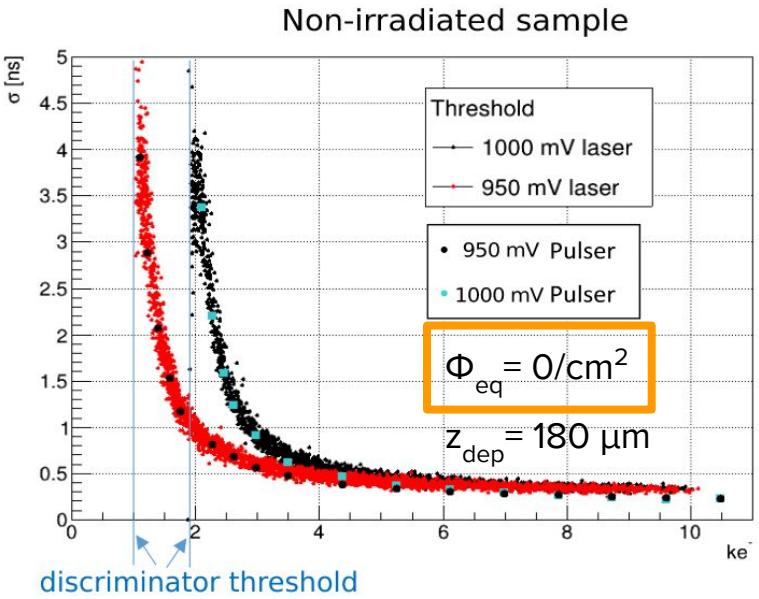
From C. Tsolanta

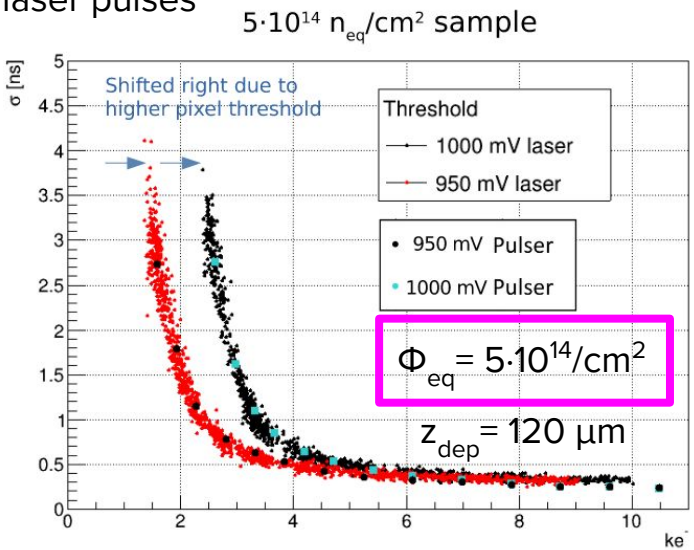


The spread in the time difference between the pulse sent to the laser and the comparator output from the chip gives the time resolution

Time resolution of previous RD50 HV CMOS chip

Resistivity 1.9 kΩ·cm
1064 nm IR laser pulses
100 V bias



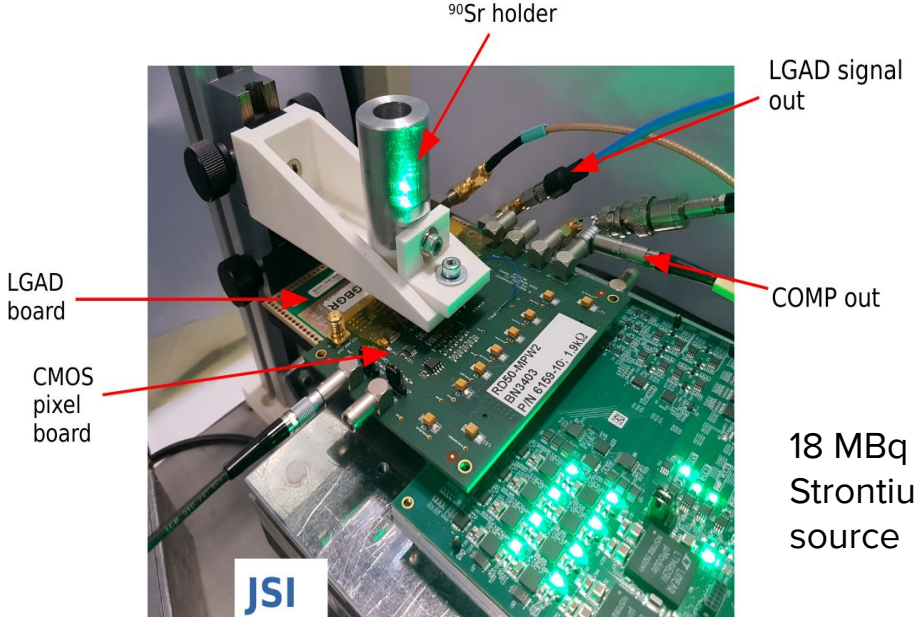


From 40th RD50 workshop

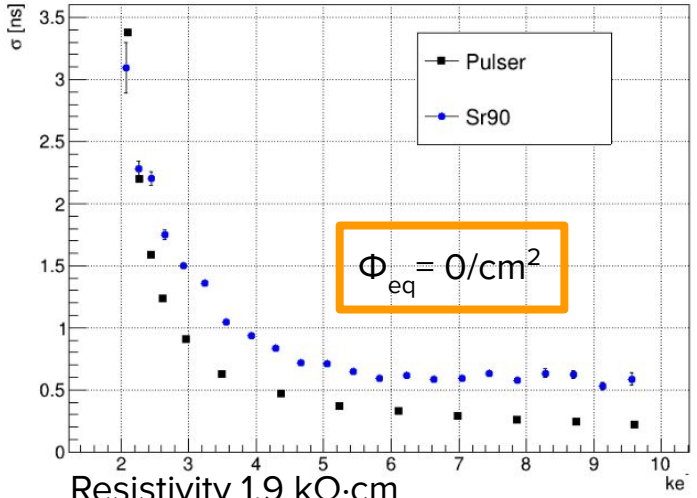
- For higher threshold a higher charge is needed for the same time resolution
- Time resolution behaves asymptotically towards higher injected charges
- After $\Phi_{eq} = 5 \cdot 10^{14}/cm^2$ irradiation the time resolution still is 300 ps for a minimum ionizing particle

Time resolution with source

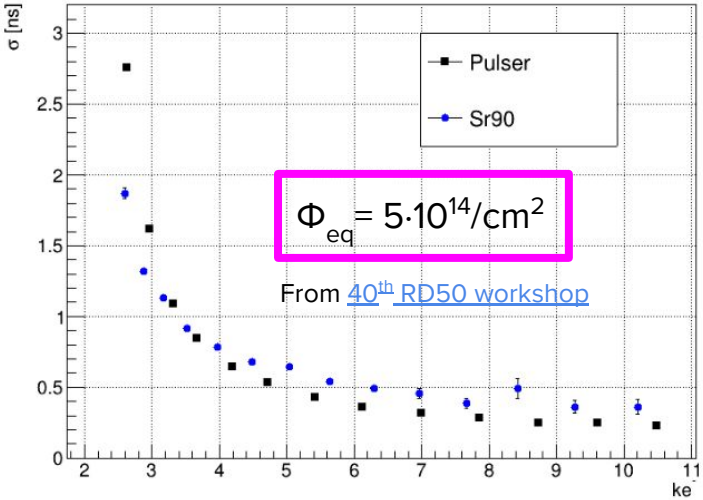
- Time resolution worse in unirradiated sample: around 600 ps vs 350 ps
- Diffusion dominates more before irradiation: after trapping of diffused charges occurs



18 MBq Strontium source

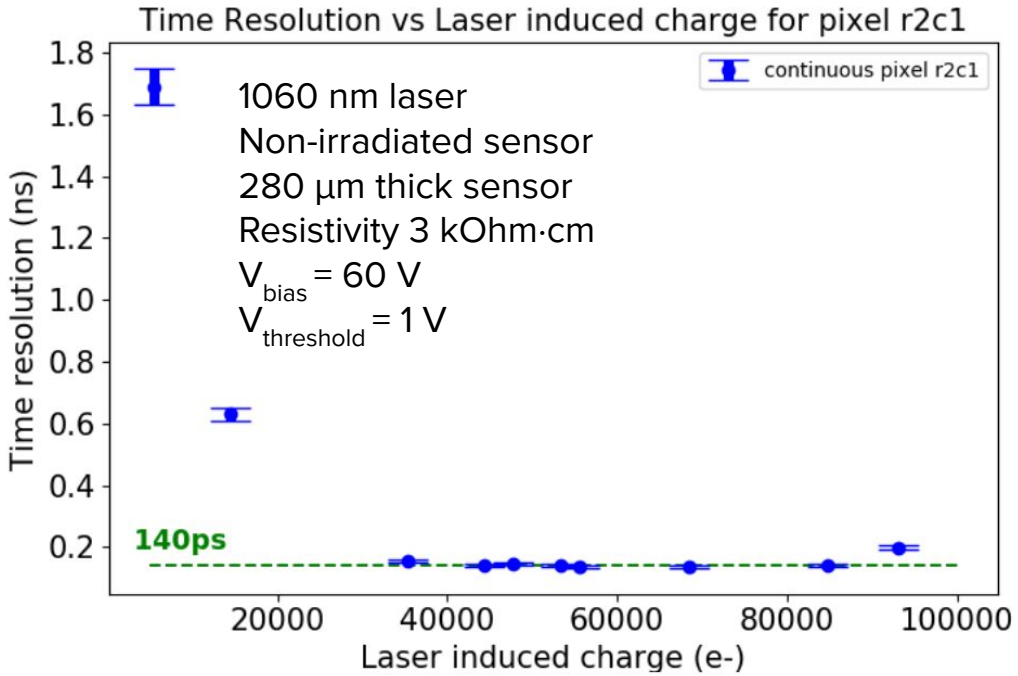


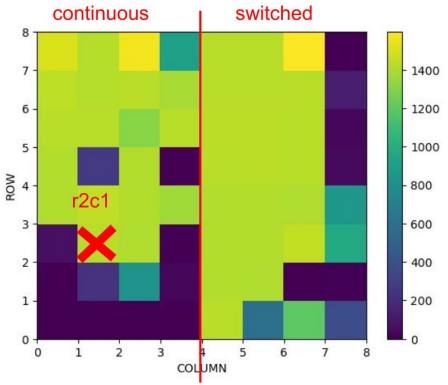
Resistivity 1.9 kΩ·cm
100 V bias



From 40th RD50 workshop

Time resolution of RD50 HV CMOS monolithic sensors



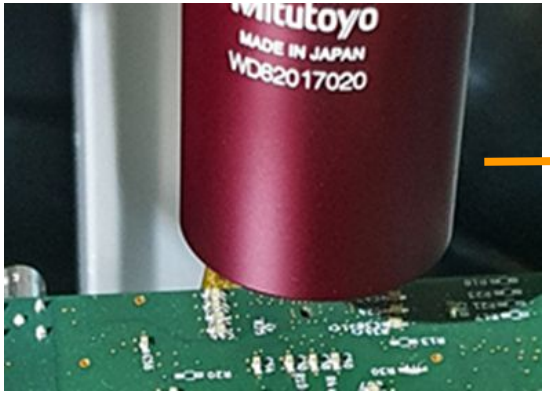


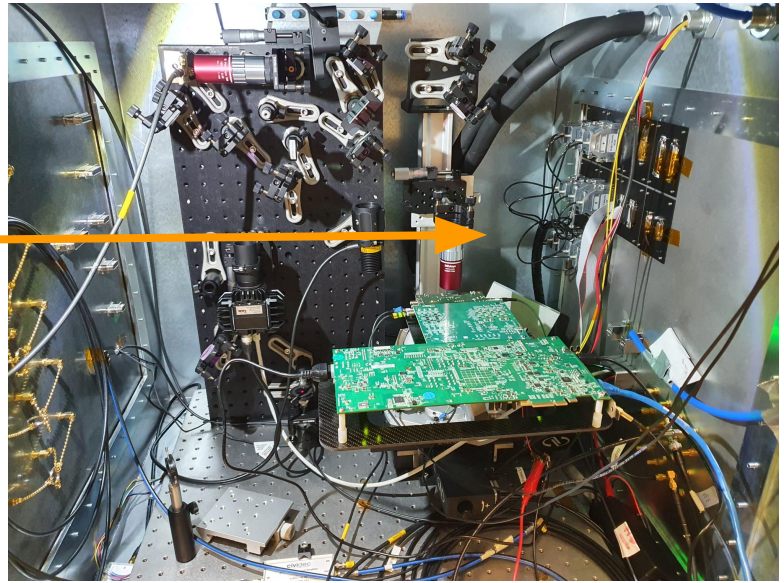
- For larger injected charge can reach 140 ps
- For a MIP-like particle time resolution is worse

From C. Tsolanta
https://scripties.uba.uva.nl/search?id=record_50779

Two photon absorption laser

Francisco Rogelio Palomo Pinto[a], Sebastian Pape[b,c], Michael Moll[b], J.María Hinojo Montero[a]
[a] Electronic Engineering Department of School for Engineering in University of Seville, Spain
[b] EP-DT CERN, [c] TU Dortmund University





At the CERN Solid State Detector lab:

- 1550 nm two-photon absorption laser
- ~400 fs
- 8.2 MHz frequency
- acousto-optic modulator to select 1 kHz
- Single shots: 1 pulse hits sensor in its response time
- Variable Z focus
- hexapod for XY
- Electromagnetic interference isolated

- 3D imaging of semiconductors
- Available in 5 HEP institutes: CERN (CH), JSI Ljubljana(SI), IFCA (ES), NIKHEF(NL), Lancaster (UK)

From RD50 CMOS meeting
https://indico.cern.ch/event/1184355/contributions/4976091/

Imaging with two photon absorption laser

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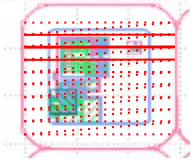
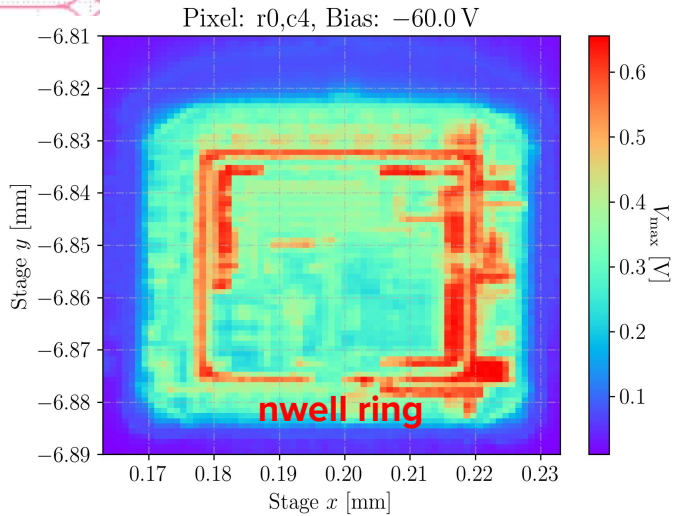
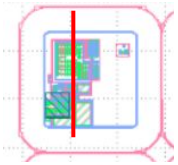
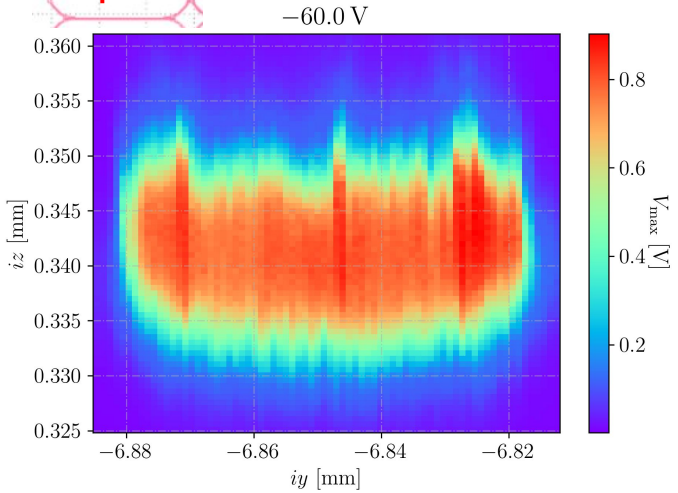


XY-Scan middle depth focus





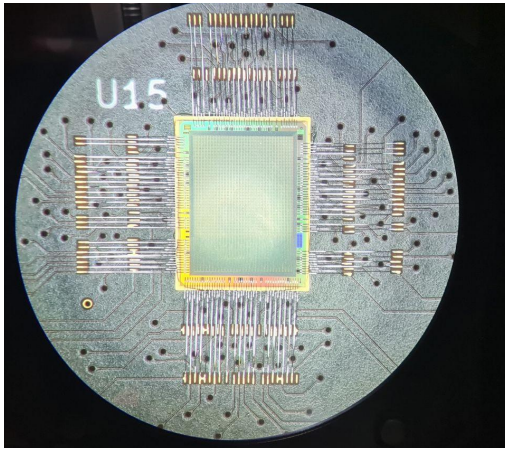
YZ-Scan across the electronics



- Chip electronics no obstacle to mapping
- N-well ring clearly visible in image made with TPA laser
- Active region is clearly visible

From RD50 CMOS meeting
https://indico.cern.ch/event/1184355/contributions/4976091/

Summary and outlook



New HV CMOS sensor designed by RD50

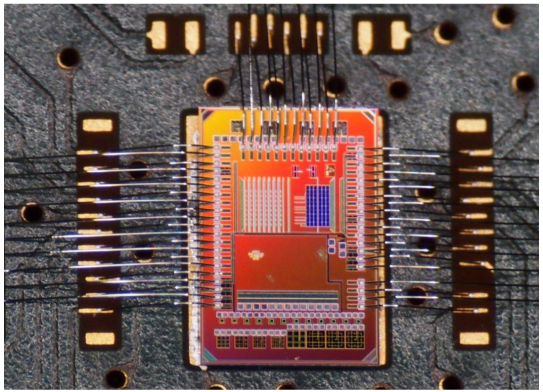
- Shows promising results such as breakdown at 150 V
- Test beam ongoing now to investigate unirradiated sample
- Advanced in-pixel digital readout

Perfomance of previous submission:

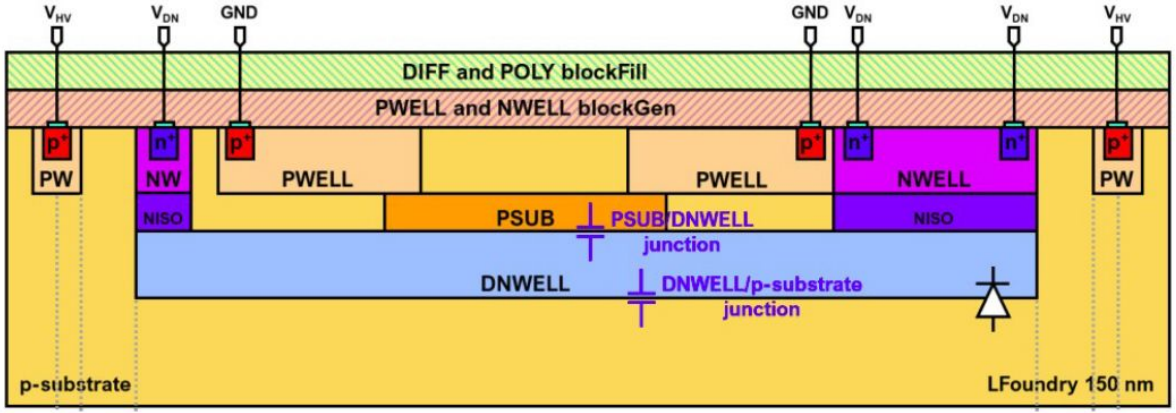
- Good threshold and noise after irradiation of $\Phi_{eq}=5{\cdot}10^{14}/cm^2$
- Time resolution for a MIP-like particle around 300 ps also after irradation

Plans to

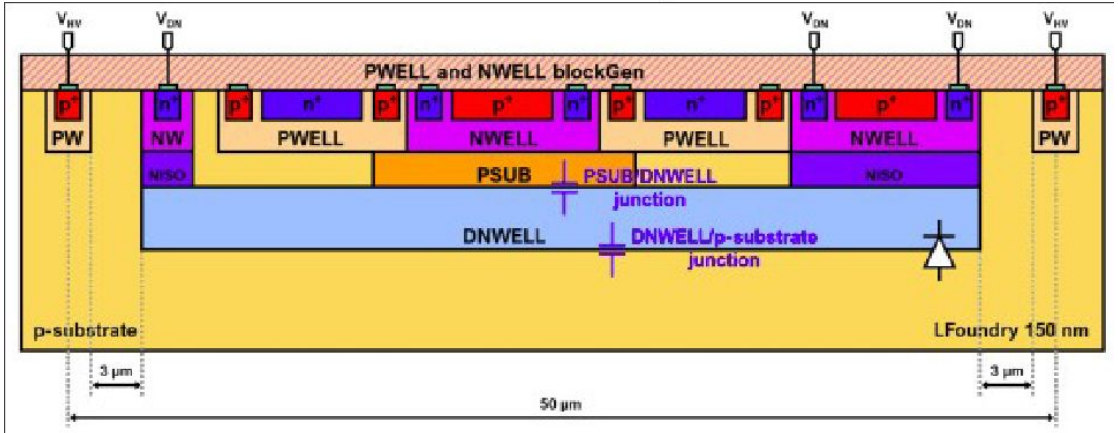
- Measure efficiency at CERN beam test facility
- Measure time resolution
- Repeat this for irradiated samples
- Improve radiation hardness in new design



Additional material

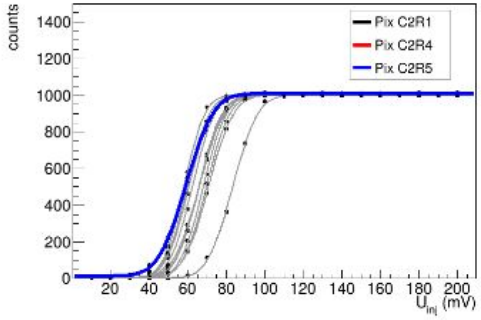


RD50-MPW2 test structure pixel cross section.

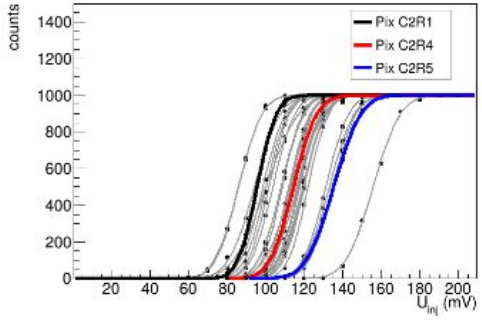


RD50-MPW1 pixel cross section

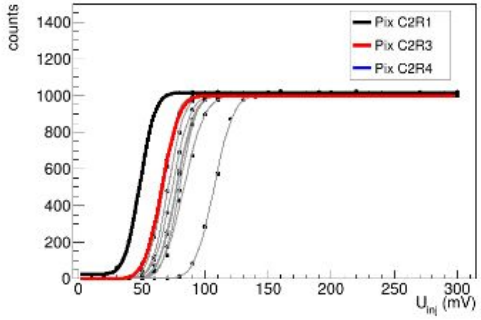
Previous HV CMOS chip threshold after irradiation



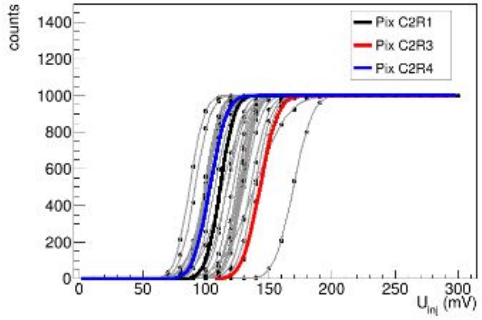
(a) Unirradiated, threshold 950 mV.



(b) Unirradiated, threshold 1000 mV.



(c) $5 \cdot 10^{14}$ n_{eq}/cm^2, threshold 950 mV.

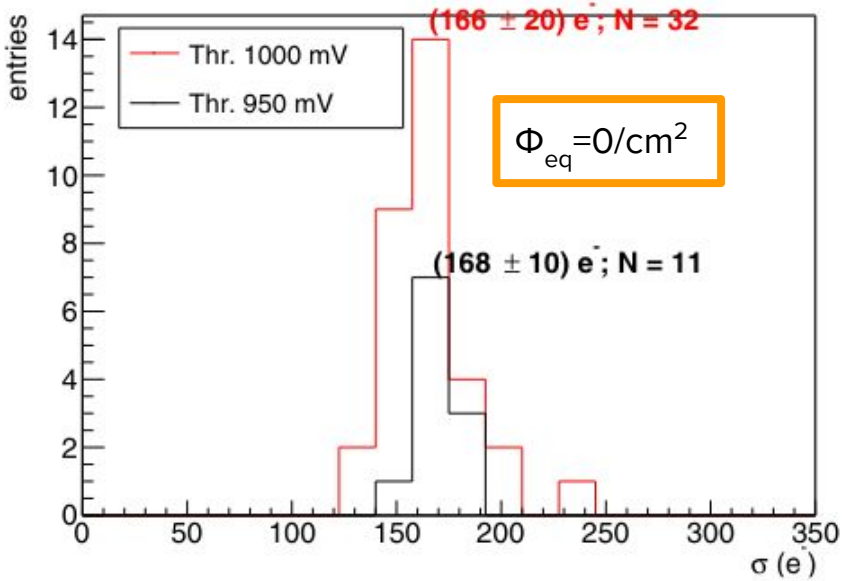


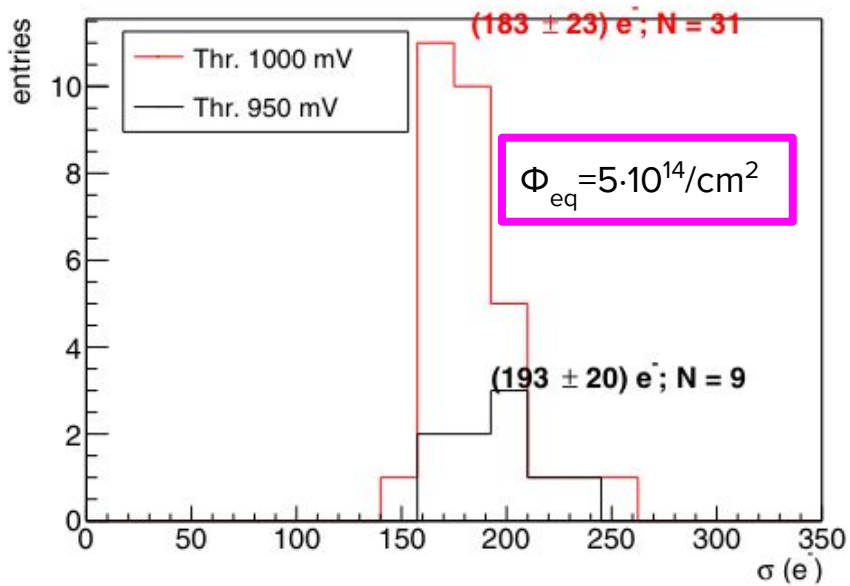
(d) $5 \cdot 10^{14}$ n_{eq}/cm^2, threshold 1000 mV.

From B. Hiti et. al https://doi.org/10.1088/1748-0221/16/12/P12020

Performance of previous HV CMOS sensor after irradiation

Noise for $q = C_{inj}U$ with C_{inj} = 2.8 fF

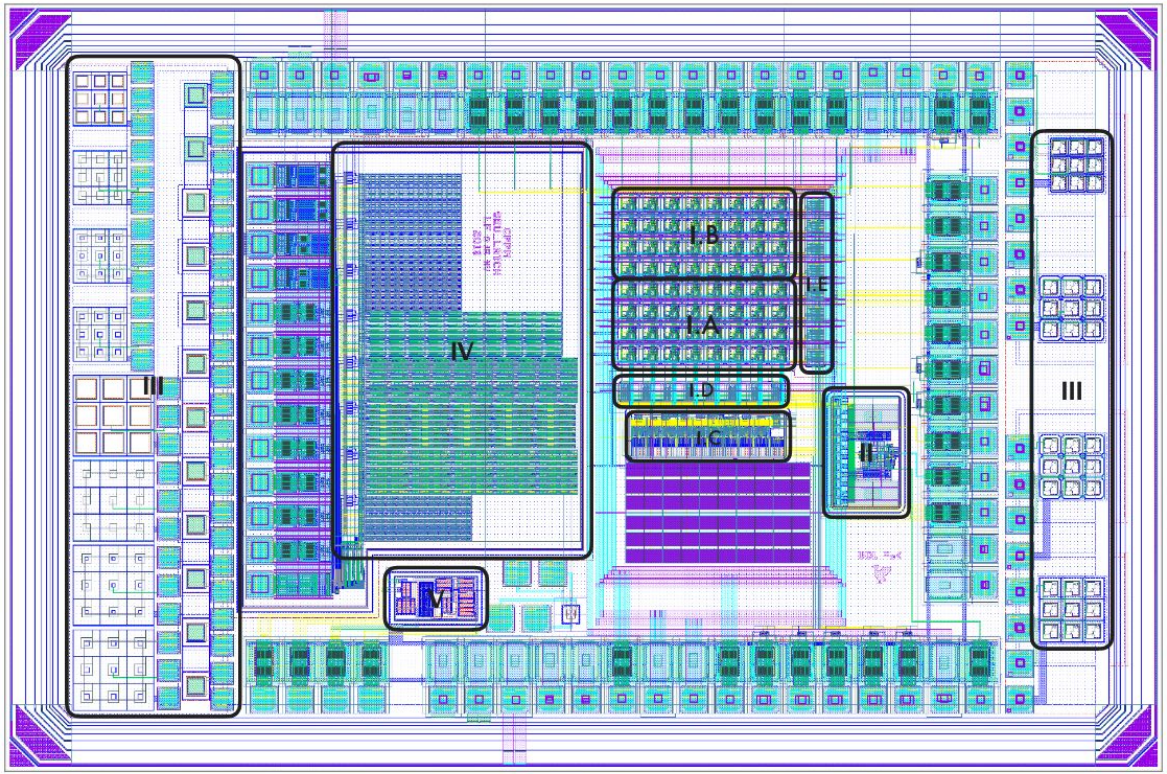




From B. Hiti et. al https://doi.org/10.1088/1748-0221/16/12/P12020

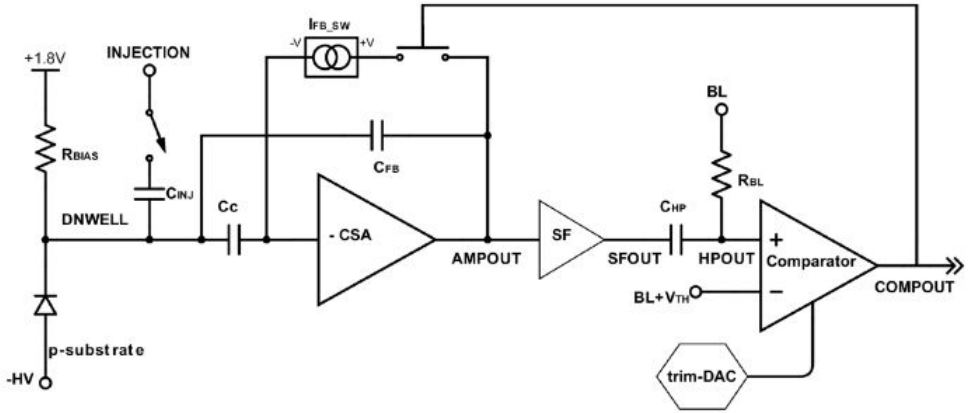
Noise increases but still < 200 e^- after irradiation

Previous DMAPS layout

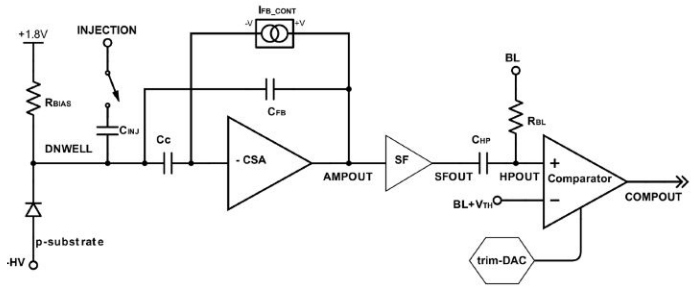


I. 8 × 8 Analog pixel matrix with pixel size of 60 µm × 60 µm, two flavors:
I.A.Continuous-reset pixels (column 0 to 3)
I.B. Switched-reset pixels
(column 4 to 7)
I.C. Bias block
I.D. Row configuration registers
I.E. Column configuration registers
II. Analog buffer
III. Test structures
IV. SEU tolerant memory
V. Bandgap

Previous HV CMOS chip frontend



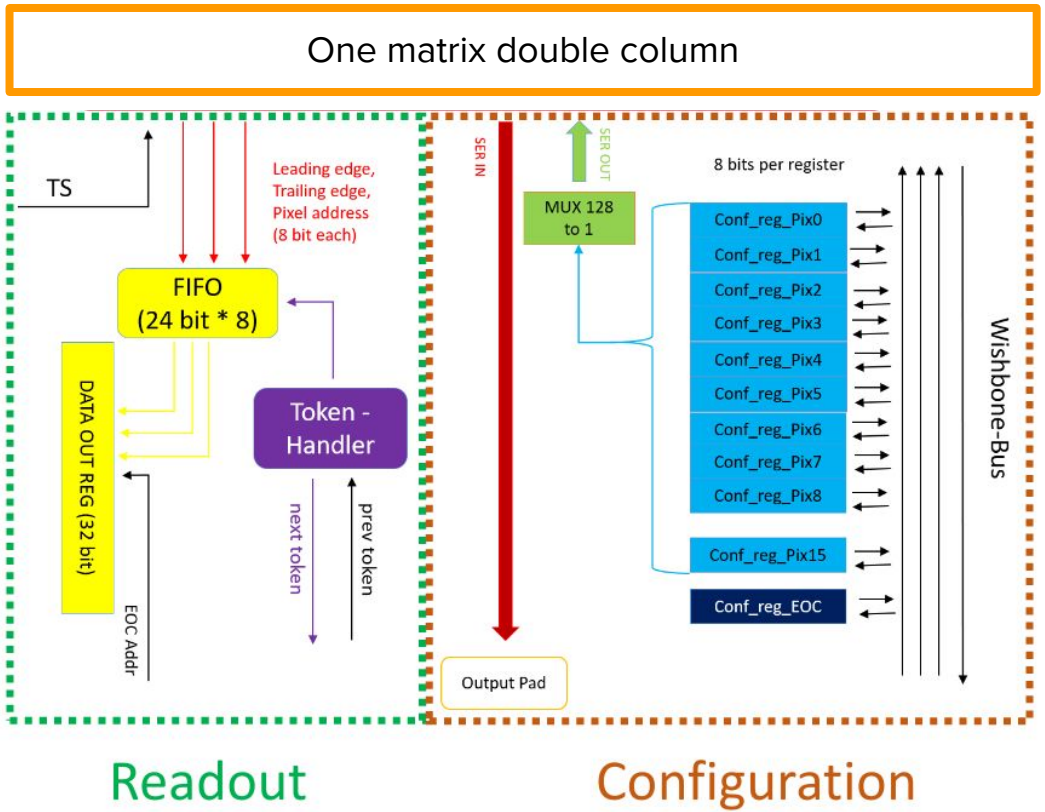
Switched reset



Continuous reset

Advanced readout periphery of current HV CMOS chip

- 16 8-bit registers for configuration
- Rolling shutter: highest address read out first
- 24-bit wide FIFO for pixel data
- Time stamps and pixel address collected in end of column (EOC)
- Serial readout of 32-bit EOC registers at 640 Mbps



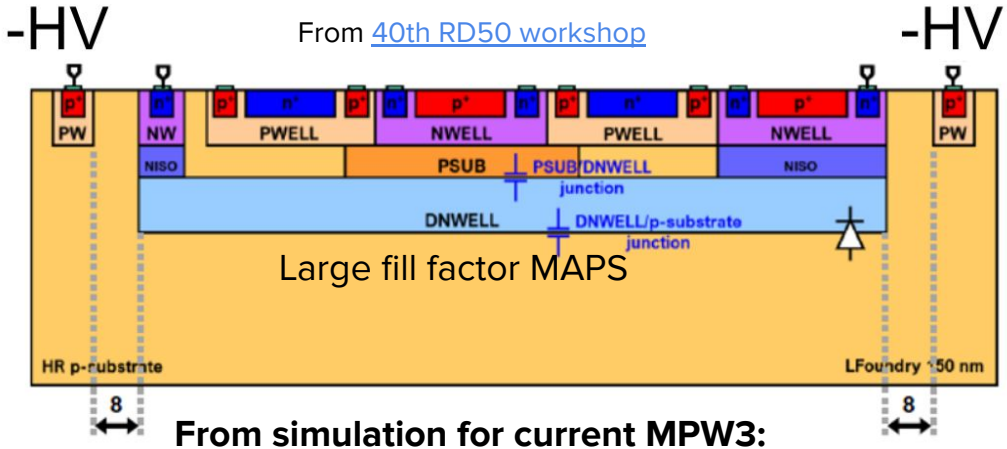
From TWEPP 2022

Measured performance of previous HV CMOS submission

Measured in previous MPW2:

- ENC < 50 e-
- Time-walk < 10 ns
- Leakage 120 pA/pixel
- ToT 30 ns
- Breakdown 120 V

From [40th RD50 workshop]



From simulation for current MPW3:

Pixel size	62 μm × 62 μm
Cd	~ 250 fF
Power	22 μW/pixel (VDD = 1.8 V)
Gain	230 mV (for 5 ke$^-$)
ToT	55 ns (for 5 ke$^-$)
ENC	120 e$^-$
Time walk	9 ns