WP6, Results and Outcomes from Latest WP6 Test Campaigns in Radiation Facilities

André M. P. Mattos (IES/University of Montpellier)
Almudena Lindoso (UC3M)
RADNEXT 2nd Annual Meeting – 9-10 May 2023
https://indico.cern.ch/e/radnext-2023

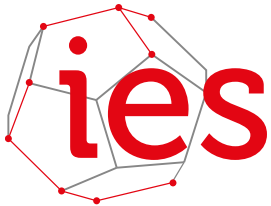
This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 101008126

Outline

- **IES/UM: Test Campaigns**
  - CHARM: RISC-V/SoC
    - Power and logging challenges
  - ChipIr: RISC-V/SoC/FPGA
  - PSI: SRAM
    - Setup, capabilities, and results
- Conclusions

- **UC3M: Test Campaigns**
  - CHARM: SoC
  - ChipIr:
    - Microprocessors/SoC
    - FPGAs
    - GPUs
  - UltraScale+
- Publications
- Conclusions

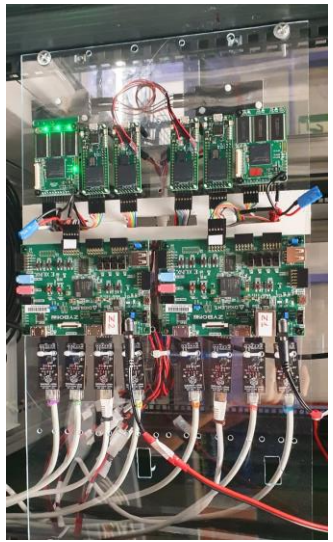
IES/UM: Test Campaigns



IES/UM: Test Campaigns

	Source	Facility	Date	Experiment
1st year	Protons	PSI	12/21*	SDRAM/HyperRAM
	Heavy Ions	RADEF	02/22	SRAM
	Neutrons	ChipIr	05/22*	RISC-V/SoC/NoC
	Protons	PARTREC	06/22*	RISC-V/SoC
2nd year	**Mixed-Field**	**CHARM**	**10/22**	**RISC-V/SoC**
	Neutrons	**ChipIr**	**11/22***	**RISC-V/SoC**
	Protons	**PSI**	**12/22**	**SRAM**
	Laser	ESTEC	05/23	SRAM

*Test campaigns through TA calls



CHARM
Irradiation room

CHARM
Control room

> CHARM: RISC-V/SoC

- **Characterization of a fault-tolerant RISC-V system-on-chip in flash-based FPGAs**
  - Two different board designs with same FPGA family, but different power regulators
  - Both boards with external SEL protection and current monitoring
  - External robust communication fixtures were used to extend the logging interfaces
  - **Similar setups and conditions, but two very distinct experimental characteristics**
  - **Despite that, there is good correlation between results considering the useful operation time**

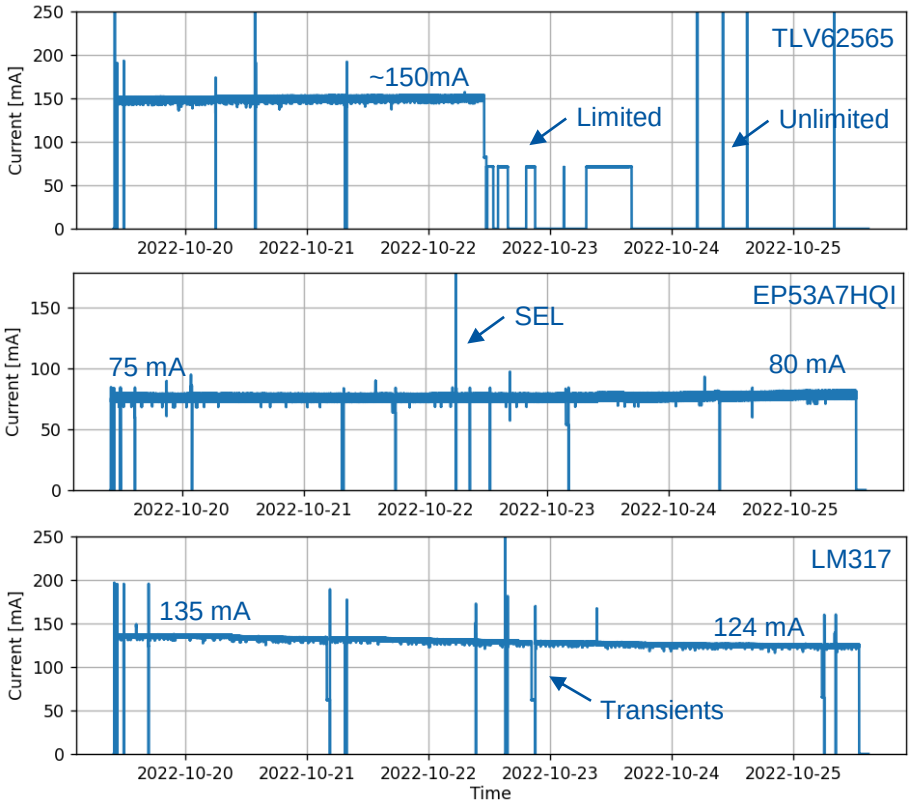
HARSH:
- **M2S025**
- 3x SDRAM

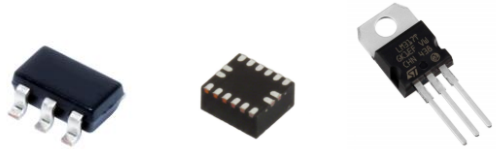
SMF2000:
- **M2S010**
- SDRAM

[1] [Under review] Douglas A. Santos, André M. P. Mattos, et. al., “Enhancing Fault Awareness and Reliability of a Fault-Tolerant RISC-V System-on-Chip”, Electronics, 2023.

[2] [Accepted] André M. P. Mattos, Douglas A. Santos, et. al., “Using HARV-SoC for Reliable Sensing Applications in Radiation Harsh Environments”, IWASI, 2023.

> CHARM: RISC-V/SoC >> Power regulators

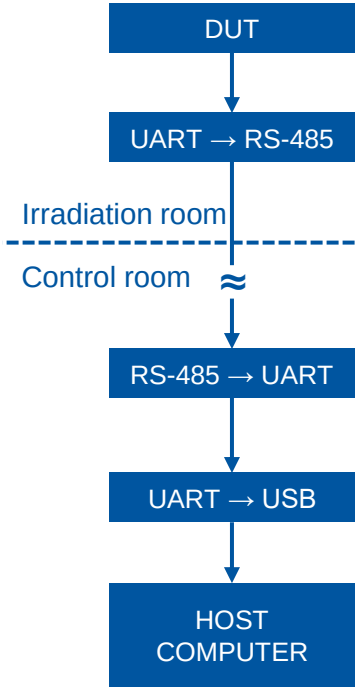




	TLV62565	EP53A7HQI	LM317
Device type	Switching regulator	Switching regulator	Linear regulator
Board critical TID	~ 19 krad	> 36 krad	> 36 krad
# SELs	1	1	1
# Transients	1	7	6
Observations	After critical TID, it was not operational, but current limited. After 29 krad, it had unlimited consumption	Steady current increase (voltage decrease) ~ 6.5%	Steady current decrease (voltage increase) ~ 8.5%

> CHARM: RISC-V/SoC >> Logging interface

- **Robust interface: UART ↔ RS-485**
  - UART **with flow control**
  - RS-485 transceiver
  - IO buffer
  - Flexible and easy to use (transparent)
  - RJ45 connector/cable for physical connection
    - Robust and often available in patch panels



	ChipIr [Neutrons]	PARTREC [High-energy protons]	CHARM [Mixed-field]
High-level failures	None[1]	Desynchronization[1]	None[2]
Observation	**Cable:** 125m (with patch panel connections) **Baud Rate:** 3Mbauds	Only one occurrence: IO buffer caused the flow control to unsync data	

[1]Functional testing only (loopback) with direct irradiation, [2]Only usage (no specific testing)

> ChipIr: RISC-V/SoC

- **Characterization of a fault-tolerant RISC-V system-on-chip in a SRAM-based FPGA**
  - Adaptation from the flash-based port
  - External bitstream memory required
  - Sensitive configuration memory
    - Custom scrubbing and correction (alternative to the SEM IP) with integration to the SoC

Zybo:
- **Zynq-7000 family**
- Flash
- SDRAM

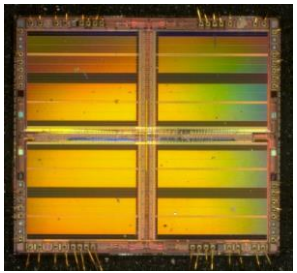
	SoC in Flash-based FPGA [Microchip] [M2S010]	SoC in SRAM-based FPGA [Xilinx] [Zynq-7010]
Total Fluence [n/cm²]	1.80×10^{12}	5.83×10^{10}
Mean Fluence to Failure [n/cm²]	2.06×10^{10}	3.60×10^{8}
Cross Section [cm²]	**4.98×10^{-11}**	**2.78×10^{-9}**

~ 200x difference in robustness

[3] [Under review] Douglas A. Santos, Pablo M. Aviles, André M. P. Mattos, et. al., “Hybrid Hardening Approach for a Fault-Tolerant RISC-V System-on-Chip”, RADECS, 2023.

> PSI: SRAM

- **Investigation on radiation-induced single-event latch-ups in SRAM memories on-board PROBA-V mission**
  - Understanding the flight behavior and error rates
- **Utilization of an experimental approach attending the target environment**
  - RADEF: **Heavy Ions**
  - PSI: **Protons**
  - ESTEC: **Laser** (further investigation of the observed phenomena)
- **Development of an experimental setup for enhanced observability**

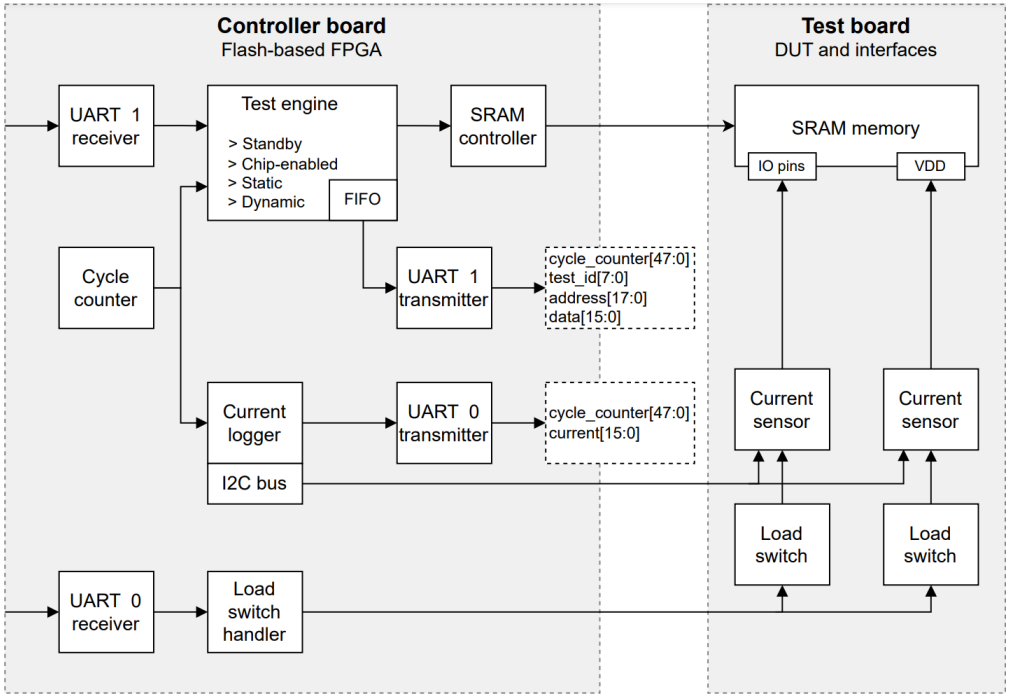


[4] [Under review] André M. P. Mattos, Douglas A. Santos, et. al., “Investigation on Radiation-Induced Single-Event Latch-up in SRAM Memories on-Board PROBA-V”, RADECS, 2023.

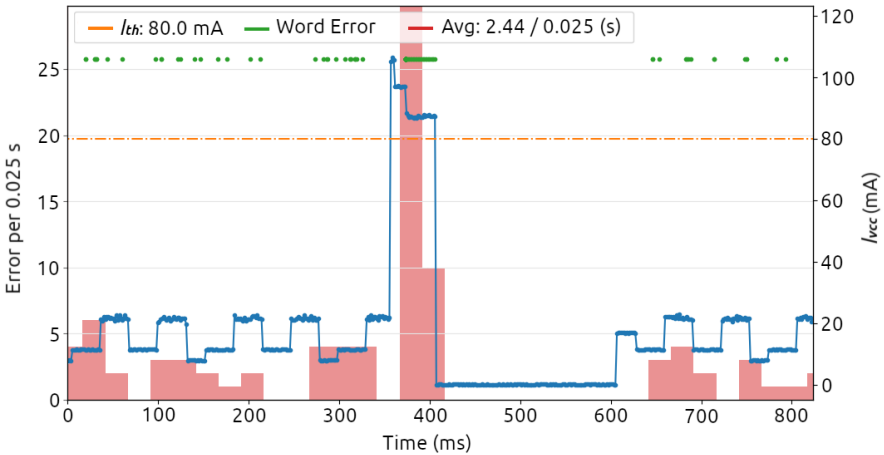
[5] [Under review] André M. P. Mattos, Douglas A. Santos, et. al., “Instrumentation and Methodology for In-Depth Analysis of Single-Event Latch-up on Memory Devices”, Journal of Instrumentation, 2023.

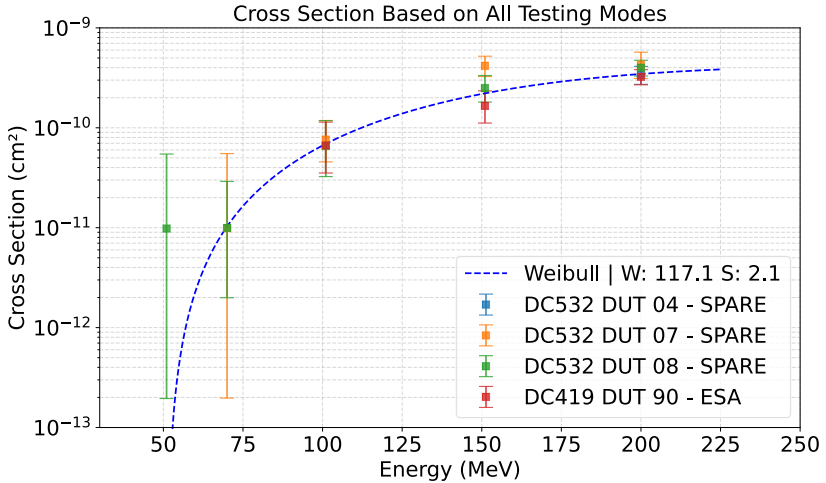
> PSI: SRAM >> Test Setup

- Enhanced experimental setup
  - Precise **timing** and current measurements
  - **Coherent monitoring** between memory errors and current measurements
  - Many test modes with **realistic stimuli**
  - Robust and flexible test setup



> PSI: SRAM >> Results





- **Error accumulation during SEL events**
  - Example within a dynamic test
  - 50ms “hold time” and 200ms “cut time”

- Event cross sections
  - **Good correlation between lots**
  - Weibull fitting

Conclusions

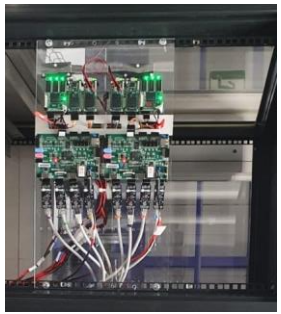
- Tests at **CHARM** presented many setup **challenges** to be addressed before the campaign
- Tests at **ChipIr** provided more insights on the **capabilities** of **Flash-** and **SRAM-based FPGAs** for radiation testing
- Tests at **PSI** allowed the elaboration of an **enhanced setup** and provided practical insights

- We are currently working in the **first WP6 milestone**, which will summarize the setup preparation experience obtained in these **first 2 years of the project**
- We intend to elaborate **more publications** using the acquired data and experience

UC3M: Test Campaigns

UC3M: Test Campaigns TA RADNEXT

	Source	Facility	Date	Experiment
1st year	Protons	PSI	12/21	µp/FPGA/SoC
	Neutrons	ChipIr (1/3)	05/22	µp/FPGA/SoC/GPUs
2nd year	Neutrons	ChipIr (2/3)	09/22	µp/FPGA/SoC/GPUs
	Mixed field	CHARM	10/22	µp/SoC
	Neutrons	**ChipIr (3/3)**	**11/22**	**µp/FPGA/SoC/GPUs** ✓ **Completed**
3rd year	Protons	PARTREC	09/23	µp/FPGA/SoC
	X-ray (microbeam)	ESREF	Under review	µp/FPGA/SoC/Memories



CHARM

CHARM

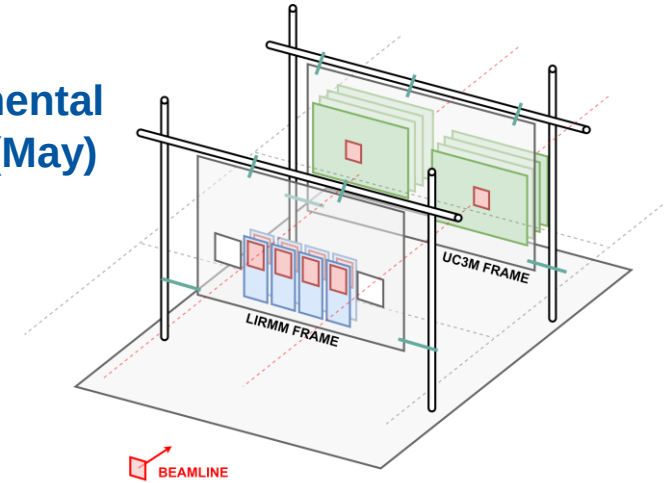
- 2 commercial boards (zybo)
- Microprocessor hardening techniques
- Complex setup
- After 6.31krad (~20 hours), board non responsive

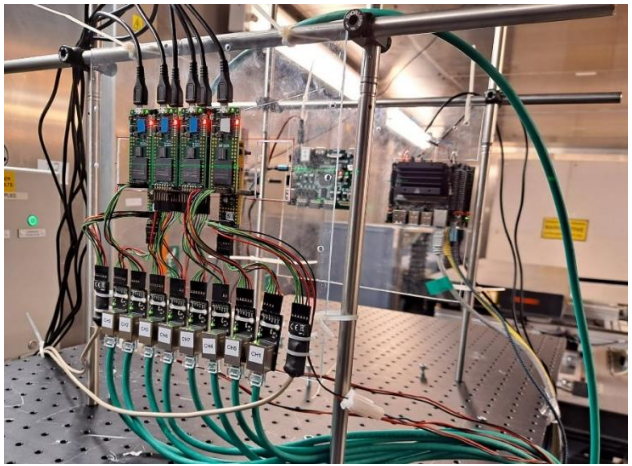
> ChipIr: Experimental setup

✓ **Several experiments per board type**

- **Experiments UC3M, complex COTS systems:**
  - 8x SoC Xilinx Zynq-7000 (28 nm): Microprocessors, FPGA, SoC
  - 6x Jetson Nano (20 nm): Quad-core A57 & NVIDIA Maxwell GPU
  - 1x SoC Xilinx UltraScale+ (16 nm FinFET)

Experimental Setup (May)



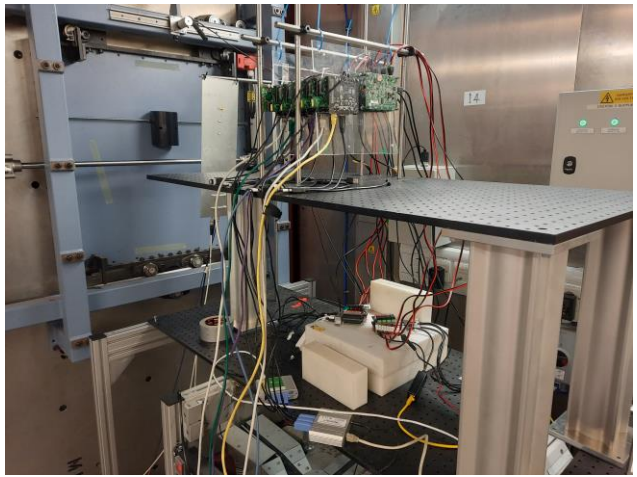


ChipIr

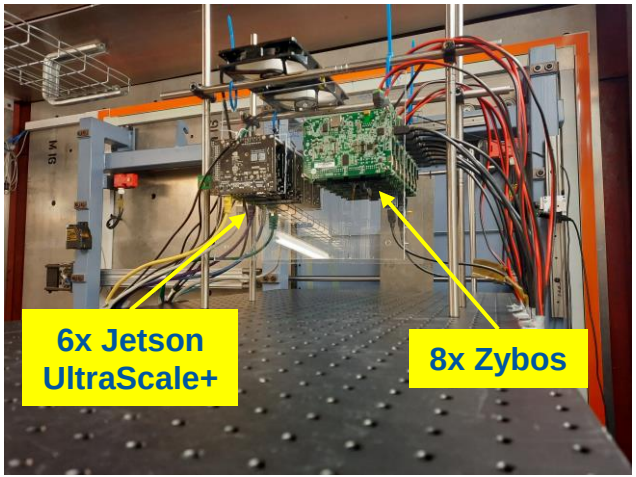
> ChipIr: Experimental setup

- **Experiments UC3M, complex COTS systems :**
  - 8x SoC Xilinx Zynq-7000 (28 nm): Microprocessors, FPGA, SoC
  - 6x Jetson Nano (20 nm): Quad-core A57 & NVIDIA Maxwell GPU
  - 1x SoC Xilinx UltraScale+ (16 nm FinFET)

Experimental Setup (November)

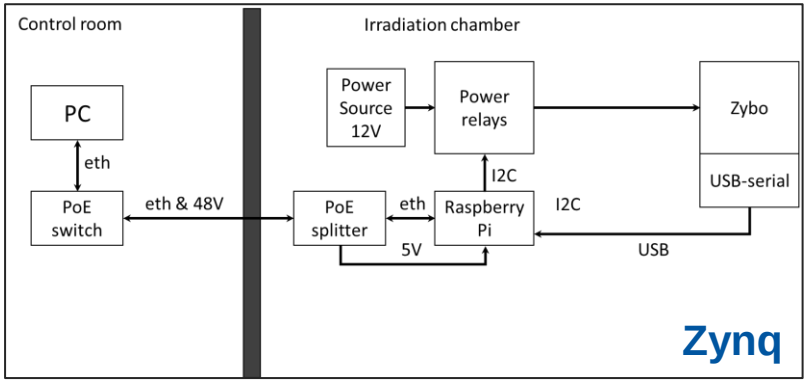


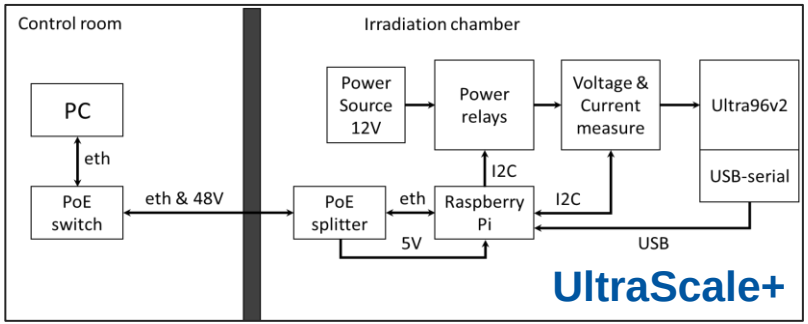
ChipIr



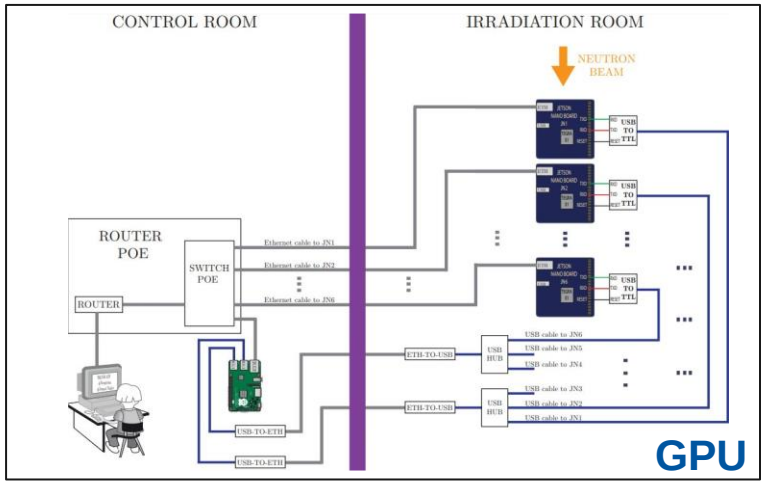
ChipIr

> ChipIr: Experimental setup





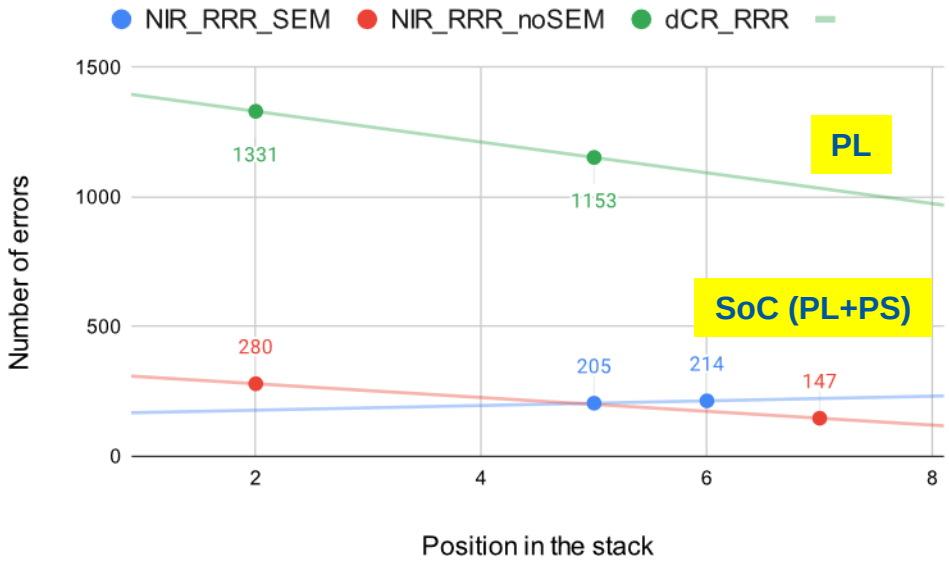
- Zynq & UltraScale+: serial communication
- GPU: Ethernet connection
- External host (Raspberry Pi) to control the experiments & Power cycles
- UltraScale+: SEL detector



> ChipIr: Evaluation of events vs board location

- Zynq 7000
- 3 Different hardening techniques
  - PL
  - SoC (PL+PS)

Experiment	Δ Errors (%)
dCR_RRR (PL)	**- 13.37 (+3 positions)**
NIR_RRR_noSEM (SoC)	**- 47.50 (+5 positions)**
NIR_RRR_SEM (SoC)	**+4.21**



- NIR_RRR_SEM behaves differently
  - Includes Xilinx SEM IP:
    Detects & corrects PL errors

Board position	SEM corrections	PL+PS events
5	**978**	205
6	**1119**	214

> ChipIr: Cross-section

Comparison different particles/ different complex systems

Previous Results RADECS DW 22

	FPGA Zynq-7000	Microprocessors Zynq-7000
Cross-section [cm²] Protons PSI	4.42×10^{-10}	1.38×10^{-9}
Cross-section [cm²] Protons CNA	1.86×10^{-10}	5.61×10^{-10}

Similar experiments

ChipIr experiments/benchmarks:

- FPGA: 3
- SoC: 1
- GPUs: 12
- Microprocessor: 3
  - 2 soft-core (RISC-V)
  - 1 hard-core (Cortex A9)

ChipIr

	FPGA Zynq-7000	Microprocessors Zynq-7000	SoC Zynq-7000	GPU Experiment 1 (6 benchmarks)	GPU Experiment 2 (12 benchmarks)
Total Fluence [n/cm²]	2.72×10^{11}	2.57×10^{11}	3.38×10^{11}	[1.51×10^{10} , 9.30×10^{10}]	[3.56×10^{11}, 1.17×10^{12}]
Cross-section [cm²] Neutrons ChipIr	1.38×10^{-9}	9.64×10^{-9}	1.28×10^{-8}	[9.68×10^{-9}, 1.56×10^{-9}]	[8.48×10^{-9}, 3.53×10^{-9}]

> ChipIr: Cross-section

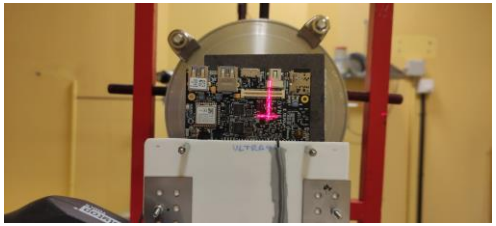
Comparison CHARM/ChipIr complex system microprocessor-based hardening technique

- Based in: P. M. Aviles, A. Lindoso, J. A. Belloch, M. Garcia-Valderas, Y. Morilla and L. Entrena, "Radiation Testing of a Multiprocessor Macrosynchronized Lockstep Architecture With FreeRTOS," in IEEE Transactions on Nuclear Science, vol. 69, no. 3, pp. 462-469, March 2022 doi: 10.1109/TNS.2021.3129164.

Microprocessor Hardening technique		CHARM	ChipIr
	Fluence [particles/m^2]	5.67×10^{11}	2.57×10^{11}
	Cross-section [cm^2] (Total events)	2.35×10^{-9}	9.64×10^{-9}
	Cross-section [cm^2] (Undetected errors)	1.23×10^{-11}	5.84×10^{-11}
	Error rate [errors/hour]	114.12	105.13
	Time [hours]	11.66	23.56

✓ Up to 2 orders of magnitude improvement

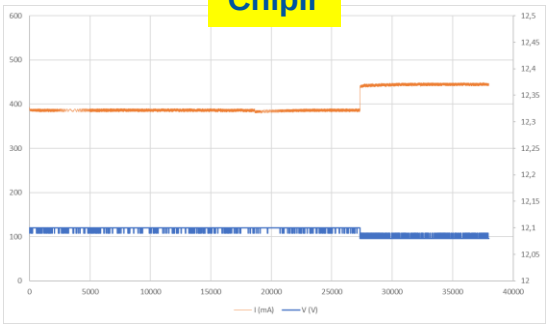
> ChipIr: SoC UltraScale+



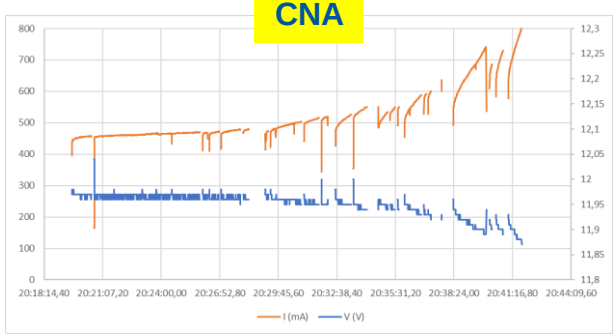
CNA

- Small number of events
- Microlatchup (under SEL stablished limit=500 mA)
- The same test was performed at CNA (15 MeV protons)
  - Small number of events
    - Flux was increased: TID effects observed (persistent current degradation)
  - No SEL observed
- Additional tests will be performed in the next TA campaigns (PARTREC)

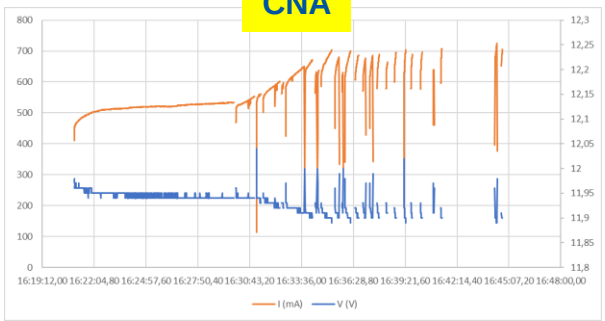
ChipIr



CNA



CNA



Publications

1. **RADECS 2022 Data Workshop:** P. M. Aviles, L. A García-Astudillo, J.A. Belloch, L. Entrena, A. Lindoso, “Comparative of proton radiation data for 28 nm Zynq-7000 SoC”
2. **IEEE TNS (Special issue RADECS 2022)** : L. A. García-Astudillo, A. Lindoso, et al., "Evaluating Reduced Resolution Redundancy for Radiation Hardening in FPGA designs" doi: 10.1109/TNS.2023.3268825

Under Review:

- **RADECS 2023**
  1. D. A. Santos, P.M. Aviles, A.M.P. Mattos, M. Garcia-Valderas, L. Entrena, A. Lindoso, L. DiLillo, “Hybrid Hardening Approach for a Fault-Tolerant RISC-V System-on-Chip”
  2. G. Leon, J.M. Badia, J.A. Belloch, M. Garcia-Valderas, A. Lindoso, L. Entrena, “Analysing the influence of memory and workload on the reliability of GPUs under radiation”

Journal publications & conference communications in progress

Conclusions

- Successful test of complex systems in different facilities
  - SoC, hard-core & soft-core microprocessors, FPGA and GPUs
- Combine different experiments/different boards & sensitivities for a radiation campaign
- Challenges in testing complex devices:
  - SoC
  - GPUs
- Comparison of irradiation campaigns results for different facilities/particles
- Developing guidelines for non-expert end users

Image Source: IES/UM

Thanks for your attention!

André M. P. Mattos (IES/UM):
andre.martins-pio-de-mattos@etu.umontpellier.fr

Almudena Lindoso (UC3M):
alindoso@ing.uc3m.es