WP6: Current progress on the accelerator system-level testing guidelines through the new SEE tester study case

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System-level testing of new electronics at CERN

System-level testing is a necessary part of the **R**adiation **H**ardness **A**ssurance (RHA) procedure for new in-house designs of radiation-tolerant systems at CERN.

For commercial systems, system-level testing (SLT) may be the only source of information about the system performance in the accelerator radiation field.

Information to be provided by the guidelines for system-level testing at CERN:

- test facility/facilities selection
  CHARM and its possible alternatives
- test procedure planning
  number of SUTs and test strategy, performed functionality, actions on failures
- system observation strategies
  observed parameters of the system – both in hardware and software
- suggestions for the test setup hardware design
  monitoring of SEE-induced events and TID/TNID degradation, test procedure automatization
- interpretation of the test campaign results
  criticality determination, event cross-section, MTBF, etc.

Mostly unstudied aspects. Current approach is largely based on common practices established by different R&D groups →

the generalization of the approach to SLT to be investigated in the PhD thesis research and contributes to tasks 6.2 (test preparation) and 6.4 (enhanced observability) of RADNEXT WP6

The guidelines should account for the different types of electronic systems:

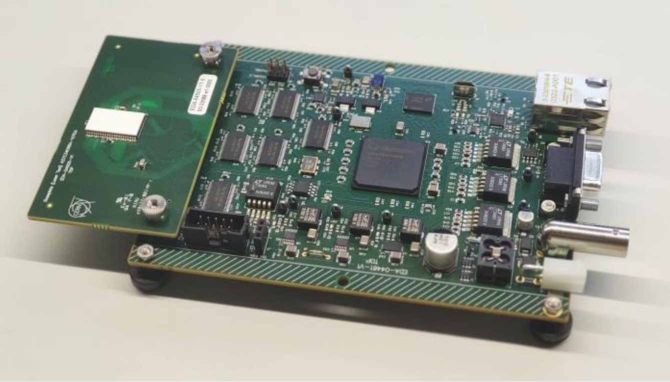
Scale of integration: System-on-Module, PCB, rack, etc.

Familiarity with the system: in-house design/modified off-the-shelf system/”white box”/”black box”, etc.

SEE Tester v2

SEE tester v2 (target environment: CHARM facility) is a universal platform for component-level testing of digital and analog ICs.

Its development followed the current guidelines for rad-tol design of in-house systems at CERN, all devices used have been qualified for use at CERN



SEE Tester v2 with the daughterboard attached

Motherboard

- Based on Microchip SmartFusion2 (M2S010T-1FGG484)
- RS-485, Ethernet interfaces to the host PC
- 4 Gbit DDR3 SDRAM for event storage
- Vcc-isolated digital I/O to the DUT
- DUT analog signal sampling with an embedded ADC
- DUT current consumption monitoring

Daughterboard

- Customizable board for the tested IC
- Powered from the motherboard or externally
- Attached directly to the motherboard or through the extension cable

System-level testing of SEE Tester v2

Comparison of radiation fields at different facilities (research question: how the accelerator environment can be recreated at different facilities to achieve same SEE, TID, DDD impact?)

1. **ChipIr** (atmospheric neutrons <500 MeV → SEE) + **Co60** (1.17, 1.33 MeV γ, 110 TBq → TID)

Test of 4 SUTs, with the implementation of software and hardware observations (research question: what is the optimal set of observed parameters to detect all system-level failures (and investigate their root causes)?)

Test campaign at ChipIr was performed between 24th and 26th of February 2023, with the total of 54 hours of irradiation

Test campaign at Co60 is preliminarily planned for June 2023

2. **CHARM** (mixed-field → SEE + TID + DD)

Test campaign is preliminarily planned for August 2023, same test setup and procedure as at ChipIr and Co60

System-level test planning for ChipIr

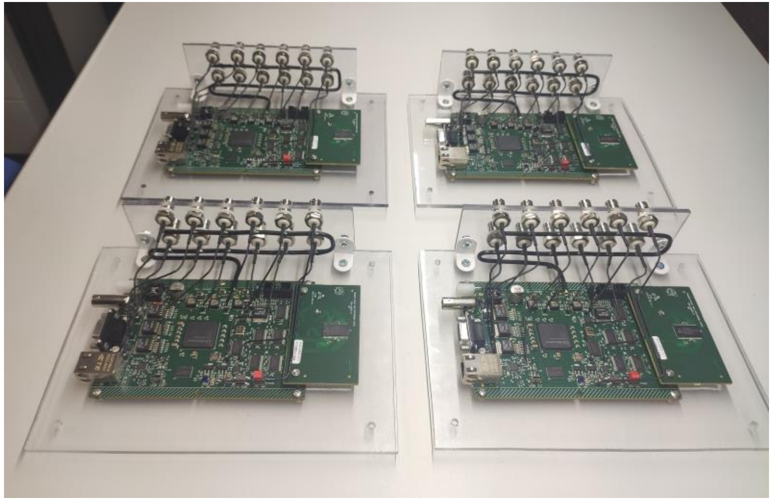
Common for each of the DUTs is the performed function: SEU and SEL monitoring in an SRAM memory (Alliance AS7C34098A).

System monitoring during irradiation was accomplished by combination of hardware and software observations. The full set of observations was implemented in each one of the DUTs.

Software observations

With the periodicity of 1 second, the following data was retrieved and saved for each of the SUTs:

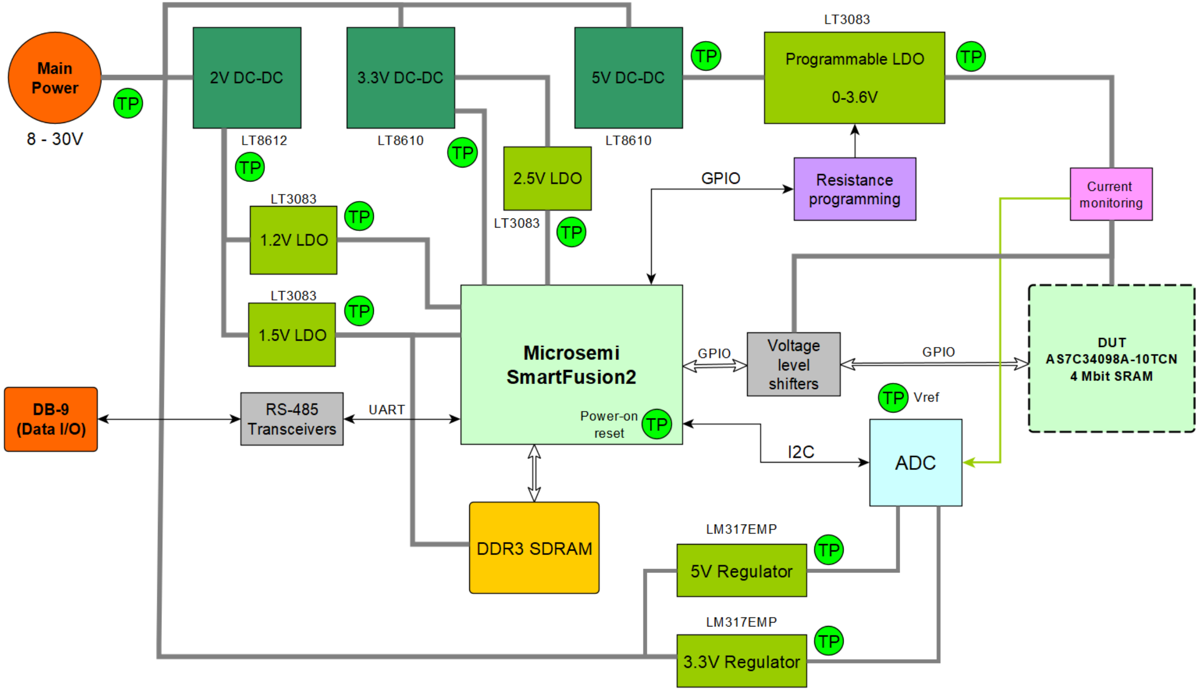
- Local date and time (initially synchronized with the PC)
- DUT (SRAM) supply voltage
- DUT (SRAM) current consumption
- Board temperature
- Checking for SEU events – retrieved from the local memory if present
- Checking for SEL events – retrieved from the local memory if present



Four SUTs assembled on the plexiglass supports

Hardware-level observations of SEE Tester v2

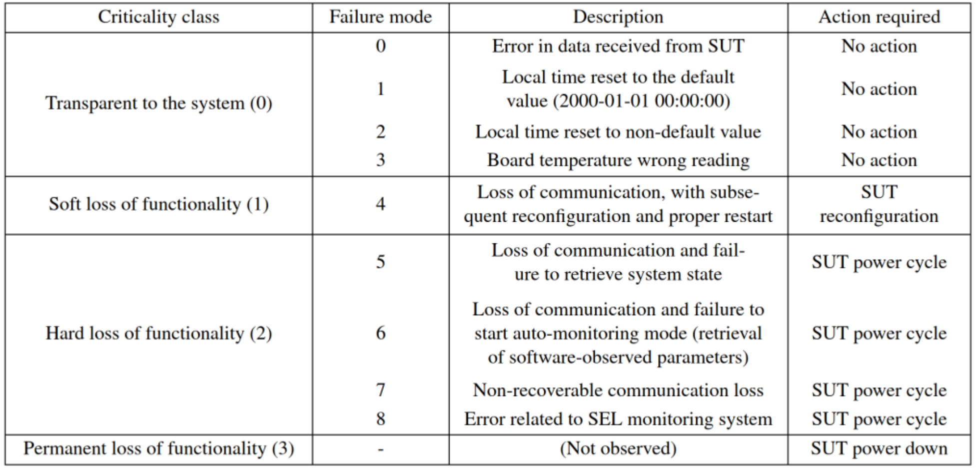
12 probes were placed at different locations of the SEU Tester v2 PCBs (48 analog signals in total). All signals were sampled in a sequence with the periodicity of around 1,5 s.



Observed SEE-induced failures

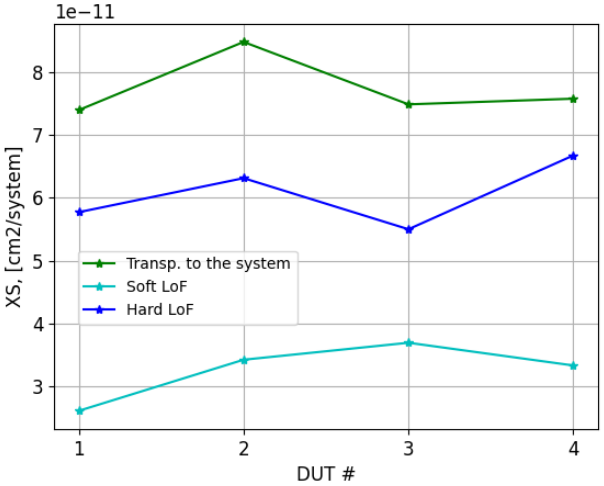
The target fluence of $1 \cdot 10^{12}\ cm^{-2}$ was reached after 49 hours 17 minutes and 20 seconds of irradiation. All the SUTs remained functional until the end of the test without any visible degradation of the functionality.

To account for the "dead observation time" which is the cumulative time through which the device was not functional as a result of SEEs and power-cycling, the irradiation time was extended to 54 hours. The actual fluence reached by the end of the test campaign was equal to $1{,}10865 \cdot 10^{12}\ cm^{-2}$



Criticality class	Failure mode	Description	Action required
Transparent to the system (0)	0	Error in data received from SUT	No action
	1	Local time reset to the default value (2000-01-01 00:00:00)	No action
	2	Local time reset to non-default value	No action
	3	Board temperature wrong reading	No action
Soft loss of functionality (1)	4	Loss of communication, with subsequent reconfiguration and proper restart	SUT reconfiguration
Hard loss of functionality (2)	5	Loss of communication and failure to retrieve system state	SUT power cycle
	6	Loss of communication and failure to start auto-monitoring mode (retrieval of software-observed parameters)	SUT power cycle
	7	Non-recoverable communication loss	SUT power cycle
	8	Error related to SEL monitoring system	SUT power cycle
Permanent loss of functionality (3)	-	(Not observed)	SUT power down

SEE-induced failure modes of SEU Tester v2 grouped by the criticality classes



Cross-sections of system failures grouped by criticalities.

SUT4 was positioned the closest to the beam guide output

Analysis of the SUT current consumption

Certain correlations can be found between the evolution of the system total current consumption (e.g. positive and negative spikes, abrupt changes by several mA) and different software observations of the SUT

Total current consumption profile of SUT4 for 12 hours. Blue areas correspond to SUT4 delivering the full expected functionality

Conclusions

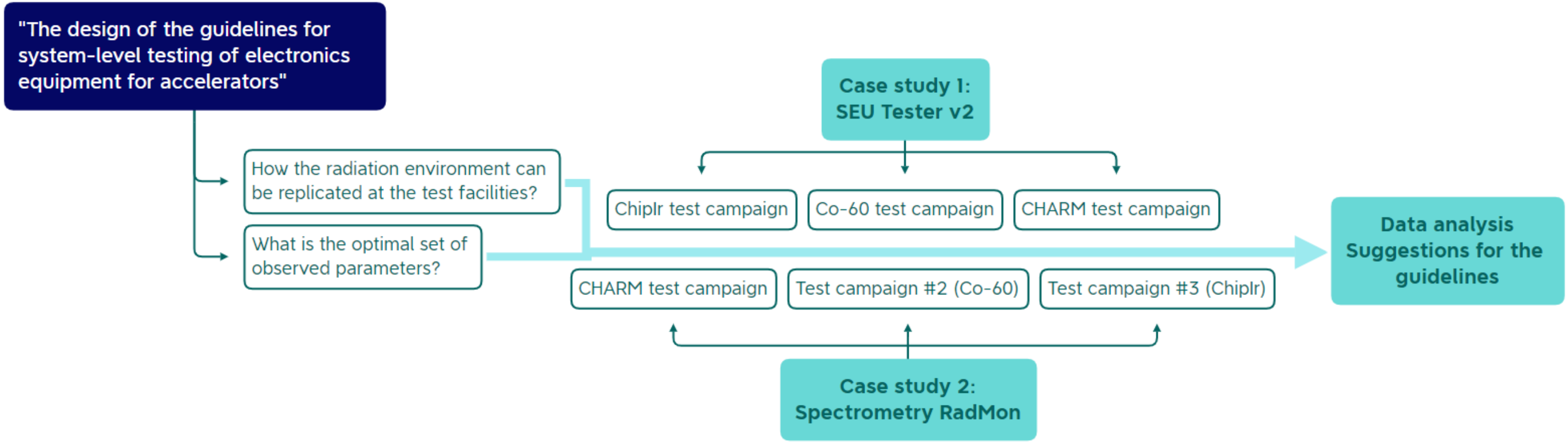
System-level test with the atmospheric neutron field at ChipIr provided large amount of data related to SUT hardware and software observations.

- SUTs have shown a comparable total amount of system-level failures (175, 202, 182 and 187 for SUT 1-4 respectively), also within same failure mode types, while being physically stacked on the top of each other → no significant alteration of beam properties after PCB crossing
- SUTs have not suffered any degradation of the functionality over irradiation time → no visible TID/TNID impact of the atmospheric neutron beam
- Combination of collected software and hardware observations open the possibility for the further investigation of root causes of the system-level failures → valuable feedback for further modifications of system design to improve radiation tolerance
- Evolution of the current consumption can be used to expand the observability of the system with limited hardware access and design familiarity (e.g., systems seen as the “black boxes”) → further analysis required
- SUTs tested at ChipIr will be exposed to the gamma-ray radiation at Co-60 alongside the “pristine” ones → the investigation of possible impact of neutron beam on SUT functionality degradation

Thanks for your attention!

Image Source: CERN

Structure of the PhD Thesis



"The design of the guidelines for system-level testing of electronics equipment for accelerators"

How the radiation environment can be replicated at the test facilities?

What is the optimal set of observed parameters?

Case study 1: SEU Tester v2

ChipIr test campaign

Co-60 test campaign

CHARM test campaign

CHARM test campaign

Test campaign #2 (Co-60)

Test campaign #3 (ChipIr)

Case study 2: Spectrometry RadMon

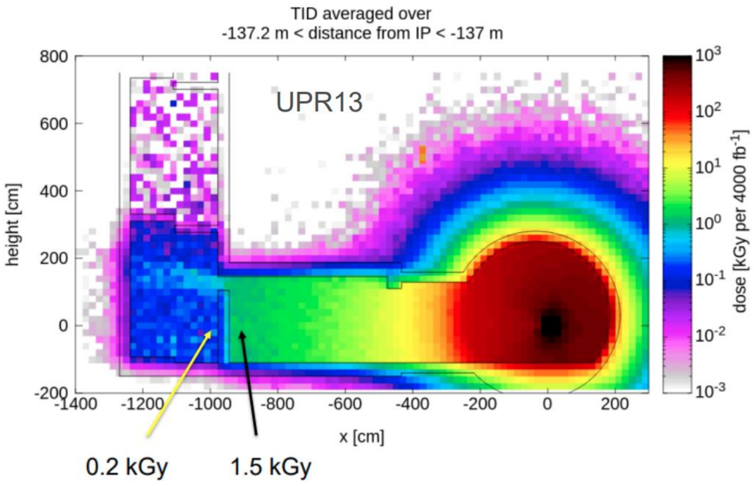
Data analysis Suggestions for the guidelines

Electronics at the CERN accelerator complex

CERN accelerator complex consists of multiple distributed electronic systems with different levels of exposure to the radiation fields present in the proximity to the accelerator. The accelerator field is composed mostly of high-energy hadrons (protons, neutrons, pions, kaons) and thermal neutrons and is commonly the result of:

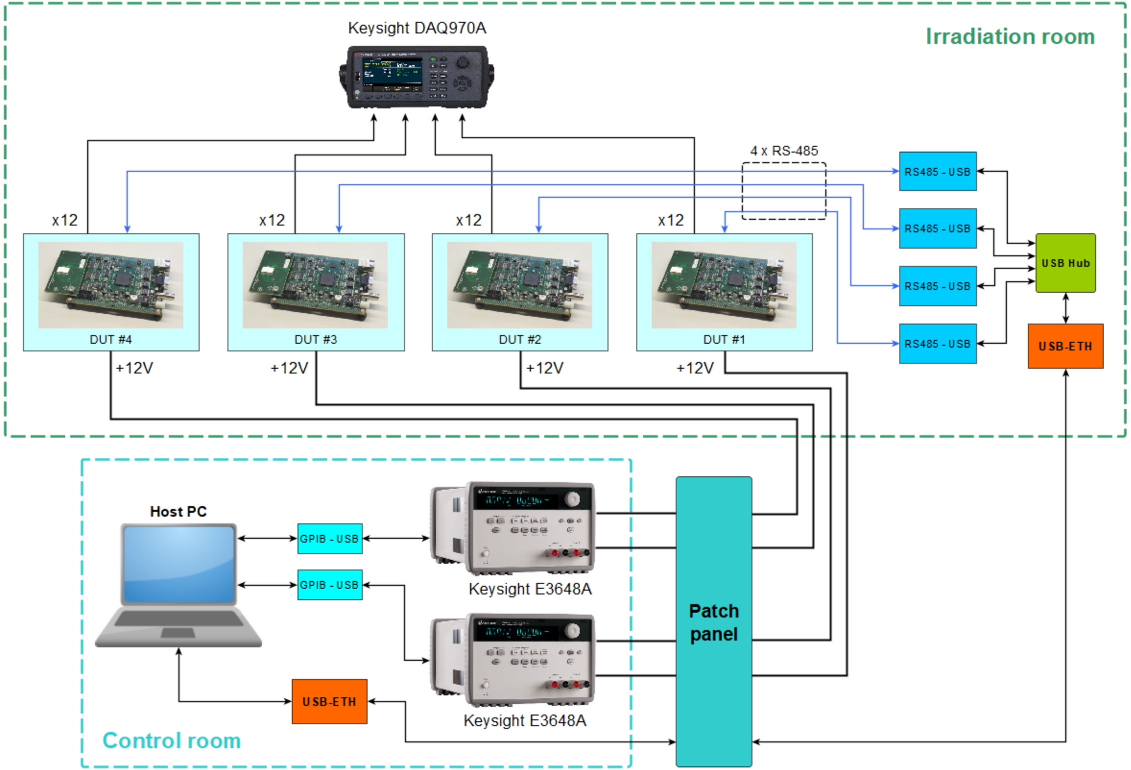
- **beam interactions with the residual gas in the vacuum pipes**
- **beam interactions with the beam intercepting devices (collimators, dumps, beam instrumentation)**
- **debris from particle collisions at interaction points**

Current requirements for the machine reliability are driven by the High-Luminosity LHC upgrade (5x reduction of failure rate per unit luminosity necessary if compared to the 2017 operation)

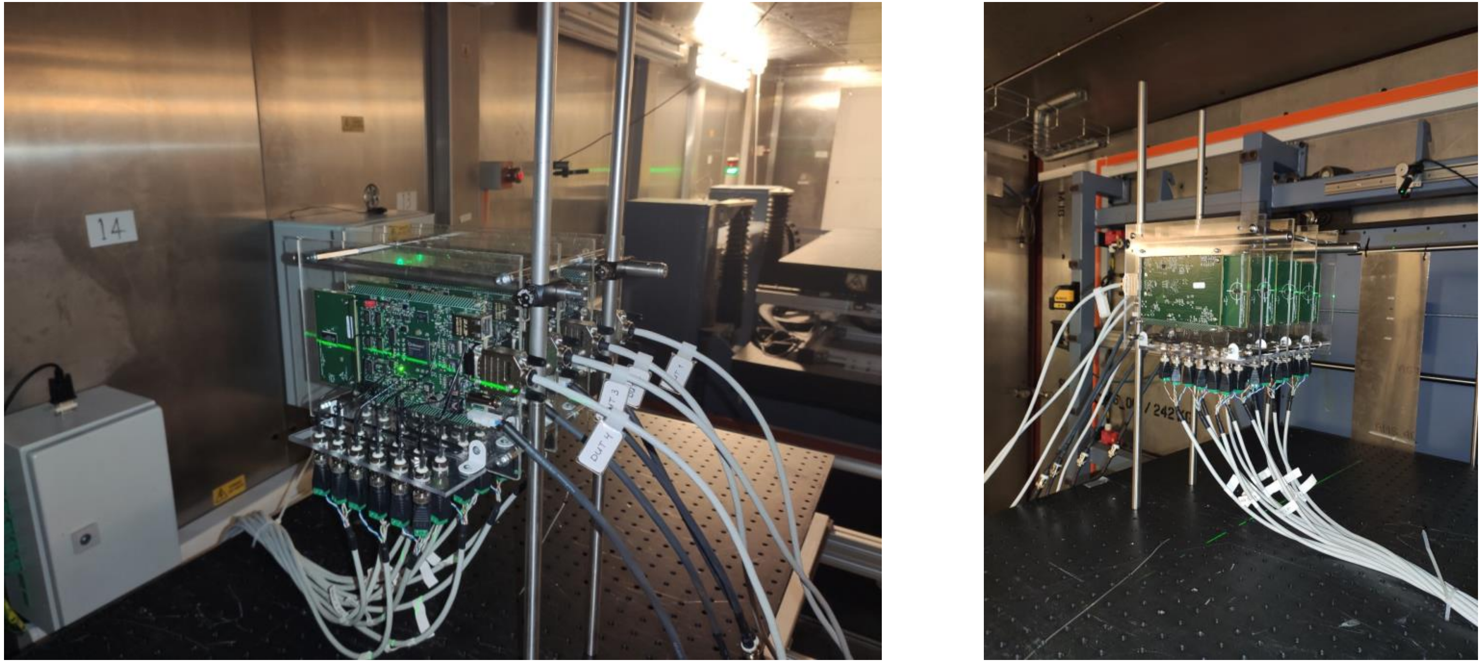


Example simulation of the total dose received by the equipment at different positions around the accelerator, over the full HL-LHC lifetime [1]

System-level test setup layout at ChipIr



Test setup installation at ChipIr



The stack of 4 DUTs installed in the irradiation room

Literature

[1] Definition of the absorbed dose for equipment located in UPR13/17/53/57 and UA13/17/53/57, Y. Body, 2021, CERN EDMS 2599444