Work Package 8:

SEU cross-section prediction

CLEITON M. MARQUES

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RADNEXT 2nd Annual Meeting
9 – 10 May 2023
https://indico.cern.ch/e/radnext-2023

Outline

- ❑ Introduction
- ❑ Circuit Level Modeling
- ❑ Results
- ❑ Next steps

Introduction

This PhD, in a framework of RADNEXT EU project, will develop and apply approaches for modelling radiation effects on electronics.

Impact of circuit modelling and low energy particles on Single-Event Effect rate prediction

WP8/JRA4
Complementary modelling tools

RADiation facility Network for the Exploration of effects for indusTry and research

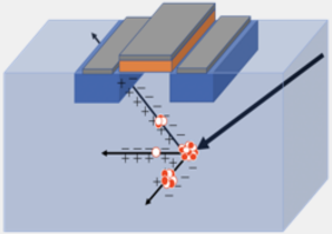
Introduction

Impact of circuit modelling and low energy particles on Single-Event Effect rate prediction

- ❑ **Impact of low energy protons and neutrons on SEU rate prediction**
  - D8.1 Simulation results of the importance of 1-10Mev energy range on the SER for neutrons
  - D8.3 Recommendation for simulating low energy protons
- ❑ **Circuit level modeling**
  - D8.4 Simulation results and report on circuit modeling
- ❑ **Impact of layout and input vector on SET Cross Section calculation**
- ❑ **Experimental part**

Circuit level modeling

The radiation-induced failures known as Single Event Upset (SEU) is a major reliability issue for electronic system.



Predictive / Post-irradiation analysis are crucial steps for a better understanding of the underlying mechanisms at circuit and transistor level

SRAM Cell
Simplified model
MC simulations
SEU Cross-Section

Main Goals

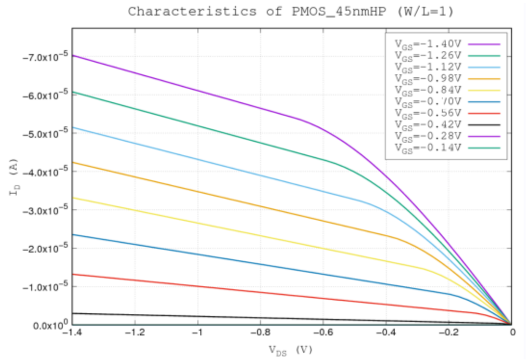
To evaluate the accuracy of using a simplified model in SEU prediction and compared to experimental data.

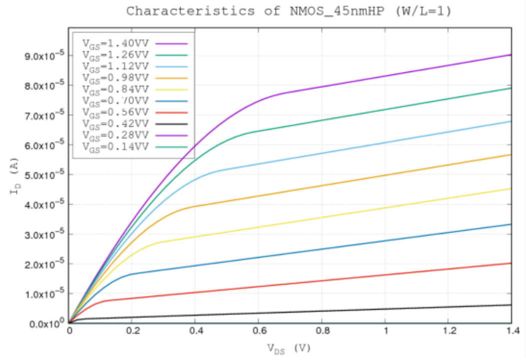
Circuit level modeling

The PredicSEE is an MC tool based on Simplified electrical model and aims to simulate radiation induced SEE in MOS technologies.

Use the diffusion-collection model.

Apply MC simulations to simulates the passage of ions, neutrons, or protons particles across the device.





The simplified model is defined based I_{DS} vs V_{DS} for different V_{GS}, replacing the structure of the transistor by a current source.

Circuit level modeling

To calculate the current associated with the transistor we use an analytical expression, which gives the three major regions of operation: subthreshold, triode, and saturation.

- Subthreshold *if* $V_{GS} < V_T$

$$I_{N;P}(V_{GS}, V_{DS}) = 0$$

- Triode *if* $V_{GS} \geq V_T$ *and* $V_{DS} < V_{GS} - V_T$

$$I_{N;P}(V_{GS}, V_{DS}) = \mu C_{ox} \frac{W}{L}(1 + \lambda V_{DS}) \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) \times V_{DS}$$

- Saturation *if* $V_{GS} \geq V_T$ *and* $V_{DS} \geq V_{GS} - V_T$

$$I_{N;P}(V_{GS}, V_{DS}) = \frac{\mu C_{ox}}{2} \frac{W}{L}(1 + \lambda V_{DS})(V_{GS} - V_T)^2$$

Circuit level modeling

There are different tools in literature to evaluate SEE. (G4SEE, FLUKA…)

Most part of these tools are dependent on the information contained in the PDK of the technology and depending on the type of analysis, the tool needs to solve complex transport and Poisson equations, making the simulation very CPU/Time consuming.

Protons / Neutrons — **DHORIN**

Ions — **SRIM Tables**

TABLE I. SIMPLIFIED MODEL PARAMETERS

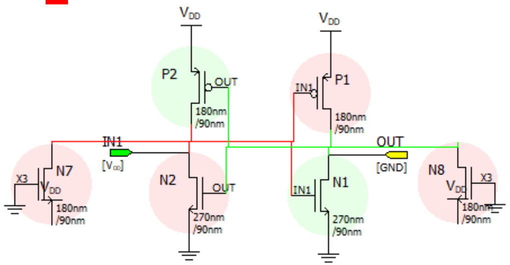
Node (nm)	Q_{crit} (fC)	T_{ox} (nm)	W/L (nm/nm)	V_t (V)	V_{dd} (V)
90	1.2	2.0	180/90	0.40	1.0
65	0.8	1.8	120/65	0.42	1.2
45	0.6	1.8	90/45	0.62	1.1
32	0.4	1.6	64/32	0.63	1.0

Circuit level modeling

Simulation Flow

1. Circuit implementation
2. Layout design
3. SEE Analysis
4. Cross Section Results

1



Circuit level modeling

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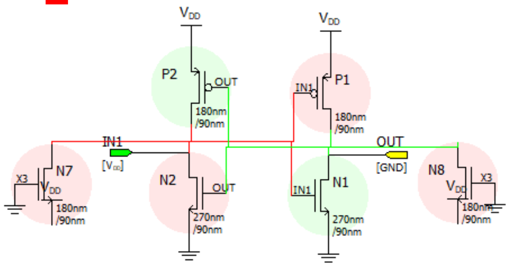
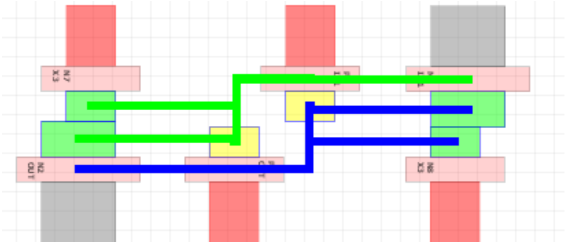
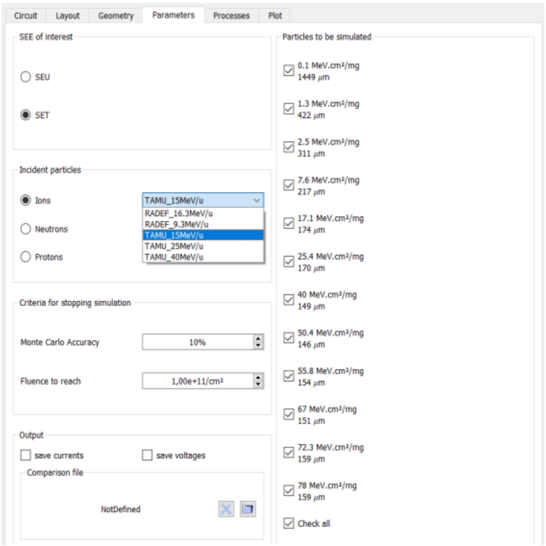


2



Circuit level modeling



Simulation Flow

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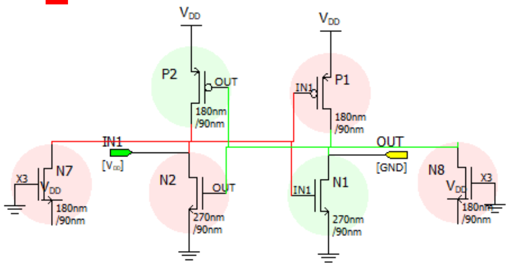

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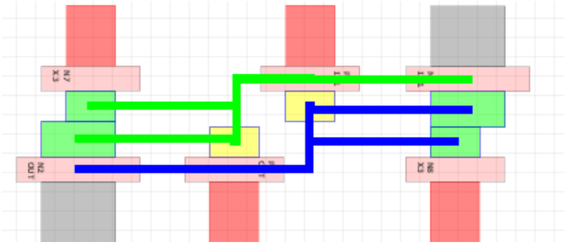

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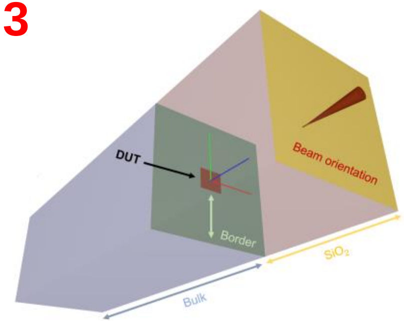


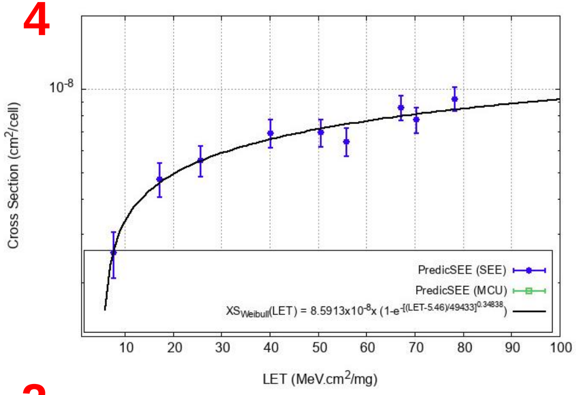
Circuit level modeling

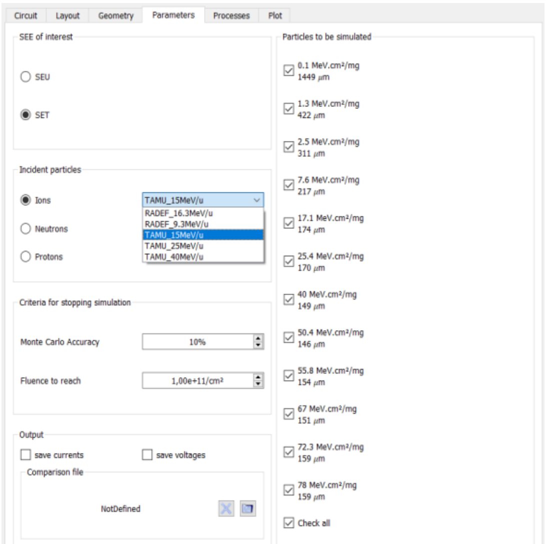
$$\sigma = \sigma_\infty \left[1 - \exp\left\{ -\left(\frac{L - L_T}{W} \right)^S \right\} \right]$$

Simulation Flow

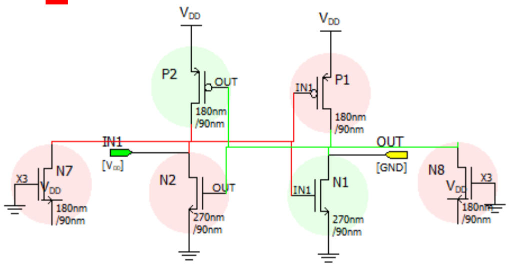
1. Circuit implementation
2. Layout design
3. SEE Analysis
4. Cross Section Results

4





1



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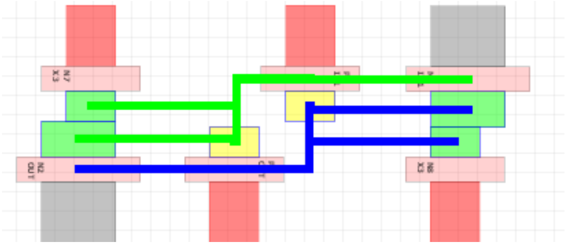

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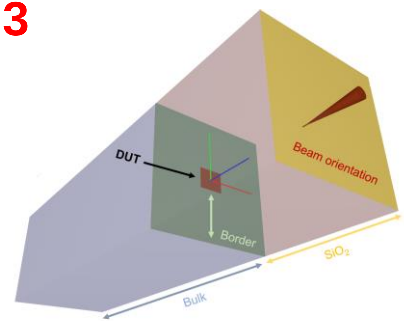
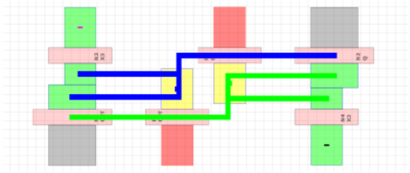
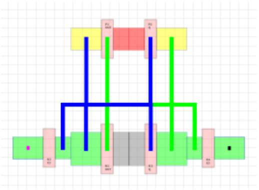
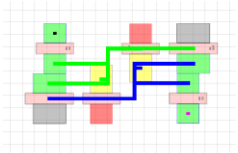
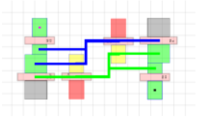
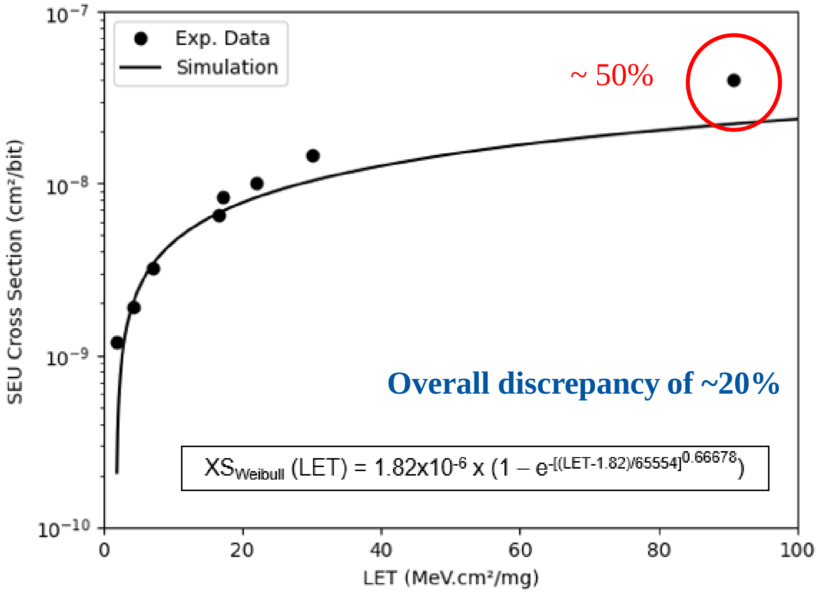


Technology	C_{out} (fF)	W/L (nm/nm)	P-Well doping (at/cm^3)	N-Well doping (at/cm^3)	Layout
90 nm	1.20	180/90	1.43E18	1.94E18	
65 nm	0.72	120/65	1.87E18	2.54E18	
45 nm	0.53	90/45	2.44E18	3.24E18	
32 nm	0.36	64/32	3.10E18	4.2E18	

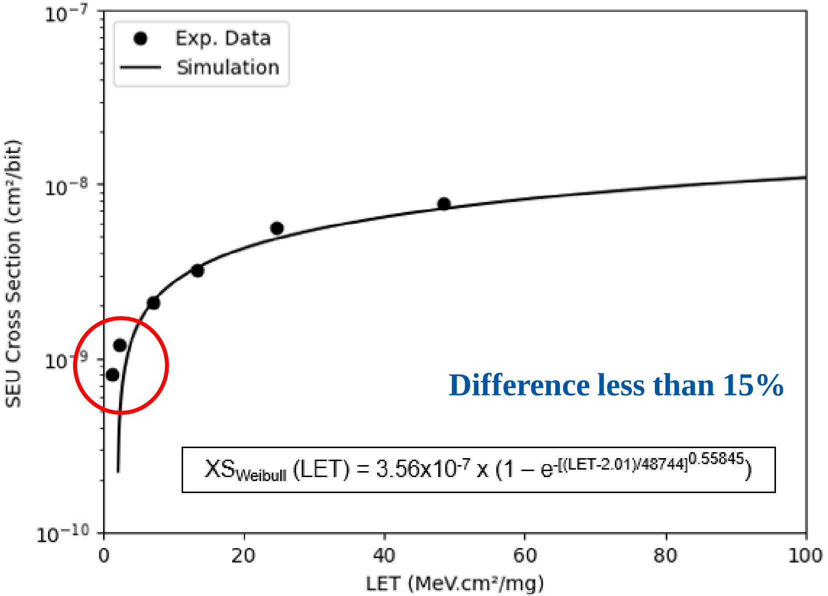
Results

Heavy ions SEU cross-section for **90 nm** SRAM. The experimental results are taken from [1].



[1] G. M. Swift, et al, "Static Upset Characteristics of the 90nm Virtex-4QV FPGAs," *2008 IEEE Radiation Effects Data Workshop*, 2008, pp. 98-105, doi: 10.1109/REDW.2008.25.

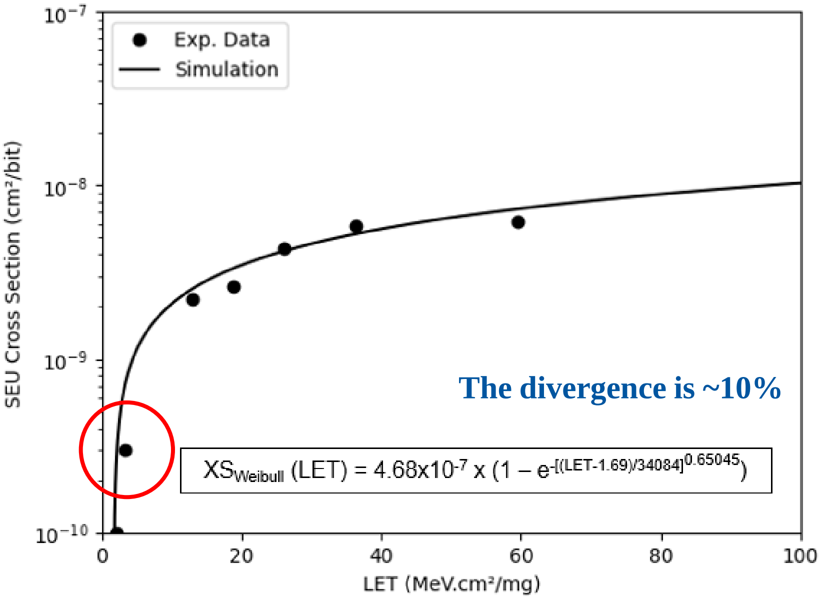
Heavy ion SEU cross-section for **65 nm** SRAM. The experimental data are taken from [2].



[2] J. Wang, et al, "Study of SEU Sensitivity of SRAM-Based Radiation Monitors in 65-nm CMOS," *IEEE Trans. Nucl. Sci. (TNS)*, vol. 68, no. 5, pp. 913-920, May 2021, doi:10.1109/TNS.2021.3072328.

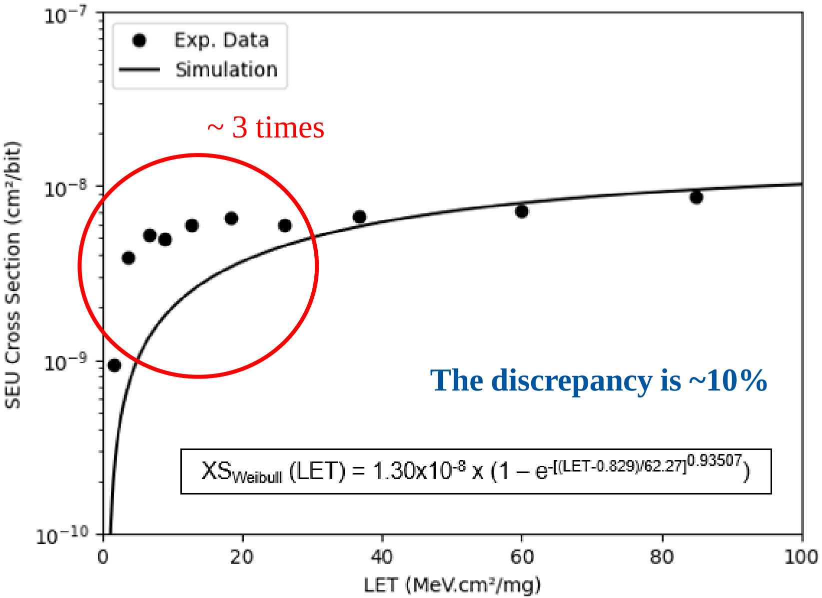
Results

Heavy ion SEU cross-section for **45 nm** SRAM. The experimental results are taken from [3].



[3] C. Weulersse, et al, "Prediction of proton cross sections for SEU in SRAMs and SDRAMs using the METIS engineer tool," *Mic. Rel.*, vol. 55, nos. 9–10, pp. 1491–1495, Aug. 2015, doi: 10.1016/j.microrel.2015.06.117

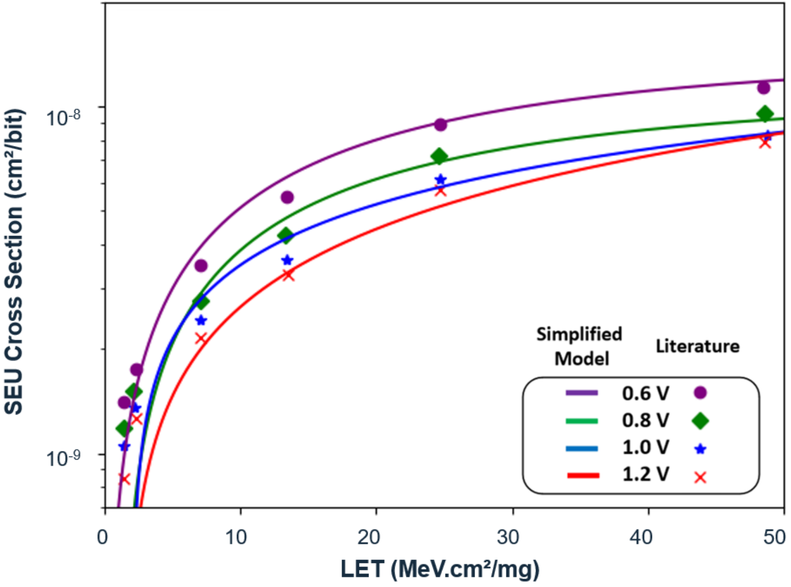
Heavy ion SEU cross-section for **32 nm** SRAM. The experimental data are taken from [4].



[4] S. Uznanski, et al, "Heavy Ion Characterization and Monte Carlo Simulation on 32nm CMOS Bulk Technology," *IEEE Trans. Nucl. Sci. (TNS)*, vol. 58, no. 6, pp. 2652-2657, Dec. 2011, doi: 10.1109/TNS.2011.2170852.

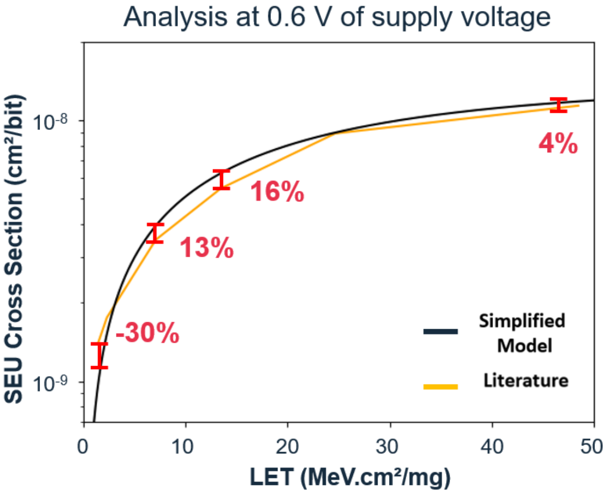
Results

Heavy ion SEU cross-section for 65 nm SRAM. The experimental data are taken from [2].



Decreasing Supply Voltage

Increasing Cross Section



Conclusions

In this work, a framework based on **a simplified electrical model** using Monte Carlo simulations to **predict the SEU cross-section** of SRAM cells was proposed.

The standard 6T SRAM cell was the DUT of this study and was evaluated at 90 nm, 65 nm, 45 nm, and 32 nm bulk-planar CMOS technology.

The results confirm a **good agreement with the experimental data**, showing that the **proposed model can accurately predict the SEU mechanism**.

Considering the voltage scaling, the simulations **results reproduce the trends in the literature**.

Conclusions

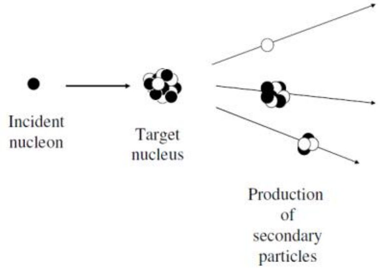
The most divergences found in the results can be explained by the following factors:

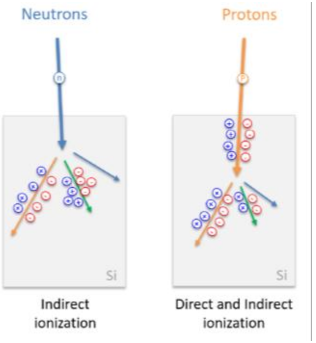
- The predictive **SPICE models used to extract basic information** from the technologies for not having access to the technology PDK of the DUT;
- The **sizing of the cells** that was standardized in the **same ratio** for the simulations, but which can vary a lot in commercial cells depending on the manufacturer and design requirements;
- The **layout rules and the approach used in the simulations** in relation to the tested commercial cells as there may be differences depending on the manufacturer.

The results show that the prediction for more consolidated technologies can be easily approximated, but for modern technologies the dependence of precise parameters increases.

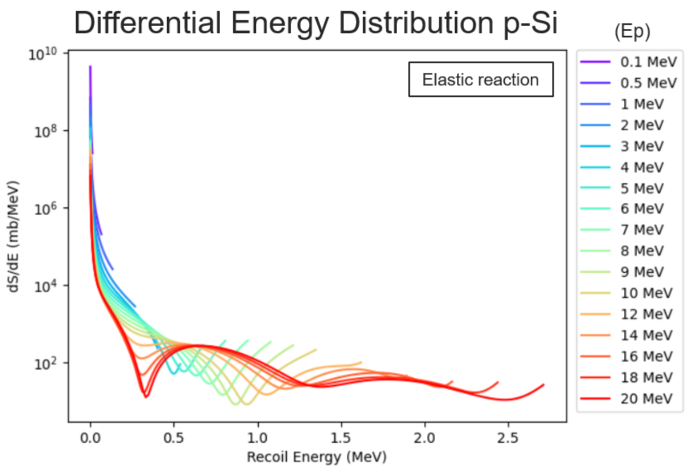
Next Steps

Evaluate the proton and neutron SEU Cross section prediction

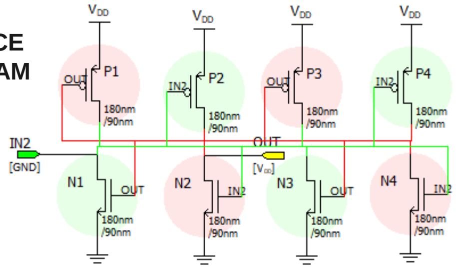


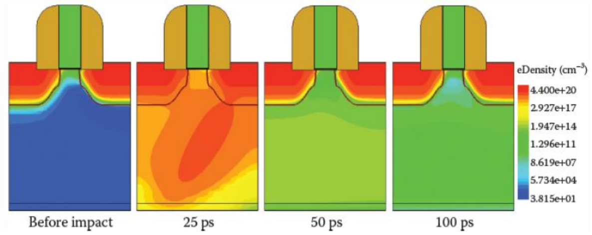


$$SER_{FIT} = 10^{9} \times \int_{E_{th}}^{E_{max}} \frac{d\Phi(E)}{dE} \times \sigma_{appx}(E)\, dE$$



DICE SRAM





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Thank you all for the attention

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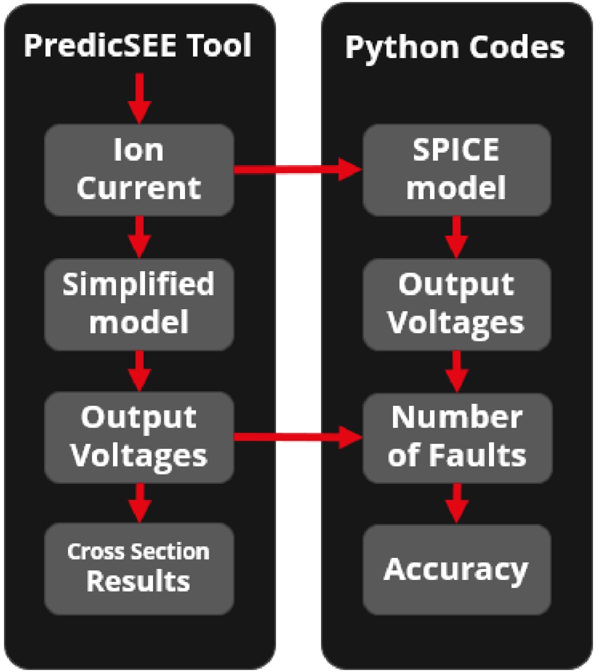
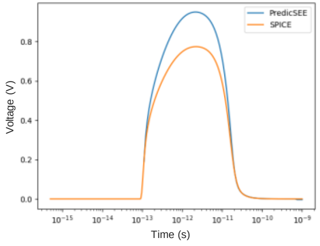
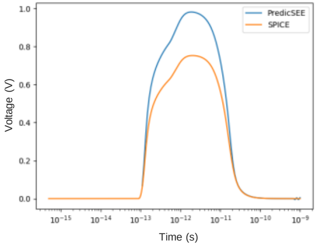
Extra




```python
from Libs import config, predicsee, general, spice

# Compare number of faults between PredicSEE and Spice simulations
def run_check_accurace():
    # 0-let_list, 1-see_type, 2-circuit_name, 3-tecnologie, 4-size_min, 5-input_signal
    # 6-output_event, 7-circuit_info, 8-supply_voltage, 9-PATH
    c = config.config_accurace()
    for let in c[0]:
        parameters = predicsee.set_param(c[1], c[2], c[3], c[4], c[5], c[6], c[7], c[8], c[9], let)
        predicsee.check_accurance(parameters)

# Move predicsee output files to folder structure
def run_move_files():
    # 0-predicsee_path, 1-sub_ids, 2-let_list, 3-csv_file
    c = config.config_move_files_preedicsee()
    general.delete_all_files(c[3])
    for i in range(len(c[2])-1):
        c[1].append(str(int(c[1][0])+i+1))
    predicsee.get_result_files(c[0], c[3], c[1])
```

```
LET=7.6
LOADING: 23 <--> 74

EVENTS:
        SPICE     - 9
     PredicSEE    - 35
```

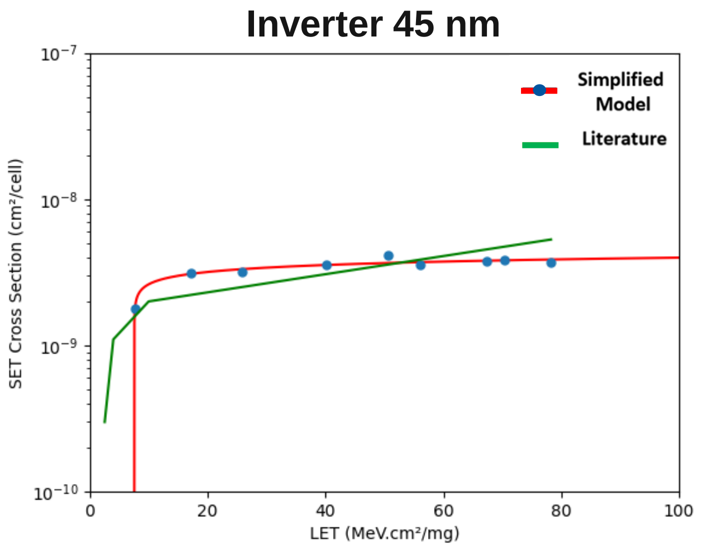


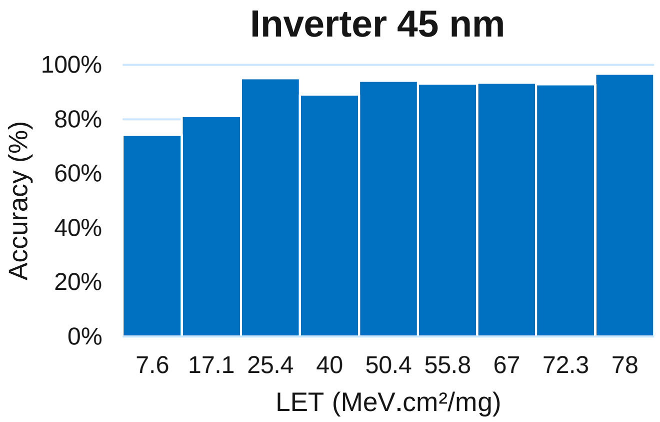


Extra

Simplified model accuracy compared to SPICE simulations

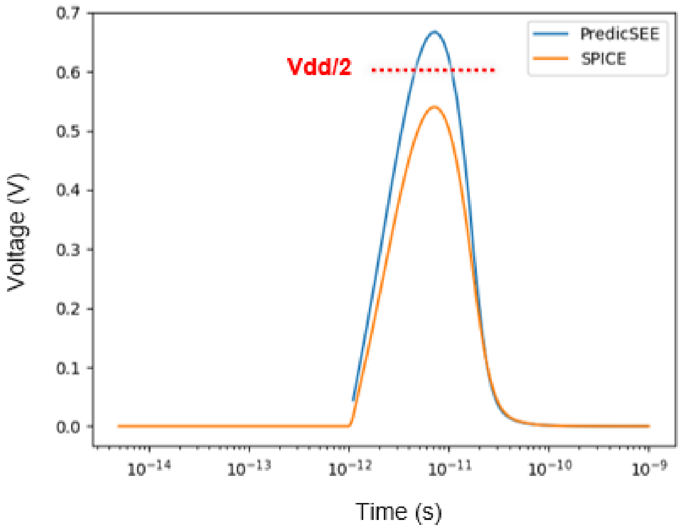
$$\text{Accuracy} = \frac{\text{Faults using SPICE}}{\text{Faults using Model}}$$

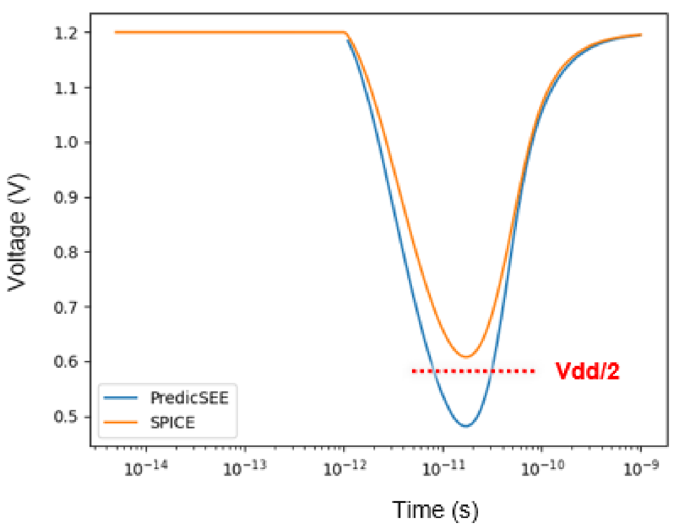




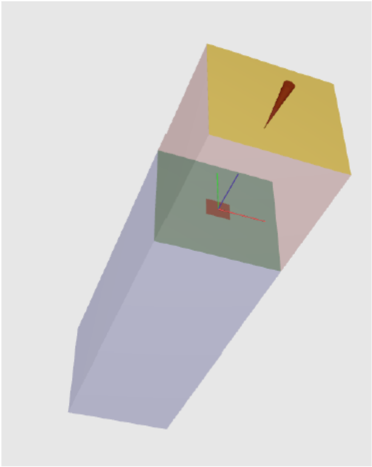
Extra

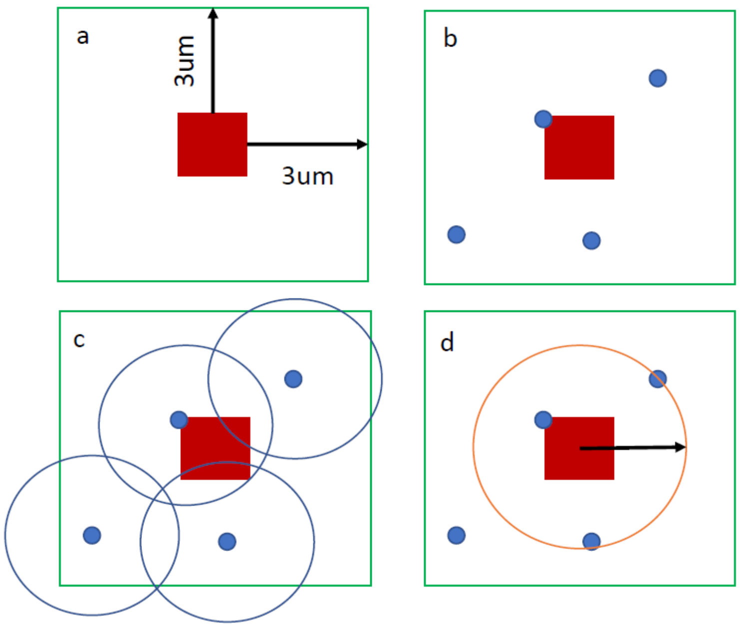
SET events that generated an output voltage variation above or below than half of the supply voltage are considered a fault.





Extra

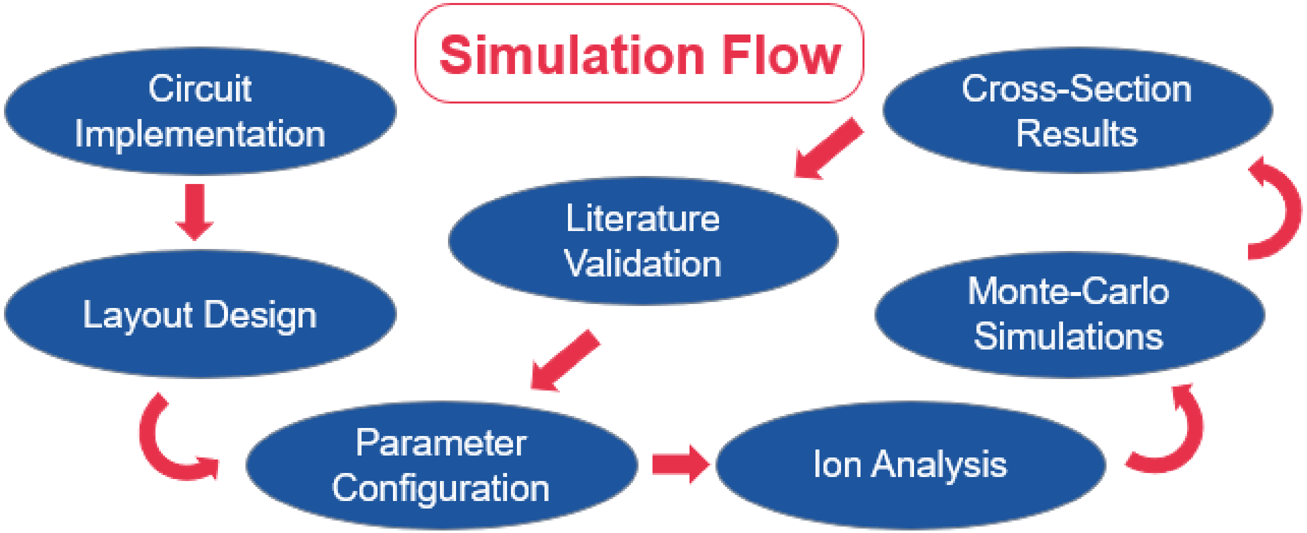




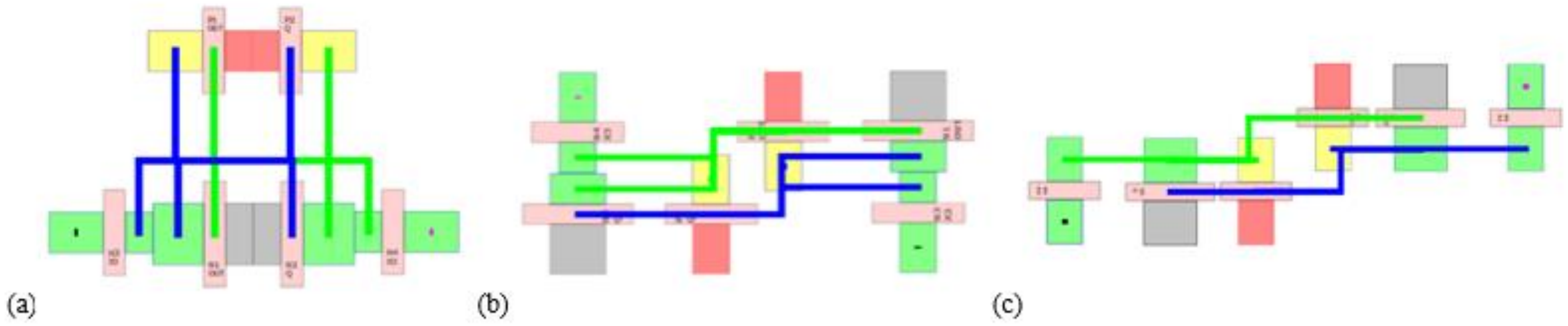
$$\sigma = \pi r^2$$

$$r = \sqrt{\frac{\sigma}{\pi}}$$

Extra


Simulation Flow
Circuit Implementation
Layout Design
Parameter Configuration
Literature Validation
Ion Analysis
Monte-Carlo Simulations
Cross-Section Results

Extra



Three different layout designs that can be applied to 6T SRAM cell:
(a) “tall” design; (b) “thin” design; (c) “ultra-thin” design.