Fast CMOS Binary Front-End for ATLAS SCT & TOTEM

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Introduction

1. Design follows the specifications for readout chip for ATLAS SCT
   - ENC ~1500e- @ 20pF input capacitance
   - Shaping with ~20ns peaking time
   - Time walk for 1.2 – 10 fC signal: <16 ns @ 1 fC threshold
   - Matching of the comparator: better than 5% of 1 fC signal (rms spread) → 5bit Trim DAC for each channel with range ~40mV (0.8fC)

2. Special effort on minimization of power and current consumption keeping the required noise and timing performance (can work down to 1.5mW/channel)
Front End prototypes

1. AC version (preamp & shaper AC coupled):
   - ABCDS/FE chip – 64 channel of preamplifier/shaper/comparator
   - TOTEM VFAT

2. DC version (preamp & shaper DC coupled):
   - ABCDC1 – 16 channels of new preamplifier/shaper

Present version – new feature added to the comparator
   – trimming circuit, hysteresis
Architecture of the FE channel (present version)

One channel comprises:
- transimpedance preamplifier with active feedback
- shaper (2 stages)
- differential discriminator with trimming capability and small (~35mV) hysteresis.
Response of the preamplifier/shaper (ABCDC1 chip – DC version)

Response of the preamplifier/shaper loaded with 20pF to 3.5fC input signal.

ENC: 1500e-   Peaking Time: 22ns
Input transistor bias: 300µA
Total current consumption of channel: 600µA
Total power consumption: 1.5mW
ENC as a function of input capacitance – ABCDC1 chip

Good agreement of the measured data (markers) with the noise model (lines)
ENC @ 20pF & 300µA input transistor current: ~1500e-
ENC @ 20pF & 600µA: < 1200e-
Peaking Time as a function of input capacitance – ABCDC1 chip

C_{detector} = 20\text{pF} \quad \text{Peaking Time: 21 - 22ns (600 - 300\text{µA} bias)}

Small variation (<100\text{ps/pF}) \rightarrow \text{low input impedance (100 - 150\text{Ω @ 10 MHz})}
Dynamic range – ABCDS/FE (AC version)

For 0 – 12 fC input signal the integral nonlinearity error < 5%
Full range of corner parameters (±3σ) and 2-2.5V range power supply
Full chain measurements – ABCDS/FE

Good agreement with the measurement of the analogue part
Focus on matching performance (56 channels on chip)

Full chain gain 60mV/fC
Gain rms < 1%

Offset rms < 3mV
(< 5% of 1 fC response)
Full chain measurements – Time Walk – ABCDS/FE

12.4ns Time walk for 1.2 – 12fC @ 1fC threshold
Good agreement with simulation
Spread due to offset mismatch (common threshold)
Summary of results from old prototypes

- For a detector of 20pF ENC<1500e- @ Iinput=300µA (Power=1.5mW)
- Peaking Time ~22ns, Δtpeak < 100ps/pF (low input impedance)
- Dynamic range 12fC, linearity better than 5% for wide range of bias and corner parameters
- Good uniformity of gain (rms<1%) and offset (rms<5% of 1fC response) → version with no Trim DAC
Analogue parameters from simulation

Simulation for nominal bias and input load (450uA input transistor current, 20pF input capacitance)

- Peaking time: 22ns
- Pulse gain (comparator input): 52mV/fC
- 1fC equivalent threshold: 50mV
- Walk for 1.25 – 16fC signal @ 1fC threshold: 12.5ns
Layout of the FE chip

- 128 regular channels
- 1 test channel with analogue outputs (after 1st stage of discriminator; possibility of tests of TRIM DAC)
- Bias generators
- Decoupling capacitors
Internal decoupling of the bias lines

- Cascode load bias 1 & 2: 2x 290pF (170pF in channels)
- Cascode bias voltage: 340pF (299pf in channels)
- Preamp buffer bias: 120pF (96pF in channels)
- Preamp feedback voltage: 510pF (225pF in channels)
- Feedback current: 120pF (119pF in channels)
- Shaper bias: 320pF (320pF in channels)
- Reference voltage for diff pair: 650pF (512pF in channels)
- Diff pair bias: 360pF (256pF in channels)
- VT1&VT2 to VCC: 2x 43pF (0pF in channels)
- VT1 to VT2: 56pF (56pF in channels)
PSRR simulation

Transistor Response

\[ \text{Cascode before buffer} \]

\[ \text{Cascode after buffer} \]

\[ \text{Shaper output} \]

\[ \text{Comparator input (differential)} \]

PSRR @ 30MHz > -3.5dB (worst case)

A: (120.226M 265.167m)  delta: (-120.226M -212.349m)  
B: (257.7n 55.8179m)  slope: 1.76624n
PSRR simulation (2)

Comparator input:
3.5fC signal
10MHz, 5mV pk-pk interference on Vcc
Verifications

- Hercules DRC OK
- LVS OK
- Simulation of the top cell (analogue) OK