“Radiation Tolerant Dual-Ported Static RAM macro blocks for the TOTEM VFAT chip.”

VFAT chip Design Review

8/3/2006
Overview

- The CERN SRAM macro cell
- Two SRAM macro cells for the VFAT chip
Motive of Work

Several Front-End ASICs for the LHC detectors are using the CERN DSM Design Kit in 0.25 μm commercial CMOS technology.

Many ASICs require the use of rather large memories in Readout Pipelines, Readout Buffers and FIFOs.

CERN DSM Design Kit lacks design automation tools for generating customized SRAM blocks.

Built an SRAM macro-cell that can be configured in terms of word counts and bit organization by means of simple floorplanning procedures.

Initially designed for the needs of the “Kchip” Front-End ASIC used in the CMS ECAL Preshower detector.
CERN-SRAM specifications

- **Scalable Design**
  - Configurable Bit organization (n x 9-bit).
  - Configurable Memory Size (128 – 4Kwords).

- **Synchronous Dual-Port Operation**
  - Permits Read/Write operations on the same clock cycle.
  - Typical Operating Frequency: 40 MHz.

- **Low Power Design**
  - Full Static Operation.
  - Divided Wordline Decoding.

- **Radiation Tolerant Design**
To minimize the macro-cell area a Single Port memory cell is used based on a conventional cross-coupled inverter scheme.

Gain in Memory Cell Layout Area = 18%
**SRAM Block Diagram**

**Dual-port** functionality is realized with a time sharing access mechanism.

- Registered Inputs
- Latched Outputs
Replica Techniques

Scalability
- Wordline select time depends on the size of the memory.
- Dummy Wordline with replica memory cells to track the wordline charge-discharge time.

Bitline Timing
- Dummy Bitlines to mimic the delay of the bitline path over all conditions.
Replica Techniques
Cell Library

Size Configurable

- Data Input Register
- Address Mux Register
- Column Decoder
- Block Pre-Decoder
- Output Data Latche

Fixed Layout

- Row Decoder
- WordLine Buffers
- SRAM column, 128 x 9bits
  (50.4 μm x 1086.2 μm)
- Timing logic

Mar. 8, 2006

Kostas Kloukinas

PH/MIC-DG
Floorplanning

Write drv.
Write drv.
Write drv.
Write drv.
Write drv.
Write drv.
Write drv.
Write drv.
Write drv.
Write drv.

Read logic
Read logic
Read logic
Read logic
Read logic
Read logic
Read logic
Read logic
Read logic
Read logic

Block

Row Decoder (128 rows)

Column Decoder

DIn
DOut

PreDecoder
Address Reg

Timing

Address Reg

vdd
gnd
SRAM 4K X 9bits
Power dissipation

Power dissipation of macro-cell.

Test chip: 4Kwords x 9bits

<table>
<thead>
<tr>
<th>Operation</th>
<th>Power (μW/MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standby</td>
<td>0.10</td>
</tr>
<tr>
<td>Idle</td>
<td>1.90</td>
</tr>
<tr>
<td>Read</td>
<td>7.40</td>
</tr>
<tr>
<td>Write</td>
<td>10.60</td>
</tr>
<tr>
<td>Read/Write</td>
<td>14.05</td>
</tr>
</tbody>
</table>

Test Conditions

<table>
<thead>
<tr>
<th>Operation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standby</td>
<td>No operation, addr. &amp; data static.</td>
</tr>
<tr>
<td>Idle</td>
<td>No operation, addr. &amp; data changing in every clk cycle</td>
</tr>
<tr>
<td>Read</td>
<td>checkerboard data pattern</td>
</tr>
<tr>
<td>Write</td>
<td>checkerboard data pattern</td>
</tr>
<tr>
<td>Read/Write</td>
<td>checkerboard data pattern</td>
</tr>
</tbody>
</table>
CERN SRAM popularity!

- **ATLAS MCC chip**
  - Memory configuration: 128 x 27bit
  - Detector: ATLAS PIXEL
  - Lab: INFN Genova

- **ALICE AMBRA chip**
  - Memory configuration: 16K X 9 bits
  - Detector: ALICE Silicon Drift Det.
  - Lab: INFN Torino

- **ALICE CARLOS chip**
  - Memory configuration: 256 X 9 bits
  - Detector: ALICE Silicon Drift Det.
  - Lab: INFN Bologna

- **LHCb SYNC chip**
  - Memory configuration: 256 X 9 bits
  - Detector: LHCb muon system
  - Lab: INFN Cagliari

- **ATLAS SCAC chip**
  - Memory configuration: 128 x 18bit
  - Detector: ATLAS tracker
  - Lab: NEVIS Labs

- **ATLAS DTMROC chip**
  - Memory configuration: 128 x 153 bits
  - Detector: ATLAS TRT
  - Lab: CERN

- **CMS Kchip**
  - Memory configuration: 2K x 18 bits
  - Detector: CMS Preshower
  - Lab: CERN

- **CMS FENIX chip**
  - Memory configuration: 256 x 27 bits
  - Detector: CMS ECAL
  - Lab: CERN
Two macro cells of different configurations are used in the design of the VFAT chip:
- SRAM 128 X 180 bits
- SRAM 256 X 144 bits

Digital Models for Verilog simulations and Logic synthesis were provided since the early stages of the design of the VFAT chip.
SRAM macros for VFAT

Special Layout Considerations for the VFAT SRAM macro cells

- The large width of the data I/O busses necessitated the placement of the Data I/O ports to be on the top and the bottom of the SRAM array instead of sideways.

- Macro blocks that had to be modified to match with the “layout pitch” of the SRAM array cells:
  - Data Input register
  - Data Output latch
SRAM 128X180

- SRAM 128 X 180-bits
  - = 23,040 bits
  - Size: 1,270μm X 1,450μm
  - Area: ~1.8mm²

- Design Status (28/2/06)
  - Layout: Ready
  - DRC: O.K.
  - LVS: O.K.
SRAM 256X144

- SRAM 256 X 144-bits
  = 36,864 bits
  Size: 1,925μm X 1,450μm
  Area: ~2.8mm²

- Design Status (28/2/06)
  Layout: Ready
  DRC: O.K.
  LVS: O.K.
Separate substrate ground

Is it really necessary for the SRAM macro cells?
- Difficult to give a firm answer!

- Most of the switching activity is taking place in the Data Input register and the Data Output latch.
  - These two blocks can easily be modified to separate the substrate ground from the digital current return ground. Cells from the digital standard cell library have been used to compose these two blocks.

- In the SRAM array the “density” of the digital switching activity is very small. Only one wordline over 127 in total is activated on every memory access cycle. Moreover the SRAM cells are by design weak current drivers.
  - Rework of the layout design for the SRAM array cells (SRAM cell, Wordline decoder, Wordline buffers, Write drivers, Read logic) is not trivial and raises some concerns about the performance of the “modified SRAM” macro cell that should be addressed.
The design of the two “standard” SRAM macro cells is finished.

Layout work for the “modified” macro cells is now in progress.

Final Verification of the “modified” macro cells (DRC, LVS, HSPICE?)