VFAT Design Review

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Digital Part *(Technology IBM 0.25um)*

- Command Decoder
- Control Logic
- Data Formatter
- Hit Counter
OUTLINE

- VFAT Logic Part Functionality
  - Single Event Upset Protection
  - Design For Testability
  - Design to Reduce Noise
- VFAT Design Flow
- Topology and Technical data
- Verification and simulation
- To Do
VFAT Functionality Logic Part

- Command decoder
  - Decoding the trigger commands (T1).

- Control Logic
  - Read Data from Front End
    - All channels stored every clock cycle in First SRAM (256x144bits)
  - Tracking Functions
    - Triggered columns stored in Second SRAM (128x180bits)
    - Assign a Bunch Crossing Number (BCN) and Event Number (EN)

- Data Formatter
  - Link Protocol for transmission through a Gigabit Optical Link

- Hit Counter
VFAT Logic Part Block Diagram

Data SRAM1
256x144

Data 128

CalPulse
CLK
T1
Reset

Command Decoder

Write State Machine

Flags State Machine

Control Logic

Hit Counter 24-bit

I2C

Ham Enc.

Ham Dec.

Data 128

Data 128 +
EN 8 + BCN 12

Data Formatter
Serial Output

Triggered Data
SRAM2
128x180

Triggered Data
148

SEU Counter
8-bit

Result SEUCounter

DataValid
Data Out

... to GOL

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Command Decoder

- The Command Decoder bloc decodes the trigger commands (T1).

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Command Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>LV1A</td>
<td>Trigger Level 1 Accept</td>
</tr>
<tr>
<td>111</td>
<td>CalPulse</td>
<td>Timing of Calibration Pulse</td>
</tr>
<tr>
<td>110</td>
<td>ReSync</td>
<td>Resynchronisation of all state machines</td>
</tr>
<tr>
<td>101</td>
<td>BC0</td>
<td>Bunch Crossing Zero identifier</td>
</tr>
</tbody>
</table>

- T1 signal is an encoded signal which contains commands all synchronous with Main Clock.
  - **LV1A**: Increments the EC and transfer to SRAM2 the Data corresponding to the triggered time.
  - **CalPulse**: Generate a calibration timing pulse of 1us applying to input channel
  - **Resynch**: Resynchronize of all state machines, reset all counter and erase all data stored
  - **BC0**: Resets the EC and BC counters
Control Logic: Write SM - Flags SM

- Max Latency Trigger LV1: 6.4us
- Latency: 8 bits programmable from 1 to 256 Tclk (up to 6.4 us)
Control Logic : Write SM - Flags SM

Timing Diagram for the Write State Machine
Data Formatter

Chip ID Flags:
- full, AFull, Empty
- BC, EN Data triggered

Calculation of error-checking code to verify integrity of word transmit

- As long as SRAM2 is not empty, data will exit one after the other following a FIFO order. If no data, DataOut and DataValid are low.
- Data Out and Data Valid are clocked on fall edge clock

15 - - - - - - - - - - - - 0

101X BCN<11:0>
110X EN<7:0> Flags<3:0>
111X CHIP ID<11:0>

Channel Data <127:0>
CRC 16-bit checksum <16:0>

Data format for 1 LV1 (Data is serialised MSB first @ 40 MHz)

IDLE (2xTclk)
Cyclic Redundancy Check

- Used to verify integrity of Data transmitted. With this type of control error, the data encoded can be of any length. The generator polynomial used is type CCIT-V41 (x^{16}+x^{12}+x^{5}+1) \rightarrow G(X)=h^{1021} and data are treated 16bit by 16bit.

  First 16-bit data

  Next 16-bit data

  Division polynomial
  \{Data;h^{0000}\} by G(X)

  Division polynomial
  \{Data;checksum\} by G(X)

  Rest of Division
  Checksum

  Initial data

  Data transmit

  Checksum

- To verify transmission, the receptor make inverse operation by dividing (Data +checksum) by G(X) (polynomial division). If the result is 0, the data is good.
Hit Counter

Hit from Fast Or

Counter Hit 24 bit
Hit pulse length : 1-8xTclk

Output Reg 24 bit

Counter Time 32 bit

Reset Counters

Transfer value of Hit Counter

yes

Counter Time > CT ?

I2C

I2C

MSClueLengh 3bit

CT - 2bit

Bloc independent synthesized and P&R separately to respect floor plan of chip VFAT

<table>
<thead>
<tr>
<th>CT 2-bit</th>
<th>Window Time</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>h'ff</td>
<td>6.4 us</td>
</tr>
<tr>
<td>1</td>
<td>h'ffff</td>
<td>1.6 ms</td>
</tr>
<tr>
<td>2</td>
<td>h'fFFFf</td>
<td>0.4 s</td>
</tr>
<tr>
<td>3</td>
<td>h'FFFFf</td>
<td>107 s</td>
</tr>
</tbody>
</table>
Design For Testability

- Goal:
  - For manufacturing test
  - Help to debug design (we hope not to do it!)

Test modules integrated are:

- Scan-Path
- Built In Self Test Memory (BIST)
- Link Test: specific “Link Test packet”.
- Probe internal node
Scan Path

- For design debugging and production testing
- Scan Path uses the 40 MHz system clock

- One Scan Chain (except module BIST)
  - Number of registers: 1068 Logic Part, 252 Hit-Counter

- Specific I/O pins:
  - Test_In, Test_Out and Enable/Disable the scan mode

- No test vector generated (no licence for ATPG Tools) but order of registers are knew (provide file)
BIST

Built In Self Test both memory

- The test are
  - All0, All1: verification stuck at 0, stuck at 1 (vector 000/111)
  - Checker board: verification short circuit between registers (vector 010101/101010)
  - Marching 0, Marching 1: verification crosstalk between line (vector 0001/0010/0100-1110/1101/1011)

- Specific I/O pins: Reset, Enable, Start, Result, Finish
- Test both memory in parallel: time test 1.98ms

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The Data Formatter features a “Link Test” mode where Data traffic can be generated continuously using a specific “Link Test packet”.

This packet in ASCII code is:

“WHERE IS THE HIGGS ? 😊 + CRC”

Notice: Test data packet hardwired.
Probe NODE

- Output Pads to probe internal nodes

- Observable nodes are
  - Read/Write command SRAMs
  - Outputs Command decoder: LV1, CalPulse, Resync, BC0
  - Flags hamming error
  - Flags: Full, AFull, Empty

- Specific Pin to Enable/Disable probe Pads
SEU Protection

- Design Cells with MOS enclosed
- Hamming Encoding for SRAM
- Triplicated all State Machine
Hamming Encoding

- Data spent most of their time waiting in the FIFOs.
  - Protect SRAM against SEUs.

- Use Hamming encoding to protect the contents of the FIFOs.
  - Capability:
    - Correct **single errors** in the same word.
    - Detect **double errors** in the same word and flag the data packet.
      - In case of a multiple-error the CRC field is set to FFFFh for that particular packet.
Triple Module Redundancy

- Protect Control Logic using Triple Module Redundancy
  - All State Machines and Configuration Registers have been triplicated.

- Leave Data Path unprotected
  - SEU errors affect the integrity of small amount of information and does not lead to a loss of readout synchronisation.
Triplicated State Machine

Erroneous state machine will recover within a maximum of 3 clock cycles.

Triplicated logic was described in Verilog and has been synthesized.

Source KCHIP (Kostas K)

F: combinatorial logic
SM: state memory
SEU Counter

SEU Counter block **count flags error** from all triplicate SM when a discrepancy in majority voter appear

- Count from 0 to FF and stop at FF – results accessible via the I²C

- Goal:
  - Diagnostic tools for understanding the SEU environment in the experiment
  - Can be used to detect a « stuck at » fault (counter clocked to FF)
Design To Reduce Noise

- All Cells and Memory with separate ground and substrate (gnd & gndd)

- In Normal mode:
  - Disable signal on probe pads
  - Disable signal test-out of Scan-Path
VFAT Design Flow

Synthesis with Synopsys (design compiler V2001.08-SP2)
- Method Mixed Compile
  - Virtual clock – set_clock_uncertainty : 1ns
- Design Flow is scripting

Place & Route with Silicon Ensemble V 5.2
- Clock tree with CTGen
- Design Flow is scripting
LAYOUT Logic Part

- **Number of Digital Standard cells**
  - Registers: 1120
  - Cells: 21,7K
    (42K equ. Nand2)
- **Clock tree statistics**
  - Number of buffers: 370
  - Number of Levels: 10
  - Max. delay: 1.6ns
  - Max. skew: 0.27ns
- **I/O pins**
  - Number I/O: 191
  - All output buffered
- **Consumption estimate**
  - 250mW @ 2.5V
- **Special Macro Cells**
  - 256 x 144 bit, dual-port SRAM
  - 128 x 180 bit, dual-port SRAM

SIZE: 5.2 x 3.4 mm²

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LAYOUT Hit Counter

- **Number of Digital Standard cells**
  - Registers: 250
  - Cells: 1,7K (4,7K equ. Nand2)

- **Clock tree statistics**
  - Number of buffers: 45
  - Number of Levels: 6
  - Max. delay: 0.475ns
  - Max. skew: 0.022ns

- **I/O pins**
  - Number I/O: 36
  - All output buffered

- **Consumption estimate**
  - 20mW @ 2.5V

SIZE: 0.7 x 1.4 mm²
Timing analysis - Consumption

- All logic is **synchronous on rise edge** of clock 40 MHz (except outputs of DataFormatter on fall edge)

- The **Maximum Frequency** simulation after PR with parasitic is **up to 71 MHz** in worst case

- **Consumption total estimate**: 270mW
  - Estimate because cell power dissipation is not modelled
  - Estimate by 2 way:
    - \( P = ncV^2f \) (with \( n \): number gates, \( c \): entry gate capacitance, \( V \):supply and \( f \): frequency)
    - Extrapolation after HSpice simulation of small representative block
Verification and Simulation

- **Integrity of RTL Code** has been verified by Conformal 5.1 (Cadence) and State machine visualised by Visual-HDL

- **Simulation at 3 levels (NC verilog)**
  - Simulation Behavioral: RTL Code with delay arbitrary
  - Simulation Code synthesized with SDF file (Parasitic extraction based on wire load model)
  - Simulation after Place & Route with SDF file (generation SDF and static timing analysis with Pearl)
Command Decoder simulation

Decoding of 4 command from T1

Notice: the SM exclude wrong word and is resynchronised after 3 low values consecutives of T1

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Logic Part - Simulation

Pulse on Resynch, Data SRAM2 cleared and flag Empty high

192 Tclk (F=50Mhz)

After Resynch, waiting Latency before read Sram1. When Flag Empty low, data from SRAM 2 is transmitted.
Logic Part - Simulation

- To ensure good functionality, elaboration of script to read simulation file: decoding data from DataOut and compare with a data target

*Below: Sample of script result @ 71 Mhz (Tclk=14ns) – Between 2 samples we have 194 Tclk.*

```plaintext
Test Data Formatter tri
*************************************************************************
TEST DataOut !!
time= 104526,
Data From DataOut = a090c0e4effffffffffffffffffffffffffffffffff9eba
Data Target DF1 = a090c0e4effffffffffffffffffffffffffffffffff9eba
Comparison Data Target & Data From DataOut =1
*************************************************************************

time= 107242,
Data From DataOut = a093e0f4eff22222222222222222222222222221f9594
Data Target DF1 = a093e0f4eff22222222222222222222222222221f9594
Comparison Data Target & Data From DataOut =1
*************************************************************************

time= 109998,
Data From DataOut = a096e102eff55555555555555555555555555555526574
Data Target DF1 = a096e102eff55555555555555555555555555555526574
Comparison Data Target & Data From DataOut =1
```

*Here, for the first data, BCN is h’090, EN h’0e, Flags h’4, ChipID h’fff and checksum h’9eba*
To Do !!

- Functional simulation of VFAT logic Part with complete VFAT2 chip (Front-End, I2C…)
- Verifying feature link test
- Place & Route with new SRAM (Design Flow is scripting)
- Static Timing analysis
- Simulation post layout (new parasitic extract)
- Import to Cadence, LVS DRC and filling
Thank you for your attention!