The MONOLITH project: towards **picosecond timing** with monolithic silicon

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UNIVERSITÉ DE GENÈVE

Swiss National Science Foundation

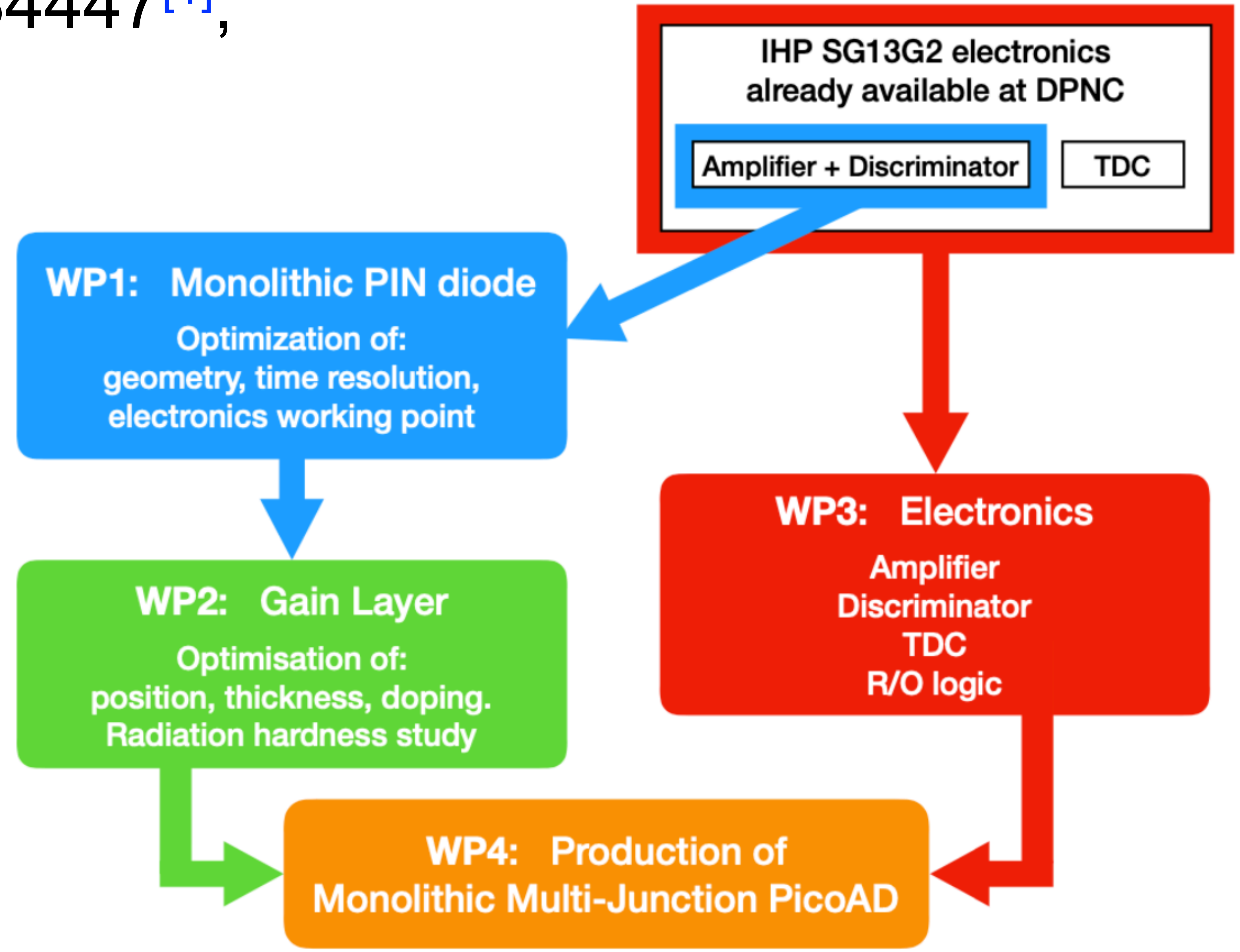
European Research Council
Established by the European Commission

The MONOLITH ERC Project

- Funded by the H2020 ERC Advanced grant 884447[1],
  July 2020 - June 2025

- Monolithic silicon sensor able to:
  - precisely measure 3D spatial position
  - provide picosecond-level time resolution

- Four working packages:
  1. Optimisation of **sensor geometry for timing**
  2. Optimisation of **gain layer, radiation hardness**
  3. Fast and low-noise **SiGe BiCMOS electronics**
  4. Novel sensor concept:
     the Picosecond Avalanche Detector (**PicoAD**)



[1] MONOLITH H2020 ERC Advanced Project Web Page - https://www.unige.ch/dpnc/en/groups/giuseppe-iacobucci/research/monolith-erc-advanced-project/

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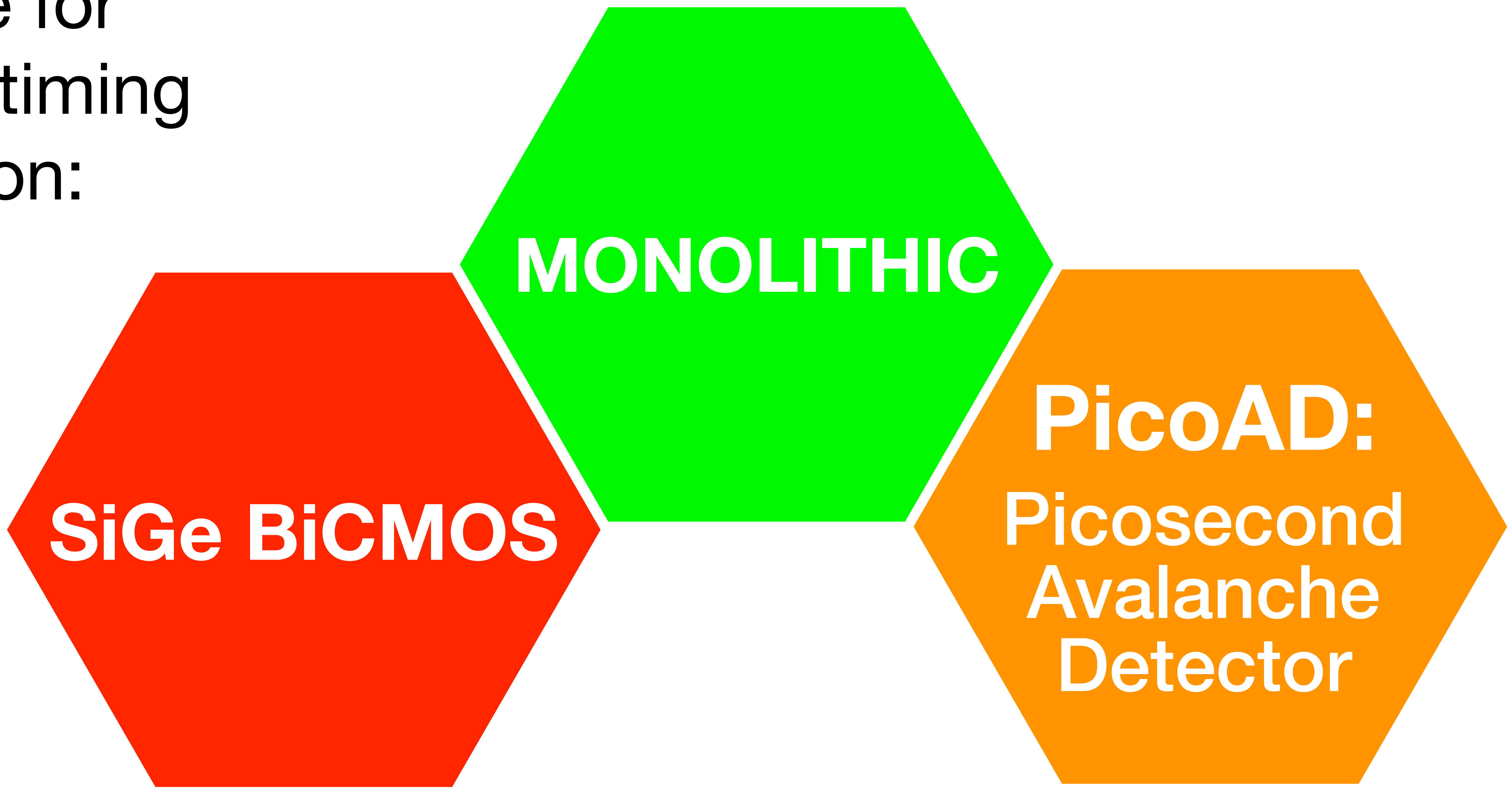
The MONOLITH Project

Our recipe for picosecond timing with silicon:



The UniGe Silicon Team

Giuseppe Iacobucci
- project P.I.
- System design

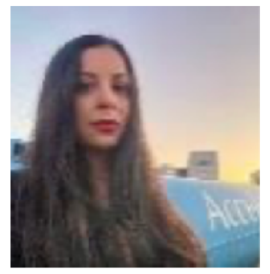
Thanushan Kugathasan
- Lead chip design
- Digital electronics

Stefano Zambito
- Laboratory tests
- Data analysis

Jordi Sabater Iglesias
- Detector simulation
- Laboratory tests

Matteo Milanesio
- Laboratory tests
- Data analysis

Antonio Picardi
- Chip design
- Firmware



Rafaella Kotitsa
- Sensor simulation
- Data analysis

Carlo Alberto Fenoglio
- Chip design
- Firmware

Lorenzo Paolozzi
- Sensor design
- Analog electronics

Roberto Cardella
- Sensor design
- Laboratory tests

Mateus Vicente
- System integration
- Laboratory tests

Chiara Magliocca
- Laboratory tests
- Data analysis

Théo Moretti
- Laboratory tests
- Data analysis

Jihad Saidi
- Laboratory tests
- Data analysis

Luca Iodice
- Chip design
- Firmware

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- Laboratory tests

Didier Ferrere
- System integration
- Laboratory tests

Yannick Favre
- Board design
- RO system

Sergio Gonzalez-Sevilla
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- Laboratory tests

Stéphane Débieux
- Board design
- RO system

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Marzio Nessi
CERN & UNIGE

Matteo Elviretti
IHP Mikroelektronik

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Sinergia

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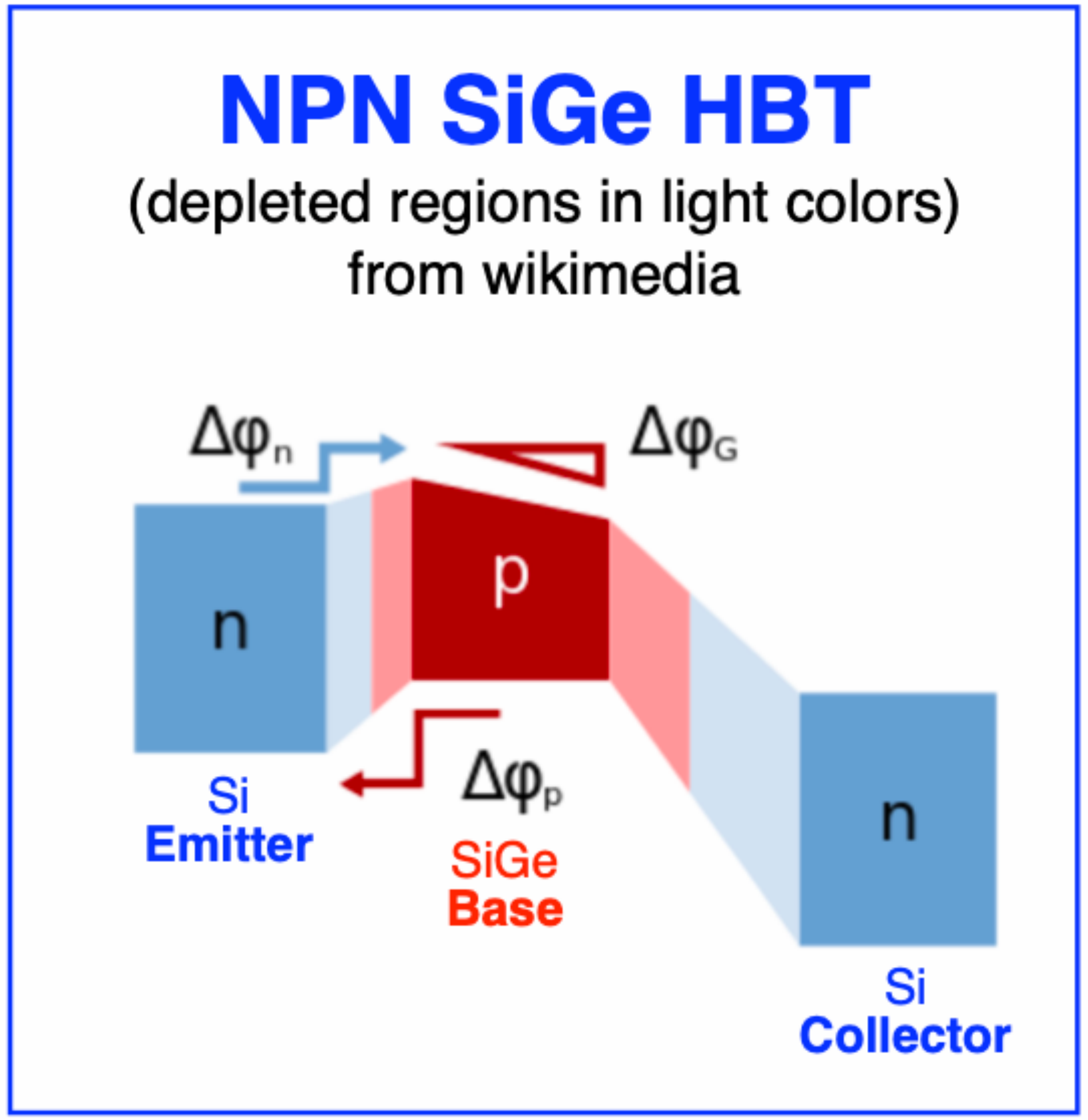
MONOLITH

SiGe BiCMOS Front-End Electronics



SiGe HBT = BJT with Germanium as base material.

Grading of Ge doping in base:

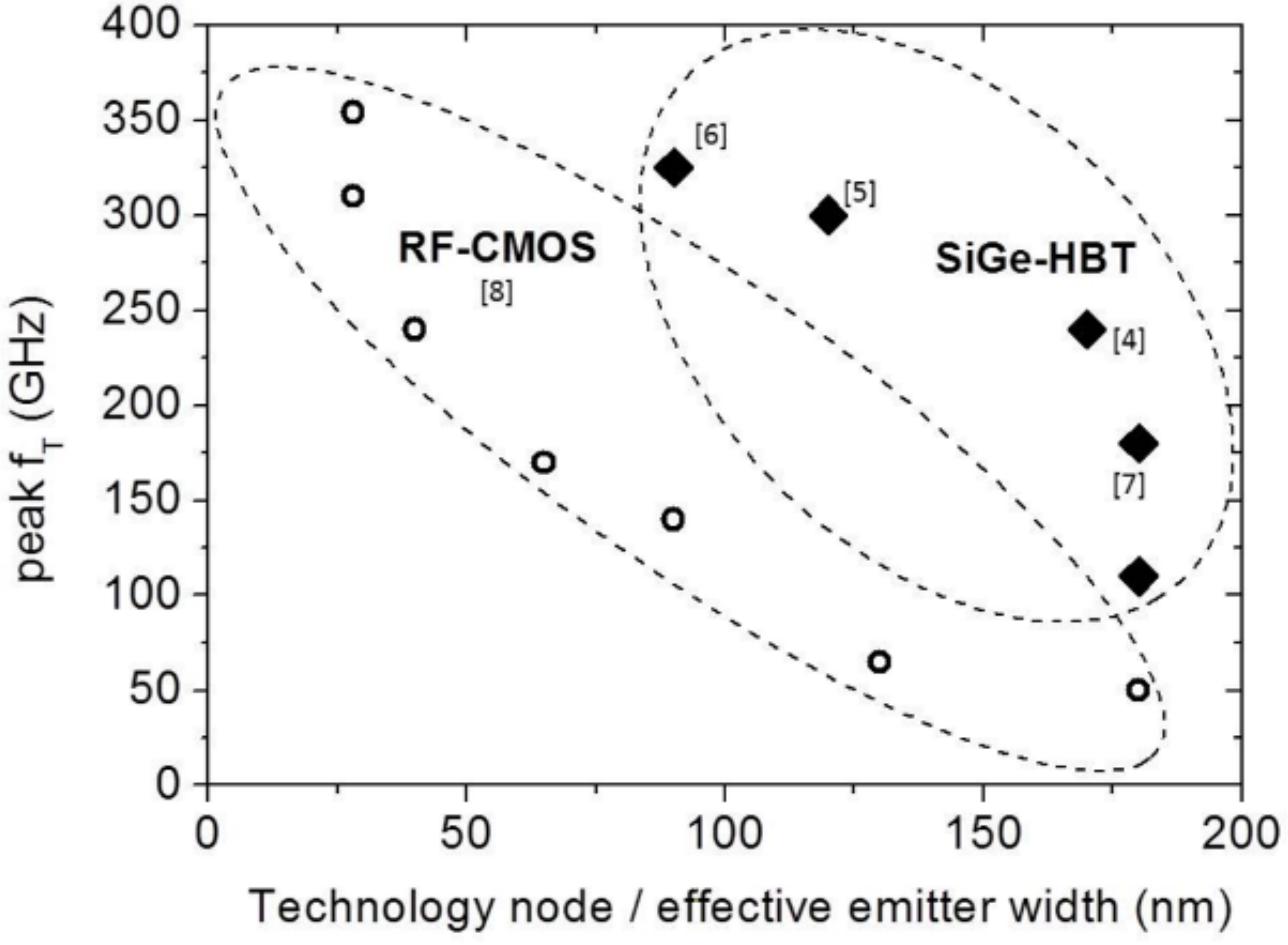
- charge-transport in base via **drift**
  - reduced charge-transit-time in base
  - **high current gain** β
- **High doping** in base is possible:
  - thinner base
  - **reduced base resistance** R_b

$$ENC_{series\ noise} \propto \sqrt{k_1 \frac{C_{tot}^2}{\beta} + k_2 R_b C_{tot}^2}$$

Leading-edge **IHP SG13G2** technology, **130 nm** process featuring **SiGe HBT**

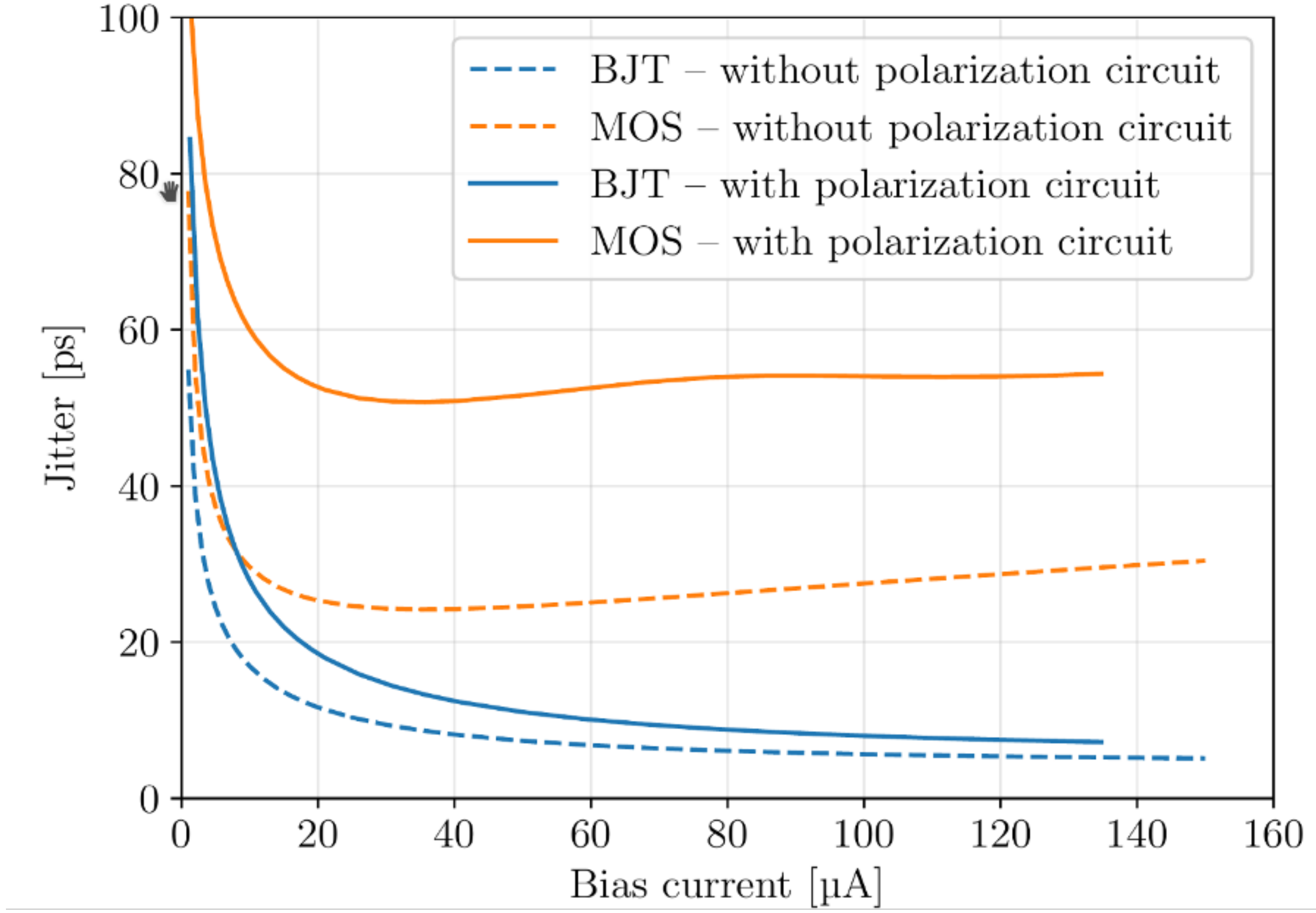
SiGe HBT vs. CMOS

Peak transition frequency vs. technology node



A. Mai and M. Kaynak,
SiGe-BiCMOS based technology platforms for mm-wave and radar applications.
DOI: 10.1109/MIKON.2016.7492062

Intrinsic **amplifier jitter**:
common emitter (source) configuration
in a 130nm technology

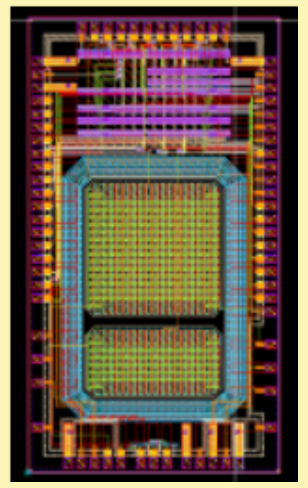


L. Paolozzi et al.,
Time resolution and power consumption of a monolithic silicon pixel prototype in SiGe BiCMOS technology,
JINST 15 (2020) P11025, https://doi.org/10.1088/1748-0221/15/11/P11025

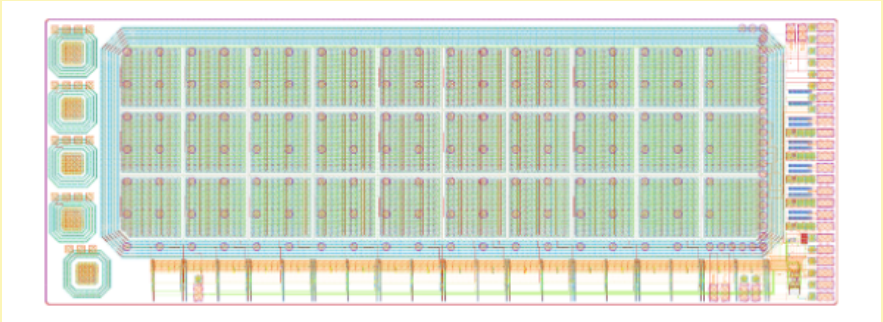
Monolithic SiGe BiCMOS for timing

Monolithic prototypes with SiGe BiCMOS (without internal gain layer)

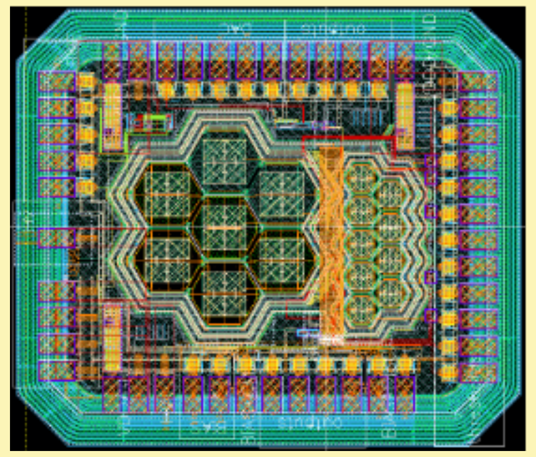
2016



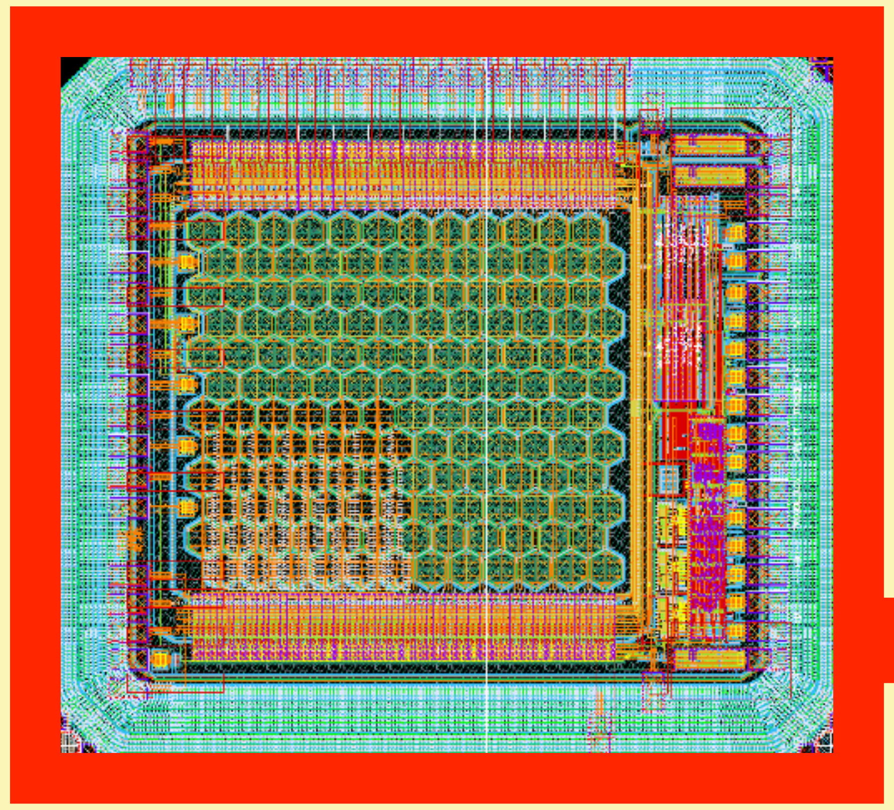
2017



2018



2020



200ps
- 1 and 0.5 mm² pixels
- Discriminator output

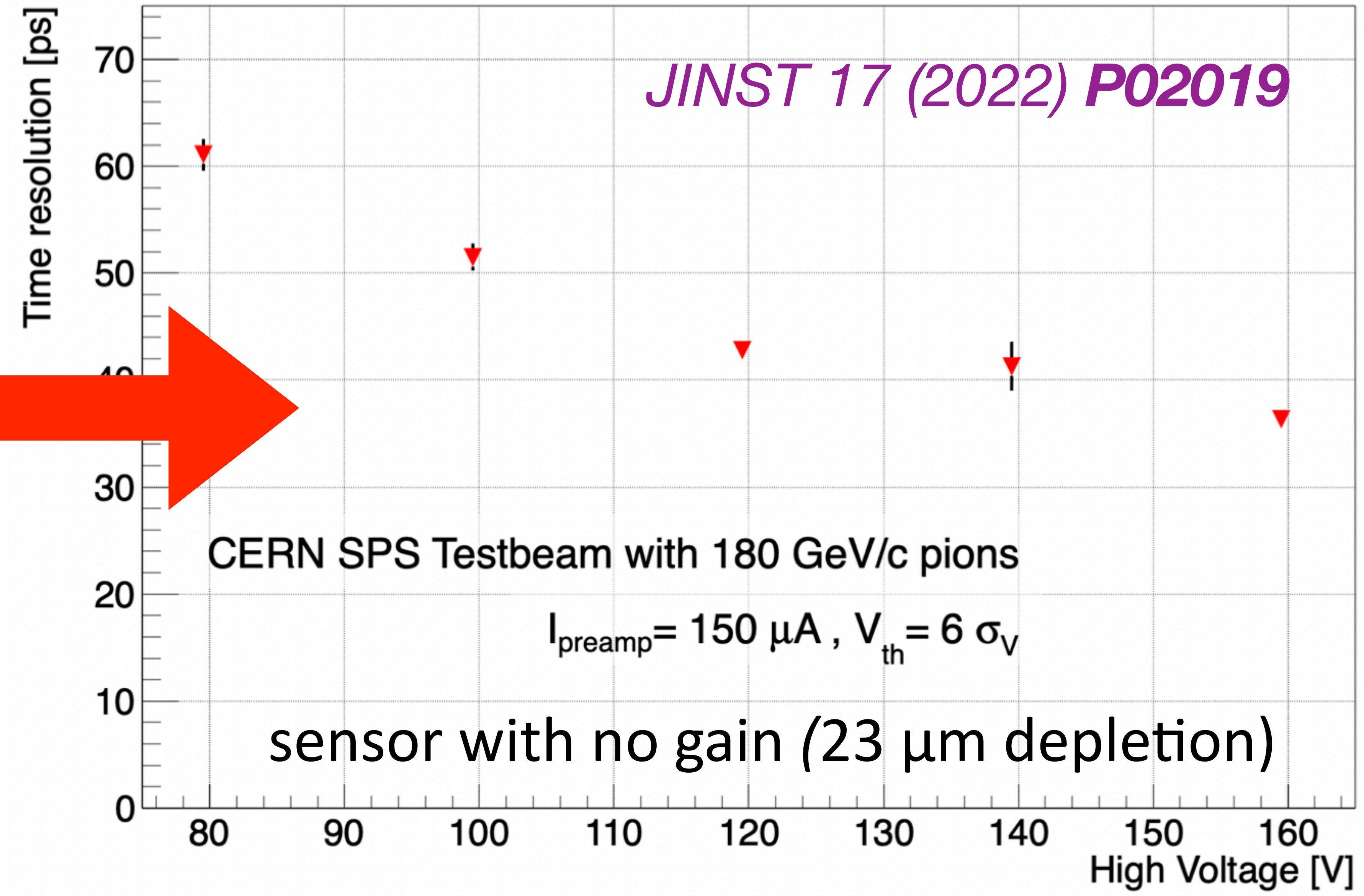
110ps
- 30 pixels 500x500μm²
- 100ps TDC +I/O logic

50ps
- Hexagonal pixels, pitch 100μm and 200μm
- Discriminator output

36 ps
- Hexagonal pixels 100μm pitch
- 30ps TDC +I/O logic
- Analog channels

"prototype1"

Test beam results of 2019 prototype



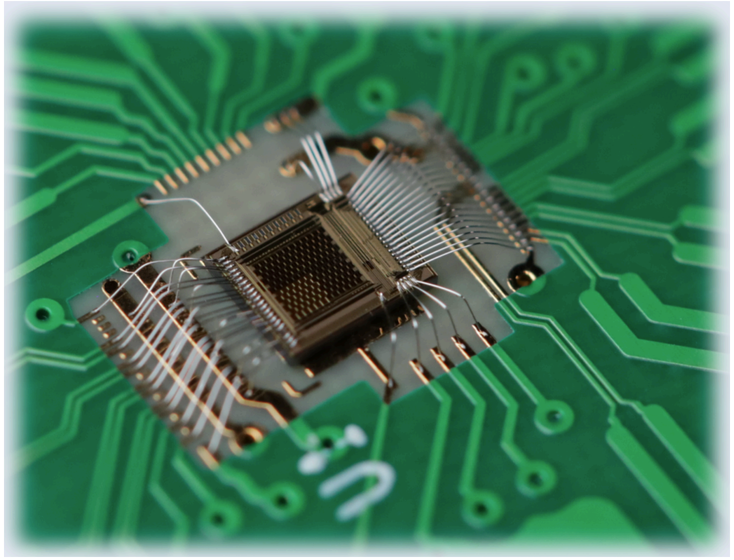
Several ASICs produced with IHP **SG13G2** technology

innovations for high performance microelectronics

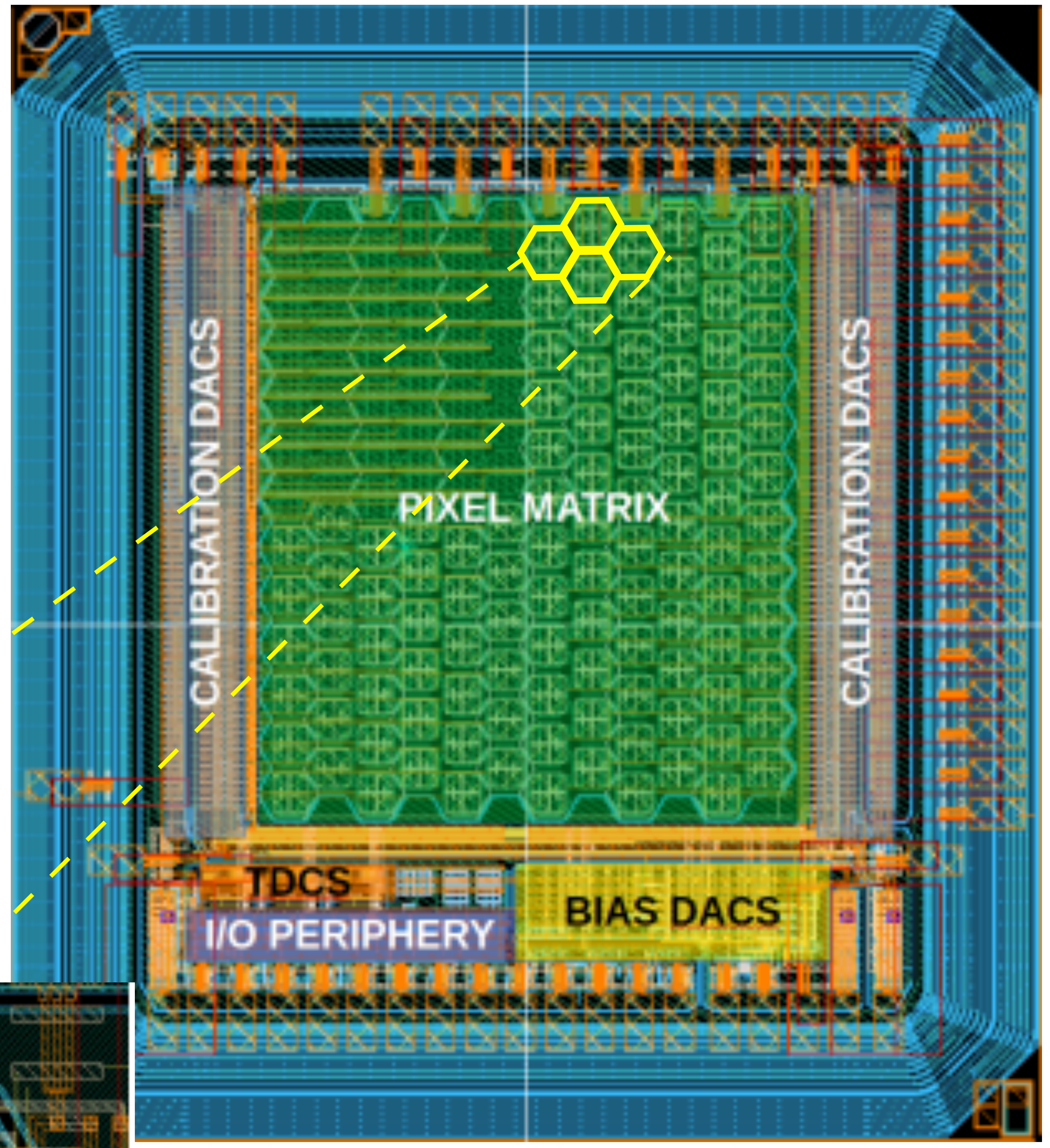
Leibniz-Institut für innovative Mikroelektronik

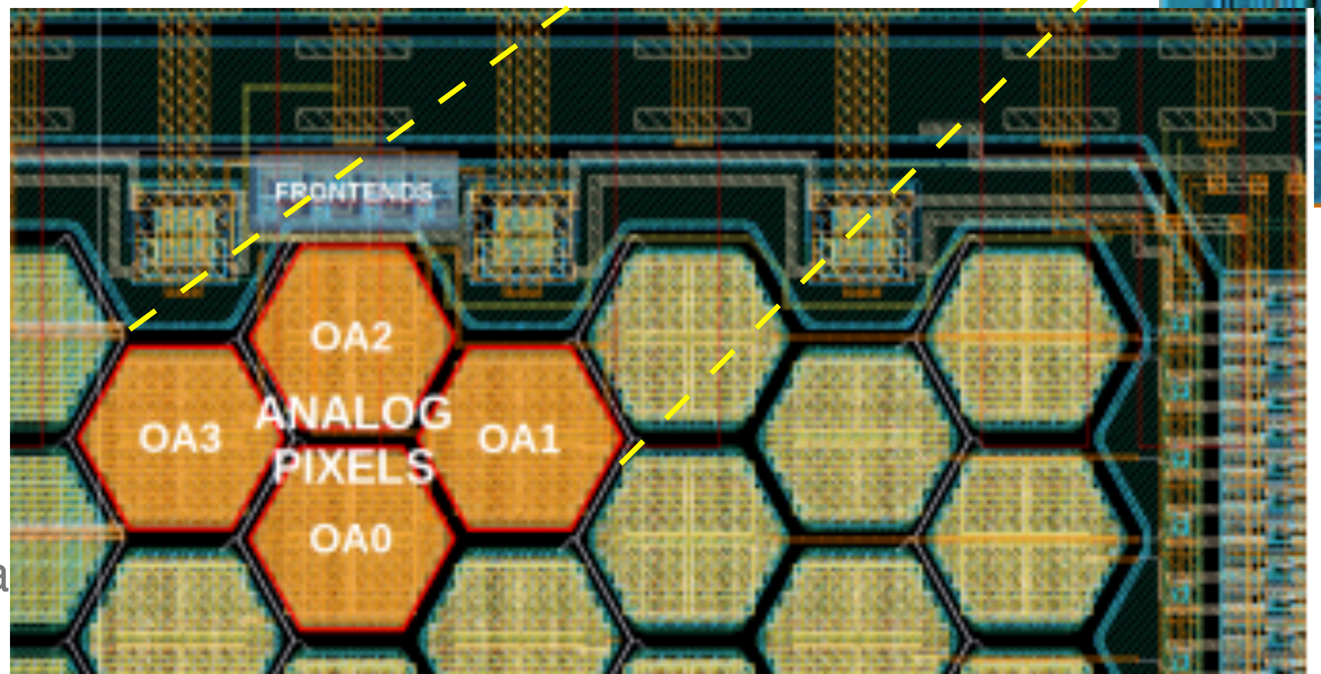
New ASIC matrix ("prototype2") produced in 2022 ⟶

2022 prototype2 — no gain layer

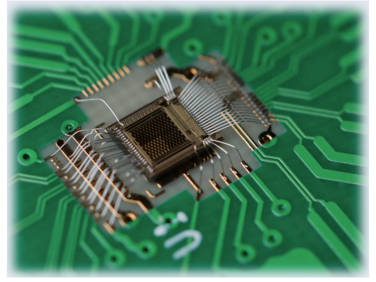


- Same matrix configuration as previous, but
  - Substrate: 50Ωcm → 350Ωcm epilayer, 50μm thick on low-res (1Ωcm) substrate
    - ➡ smaller pixel capacitance
    - ➡ depletion 23μm → 50μm
    - ➡ much larger voltage plateau
    - ➡ can operate sensor with v_{drift} saturated everywhere
  - Preamp and driver voltage decoupled:
    - ➡ was limiting optimal amplifier operation
    - ➡ cross-talk removed
  - Optimised FE layout, differential output, high-frequency cables:
    - ➡ better rise time (600ps → 300ps)



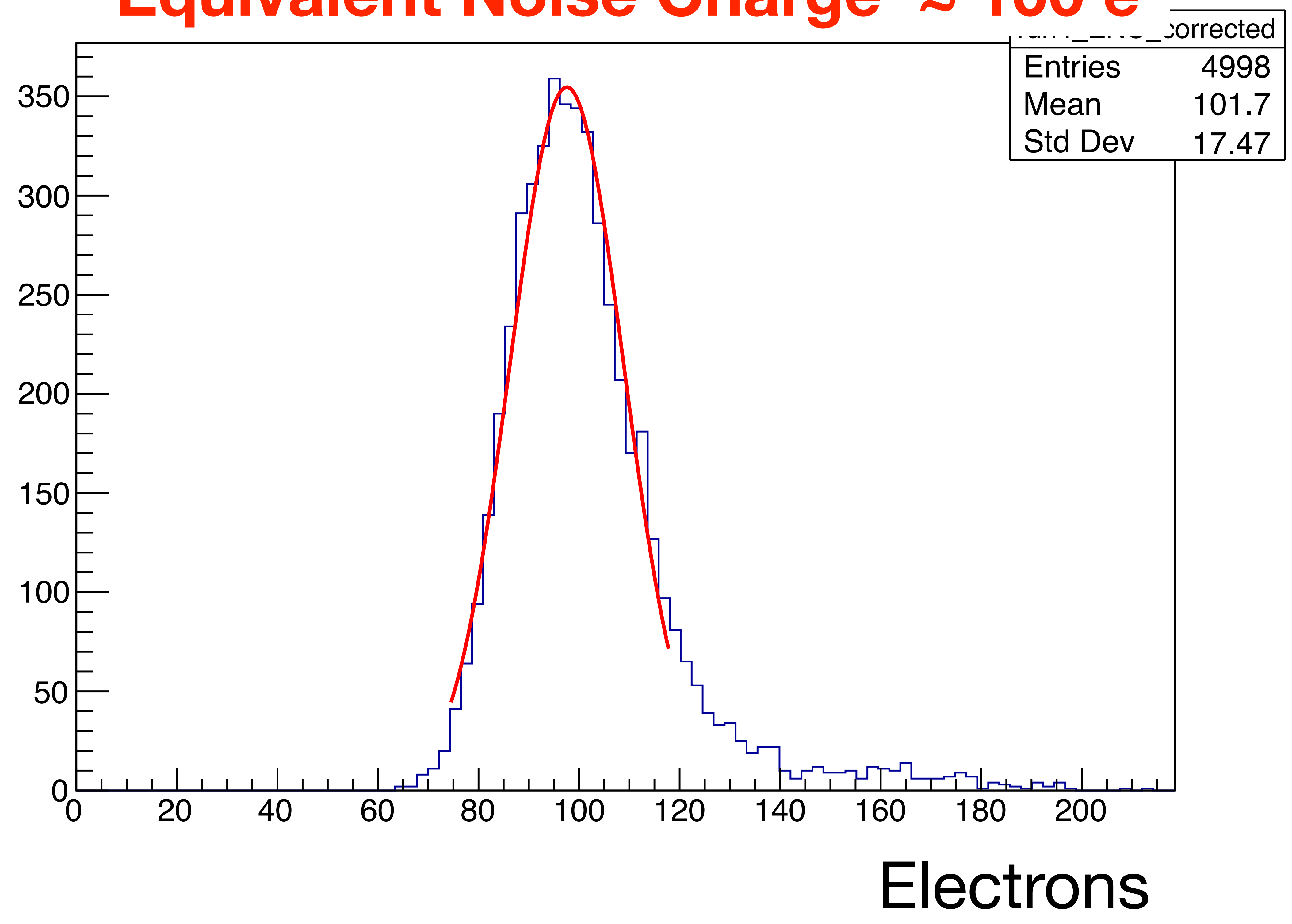


2022 prototype2 — no gain layer

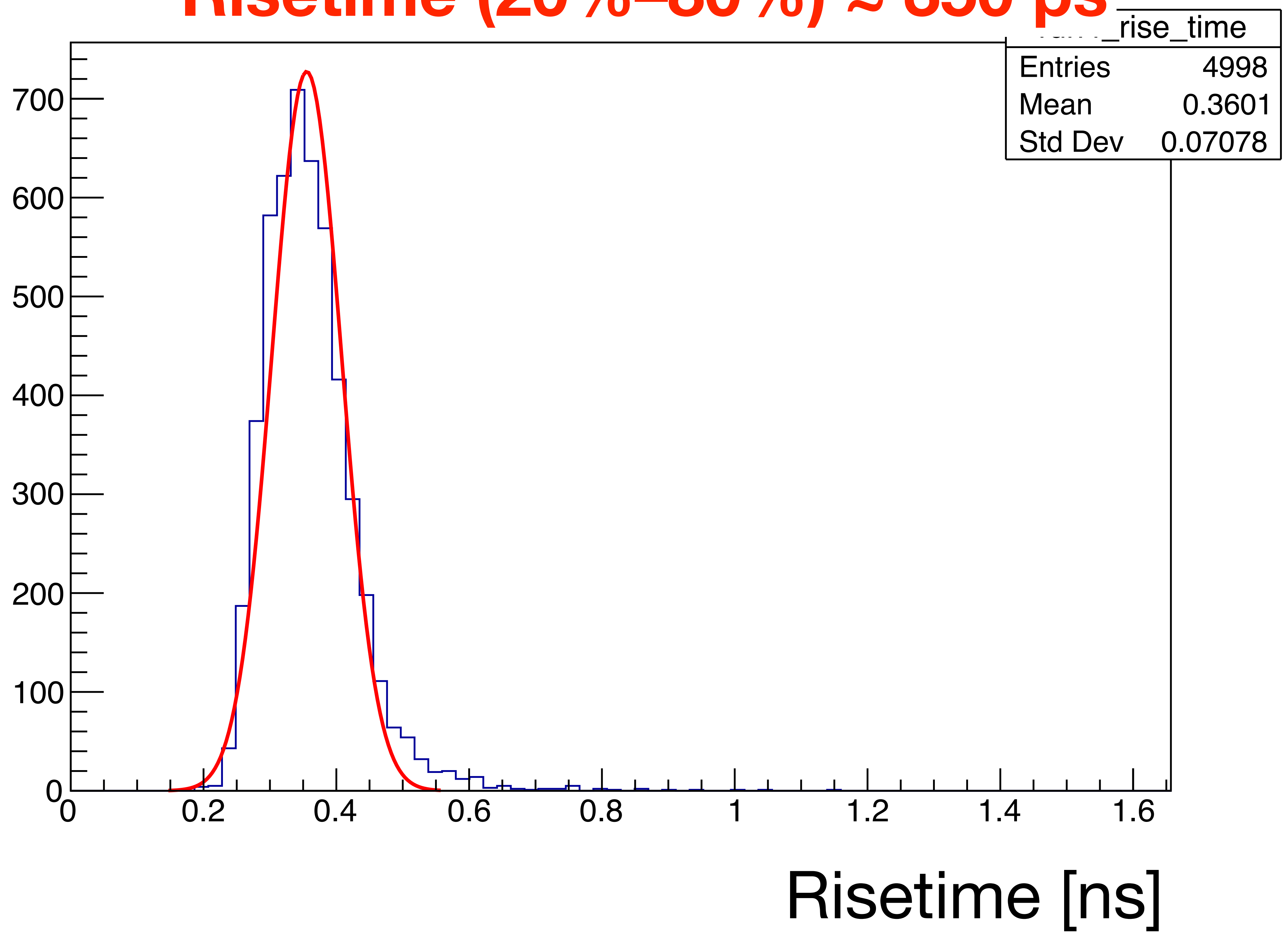


^{55}Fe measurements in cleanroom:

Equivalent Noise Charge ≈ 100 e⁻

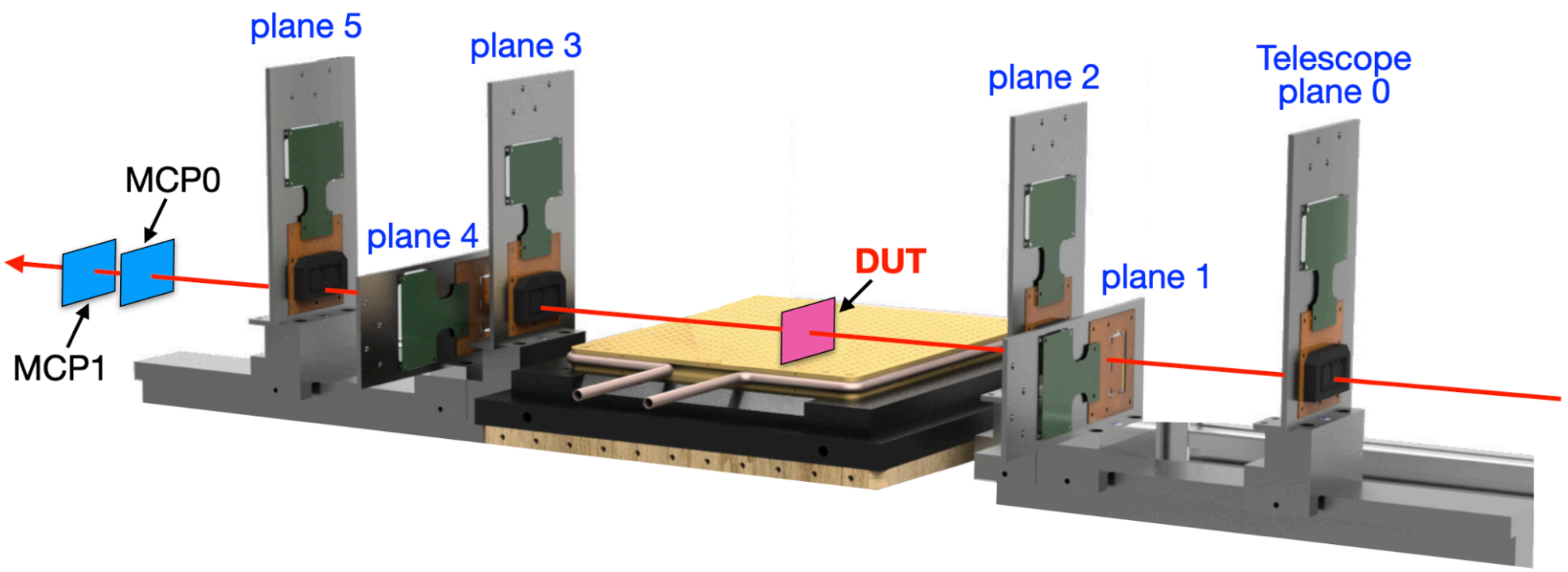


Risetime (20%–80%) ≈ 350 ps



Test Beam: Experimental Setup

Mid October SPS testbeam with 180 GeV/c π to measure **efficiency** and **time resolution**

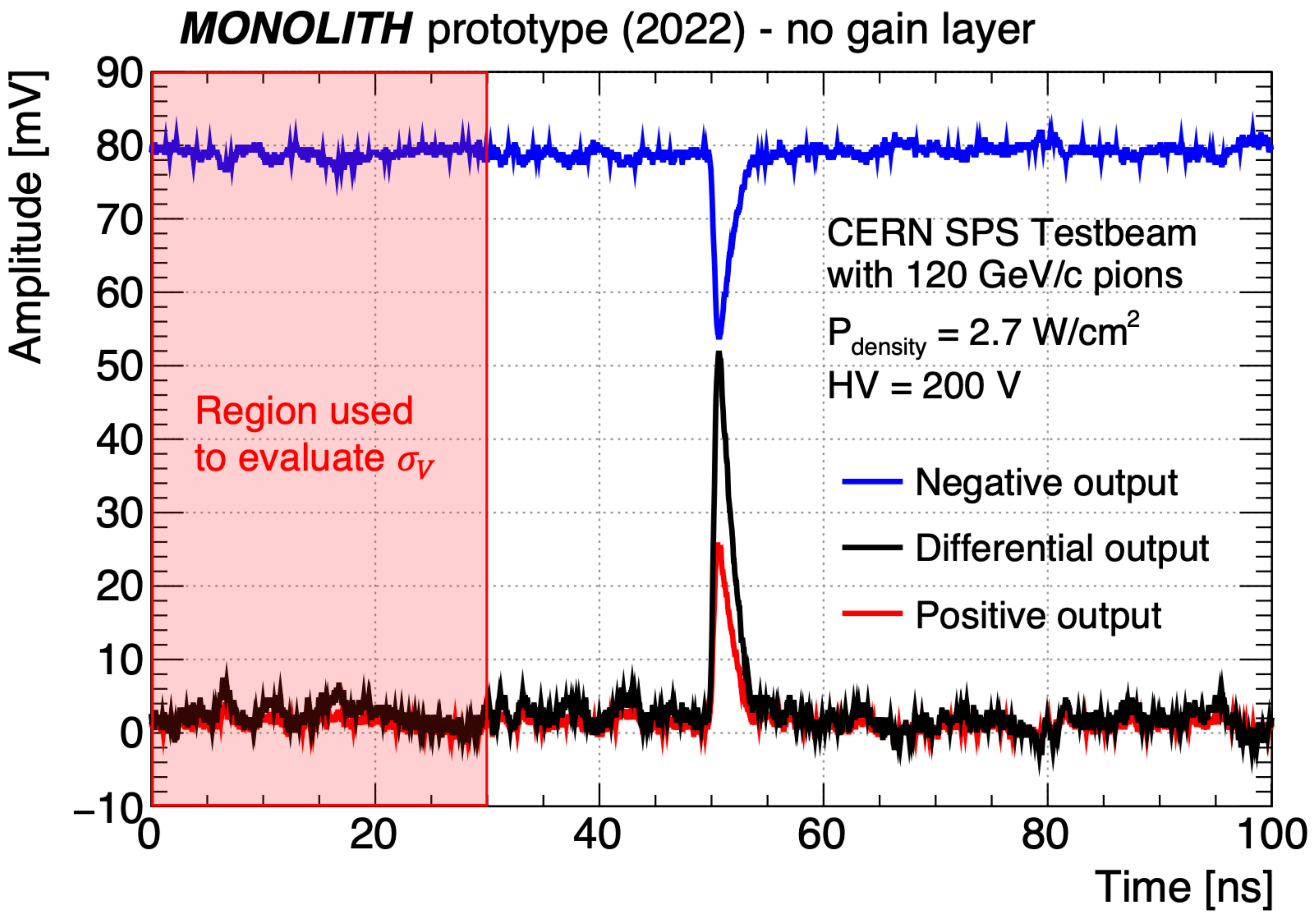


UNIGE FE-I4 telescope to provide spatial information ($\sigma_{x,y} \approx 10$ μm)

Two MCPs ($\sigma_t \approx 5$ ps) to provide the timing reference

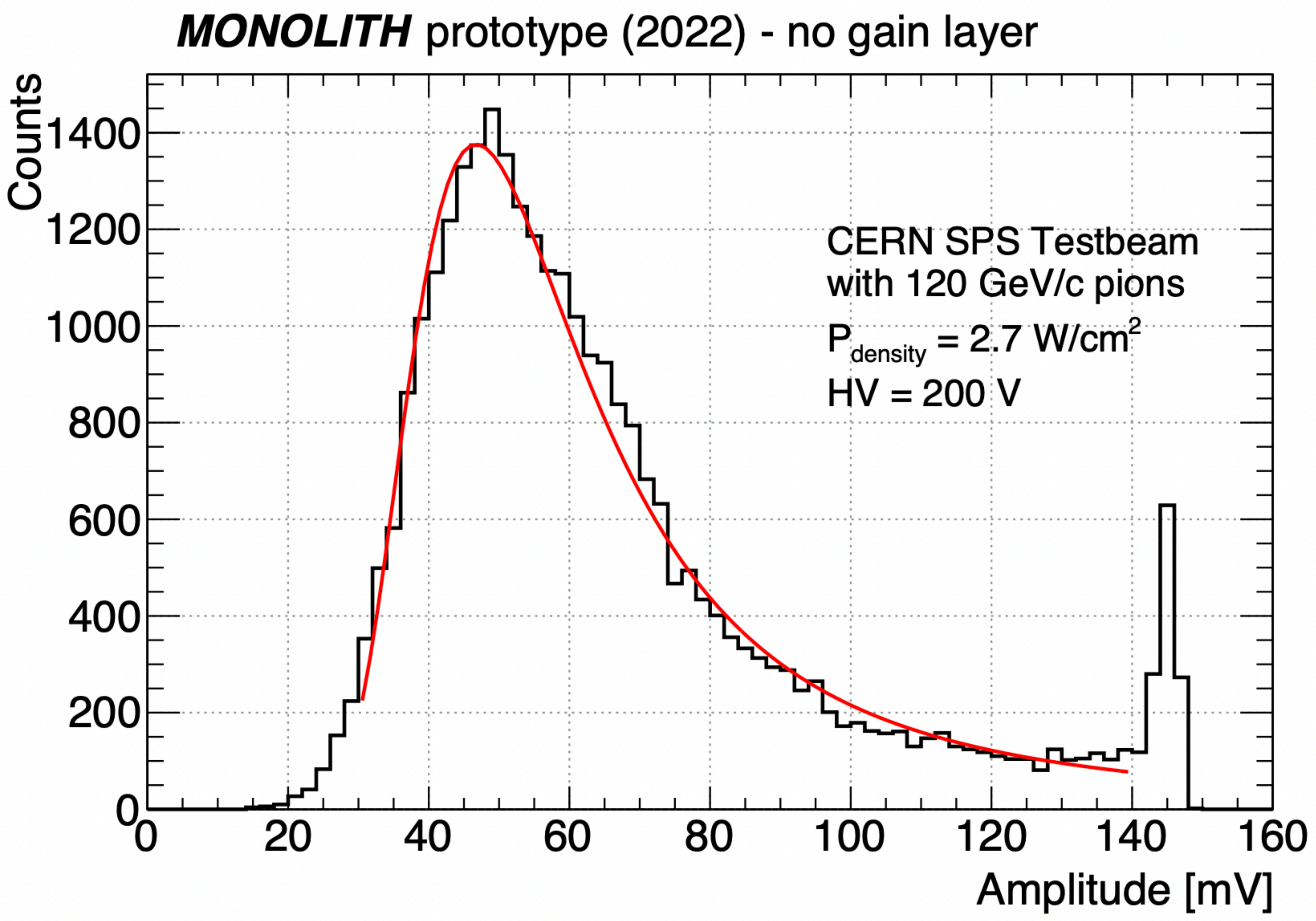
Lots of data taken: results in **JINST 18 (2023) P03047**

2022 prototype2 — no gain layer



Voltage noise of the differential signal:

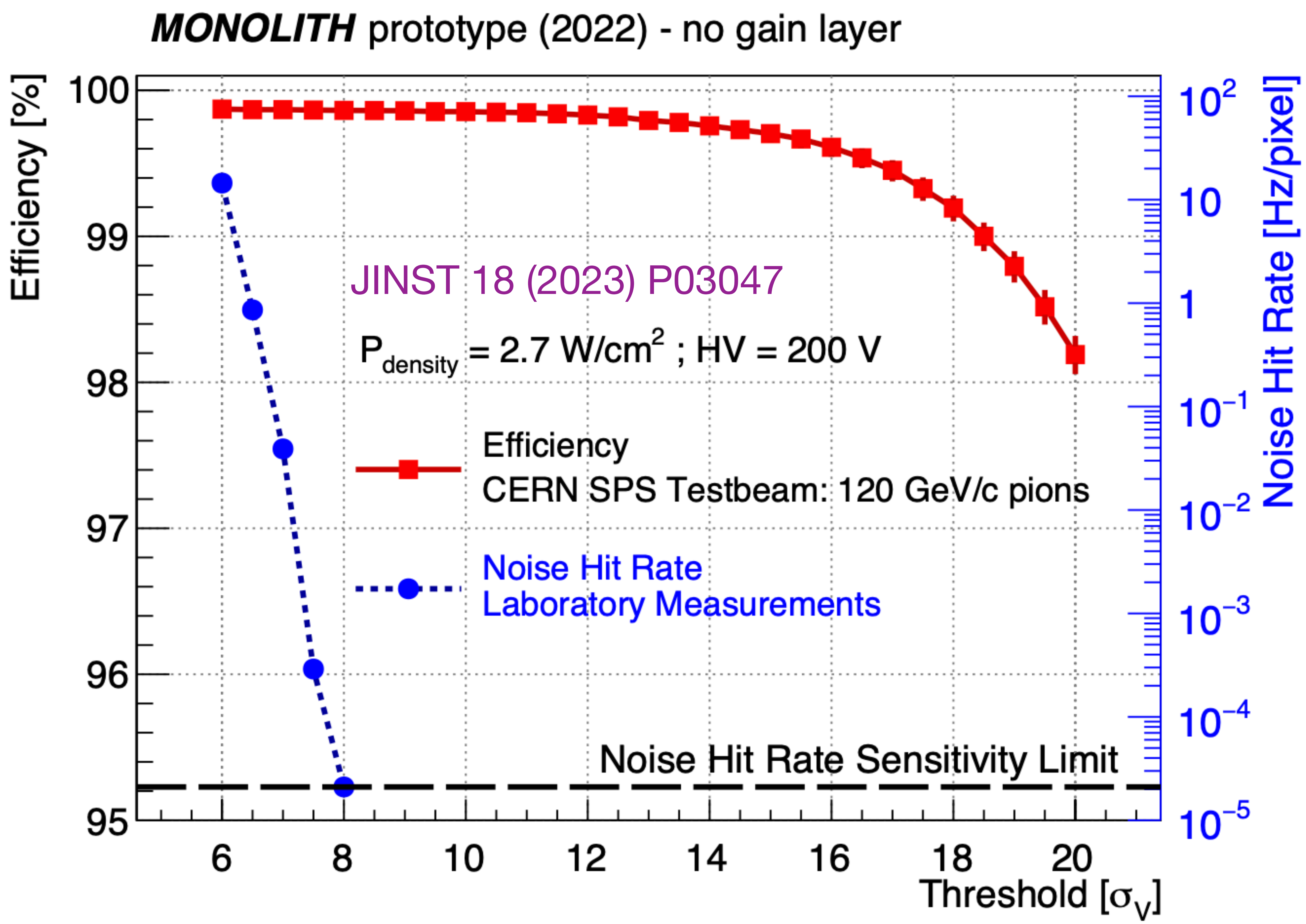
$\sigma_V \approx 1$ mV



Amplitude distribution of differential signal:

Landau with most probable value ≈ 50 mV

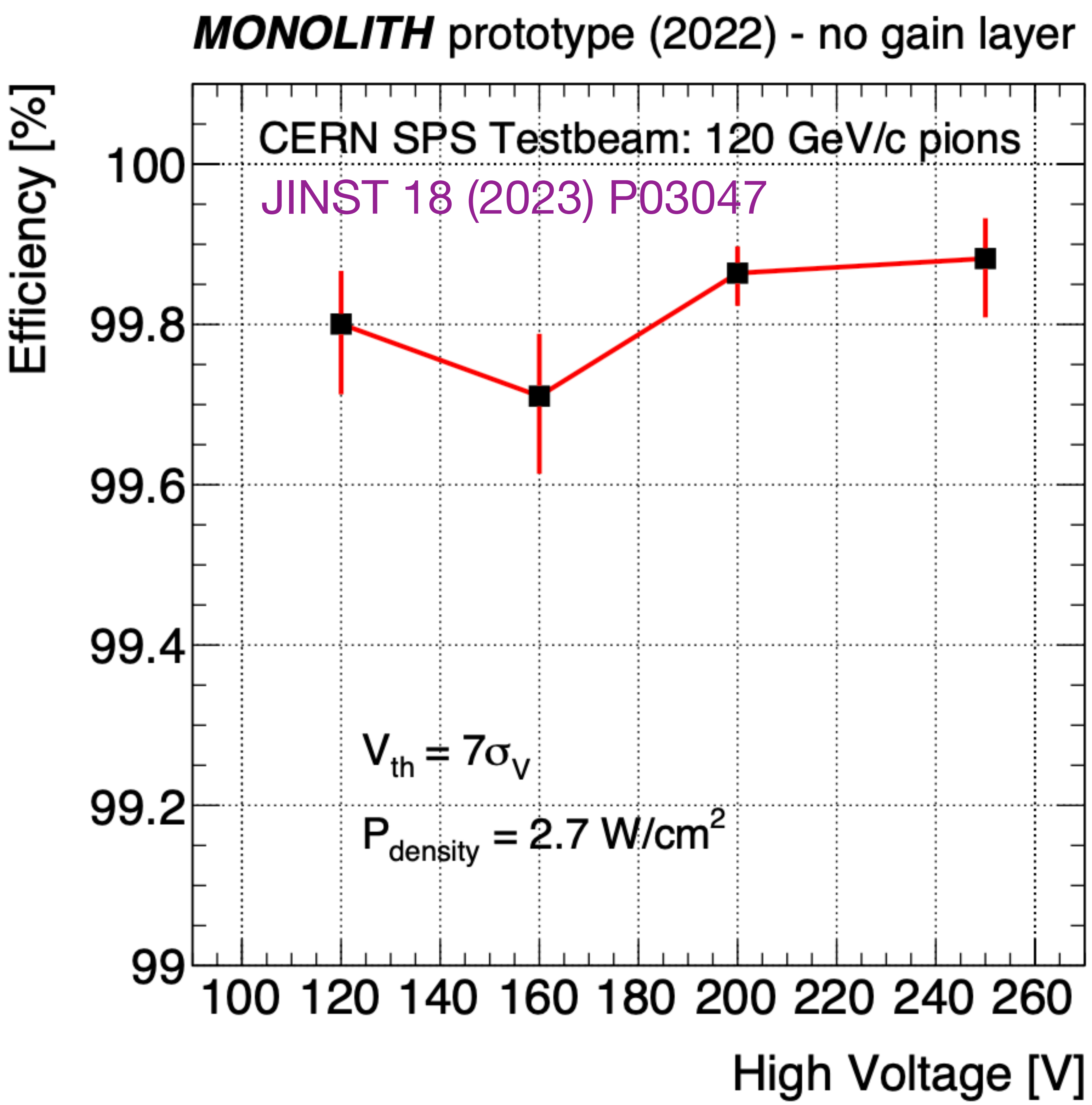
2022 prototype2 — no gain layer

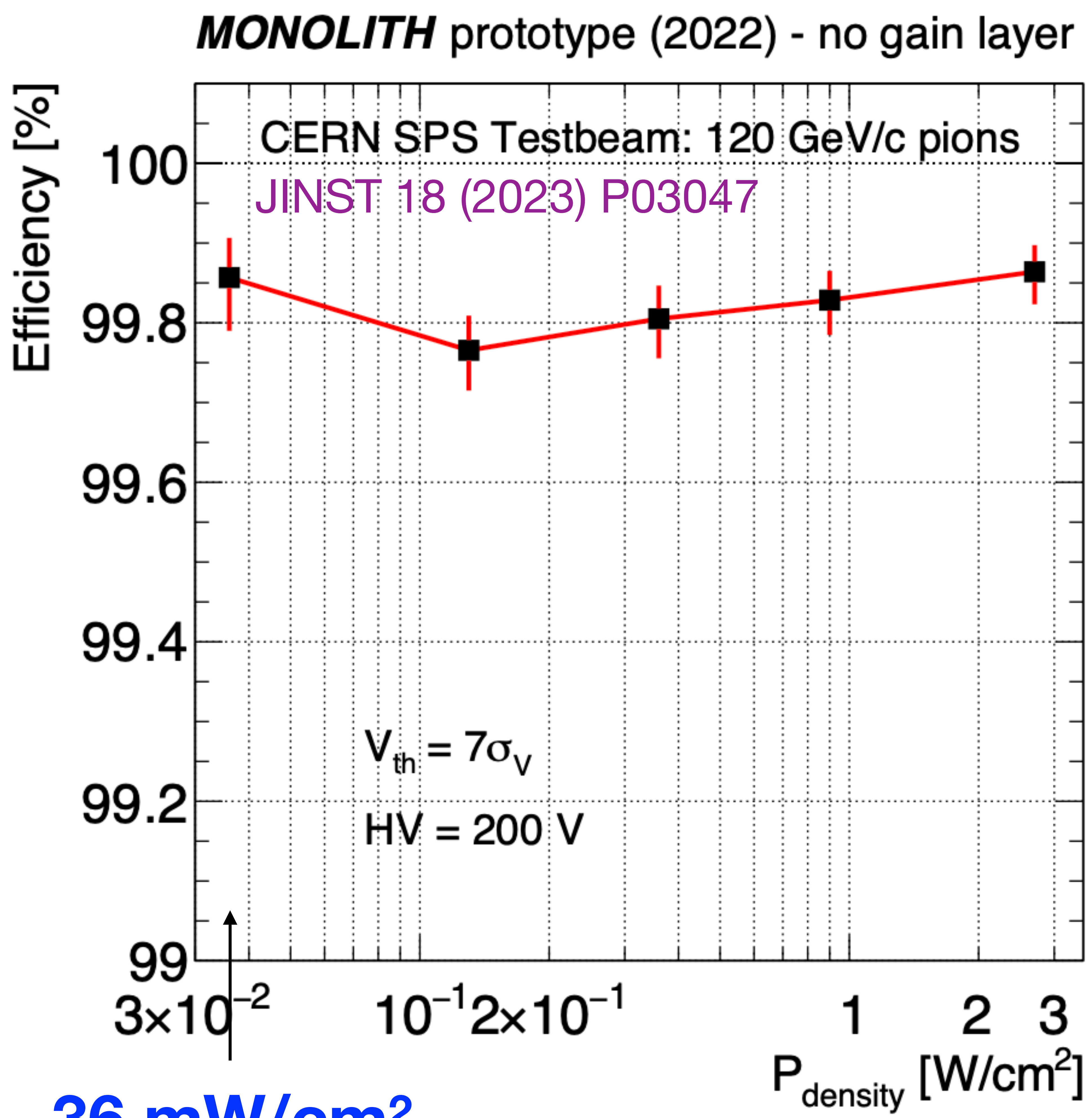


Large efficiency plateau at ≈ **99.8%**,
that allows operation at very low noise-hit rate

2022 prototype2 — no gain layer

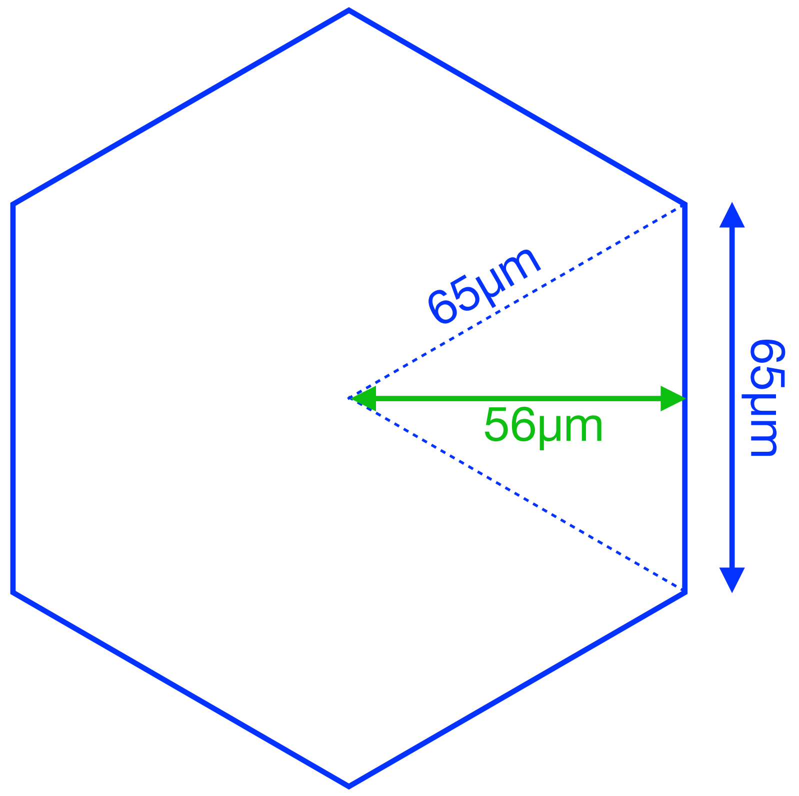
8 working points (HV, power consumption) taken at the testbeam:

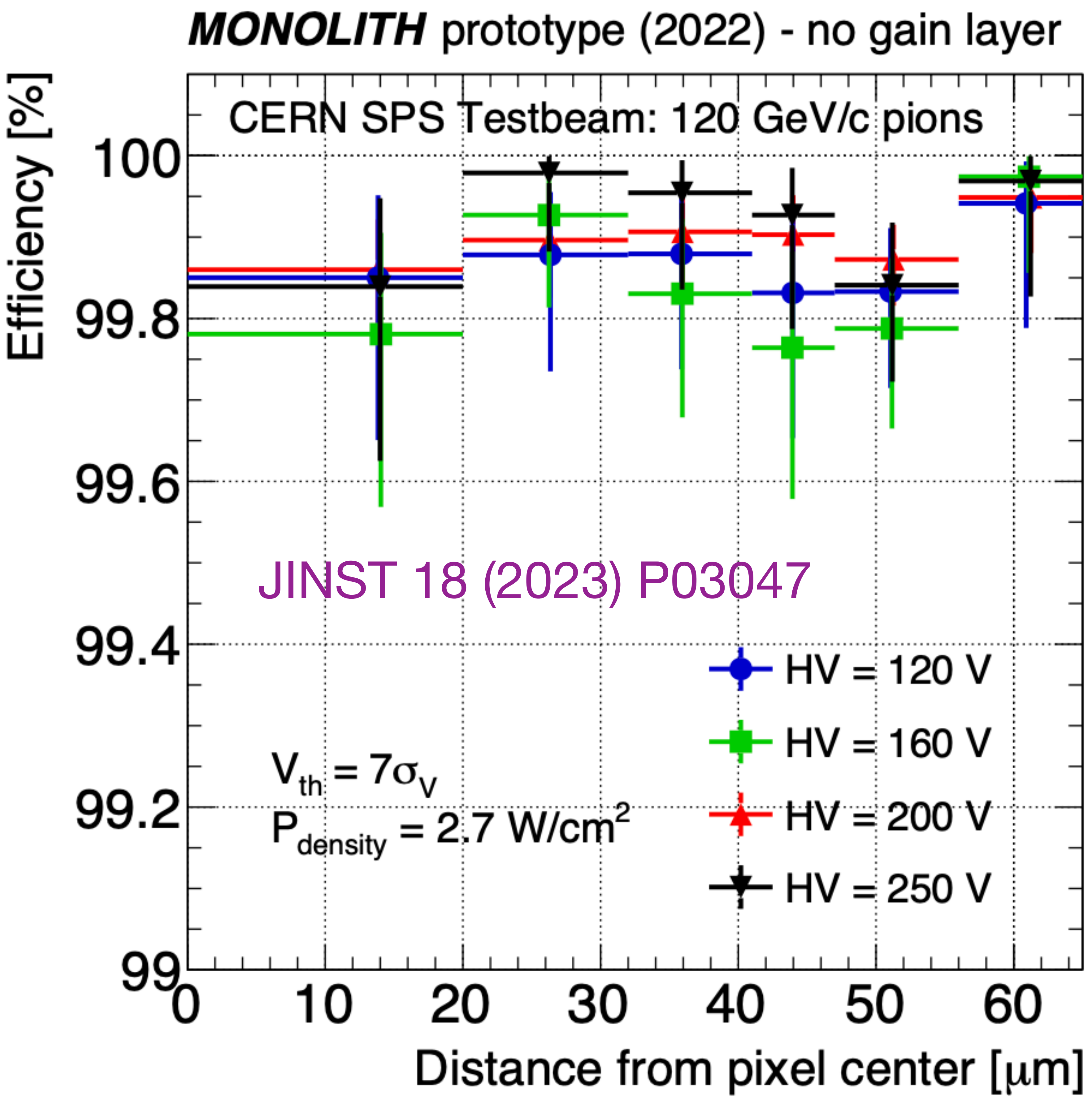


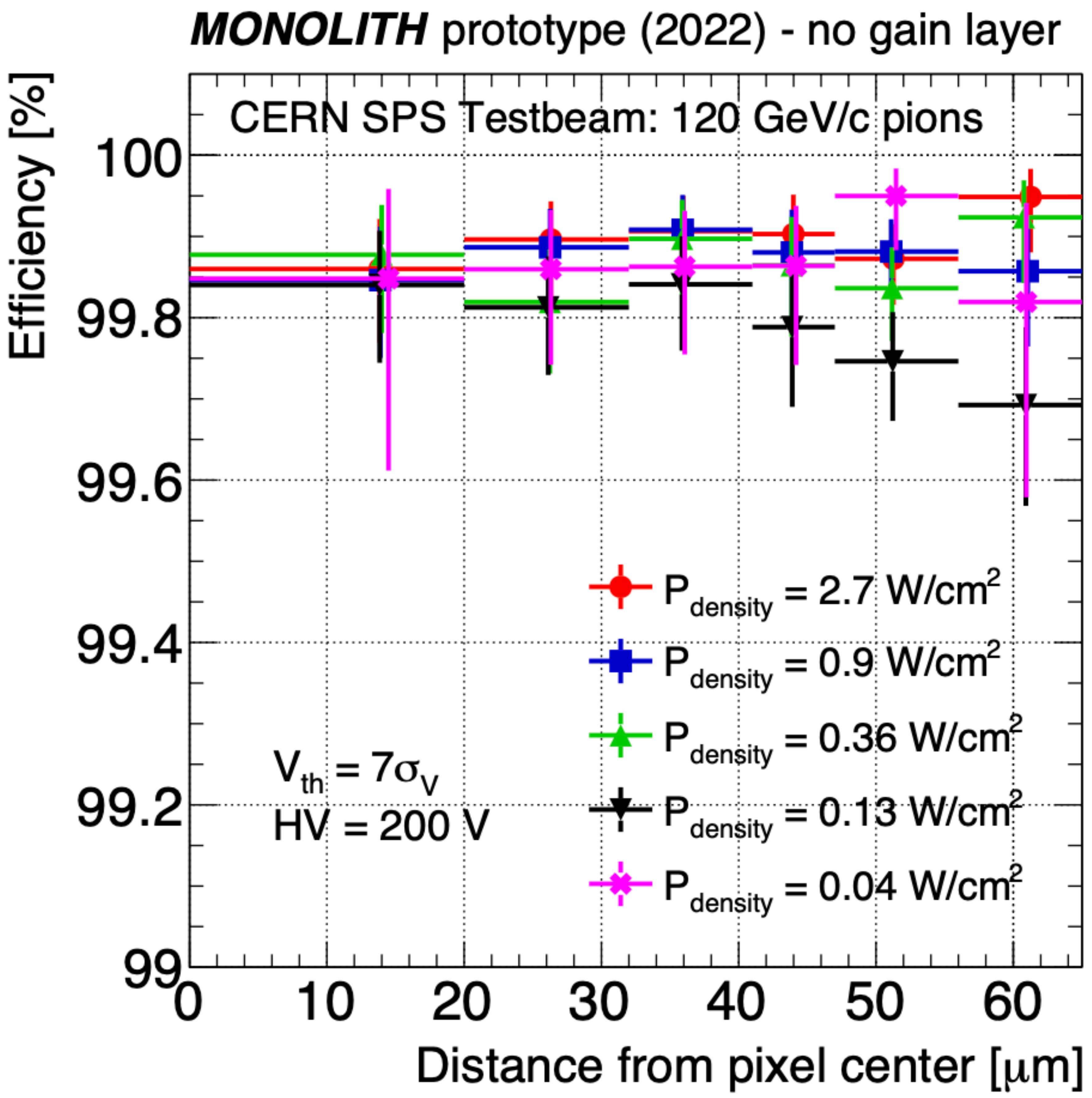


36 mW/cm²

2022 prototype2 — no gain layer

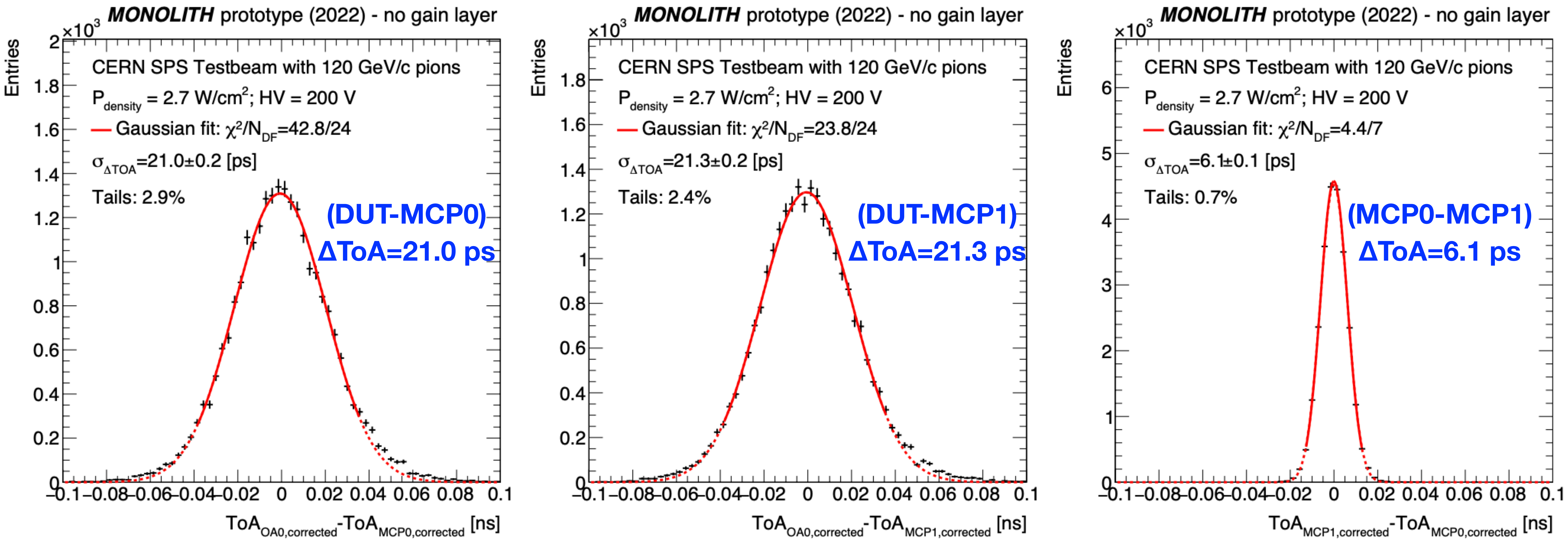






Efficiency ≈ **99.8%** even in the **inter-pixel region**, for all working points

2022 prototype2 — no gain layer



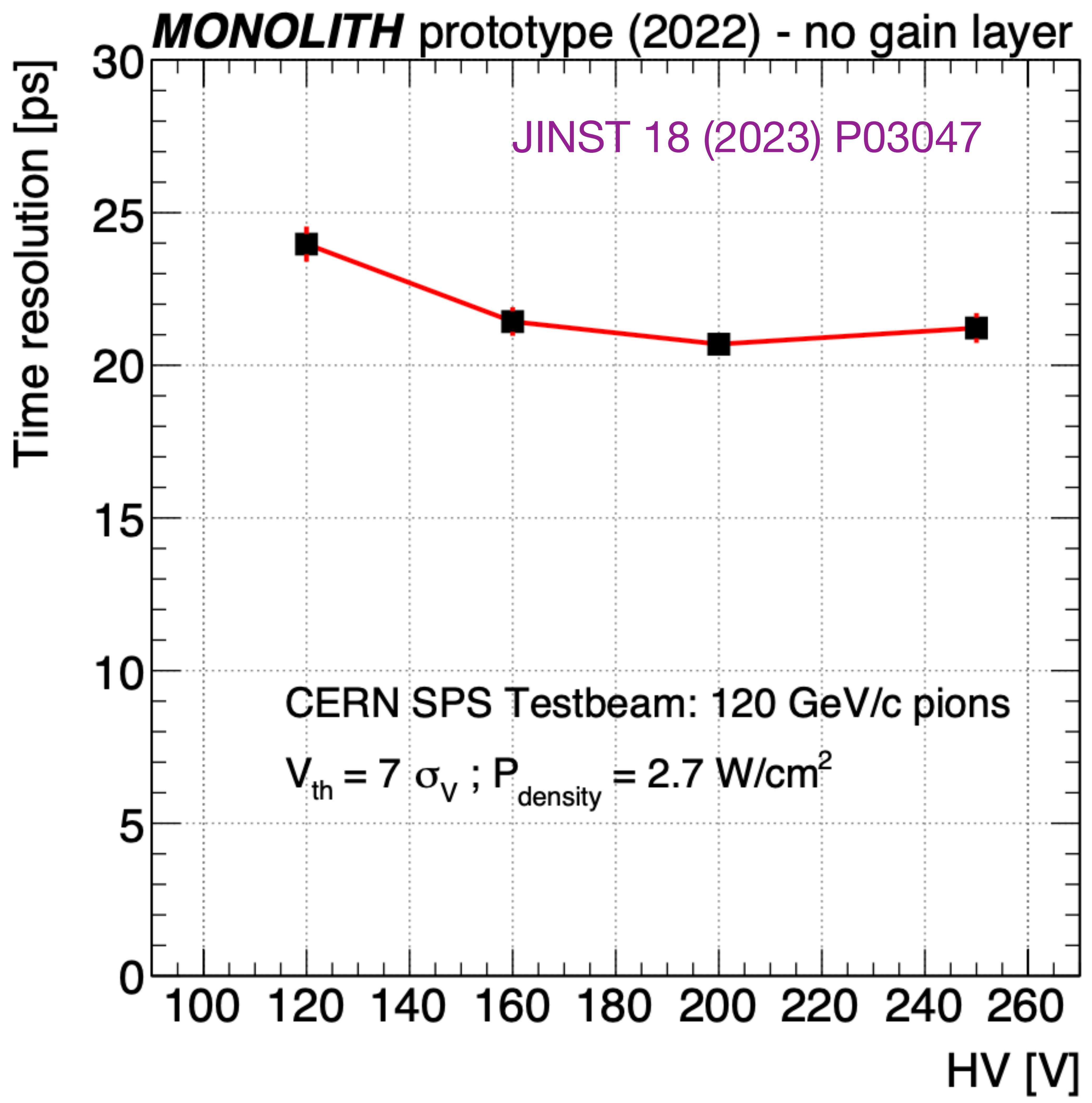
- Simultaneous fit to extract time resolutions of the DUT, MCP0, MCP1:

Fit results: MCP0 σ_T = (3.6 ± 1.5) ps
MCP1 σ_T = (5.0 ± 1.1) ps

σ_T = (20.7 ± 0.3) ps

non-Gaussian tails ≈ **3%**

2022 prototype2 — no gain layer



Plateau of 100V with time resolution of **≈ 20 ps** with simple analysis and simple signal processing.

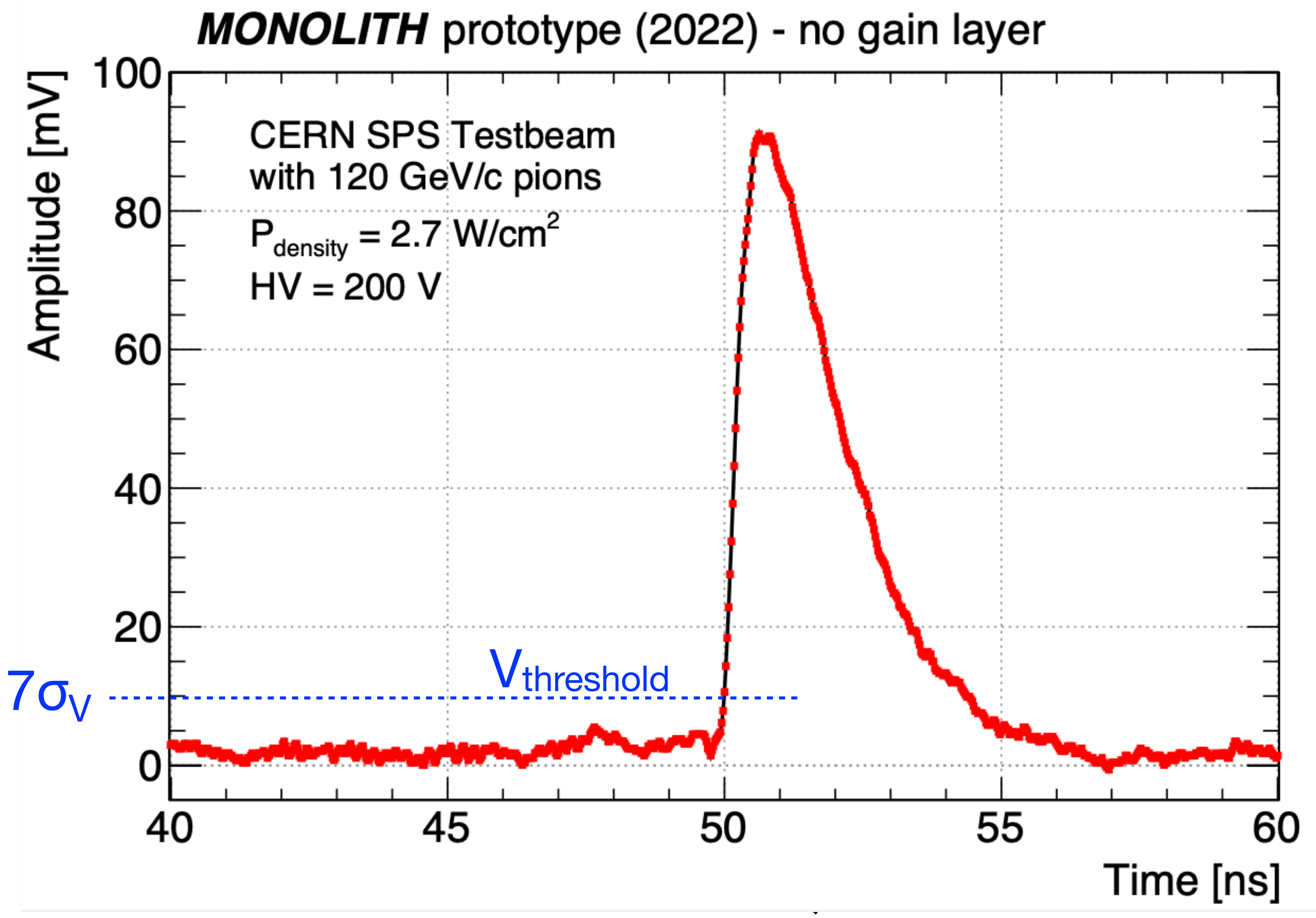
2022 prototype2 — no gain layer

Time resolution measurements

Remark :

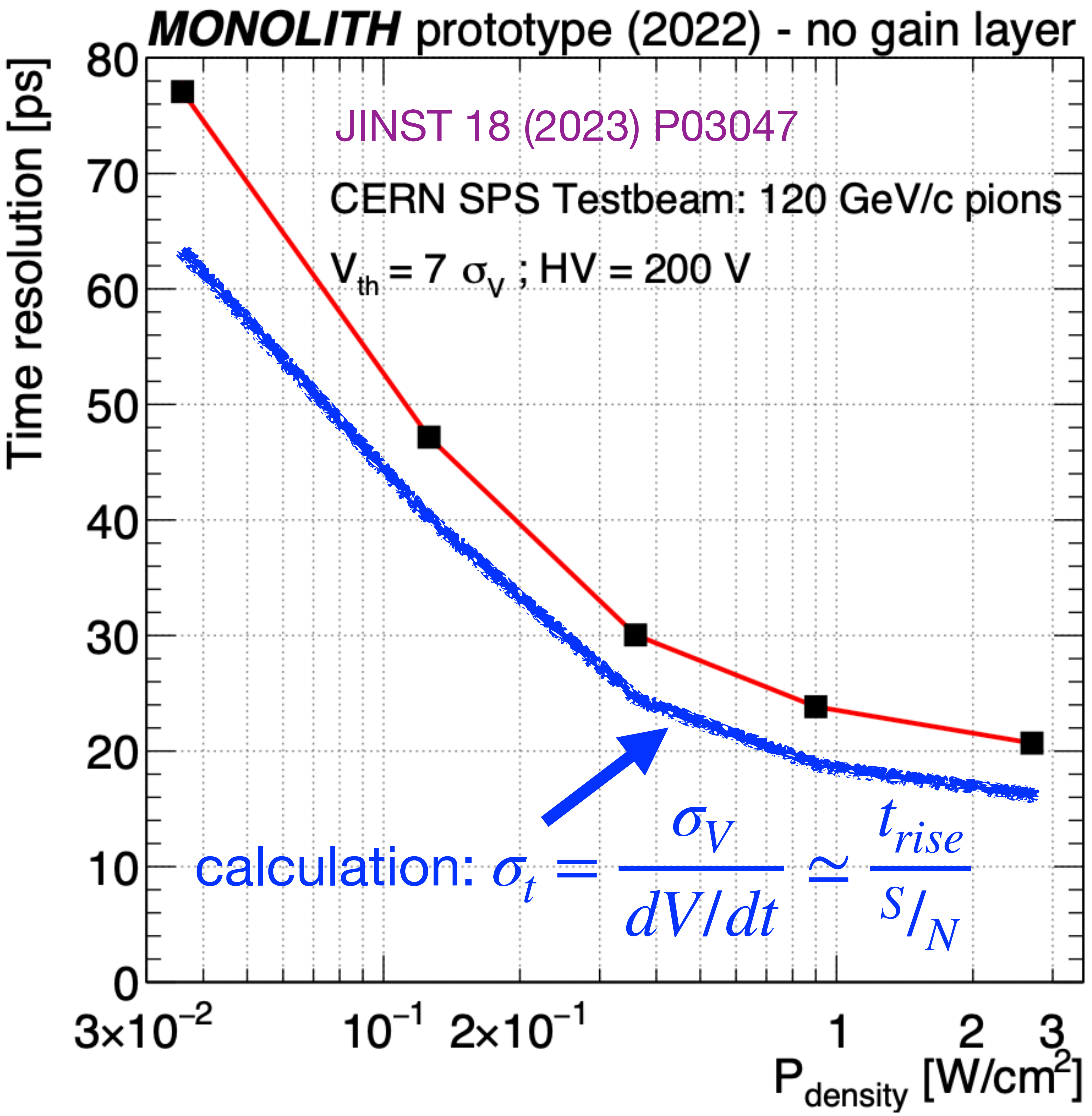
20.7 ps with very simple analysis:

- **Linear interpolation** of oscilloscope samplings (25ps)
- Time Of Arrival (ToA): time at **$V_{threshold} = 7\sigma_V$**
- Δ_{ToA} distributions are **time-walk corrected**



More complex analysis (spline interpolation, filtering, …) reaches **17.7 ps**

2022 prototype2 — no gain layer



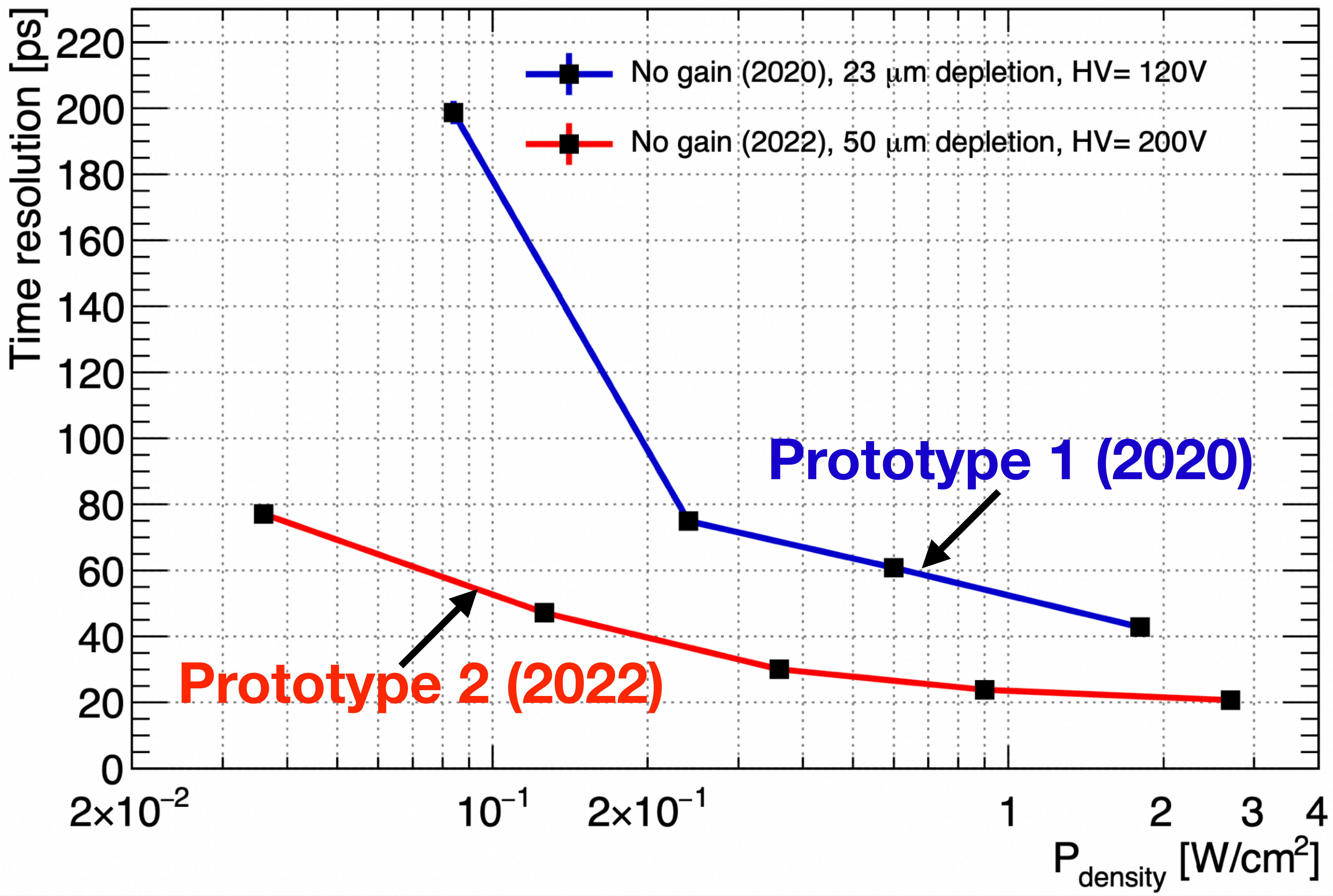
DUT operated at $HV = 200$ V and $V_{th} = 7\sigma_V$		
$P_{density}$ [W/cm^2]	Amplitude MPV [mV]	Time Resolution [ps]
2.7	48.6 ± 0.5	20.7 ± 0.3
0.9	35.8 ± 0.5	23.8 ± 0.3
0.36	22.6 ± 0.4	30.1 ± 0.4
0.13	14.2 ± 0.3	47.2 ± 0.7
0.04	16.2 ± 0.3	77.1 ± 0.9

20 ps at 2.7 W/cm²
50 ps at 100 mW/cm²

Testbeam results: Time Resolution

European Research Council
Established by the European Commission

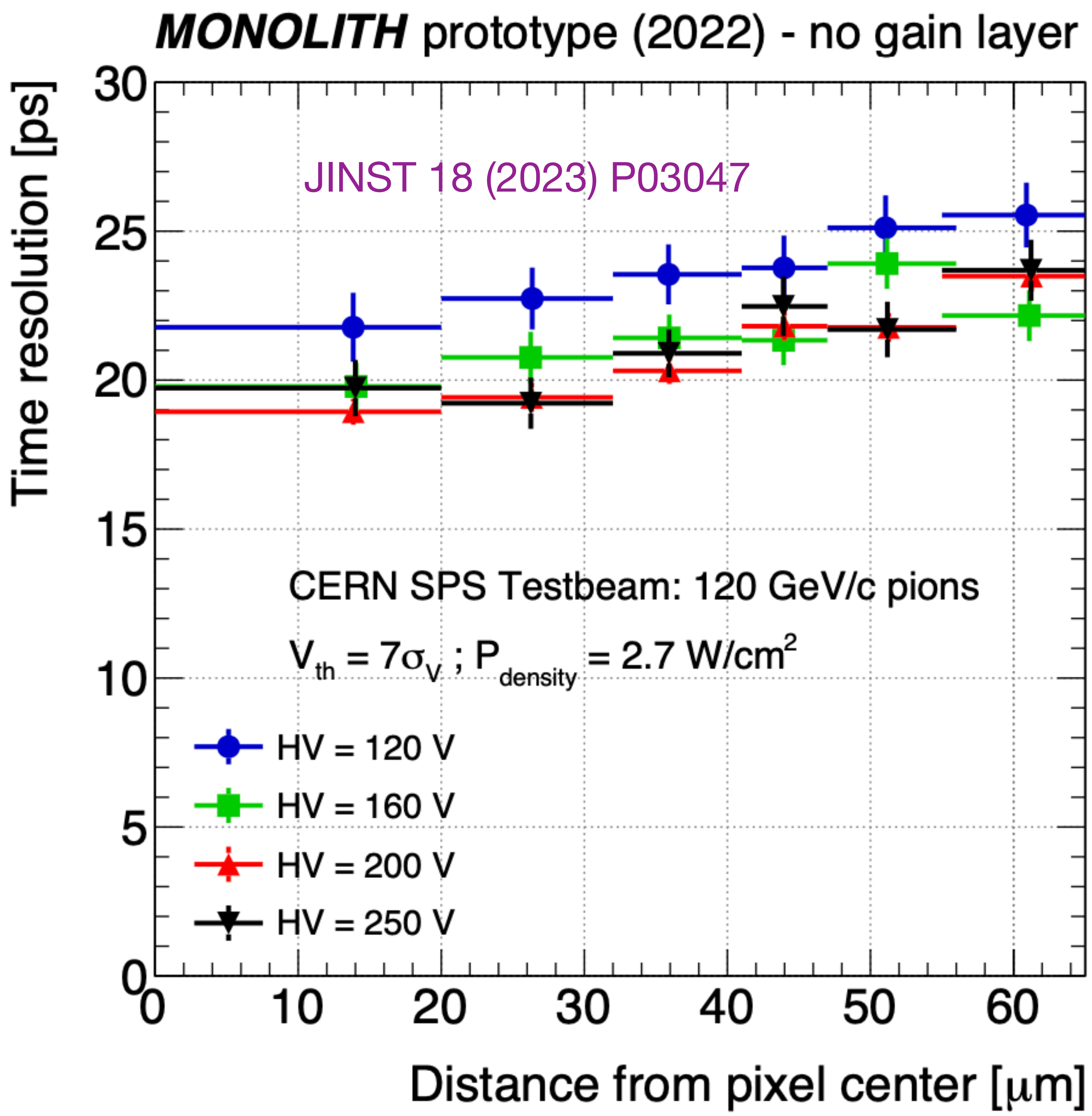
Comparison prototype1 vs. prototype2



Prototype 2 improvement in time resolution w.r.t. prototype 1 is **more than a factor of 2**

Note: both are **without gain layer**

2022 prototype2 — no gain layer



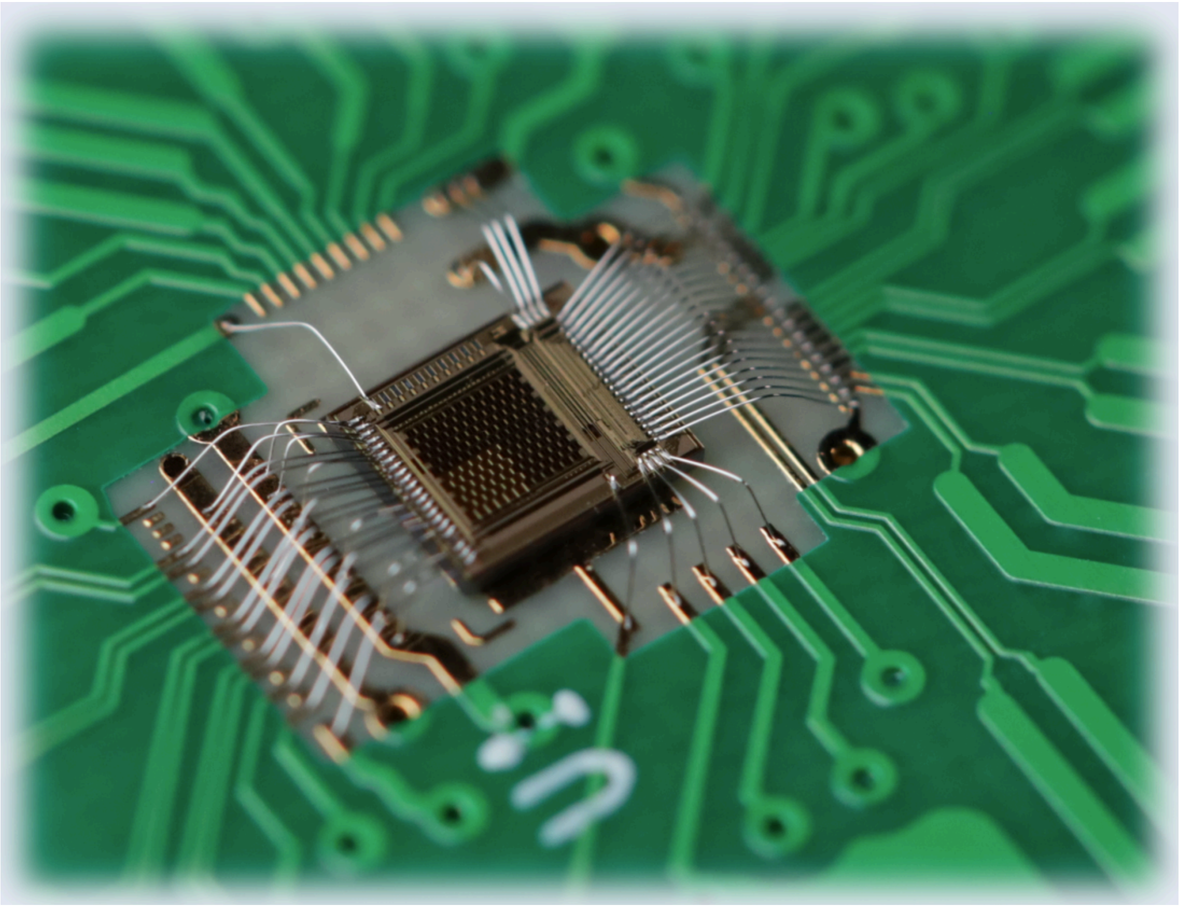
For HV ≥ 160V, time resolution ranges from ≈ **19 ps** at the center to ≈ **23 ps** at the edge of the pixel

Still something to improve with the weighting field far from pixel center.

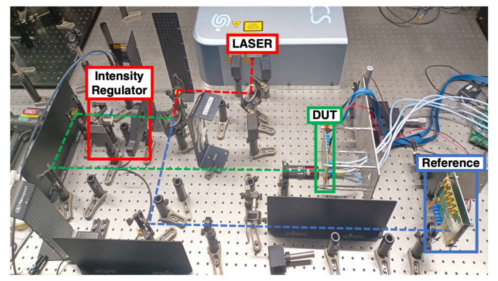
For HV = 120 V: ≈ 3 ps worse.

Laser measurements

with the 2022 prototype2 without gain



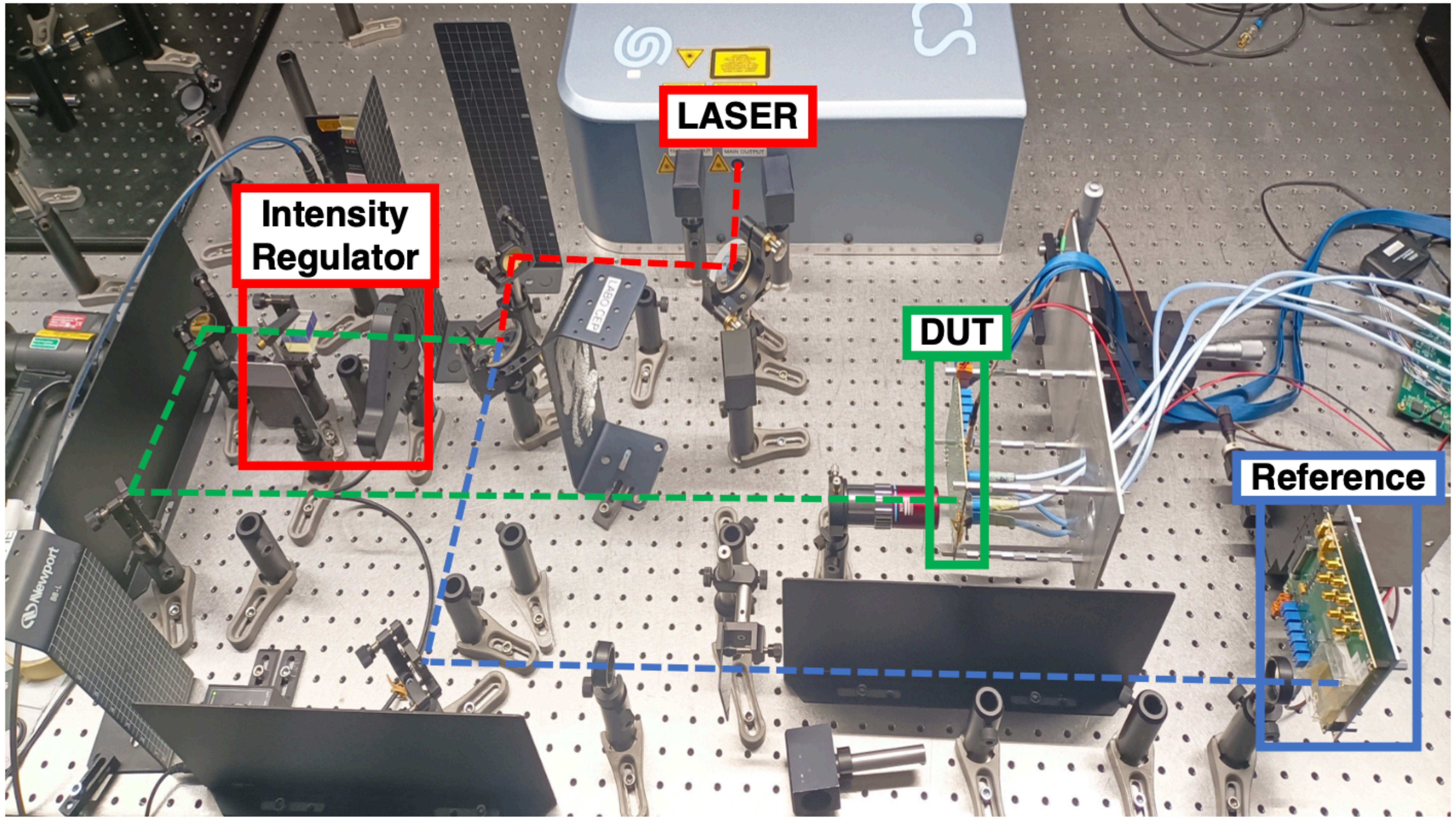
2022 prototype2 — no gain layer

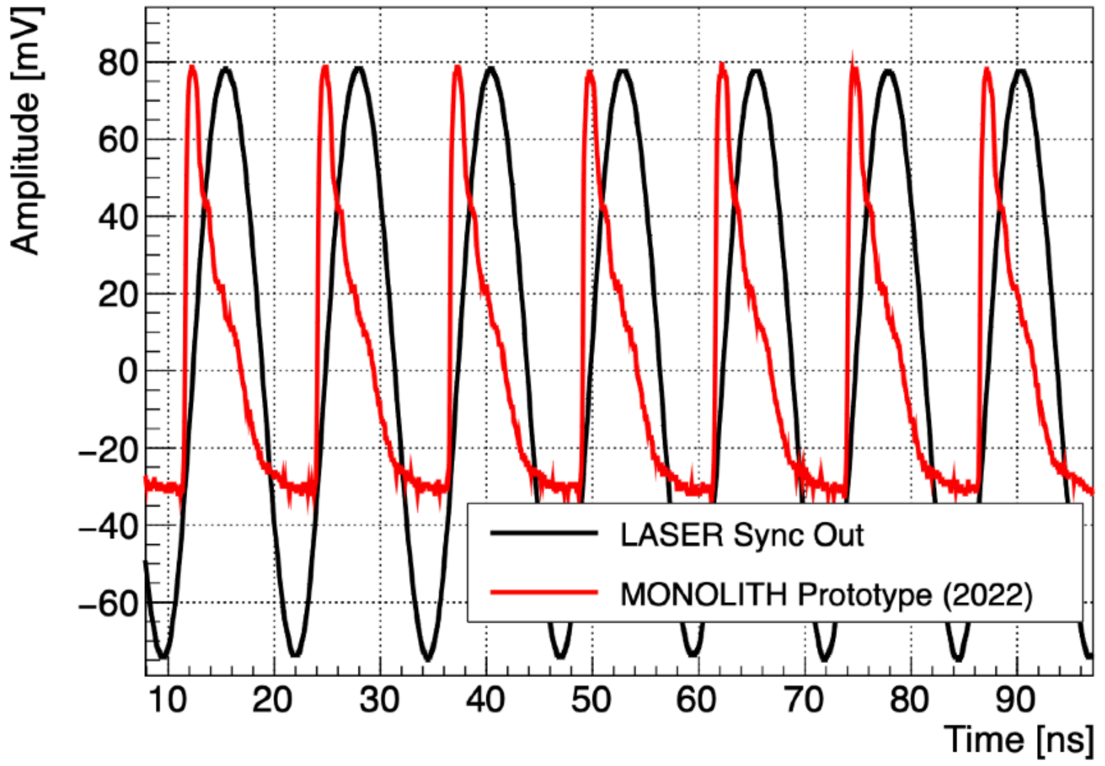


Laser Measurement

Preliminary measurement with a **laser** with a jitter of **100 fs** (repetition frequency = **80 MHz**)

Many thanks to
L. Bonacina's lab of GAP UNIGE





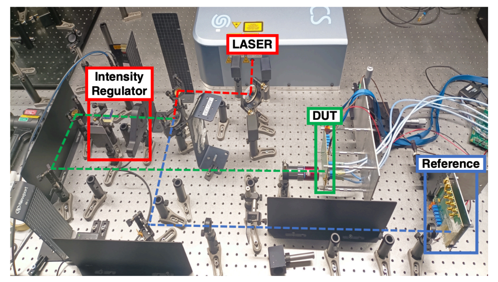
Time coincidence between two of our samples:

➡ "**Reference**" receiving always large laser pulse producing 17k electrons (σ_t = 2.5 ps)

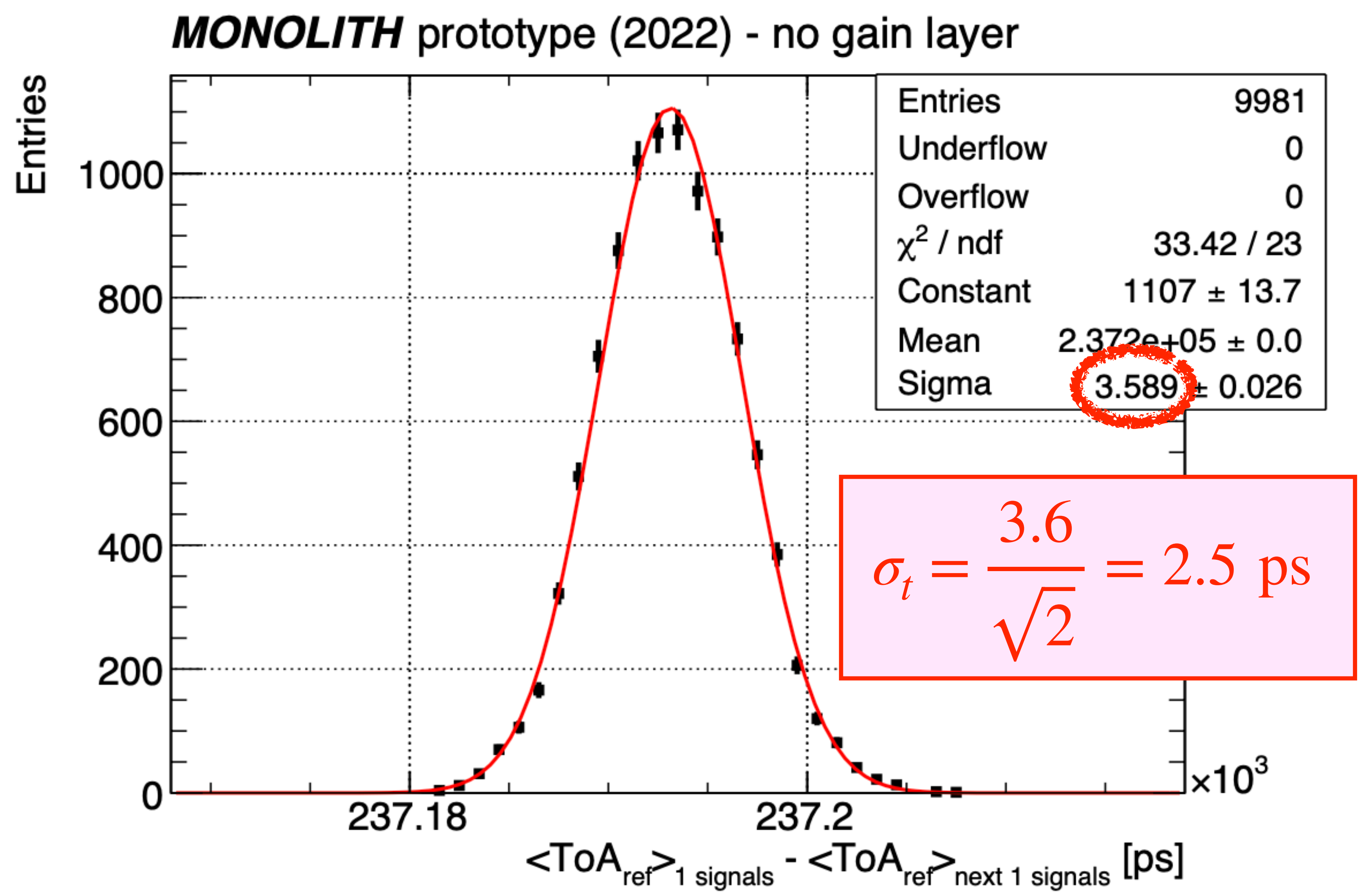
➡ "**DUT**" receiving variable laser power, to study the performance vs. amplitude

2022 prototype2 — no gain layer

Laser Measurement (preliminary)



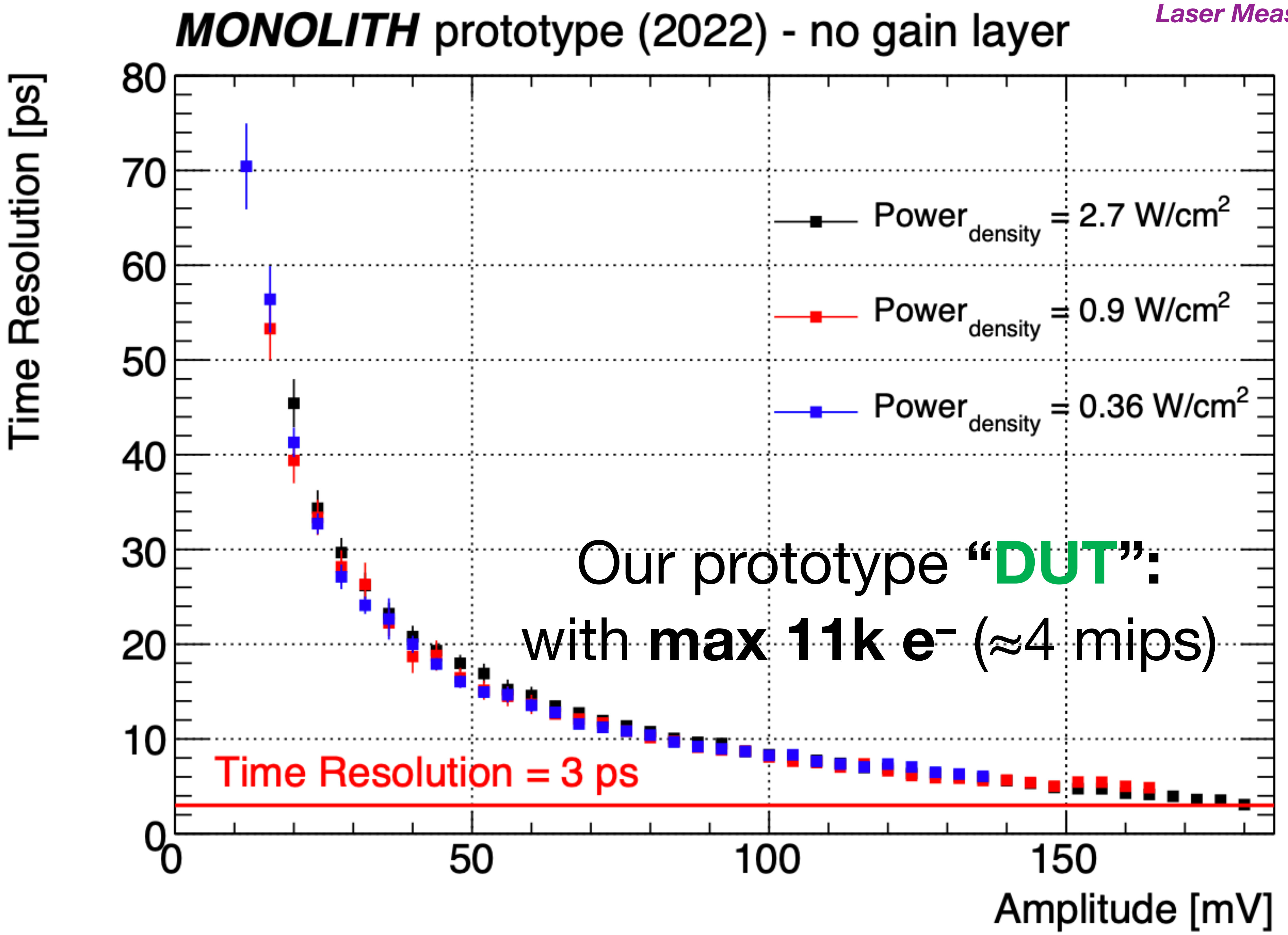
Laser Measurement



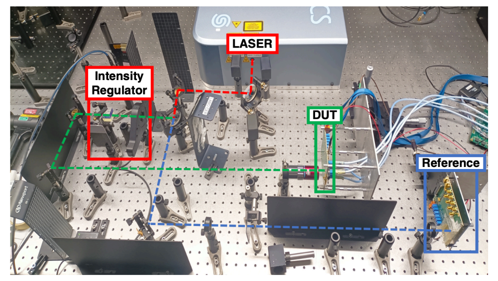
Our prototype "**Reference**":

Time resolution = 2.5 ps

with **17k e⁻** (5—6 mips)

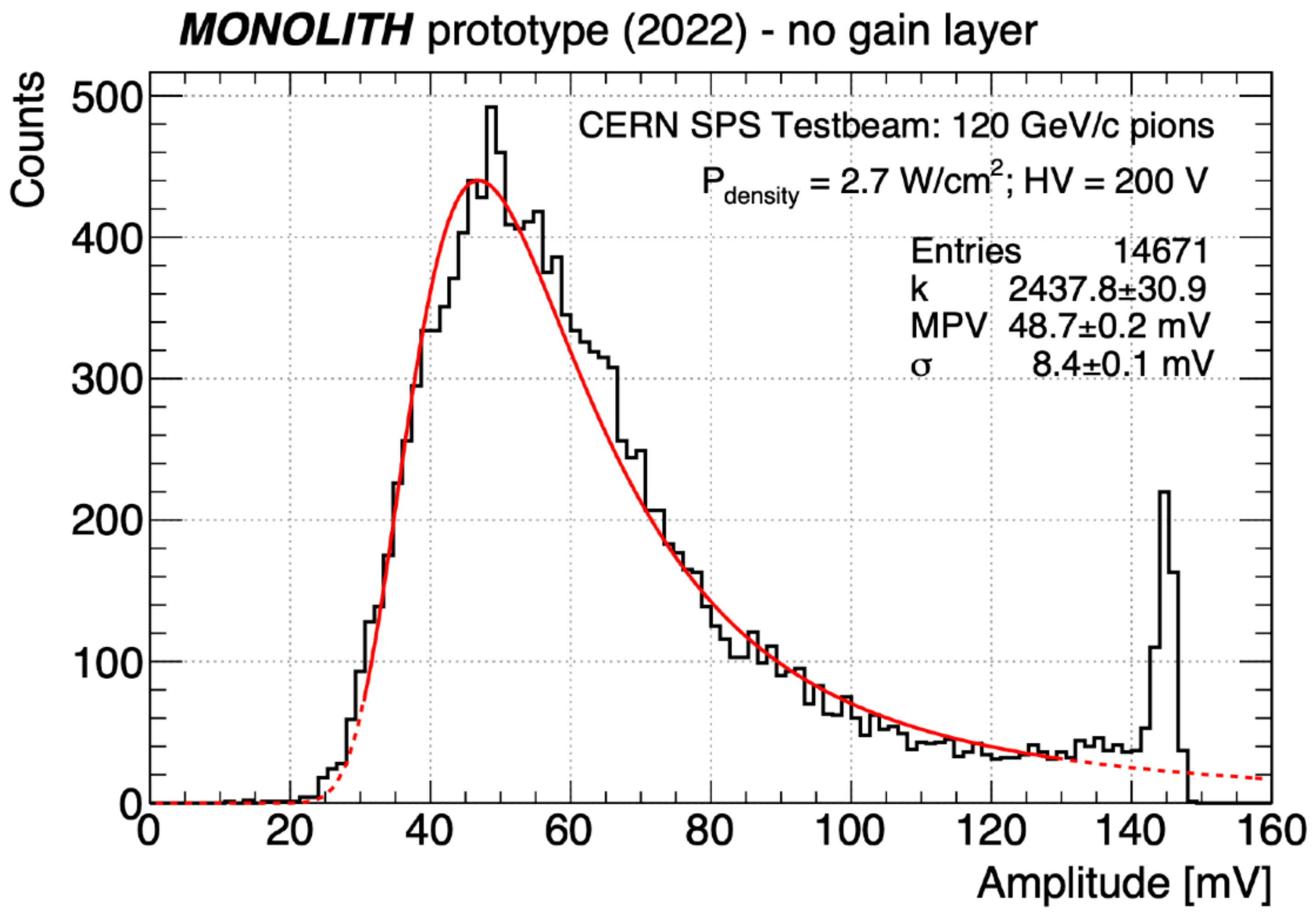


Laser Measurement (preliminary)

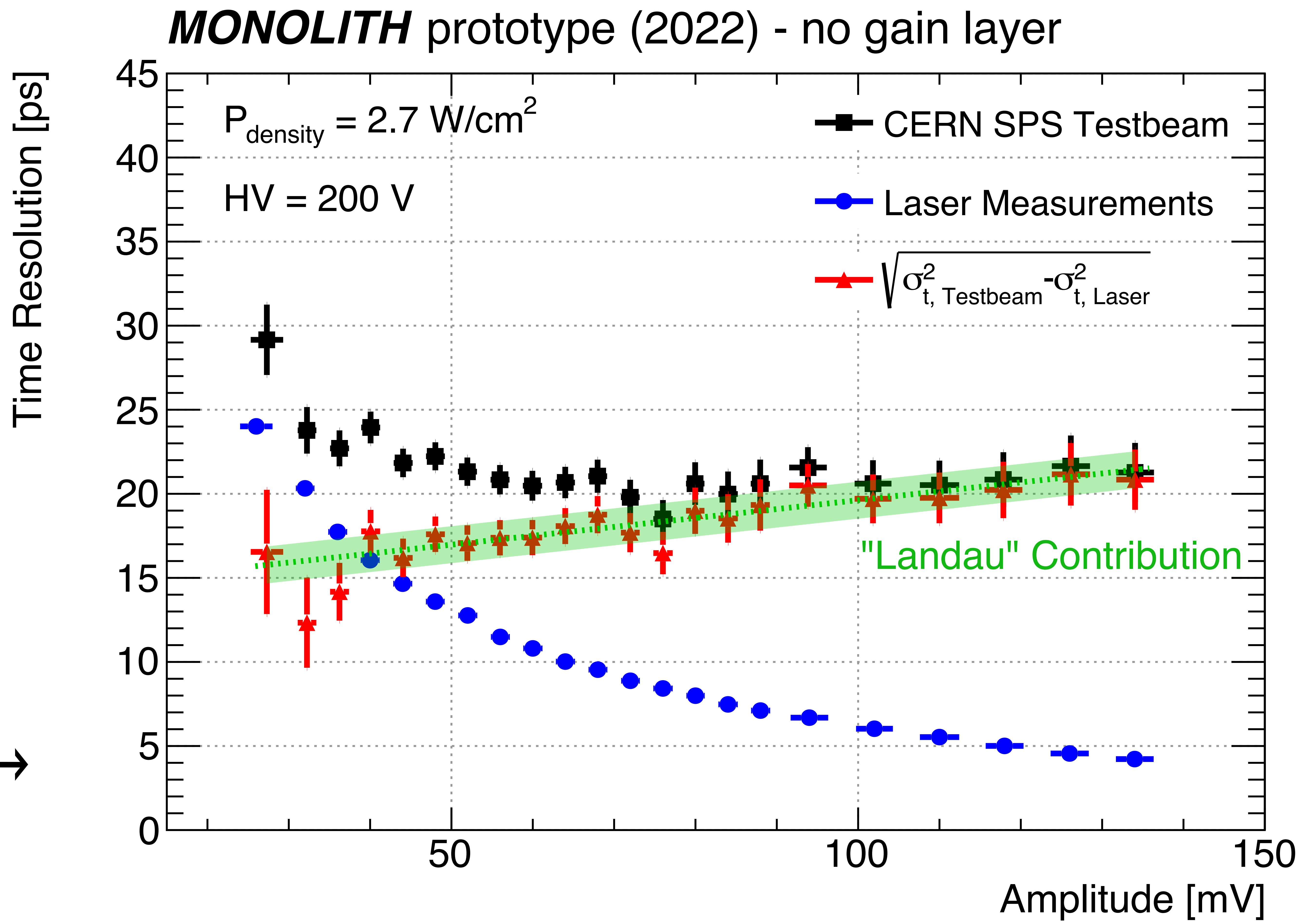


Laser Measurement

Laser amplitudes were reweighed to the testbeam amplitude distribution:



to estimate the charge-collection (“Landau”) noise →

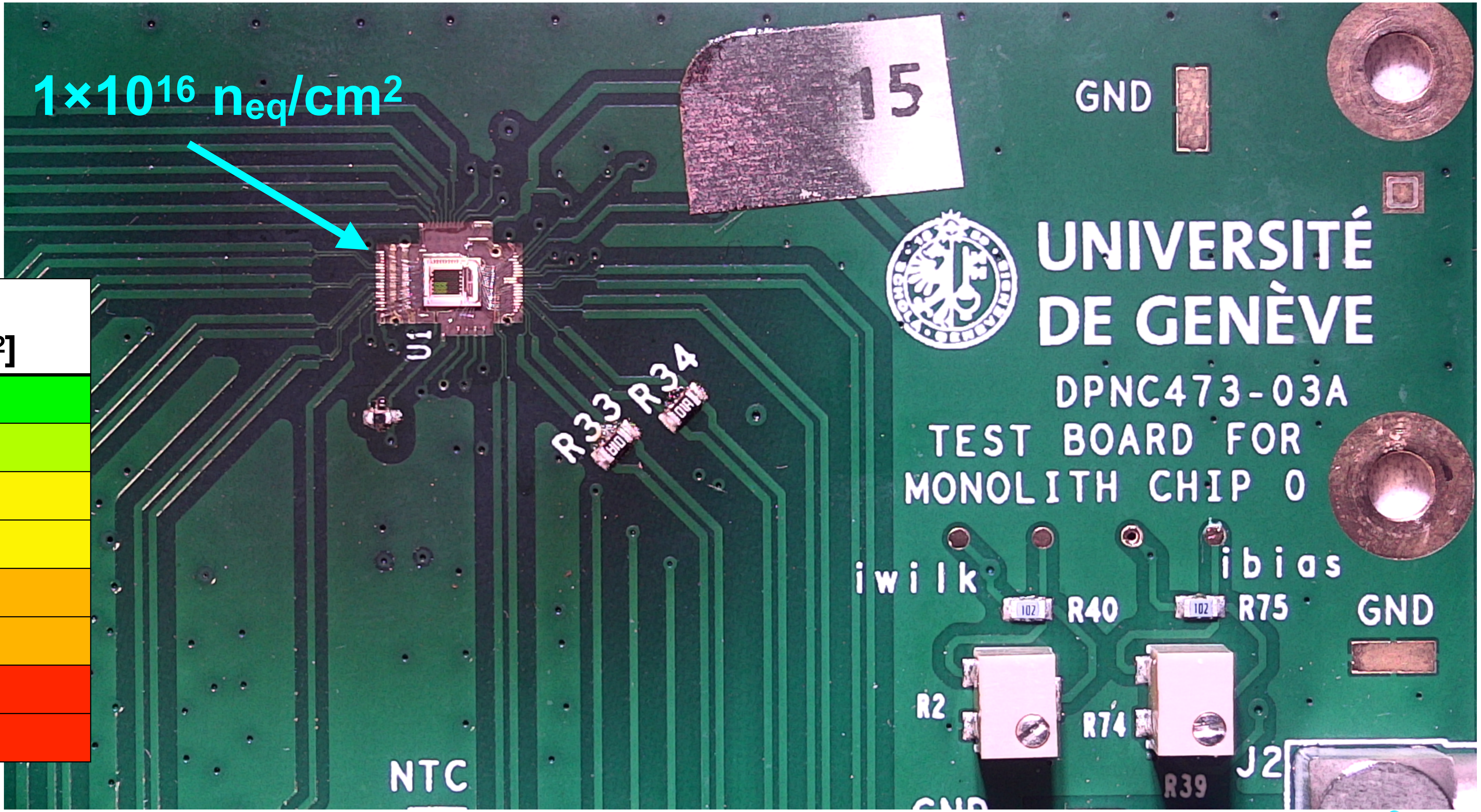


Radiation hardness studies

with the 2022 prototype2 without gain

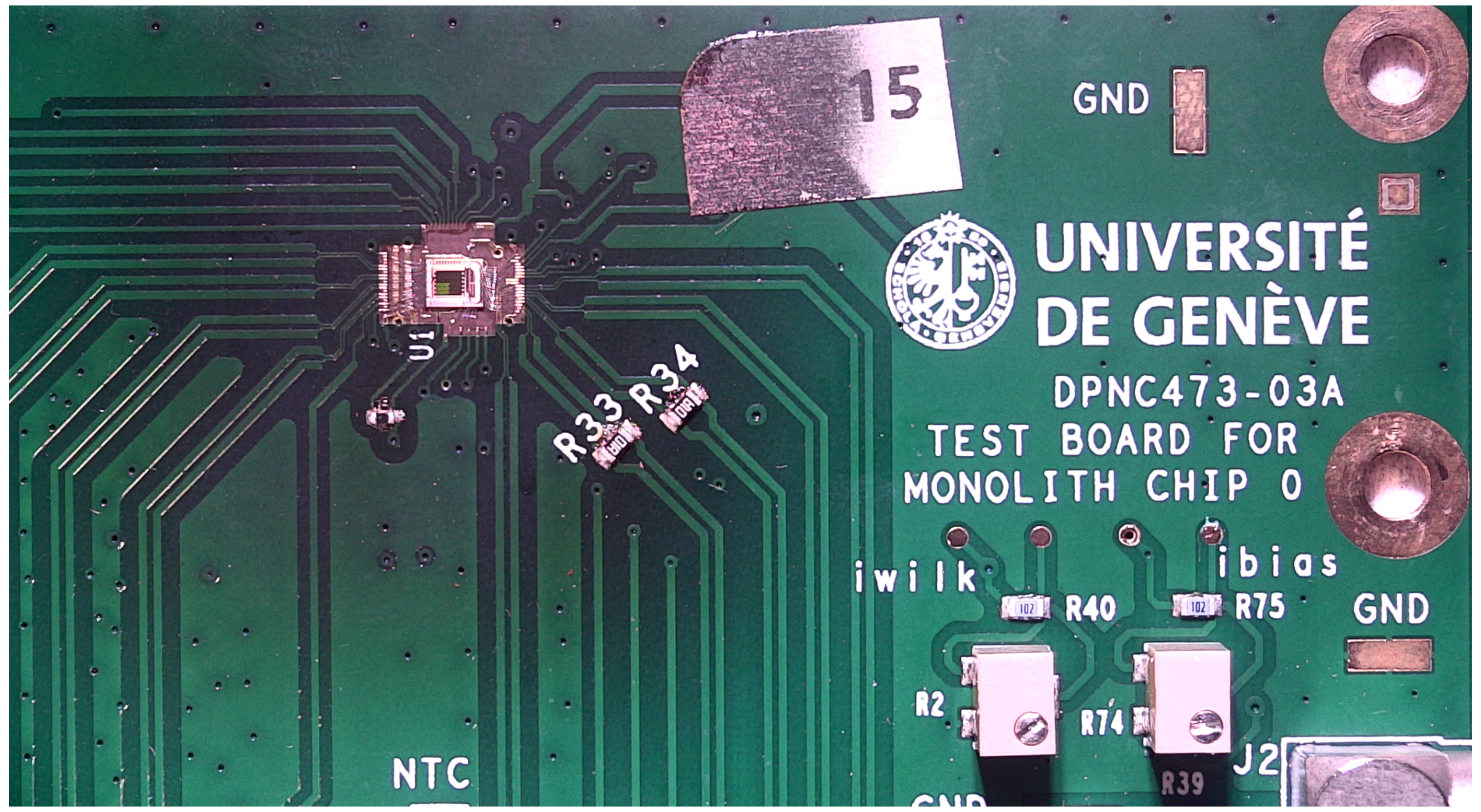
Radiation hardness of SiGe HBTs

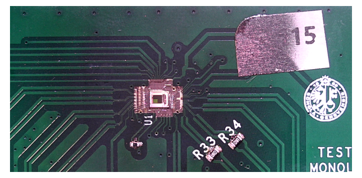
Radiation tolerance studies in collaboration with **KEK** and **IHP** colleagues.
10 samples of prototype2 ASIC were irradiated in Japan up to $1{\times}10^{16}$ n_{eq}/cm^2.



Board Name	Fluence [1 MeV n_{eq}/cm^2]
M23	$2 \cdot 10^{13}$
M22	$9 \cdot 10^{13}$
M21	$6 \cdot 10^{14}$
M19	$6 \cdot 10^{14}$
M18	$3 \cdot 10^{15}$
M17	$3 \cdot 10^{15}$
M16	$1 \cdot 10^{16}$
M15	$1 \cdot 10^{16}$

Radiation hardness of SiGe HBTs





Very good news:

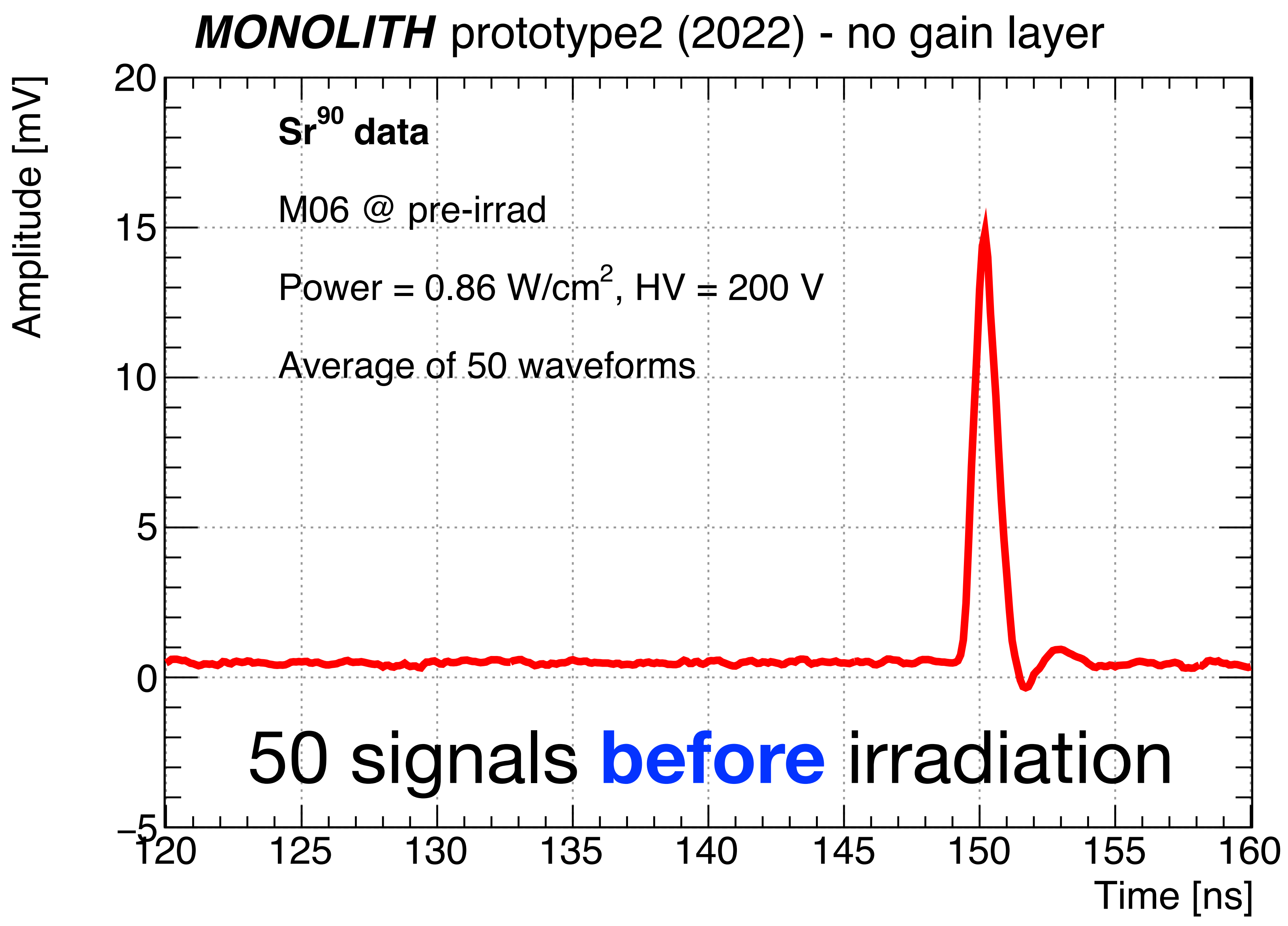
even after 10^{16} n_{eq}/cm^2 the prototypes work !!!

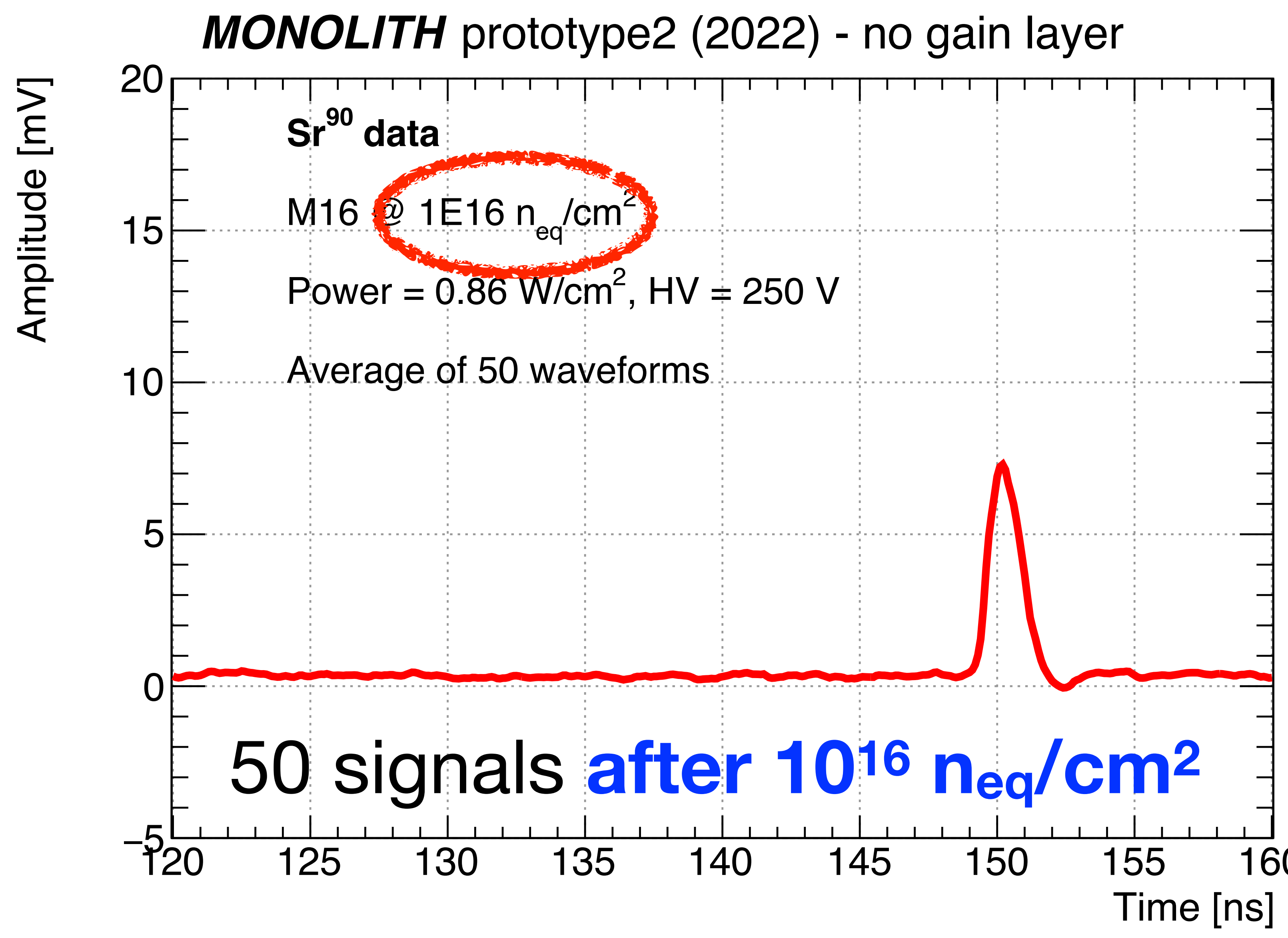
The boards hosting the ASICs seriously damaged at > 10^{14} n_{eq}/cm^2

voltage regulators broken

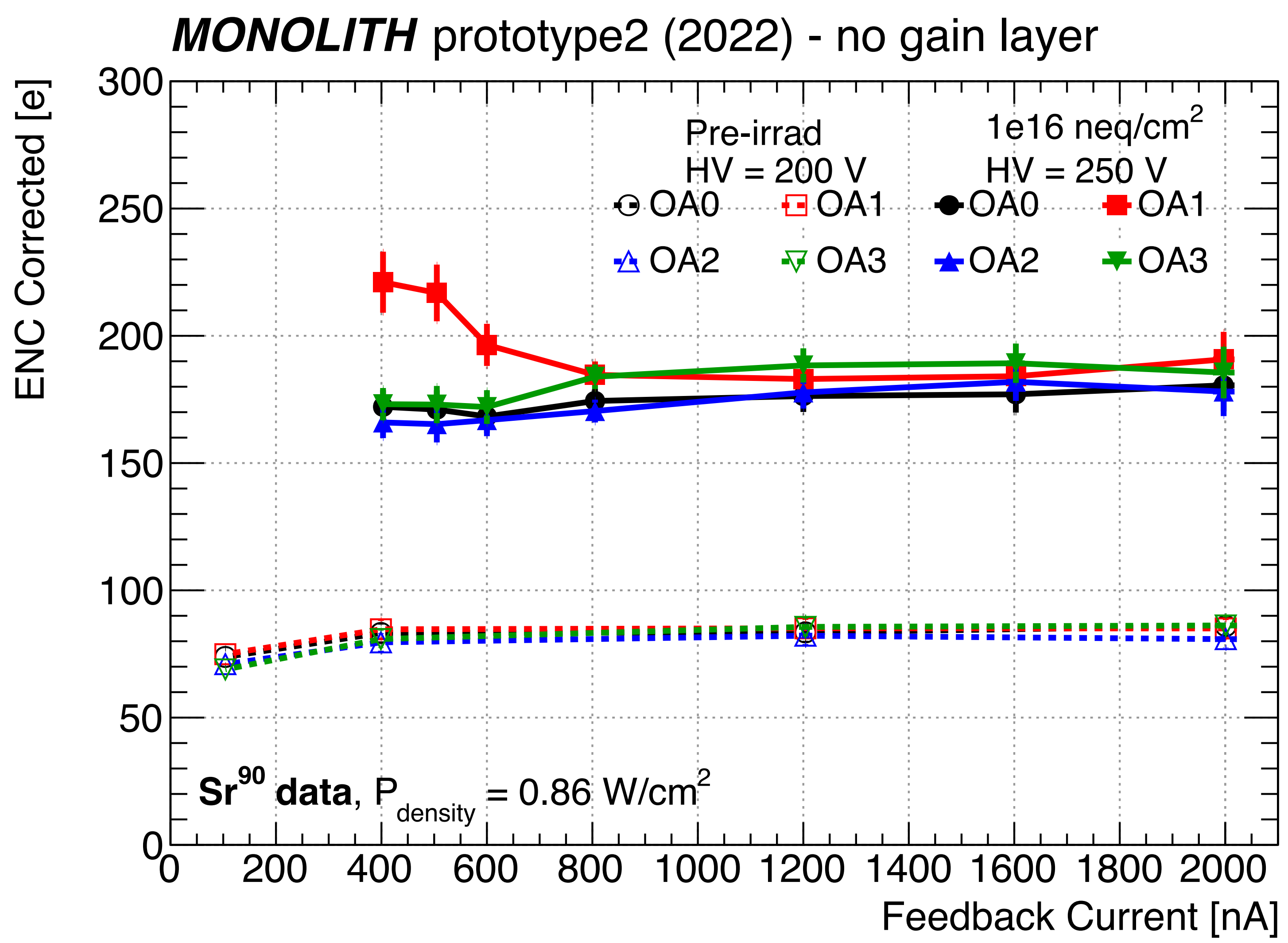
⇩

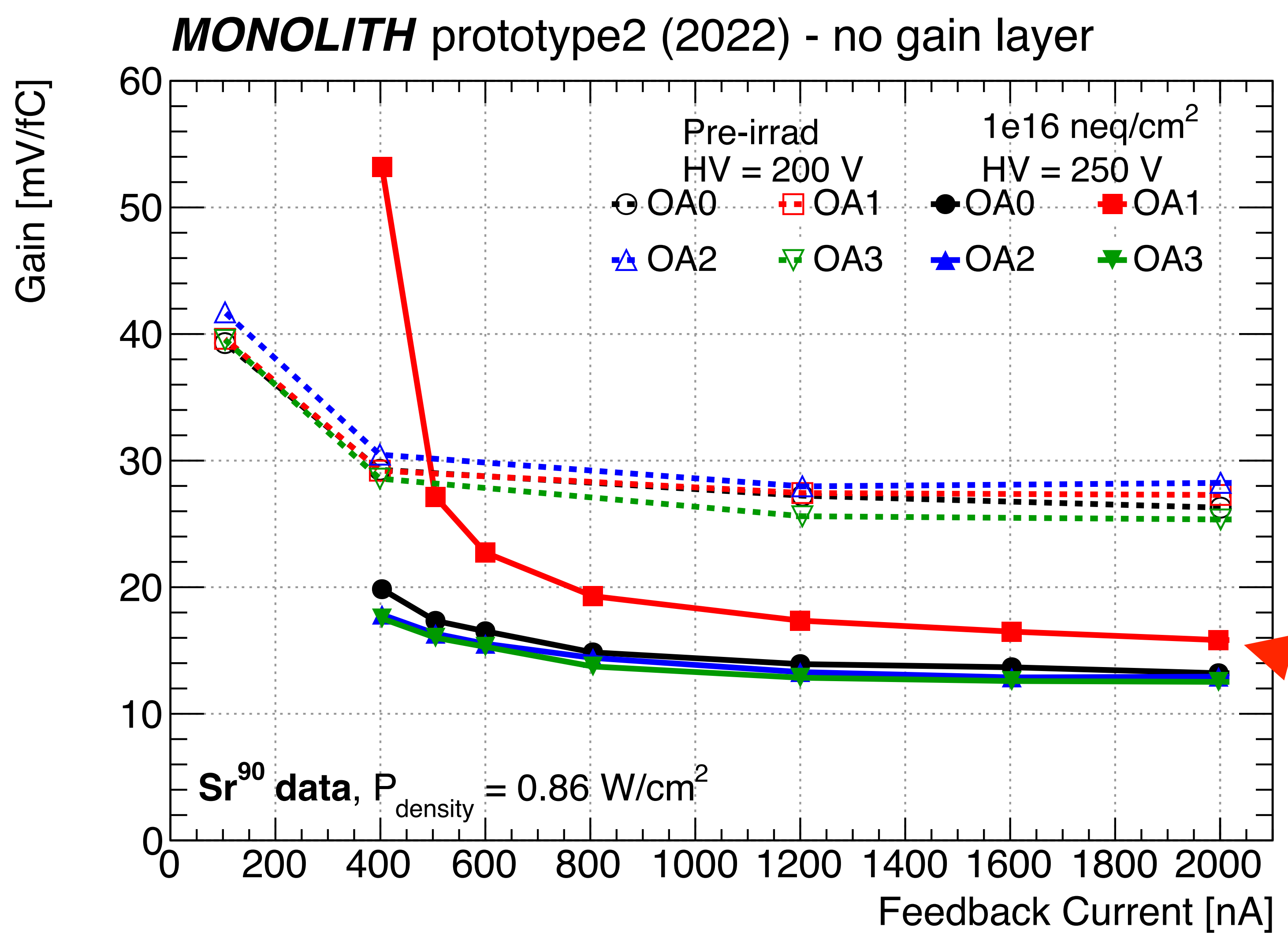
wires soldered on the boards to force LV bias directly from a PS

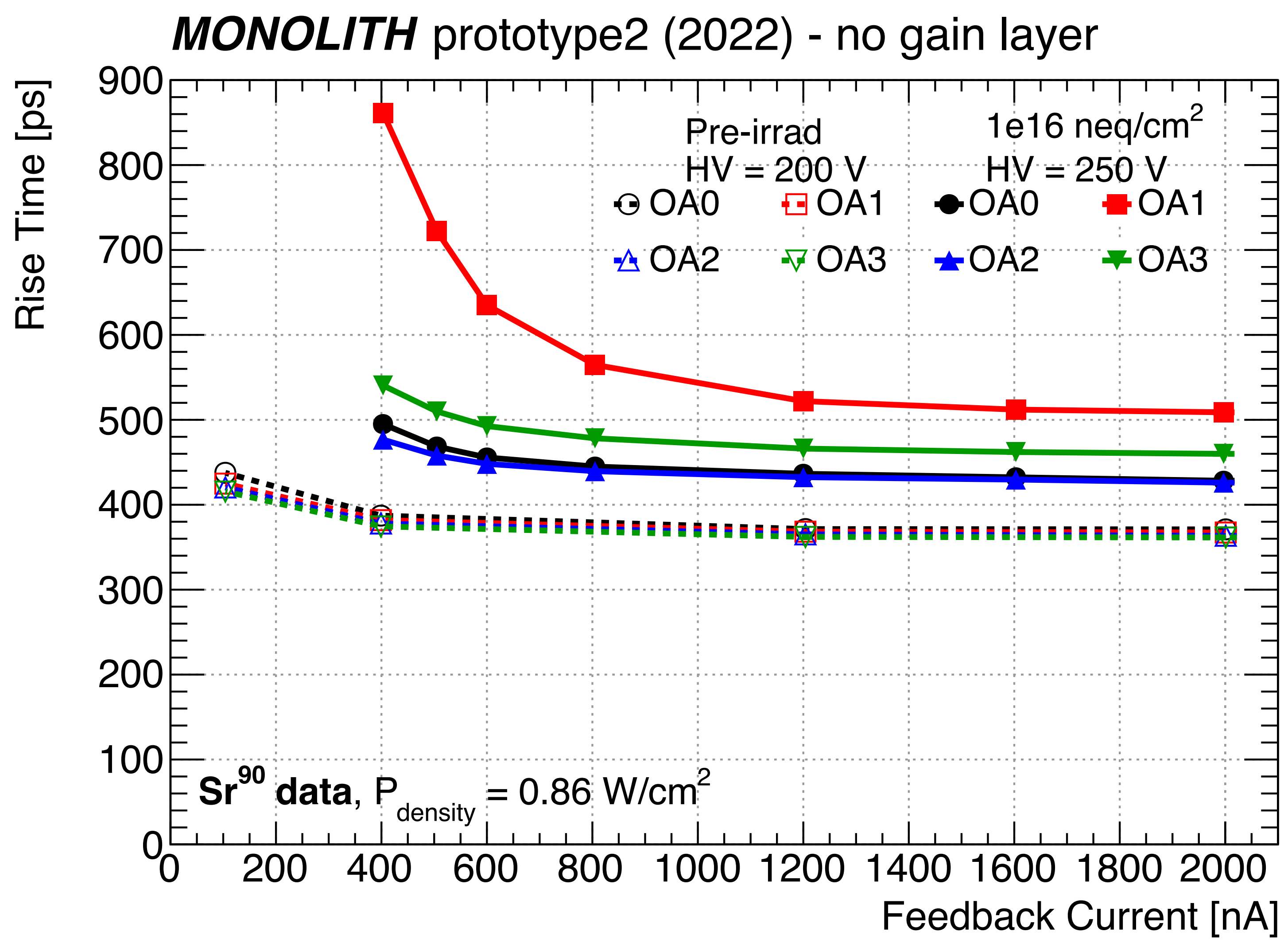


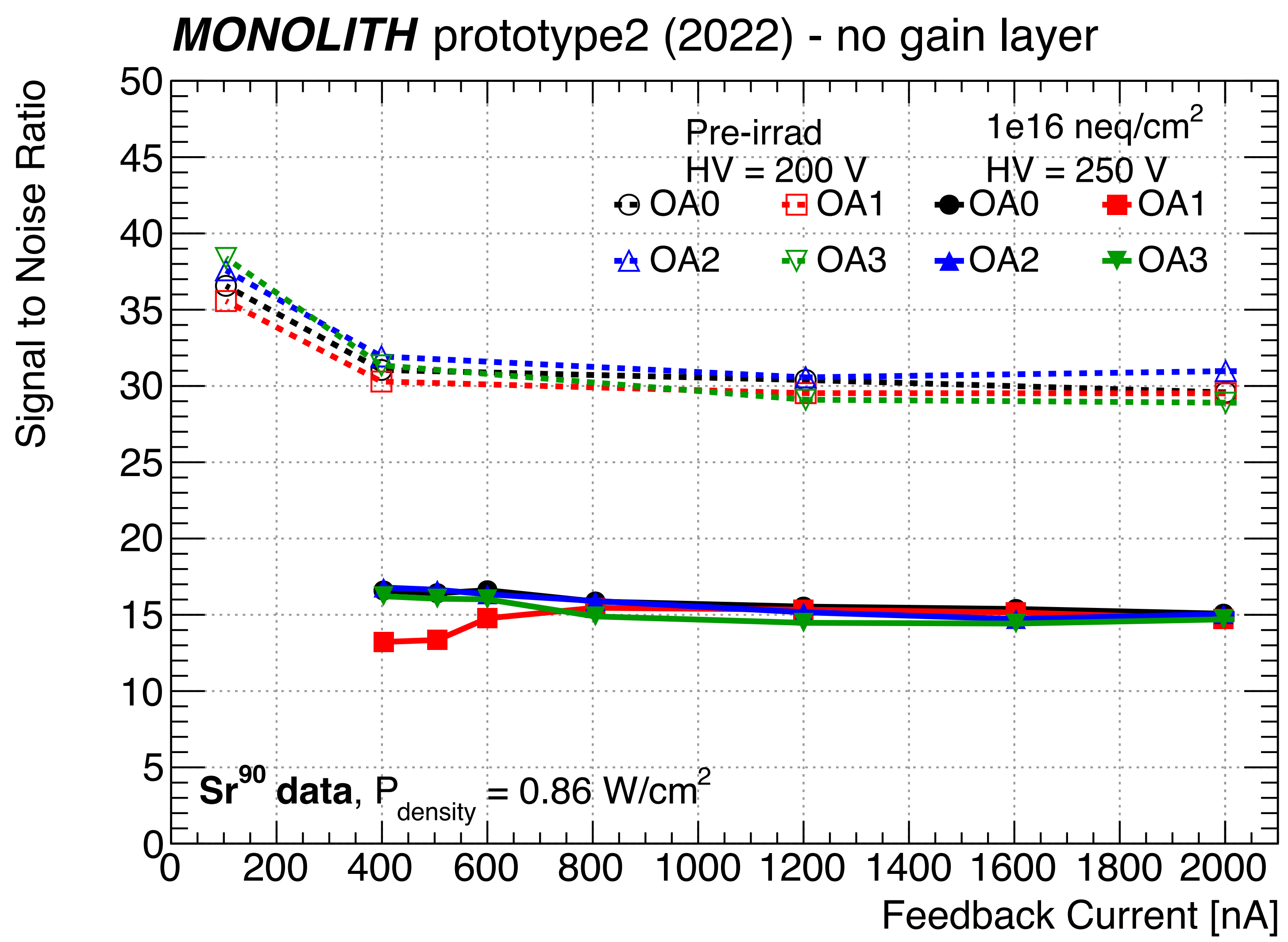


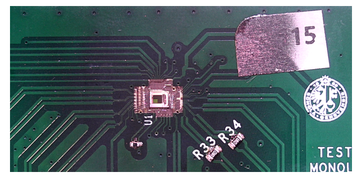
Radiation hardness of SiGe HBTs







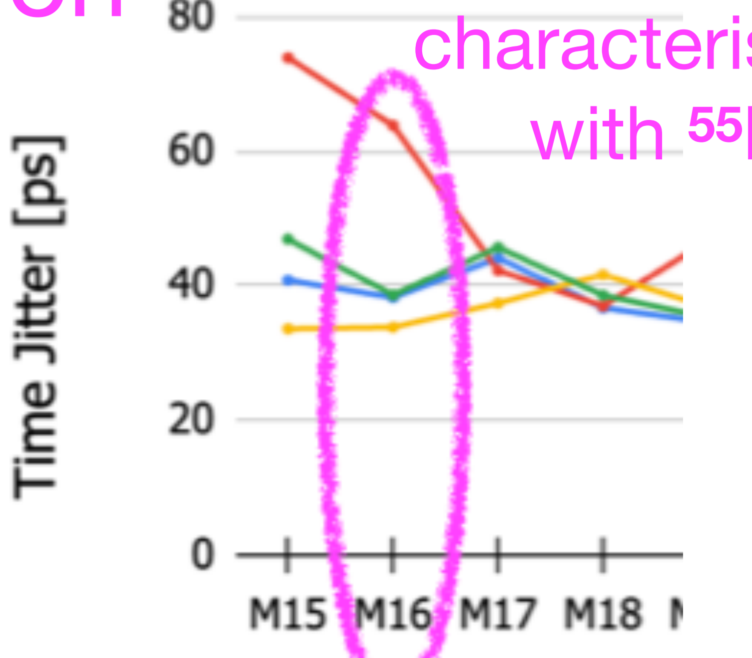




Characterisation with ^{90}Sr source of the four pixels of the board M16 irradiated at 10^{16} n_{eq}/cm^2

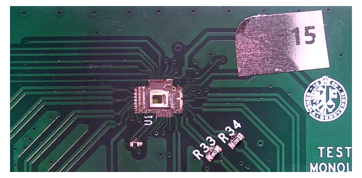
The different behaviour of pixel OA0 was present also before irradiation

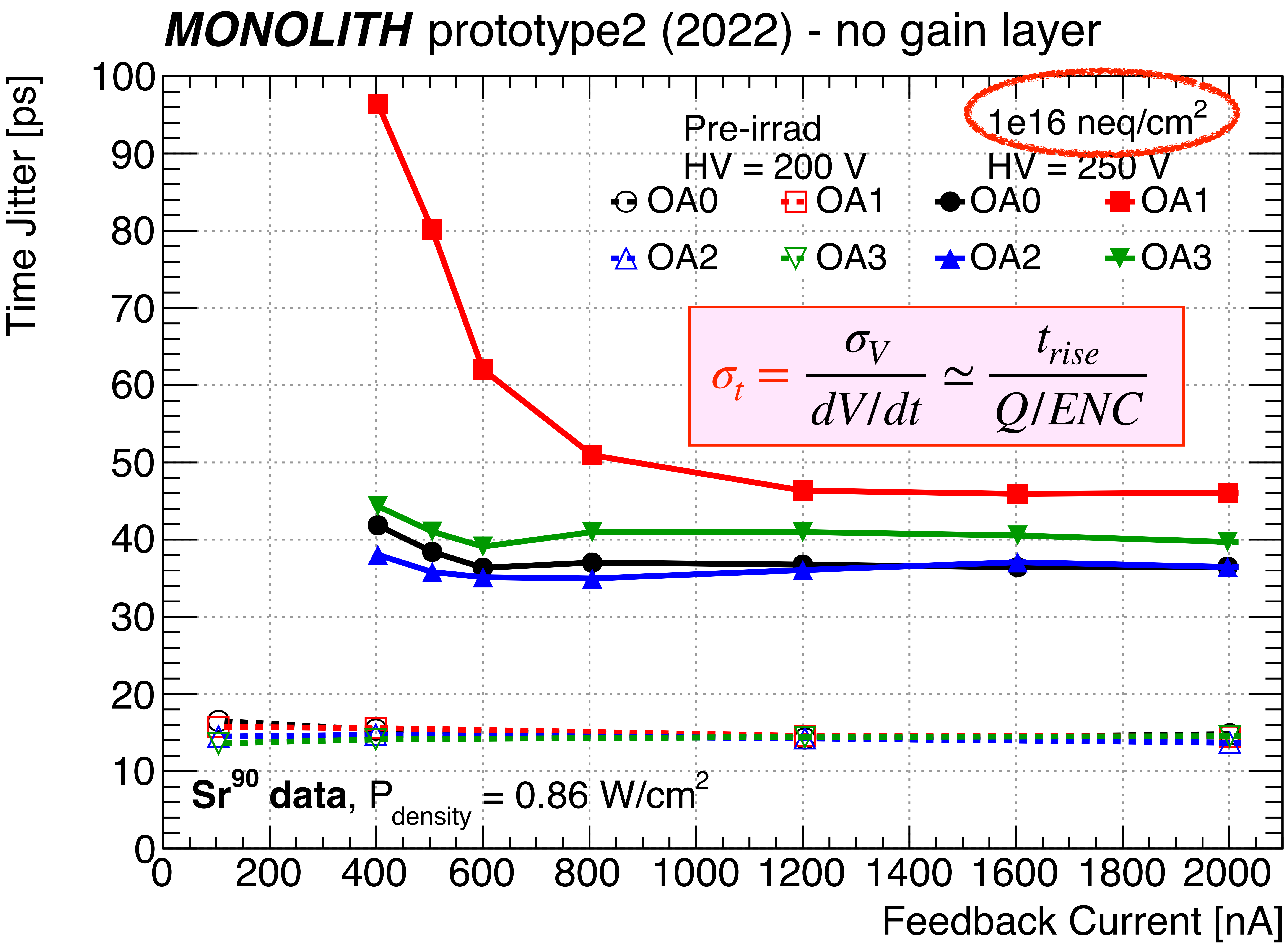
pre-irrad. characterisation with ^{55}Fe



probably due to electronics mismatch (will be reduced in future submission)

Radiation hardness of SiGe HBTs





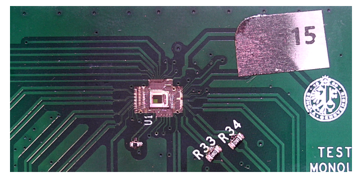
Excellent news from radiation tolerance studies:

ASIC work even at $1{\times}10^{16}\ n_{eq}/cm^2$ and present large $i_{feedback}$ plateaux.

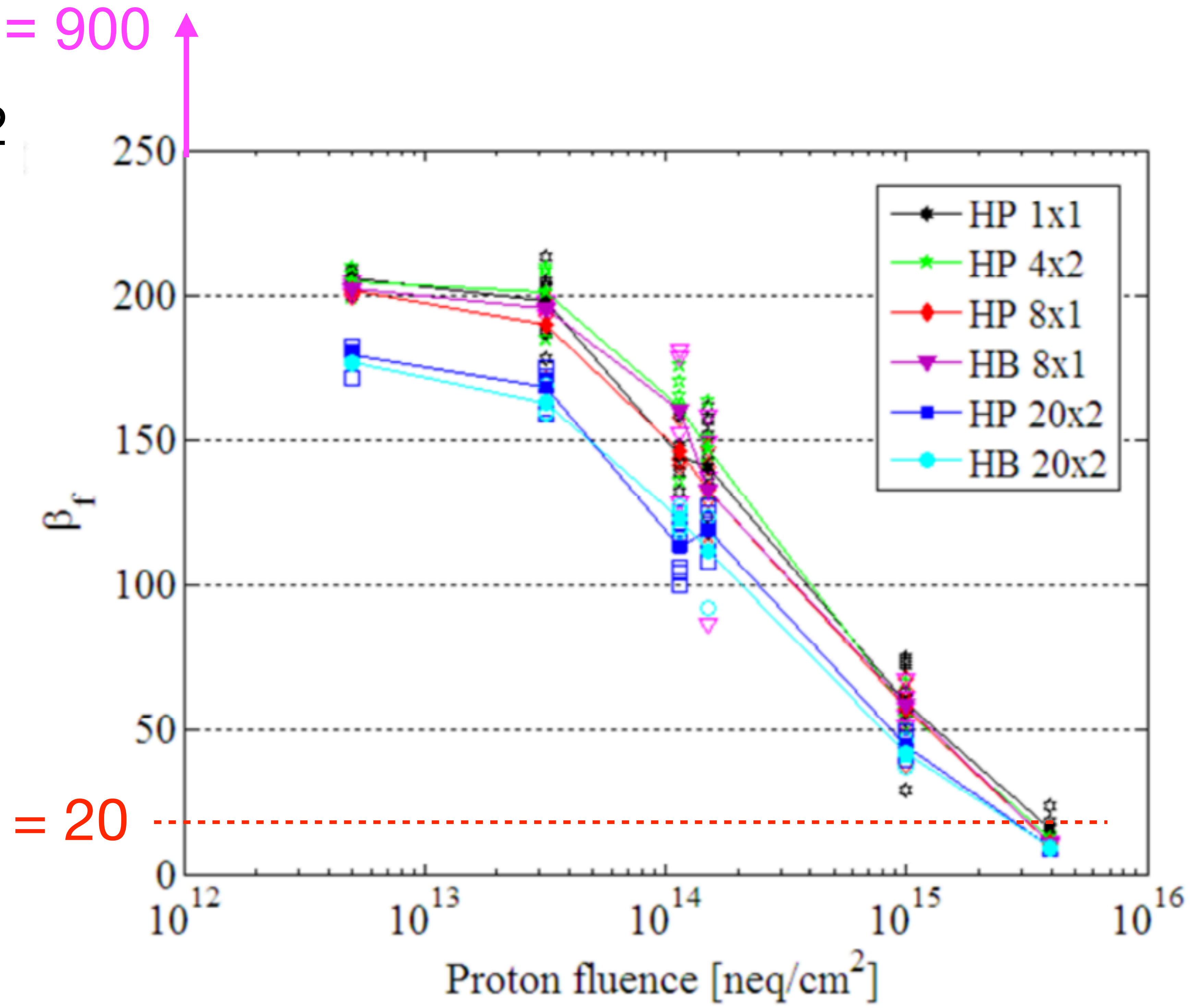
The electronics time jitter increases **from ≈16ps to ≈40ps** with HV increased only by 50 V (200→250 V)

Efficiency & time resolution with mips from testbeam this summer

Radiation hardness of SiGe HBTs

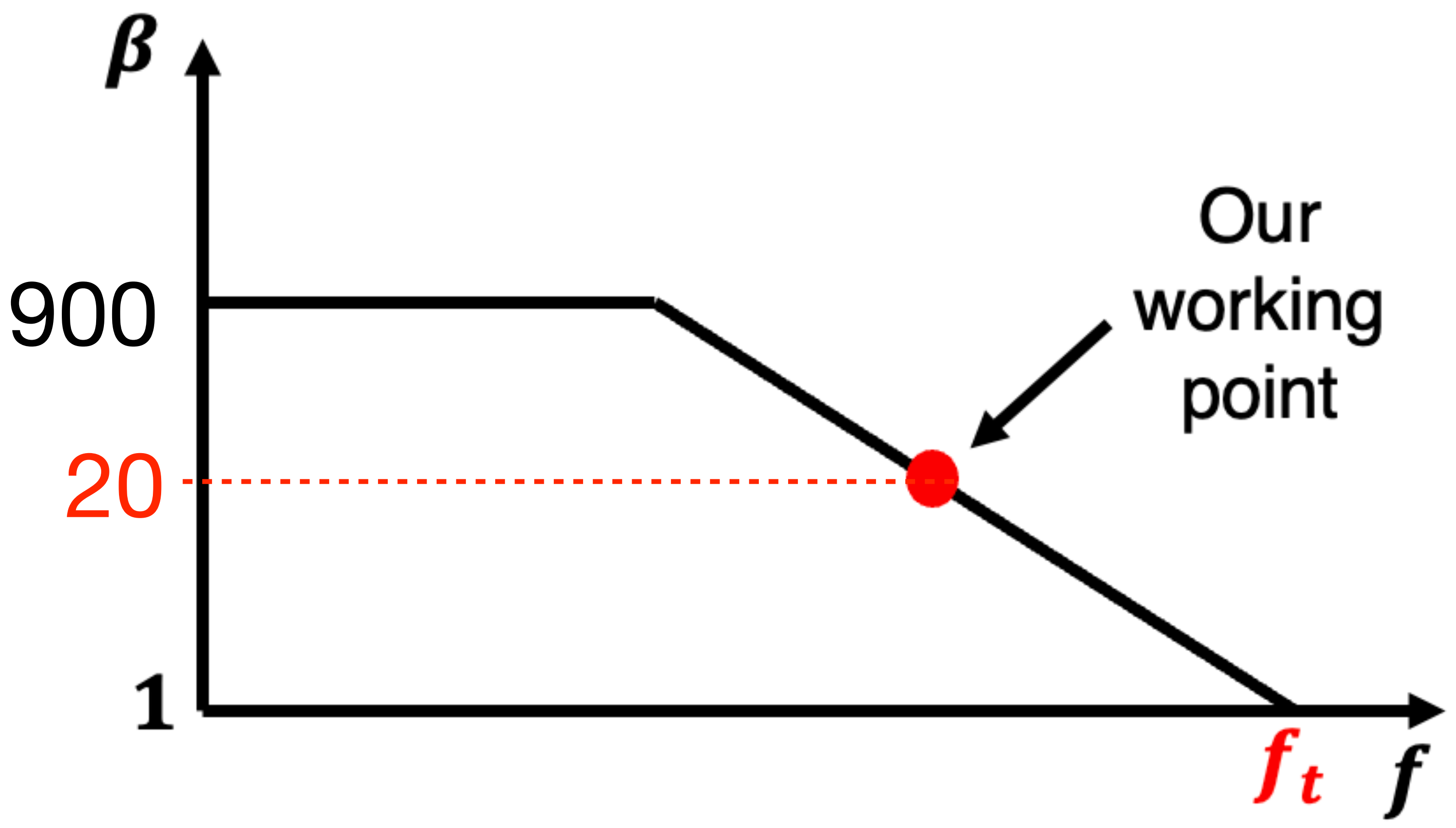


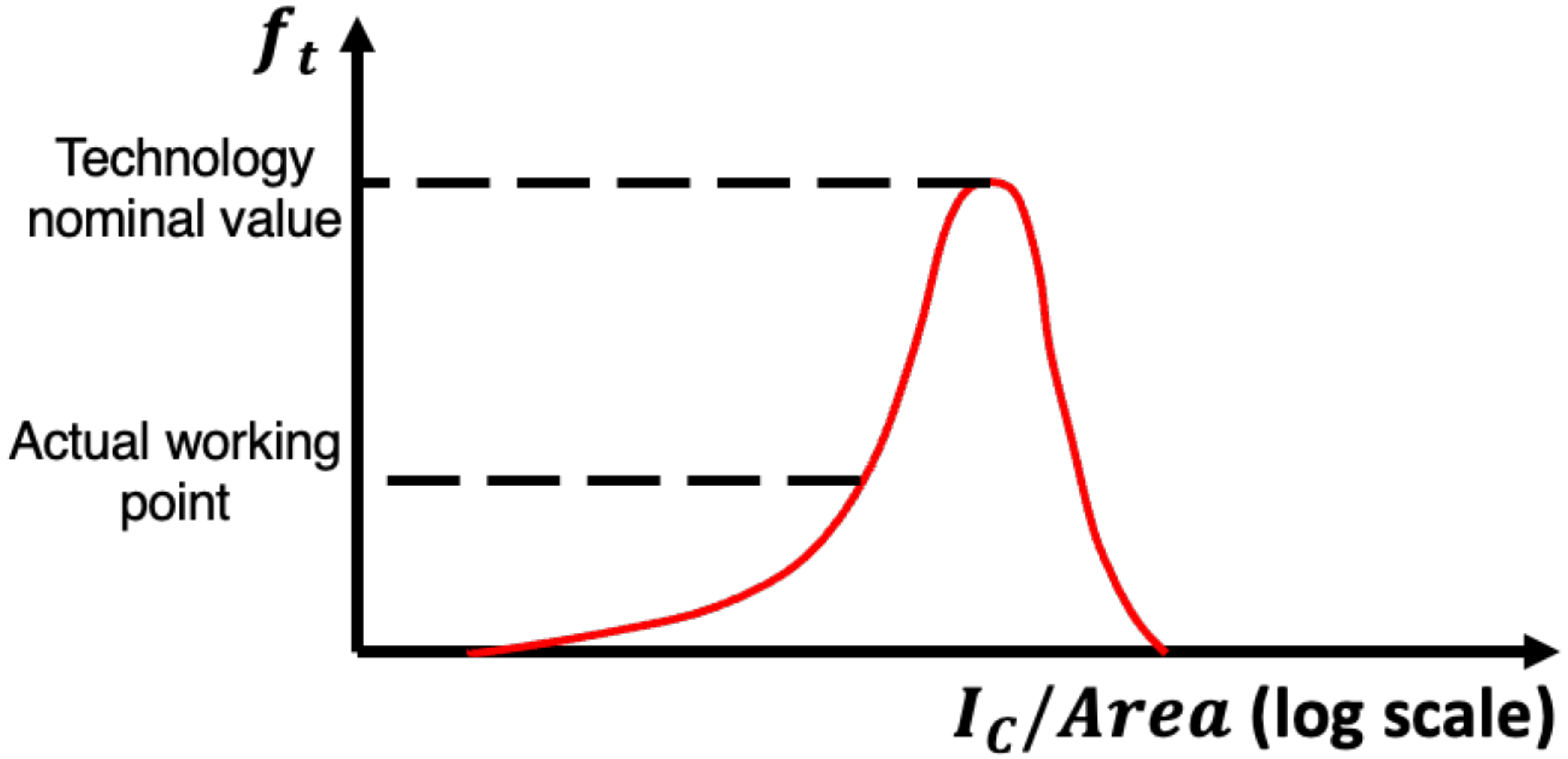
Our SG13G2 process



Our working point

S. Díez et al, IEEE Nuclear Science Symposium & Medical Imaging Conference, Knoxville, TN, 2010, pp. 587-593, doi: 10.1109/NSSMIC.2010.5873828.

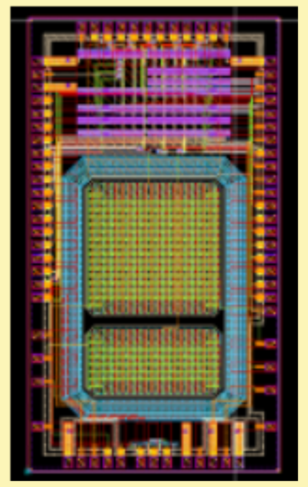




Monolithic SiGe BiCMOS for timing

Monolithic prototypes with SiGe BiCMOS (without internal gain layer)

2016



200ps

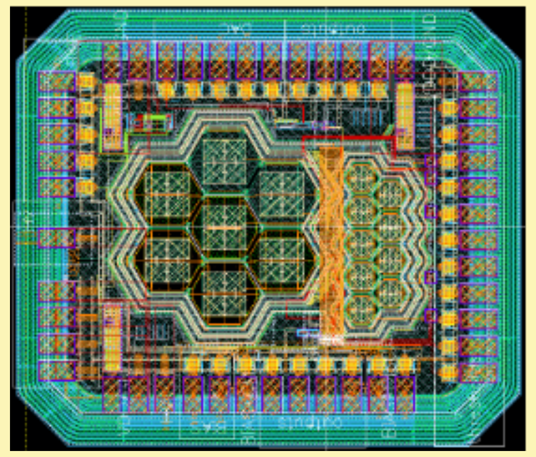
- 1 mm² pixel
- Discriminator

2017

110ps

- 30 pixels 500x500μm²
- 100ps TDC +I/O logic

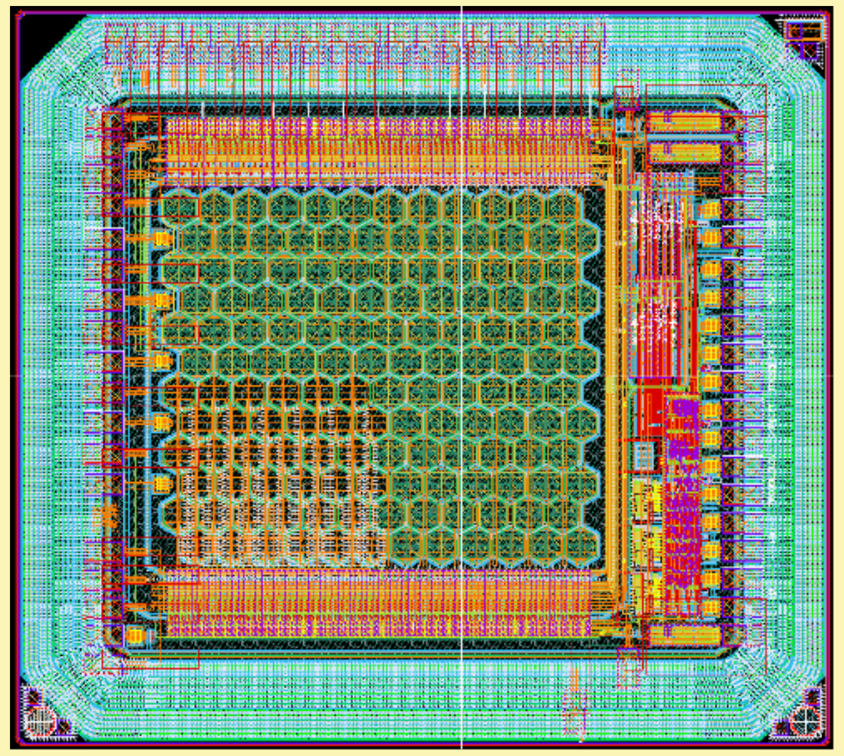
2018



50ps

- Hexagonal pixels 100μm and 200μm pitch
- Discriminator output

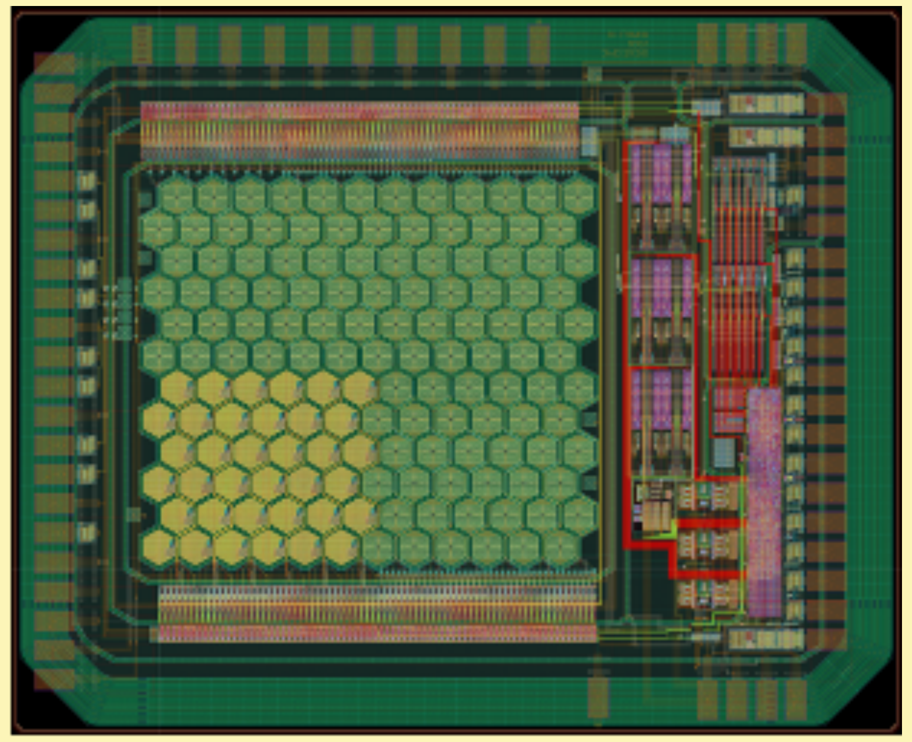
2020



36 ps

- Hexagonal pixels 100μm pitch
- 30ps TDC +I/O logic
- Analog channels

2022

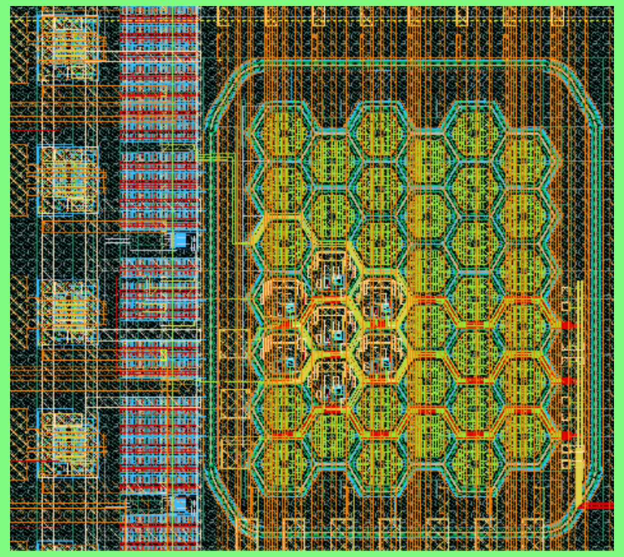


20 ps

- Hexagonal pixels 100μm pitch
- improved electronics
- 50μm epitaxial layer (350Ωcm)

BJT radiation hardness demonstrated

May 2023



< 20 ps ?

- Hexagonal pixels **50μm pitch**
- improved electronics (4 times less power consumption)

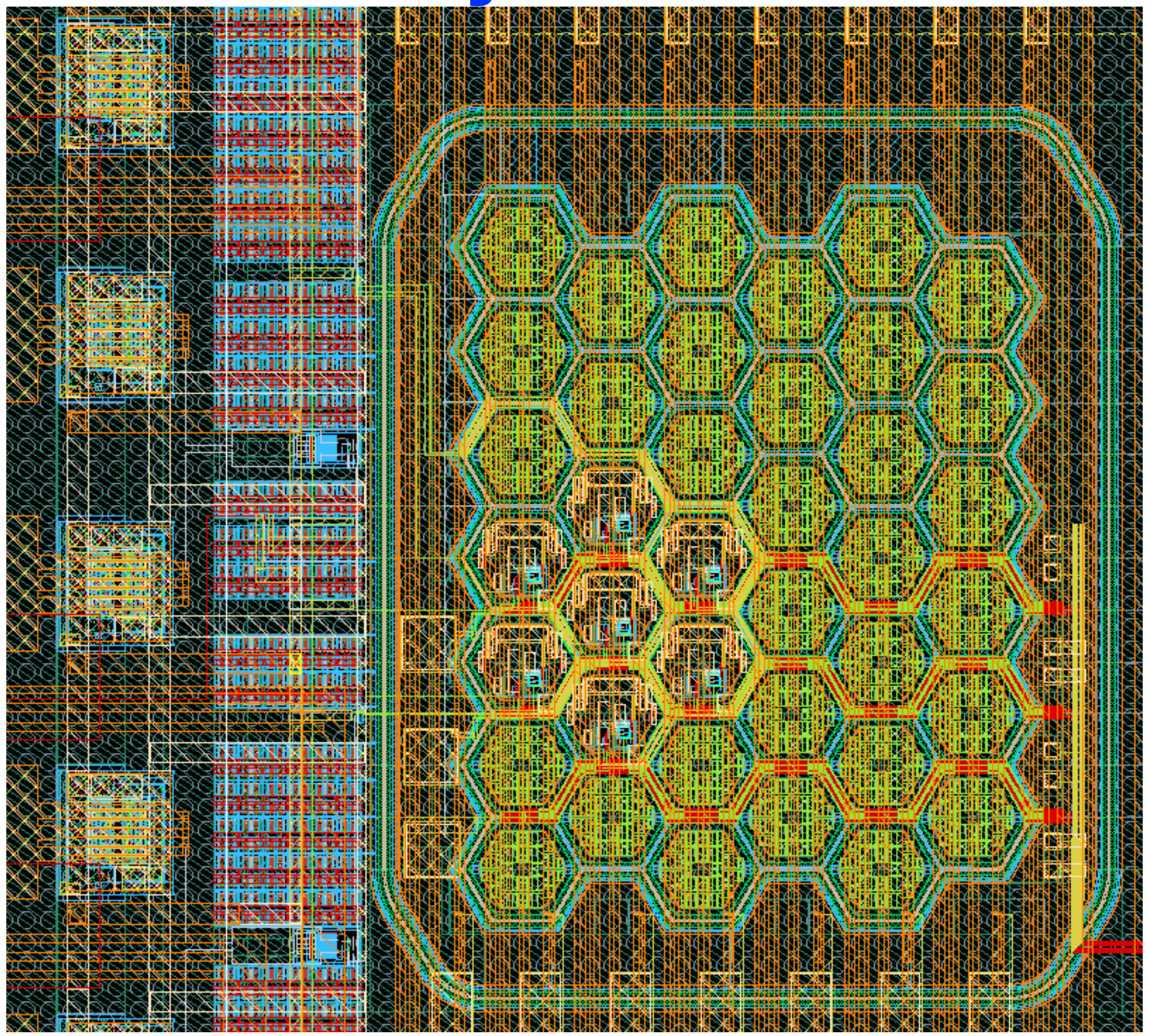
Next step of our R&D

without internal gain layer

Third MONOLITH prototype: 50μm pitch

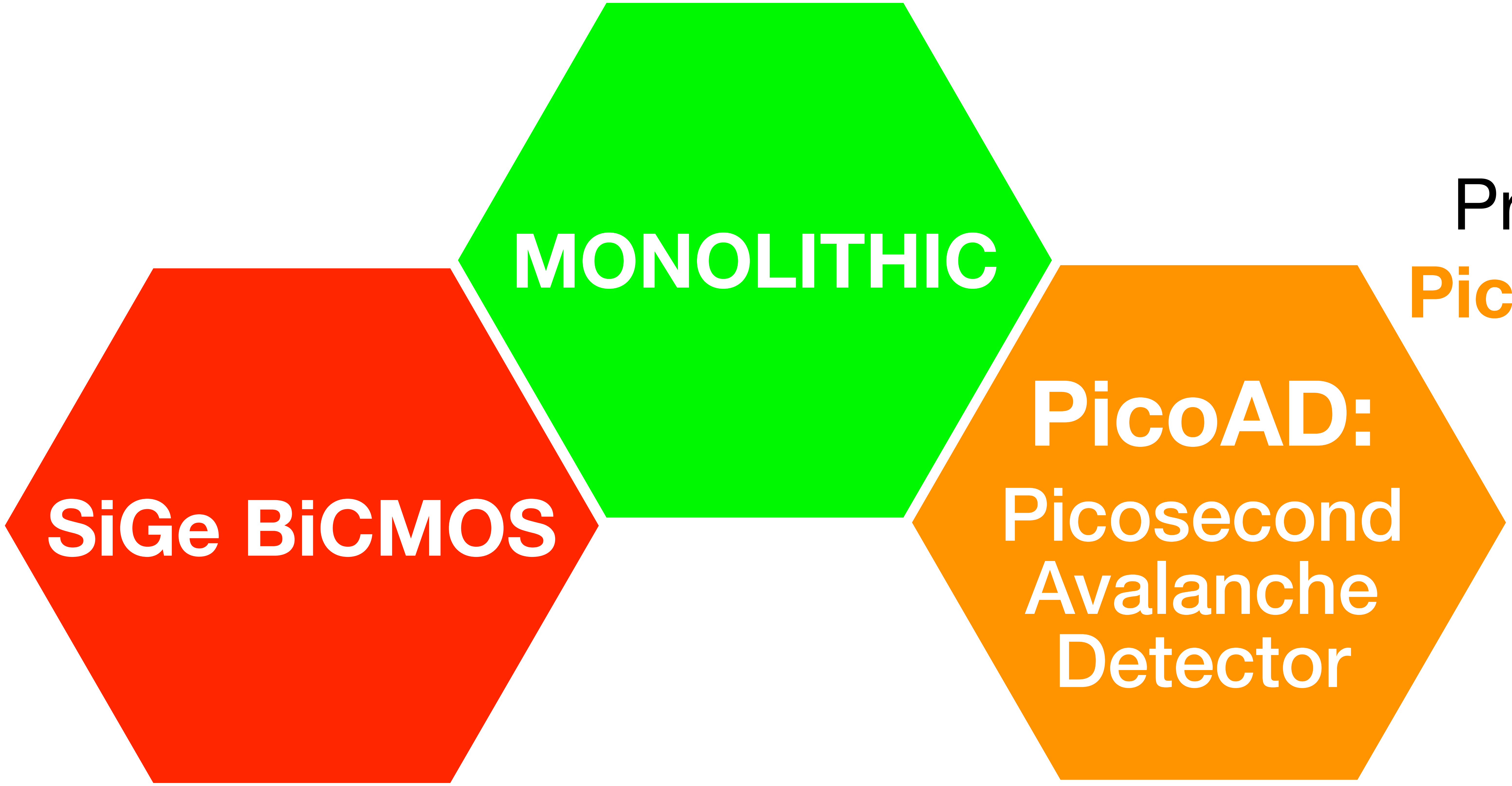
- New prototype: pixels with **50μm pitch**
  - smaller capacitance
- **improved FE electronics**
  - same timing performance with 4-times less power
  - 3 different configurations:
    - ➡ analog output with FE in pixel
    - ➡ analog output with FE off pixel
    - ➡ discriminated output with FE and discriminator in pixel
  - reduced inter-pixel distance from 10μm to 6μm to maintain time resolution at pixel edges
- Back from foundry last Friday

May 2023



European Research Council
Established by the European Commission

The MONOLITH Project



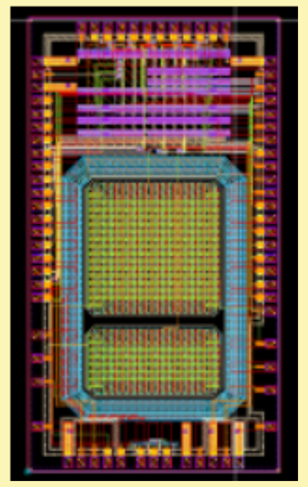
Production of
PicoAD sensors

Monolithic SiGe BiCMOS for timing

European Research Council
Established by the European Commission

Monolithic prototypes with SiGe BiCMOS (without internal gain layer)

2016



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110ps

- 30 pixels 500x500μm²
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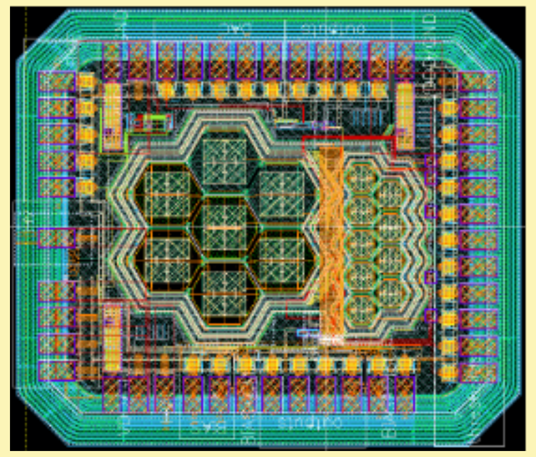
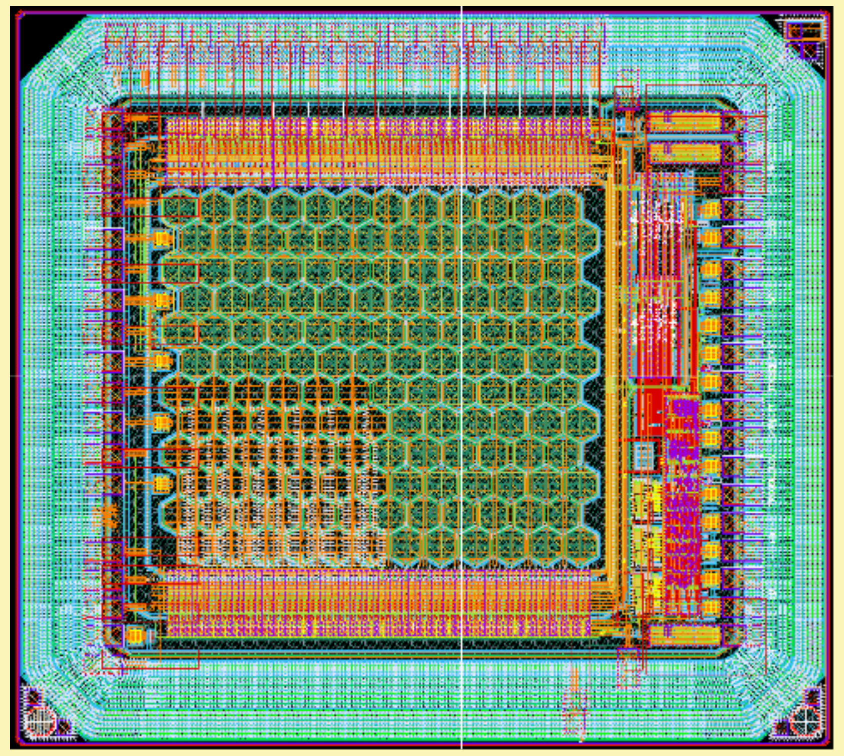


50ps

- Hexagonal pixels 100μm and 200μm pitch
- Discriminator output

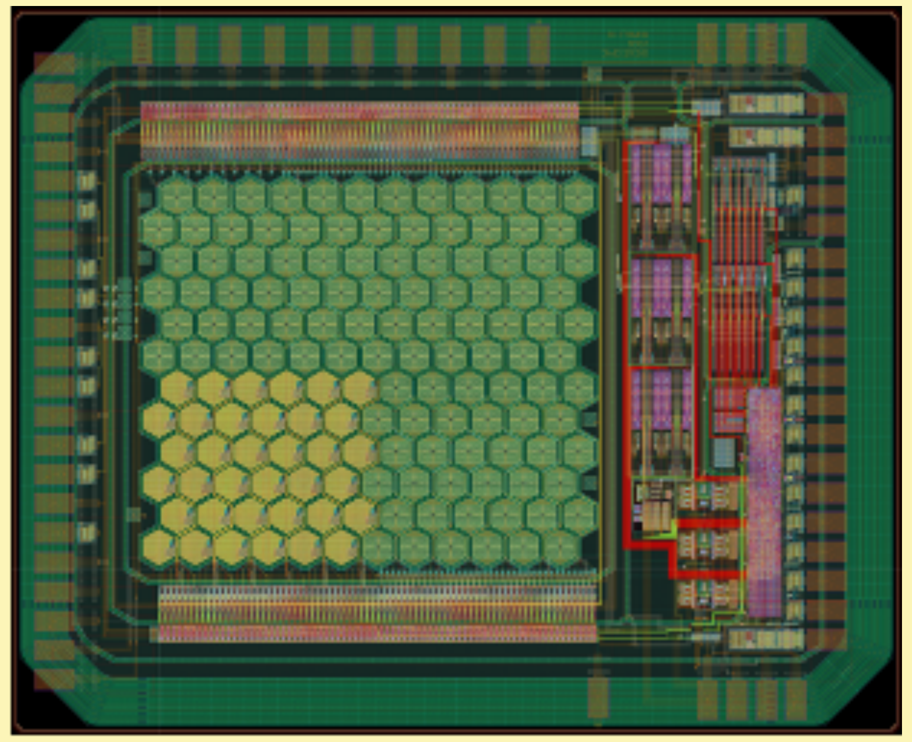
2020



36 ps

- Hexagonal pixels 100μm pitch
- 30ps TDC +I/O logic
- Analog channels

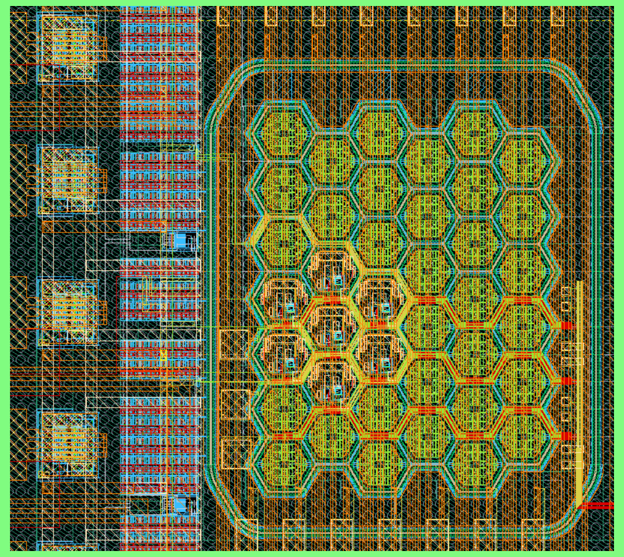
2022



20 ps

- Hexagonal pixels 100μm pitch
- improved electronics
- 50μm epitaxial layer (350Ωcm)

May 2023



< 20 ps ?

- Hexagonal pixels **50μm pitch**
- improved electronics

In 2022 : **proof-of-concept**
monolithic prototype
with internal gain layer
(using 2020 masks)

PicoAD
special wafers produced internally by IHP
(not optimised yet)

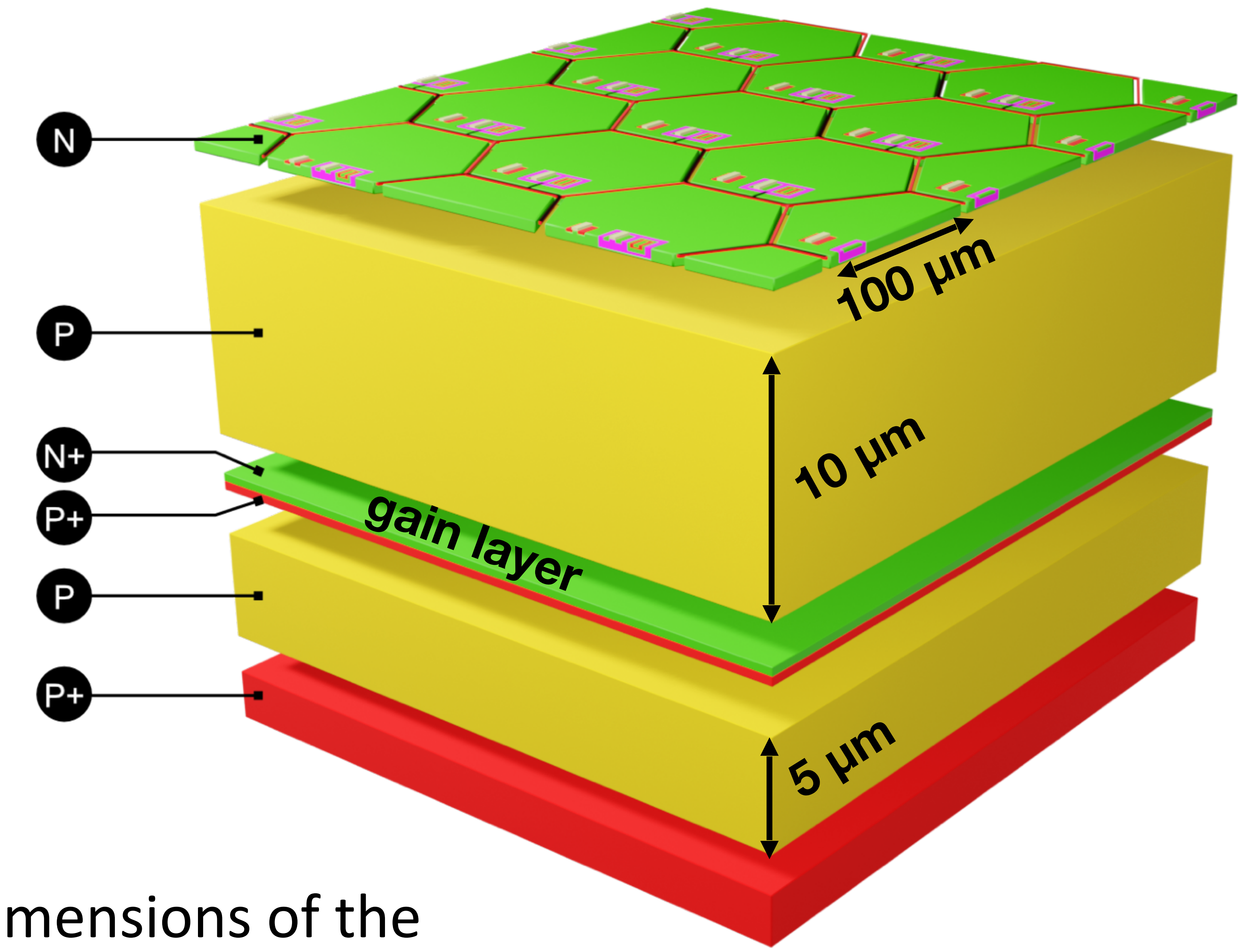
PicoAD Sensor Concept

© G. Iacobucci, L. Paolozzi and P. Valerio. Multi-junction pico-avalanche detector;
European Patent EP3654376A1, US Patent US2021280734A1, Nov 2018

PicoAD:

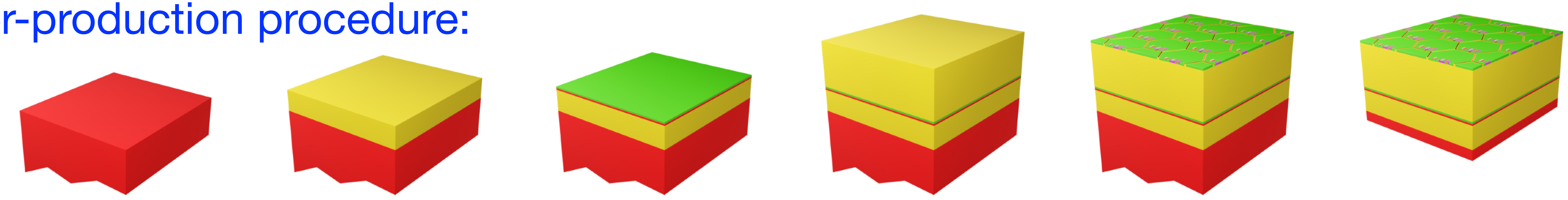
Multi-Junction Picosecond-Avalanche Detector©
with continuous and deep gain layer:

- De-correlation from implant size/geometry
  → **high pixel granularity and full fill factor**
  (high spatial resolution and efficiency)
- Only small fraction of charge gets amplified
  → **reduced charge-collection noise**
  (enhance timing resolution)



Dimensions of the
proof-of-concept prototype (not optimised for timing)

Wafer-production procedure:



Step 1 Step 2 Step 3 Step 4 Step 5 Step 6

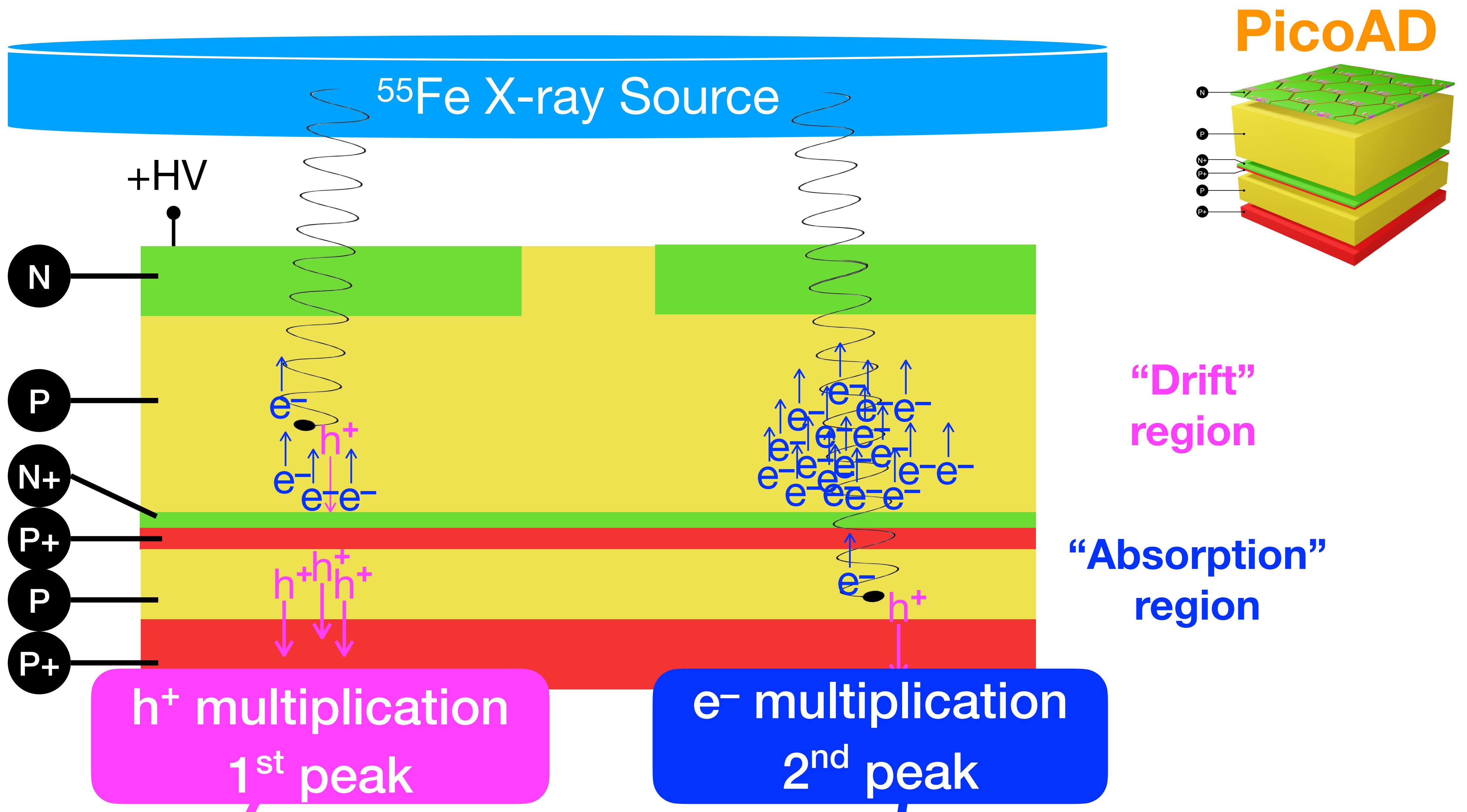
Gain Measurement with ^{55}Fe source

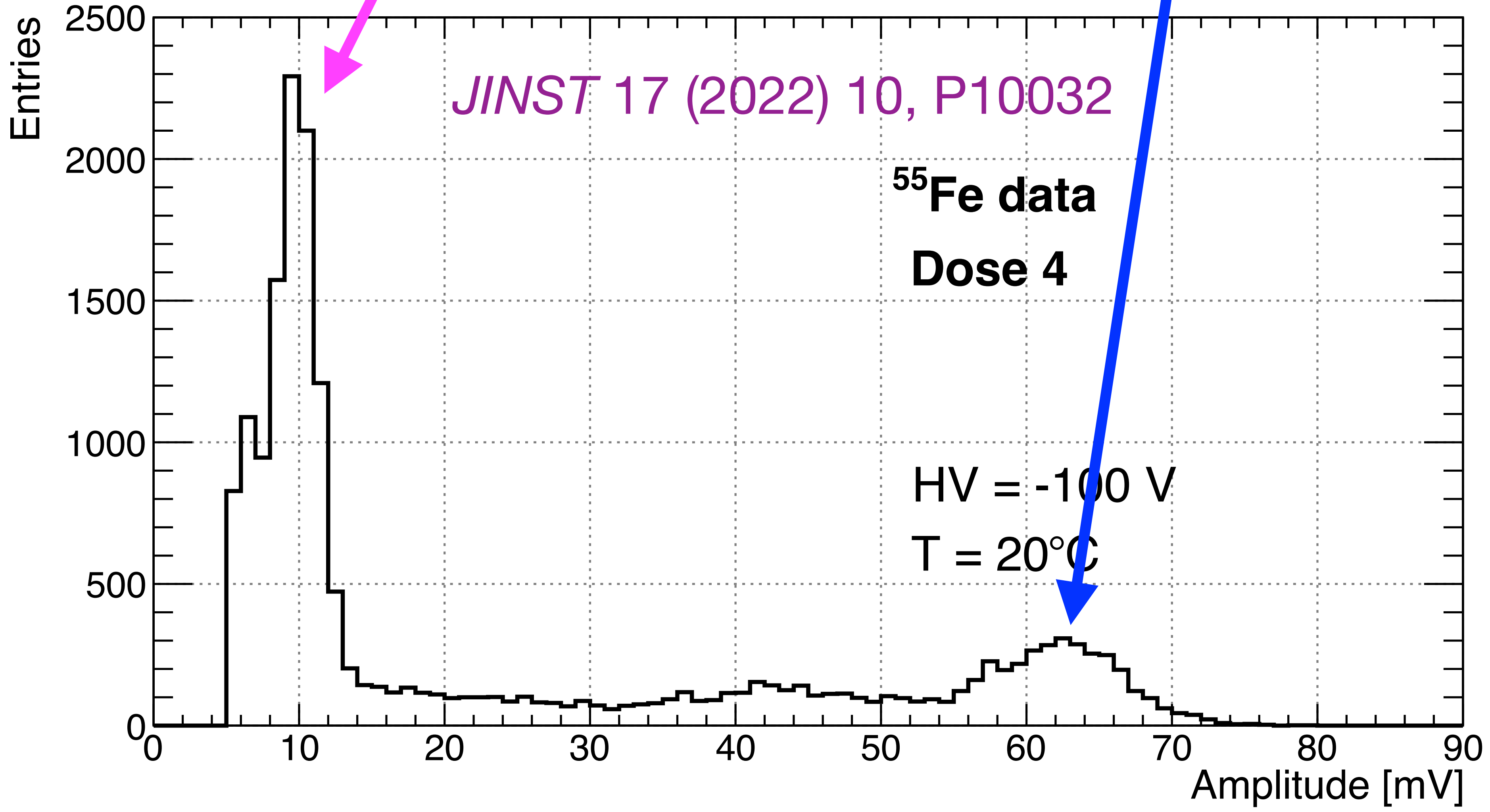
X-rays from ^{55}Fe radioactive source:

- mainly ~5.9 keV photons
- point-like charge deposition

Characteristic double-peak spectrum

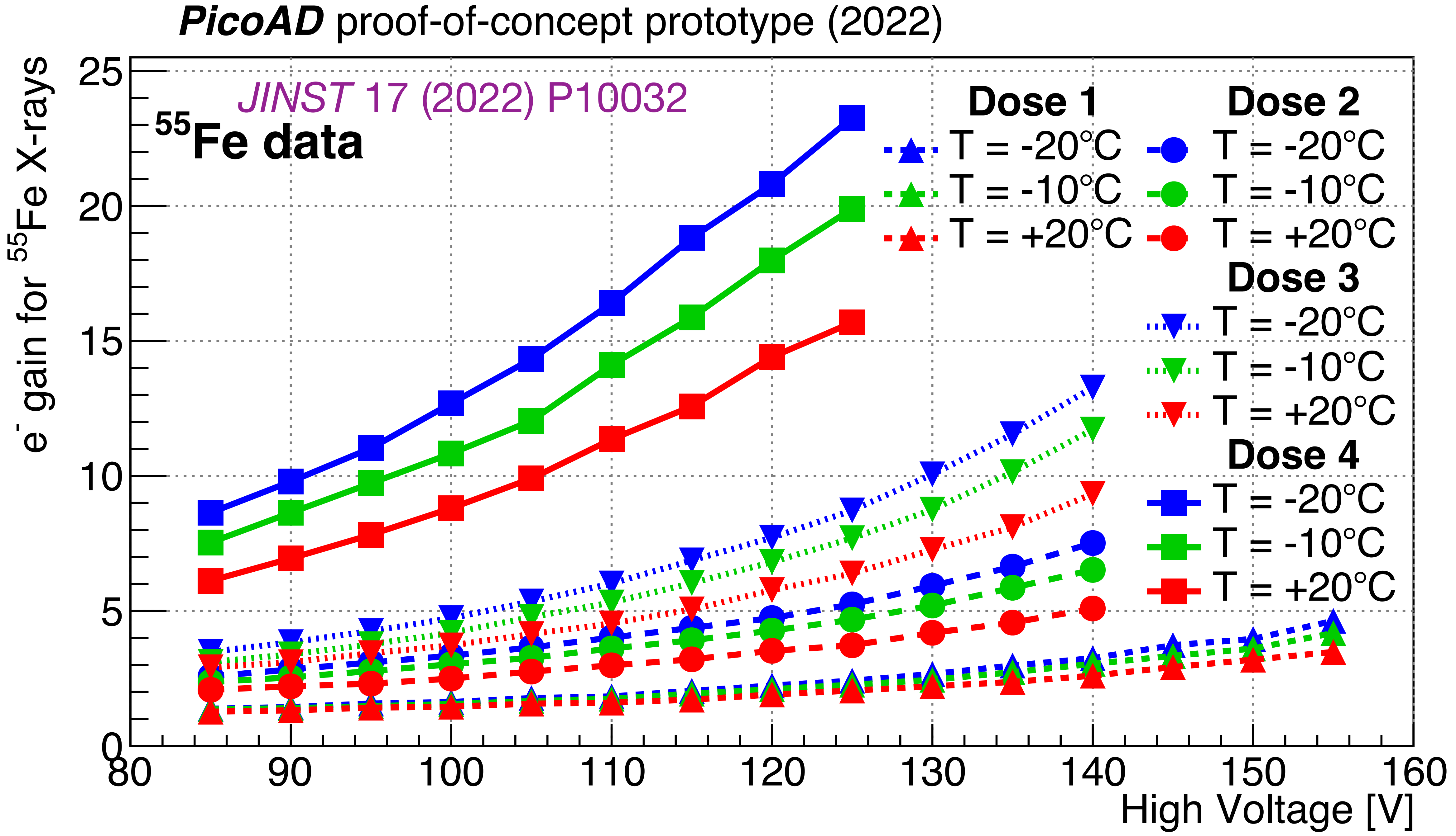
- photon absorbed in **drift region**
  - ➡ **holes** drift through gain layer & multiplied
  - ➡ **first peak** in the spectrum
- photon absorbed in **absorption region**
  - ➡ **electrons** through gain layer & multiplied
  - ➡ **second peak** in the spectrum

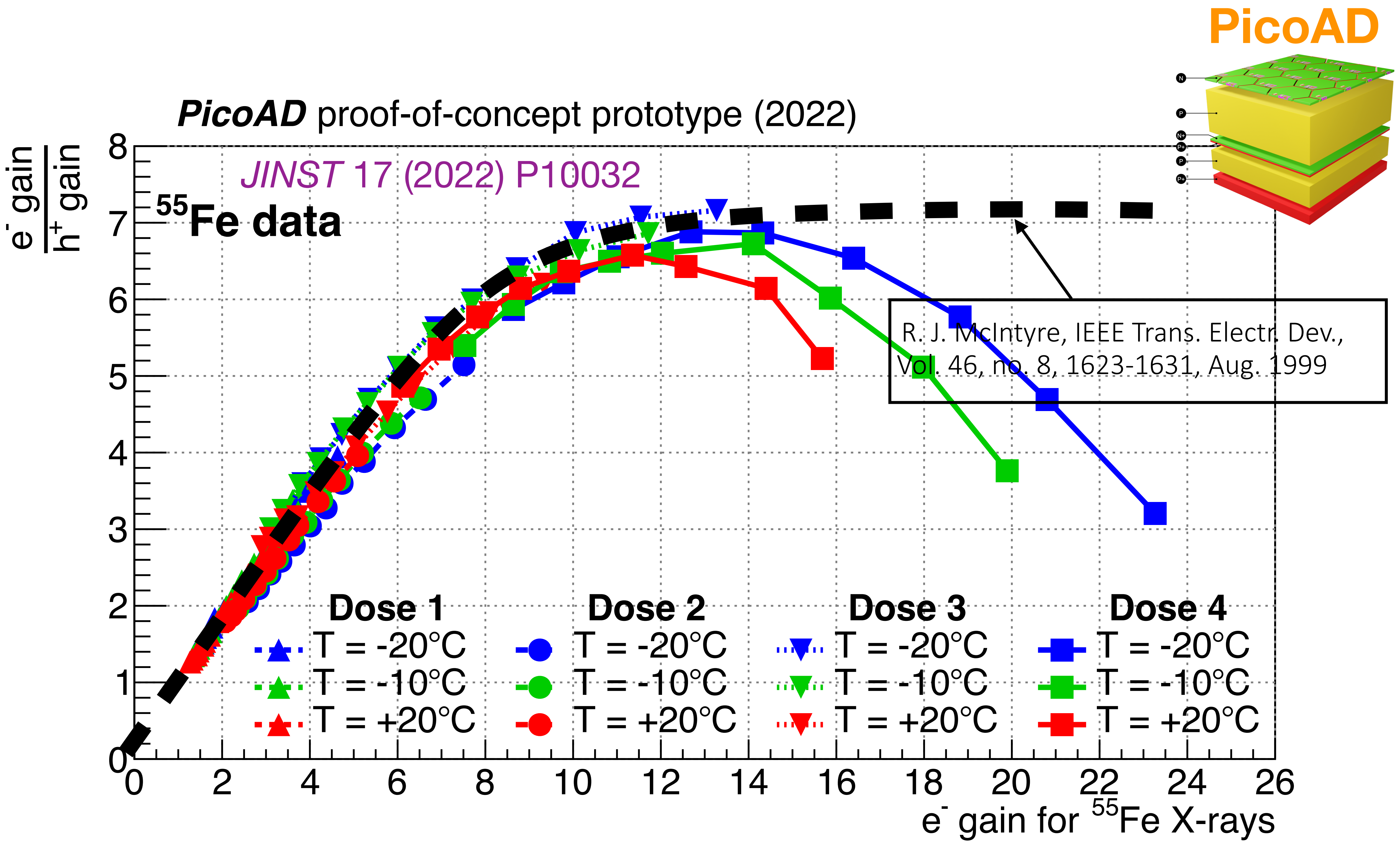




Gain Measurement with ^{55}Fe source

PicoAD





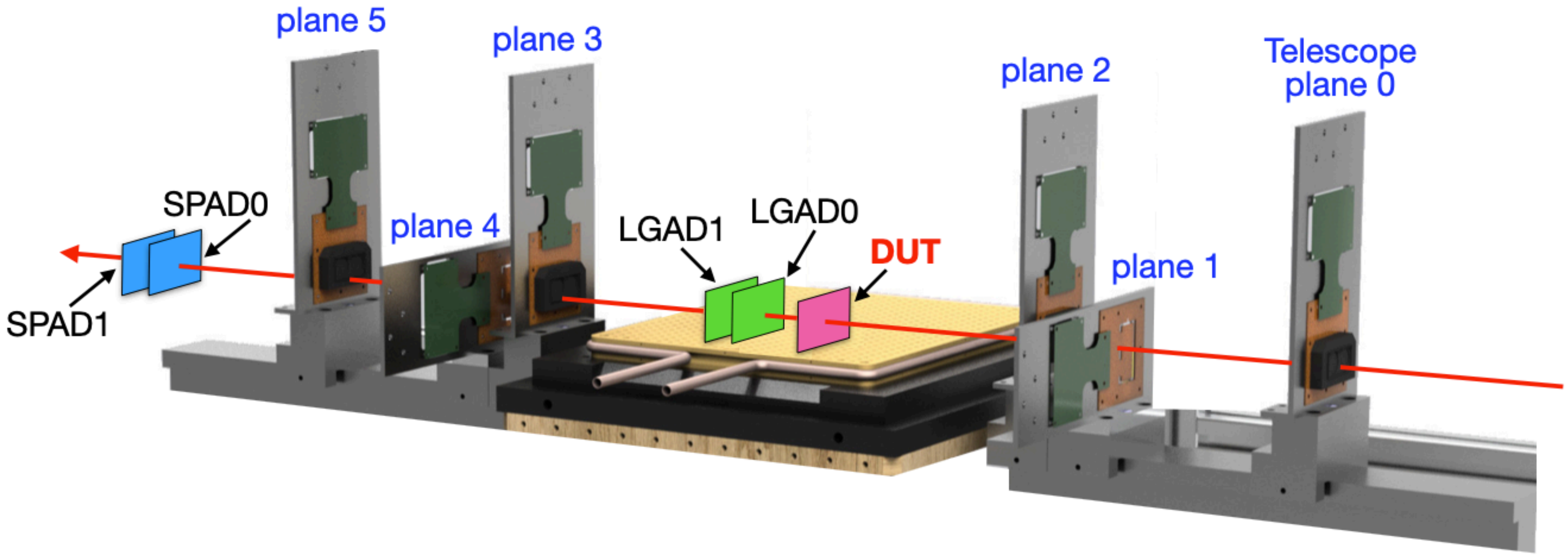
A **gain up to ≈ 20 for ^{55}Fe X-rays** obtained at HV = 120 V and T = -20 °C

Evidence for **gain suppression** due to space-charge effects **in the case of ^{55}Fe X-rays**

We estimated that ^{55}Fe gain of ≈23 corresponds to **gain 60–70 for a MIP**

Test Beam: Experimental Setup

CERN SPS Testbeam with 180 GeV/c pions to measure **efficiency** and **time resolution**

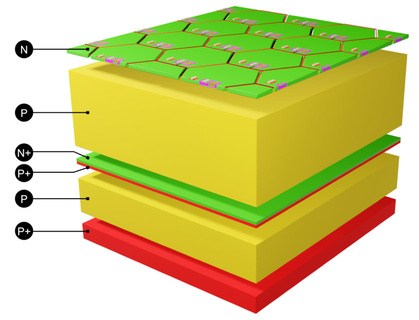


UNIGE FE-I4 telescope to provide spatial information ($\sigma_{x,y} \approx 10\ \mu m$)

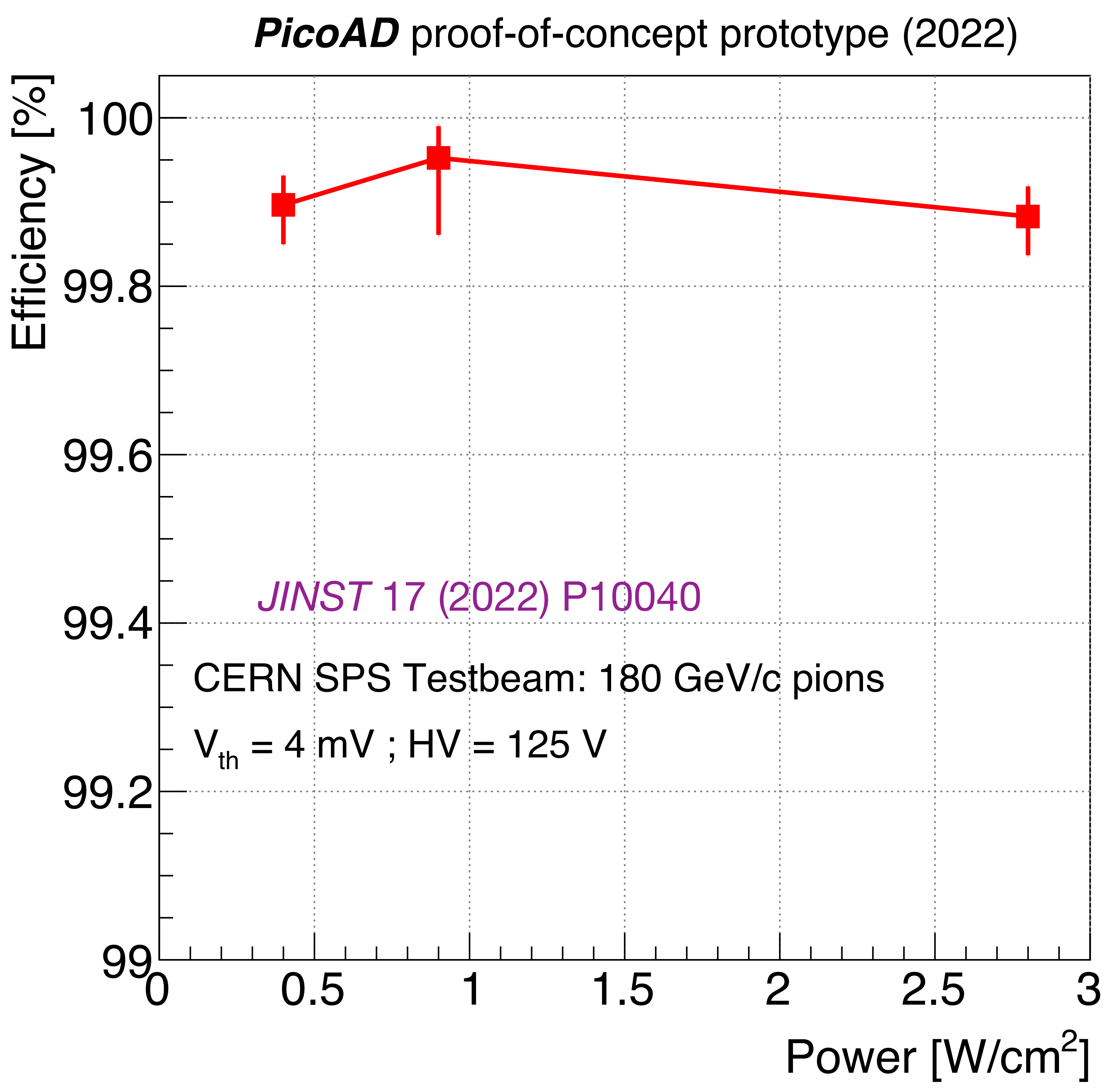
Two LGADs ($\sigma_t \approx 35$ ps) to provide the timing reference (and **two SPADs** with $\sigma_t \approx 20$ ps)

Testbeam results: Detection Efficiency

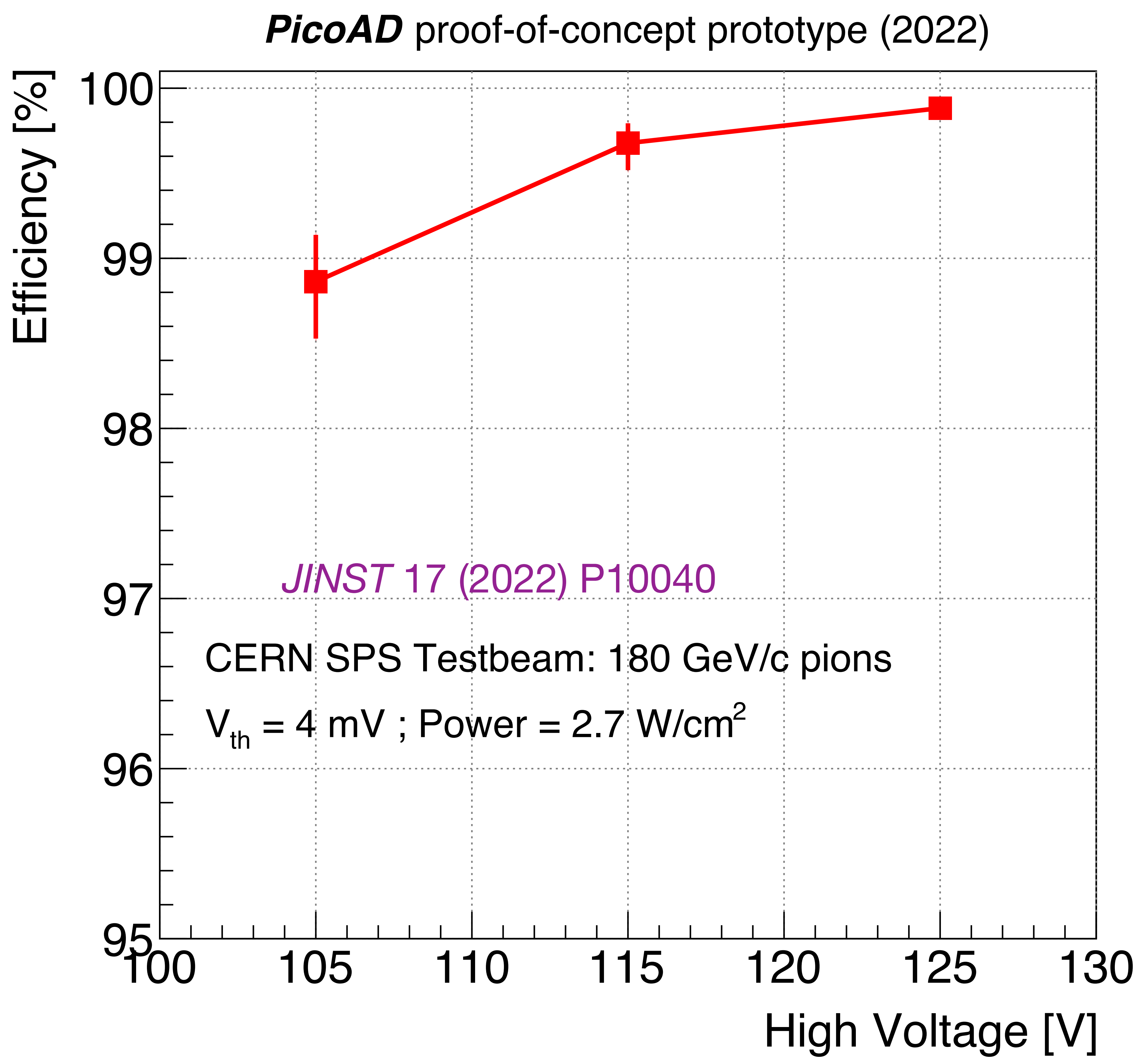
PicoAD



99.9% for all power consumptions

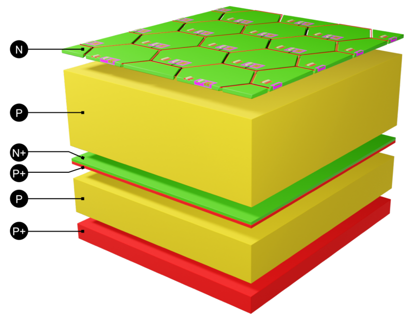


Drops to 99% for HV=105 V



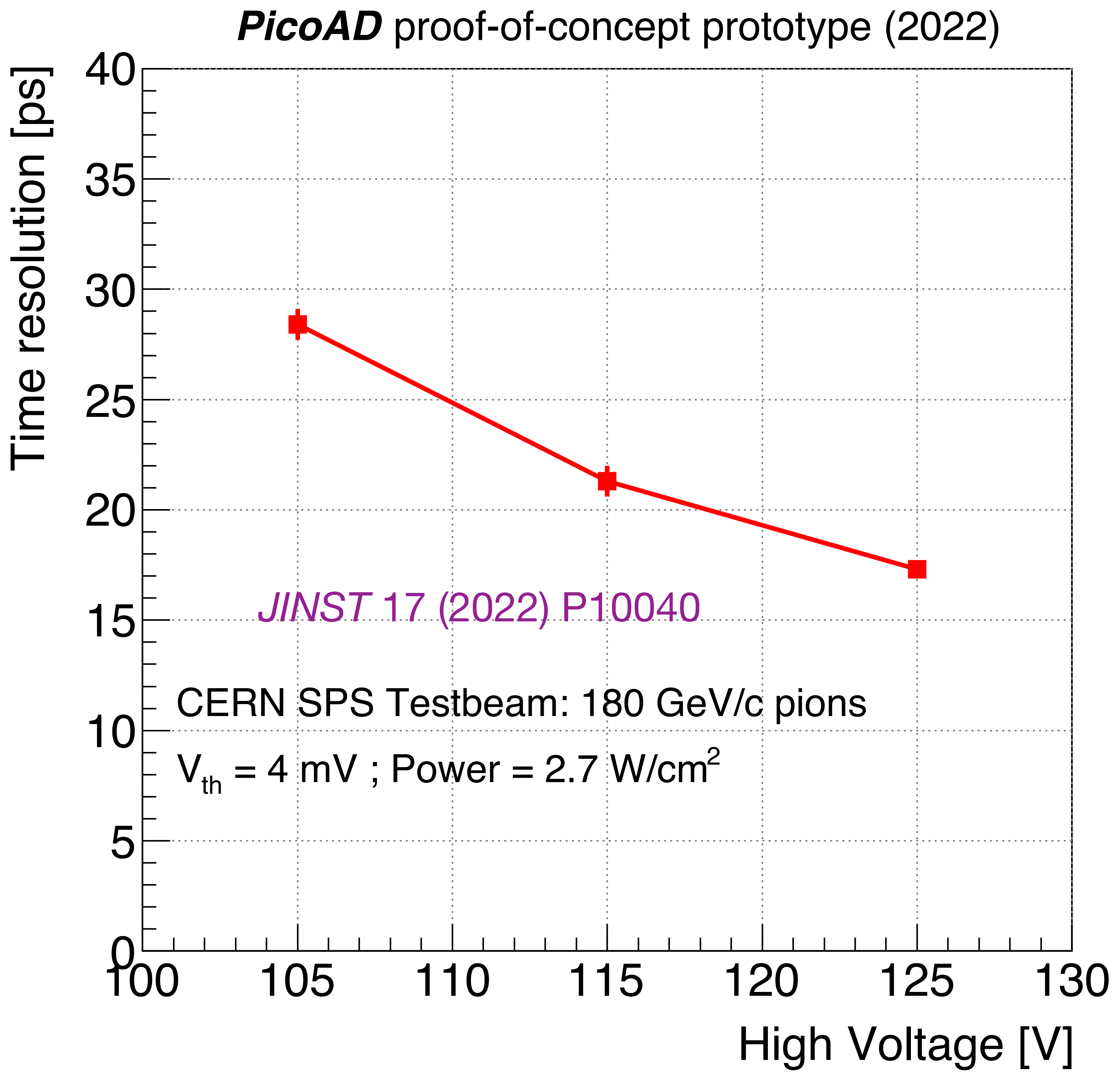
Testbeam results: Time Resolution

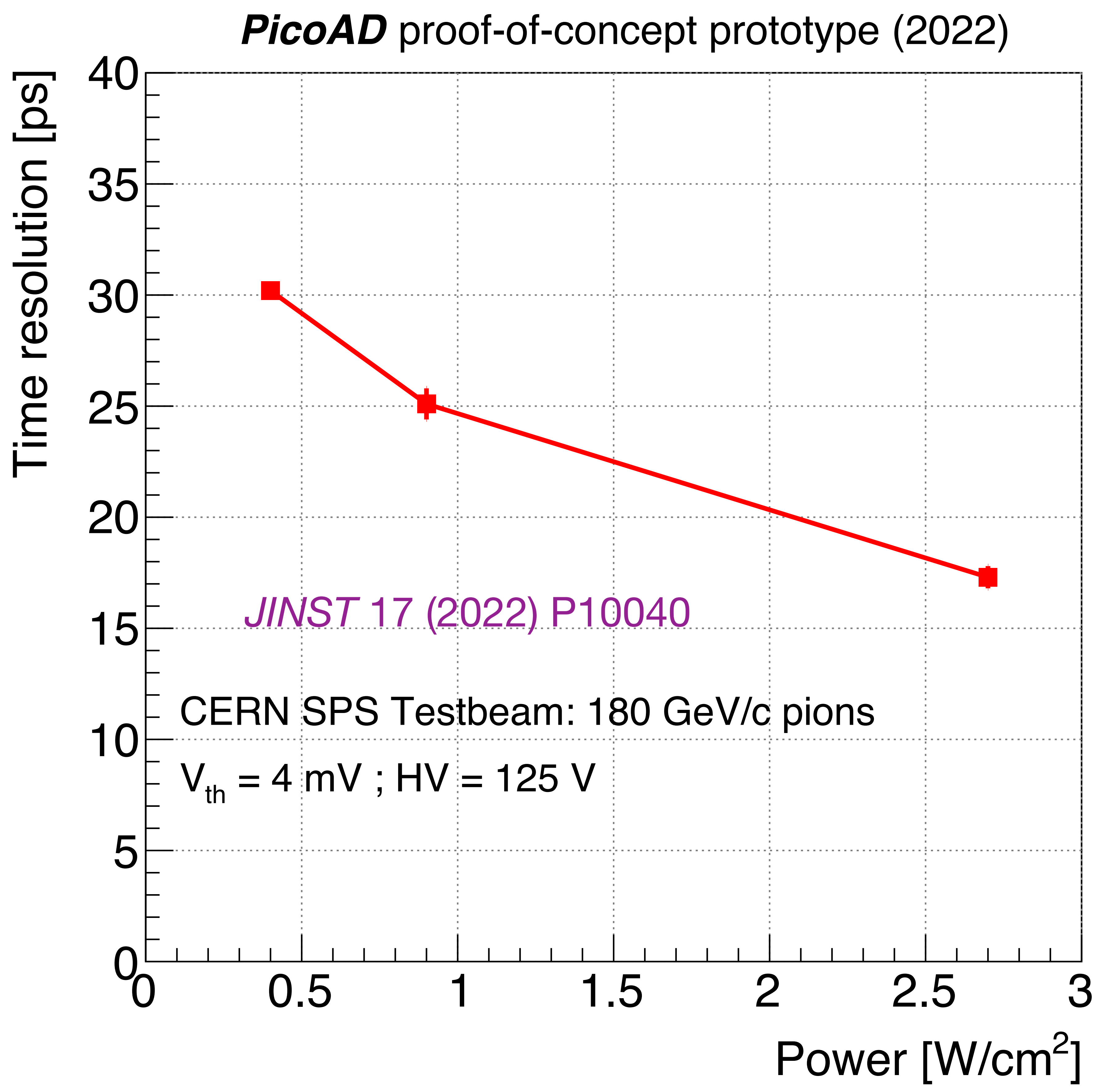
PicoAD



Best performance: (17.3±0.4) ps
for HV=125 V and Power = **2.7 W/cm²**

Timing resolution of **30 ps** even
at power consumption of **0.4 W/cm²**





Testbeam results: dependence on position

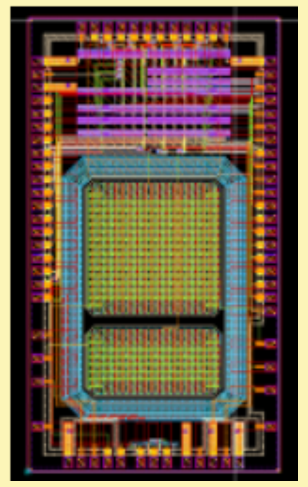
(13.2 ± 0.8) ps at the pixel center

PicoAD proof-of-concept: stronger dependence on hit position than for prototype 2

Monolithic SiGe BiCMOS for timing

Monolithic prototypes with SiGe BiCMOS (without internal gain layer)

2016



200ps

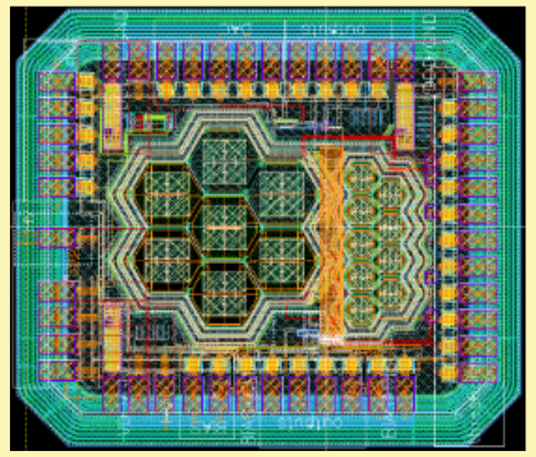
- 1 mm² pixel
- Discriminator

2017

110ps

- 30 pixels 500x500μm²
- 100ps TDC +I/O logic

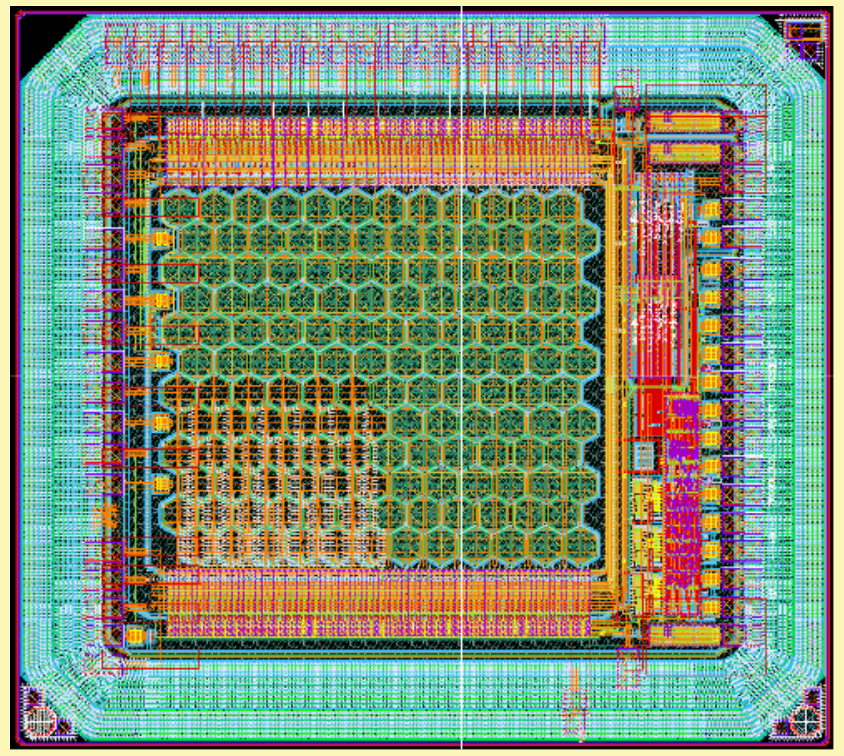
2018



50ps

- Hexagonal pixels 100μm and 200μm pitch
- Discriminator output

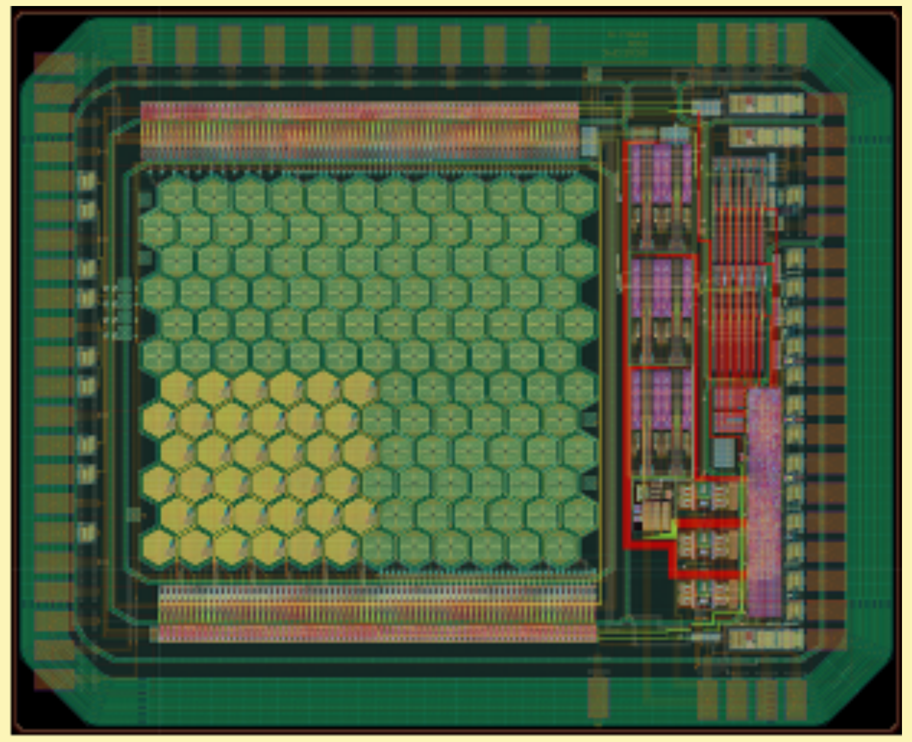
2020



36 ps

- Hexagonal s 100μm pitch
- 30ps TDC gic
- Analog cha

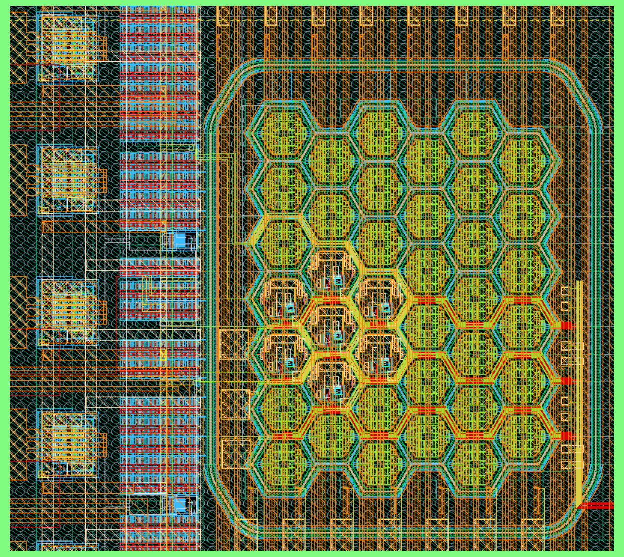
2022



20 ps

- Hexagonal s 100μm pitch
- improved e nics
- 50μm epita yer (350Ωcm)

March 2023



< 20 ps ?

- Hexagonal **32μm side**
- improved e nics

Monolithic prototypes **with internal gain layer:**

PicoAD version (proof-of-concept) **17 ps**

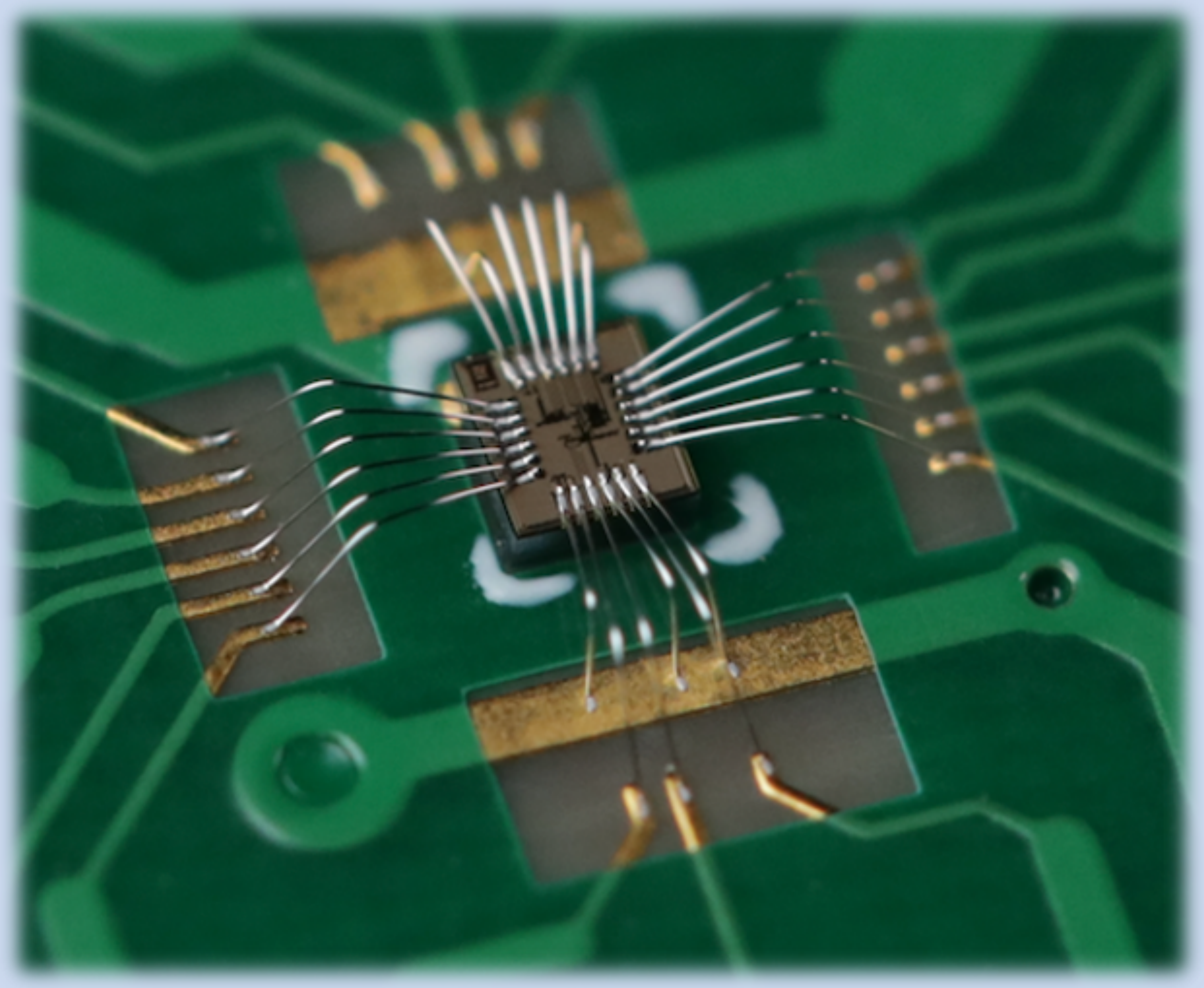
PicoAD version **in production** (back: **Sept. 2023**)

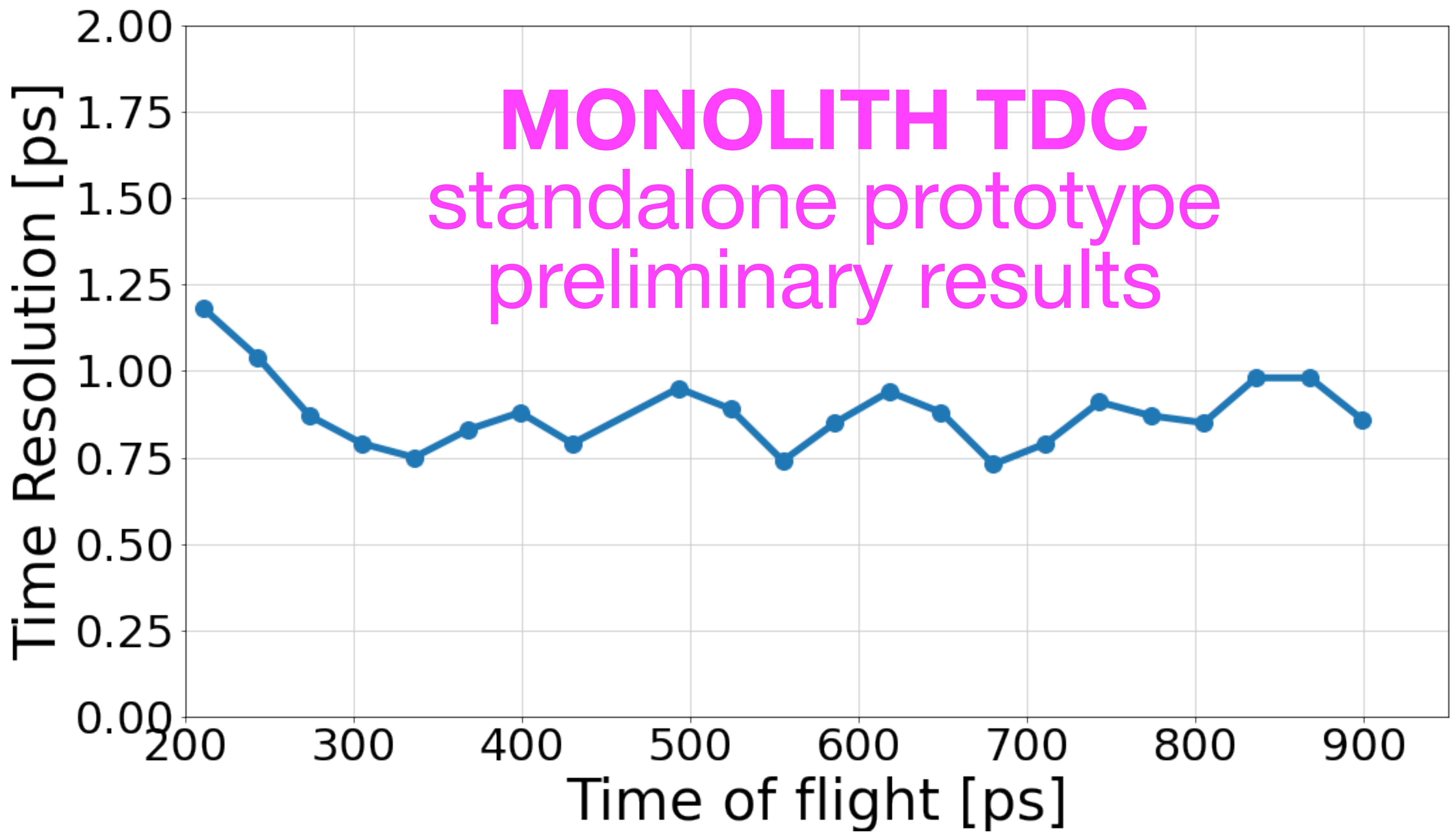
PicoAD version expected in **Early 2024**

MONOLITH sub-picosecond TDC

We are developing a sub-picosecond TDC based on a novel design (our patent© & more):

© R. Cardarelli, L. Paolozzi, P. Valerio and G. Iacobucci, European Patent Application / Filing - UGKP-P-001-EP, Europe Patent EP 18181123.3. 2 July 2018.





It was integrated in MONOLITH 2022 prototype2 ASIC

Summary & Outlook

The PicoAD© sensor works. Testbeam of the monolithic proof-of-concept ASIC provided:

- **Efficiency = 99.9 %** including inter-pixel regions
- **Time resolution σ_t = (17.3 ± 0.4) ps : 13 ps** at center and **25 ps** at pixel edge (although sensor not yet optimized for timing)

Testbeam of second prototype ASIC, without gain layer, provided:

- **Efficiency = 99.8%** and **σ_t = (20.7 ± 0.3) ps**
- Laser measurement: down to 2.5 ps. Contributions from Landau noise studied
- Irradiation with protons (together with KEK) shows **radiation tolerance up to 10^{16} n_{eq}/cm^2**
- PicoAD sensor based on this prototype to be delivered in **September 2023**, optimised for timing with TCAD to achieve ≈10 ps (thicker drift layer; improved inter-pixel region)
- **Low power picosecond TDC** development for fully monolithic chip ongoing

Deliverable of MONOLITH ERC project:

- Full-reticle monolithic ASIC in **Summer 2025** with 50μm pitch and sub-10ps timing