Timing studies of 65 nm CMOS monolithic silicon pixel structure for the ALICE tracker upgrade

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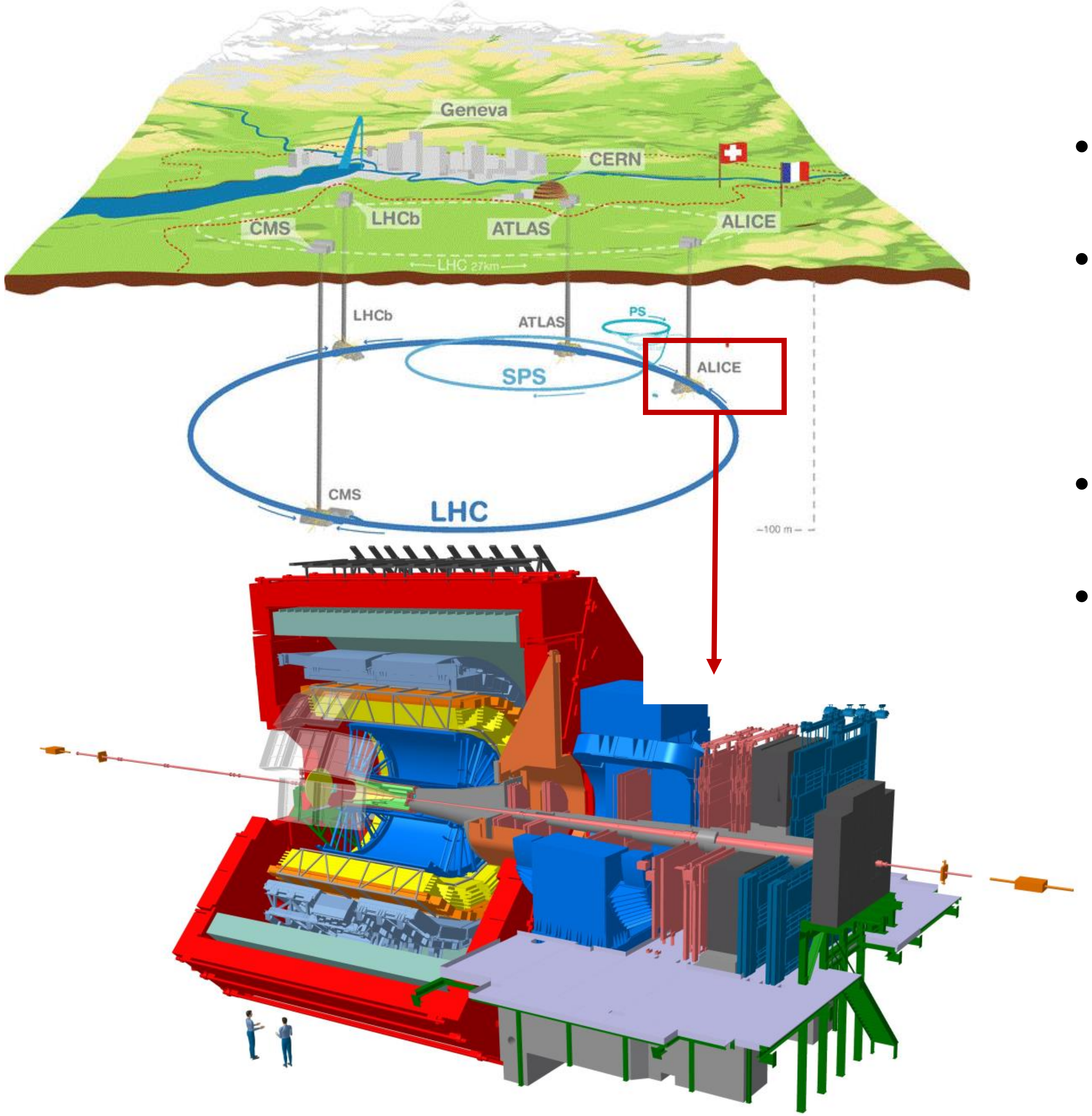
On behalf of the ALICE collaboration

FAST 2023
May 31st 2023

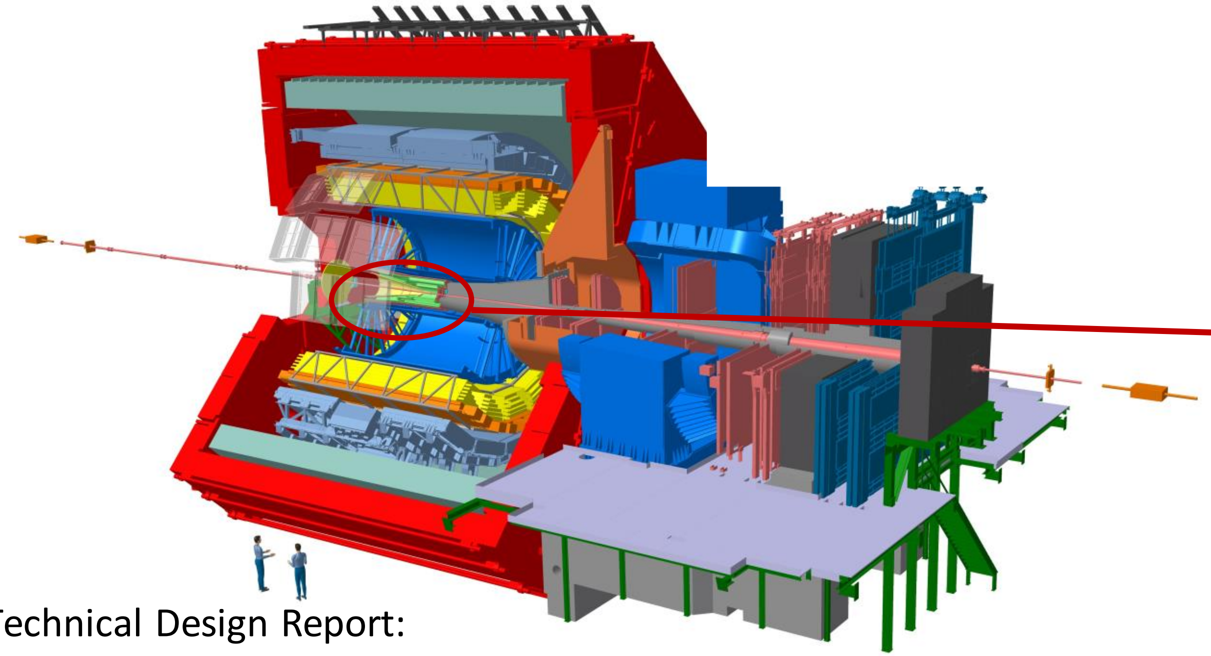
The ALICE experiment

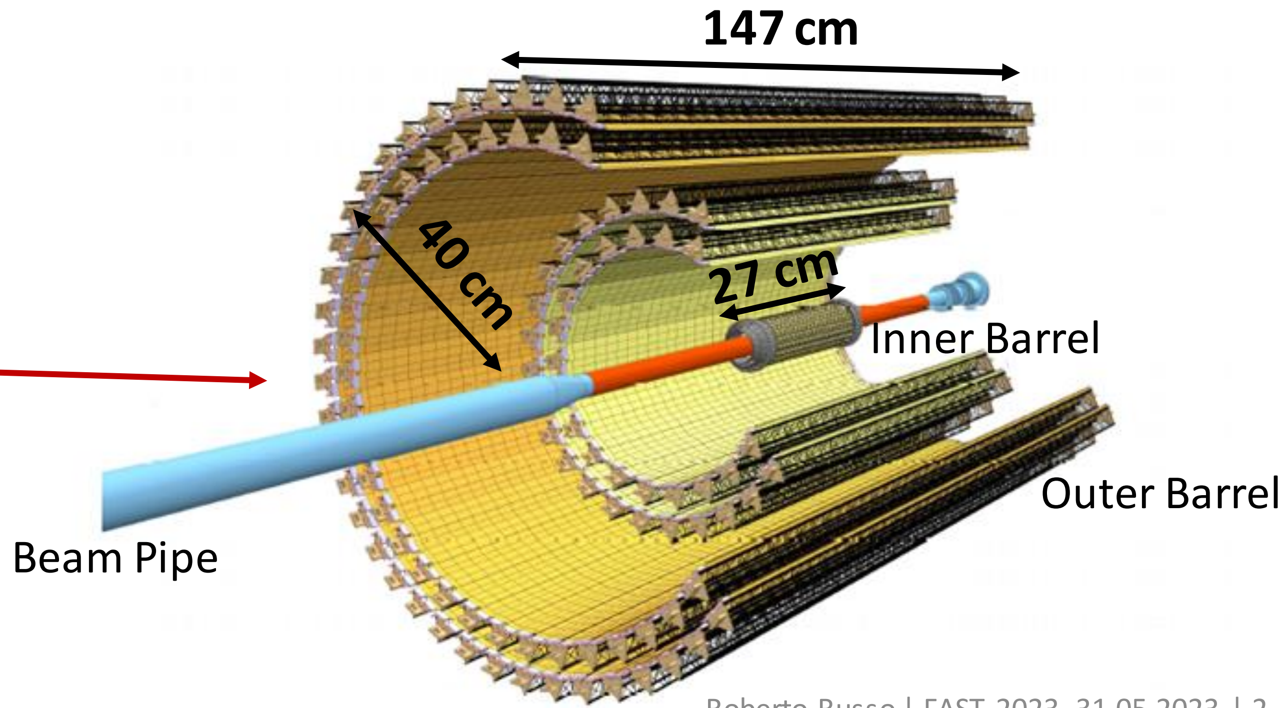


- ALICE (A Large Ion Collider Experiment) is a detector at the Larger Hadron Collider (LHC), CERN
- Study of quark-gluon plasma (QGP) in heavy-ion collisions
  - ➢ Up to O(10k) particles to be tracked in a single bunch crossing
- Reconstruction of charm and beauty hadrons
  - ➢ Precise vertexing and tracking capabilities needed
- Interest in low momentum ($\lesssim 1$ GeV/c) particle reconstruction
  - ➢ Low material budget required

The current ALICE Inner Tracking System

- ALICE Inner Tracking System 2 (**ITS2**)
  - Installed during LHC Long Shutdown 2, replacing previous ITS
  - Taking data since September 2021
  - Fully based on Monolithic Active Pixel Sensors (MAPS),~10 m^2 of silicon,~24k chips
- Inner Barrel
  - 3 layers, placed at ~22-42 mm from the interaction point, 0.35% X_0 per layer
- Outer Barrel
  - 4 layers, placed at ~194-395 mm from the interaction point, 1.1% X_0 per layer

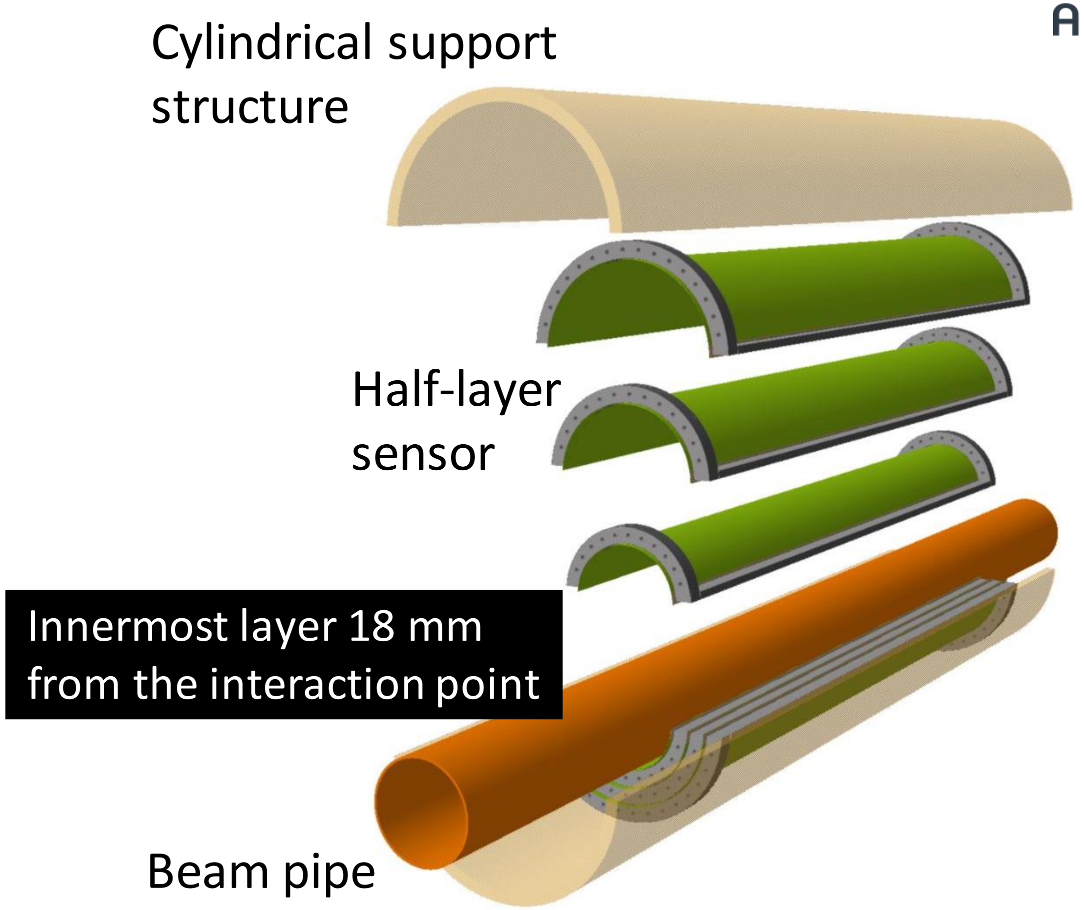




Technical Design Report:
doi:10.1088/0954-3899/41/8/087002

The ALICE Inner Tracking System 3

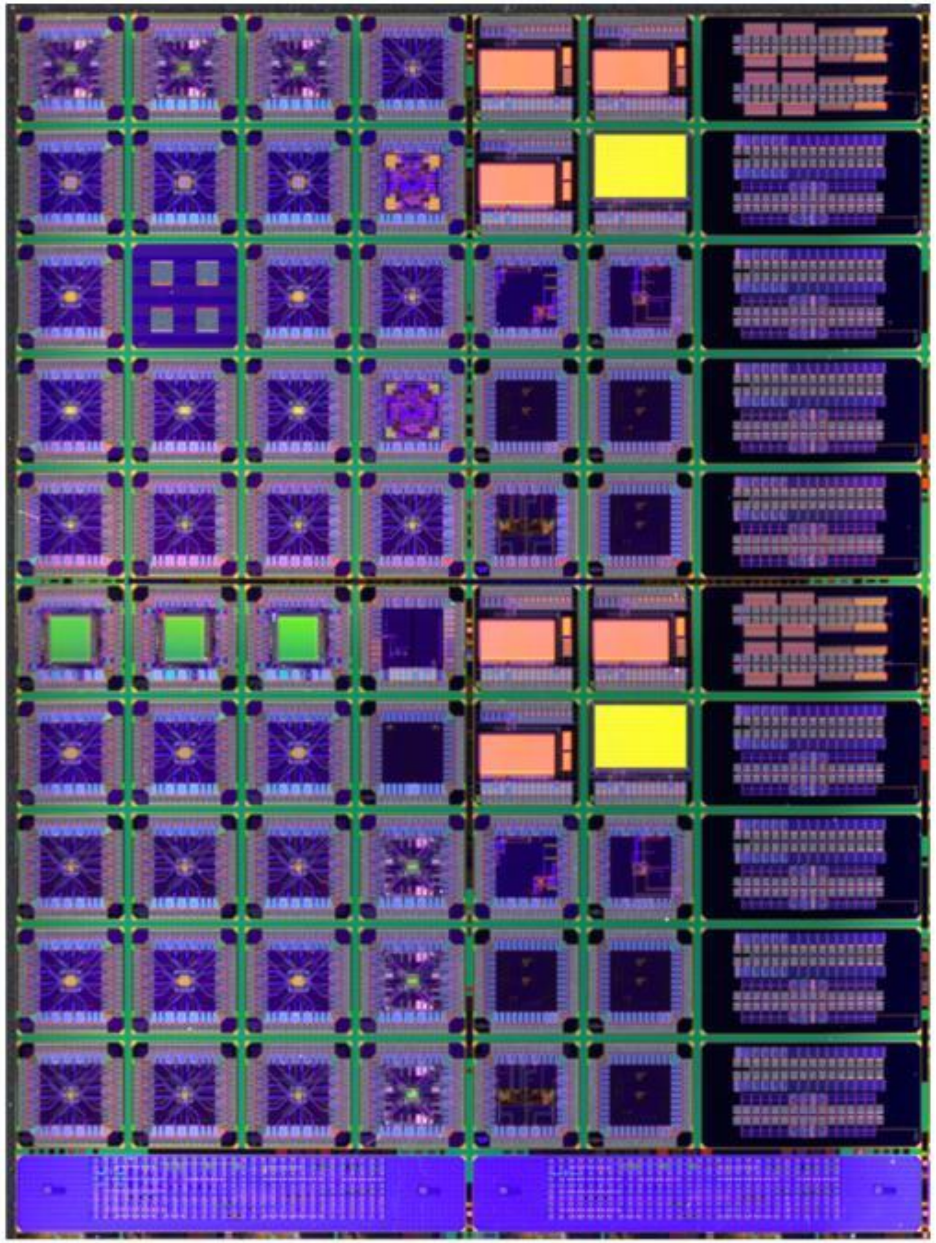
- Inner Tracking System 3 (**ITS3**): replacement of the innermost 3 layers of the tracker
- Planned to be installed during LHC Long Shutdown 3 (2026-2028)
  - ➢ **300 mm wafer-scale MAPS** sensors produced with the stitching technique
  - ➢ Thinned down to **50 μm or below**
  - ➢ Bent in a **truly cylindrical** shape
    - ▪ First layer moved **closer** to the interaction point (23 mm → 18 mm)
  - ➢ Material budget: 0.05% X_0 per layer (0.35% X_0 for ITS2)
  - ➢ Sensors implemented in Tower Partners Semiconductor Co (TPSCo) **65 nm CMOS** process



ALICE ITS3 Letter of Intent

65 nm CMOS imaging process

- Combined effort of CERN EP R&D and ALICE ITS3
- First exploratory chip submission MLR1 in the **Tower Partners Semiconductor Co (TPSCo) 65 nm CMOS process**
- 55 different test structures
- Added value of 65 nm process:
  - ➢ Increase in-pixel circuitry density
  - ➢ Decrease pixel size
  - ➢ Lower power consumption
  - ➢ Potentially better radiation hardness
  - ➢ Larger wafers of 300 mm (instead of 200 mm) available

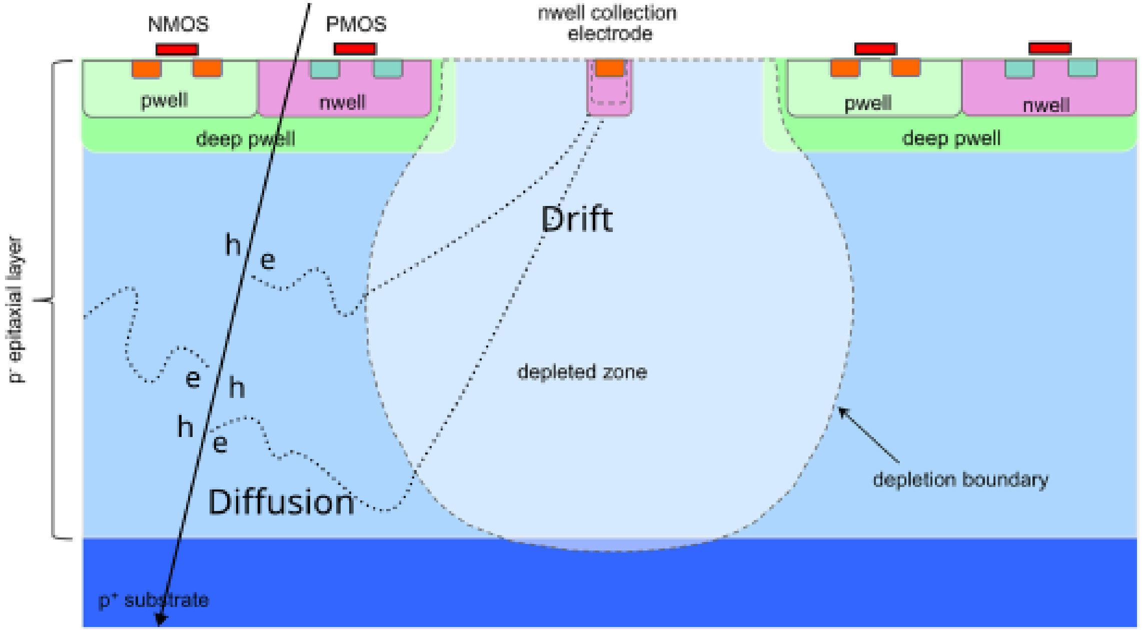


MLR1 reticle

65 nm CMOS imaging process: sensor design and optimization

- Sensor design optimization started as ALICE “offspring” development with TowerJazz 180 nm CMOS technology
- Development further taken on by other groups outside ALICE
- Same principles now applied to 65 nm CMOS technology

- **Standard process**
  - Small n-well collection electrode on high-resistivity p-type epitaxial layer
  - Reverse substrate bias applied to increase depleted zone
  - Sensitive epitaxial layer partially depleted
  - Part of signal charge collected from the non-depleted layer via diffusion
  - Operational up to 500 krad TID and 1.7×10^{13} 1 MeV n_{eq} cm^{-2} NIEL doses



Optimization of 65 nm CMOS process:
doi:10.22323/1.420.0083

65 nm CMOS imaging process: sensor design and optimization

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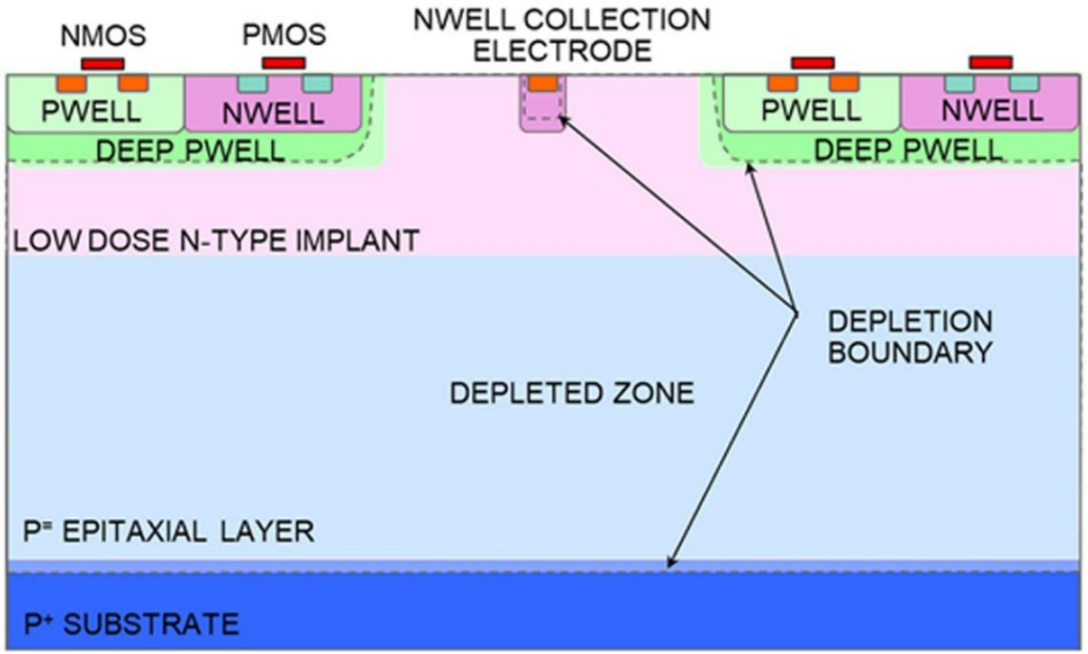
- **Modified process**
  - Addition of a low-dose n-implant below the electrode
  - Extends the junction to fully deplete the epitaxial layer
  - Weak lateral electric field at pixel edges and corners



More details in doi:10.1016/j.nima.2017.07.046

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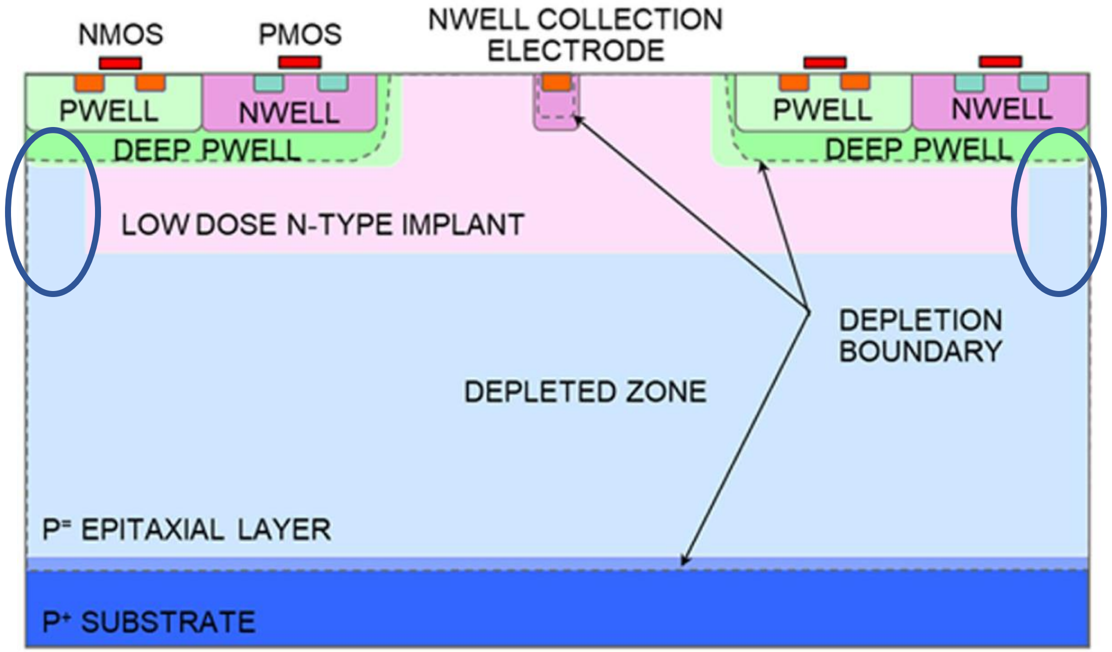
- **Modified with gap process**
  - Gap in the n-implant at the pixel borders
  - Improves lateral field near the pixel boundary
  - Accelerates the charge collection to the electrode and improves the radiation hardness



More details in doi:10.1088/1748-0221/14/05/C05013

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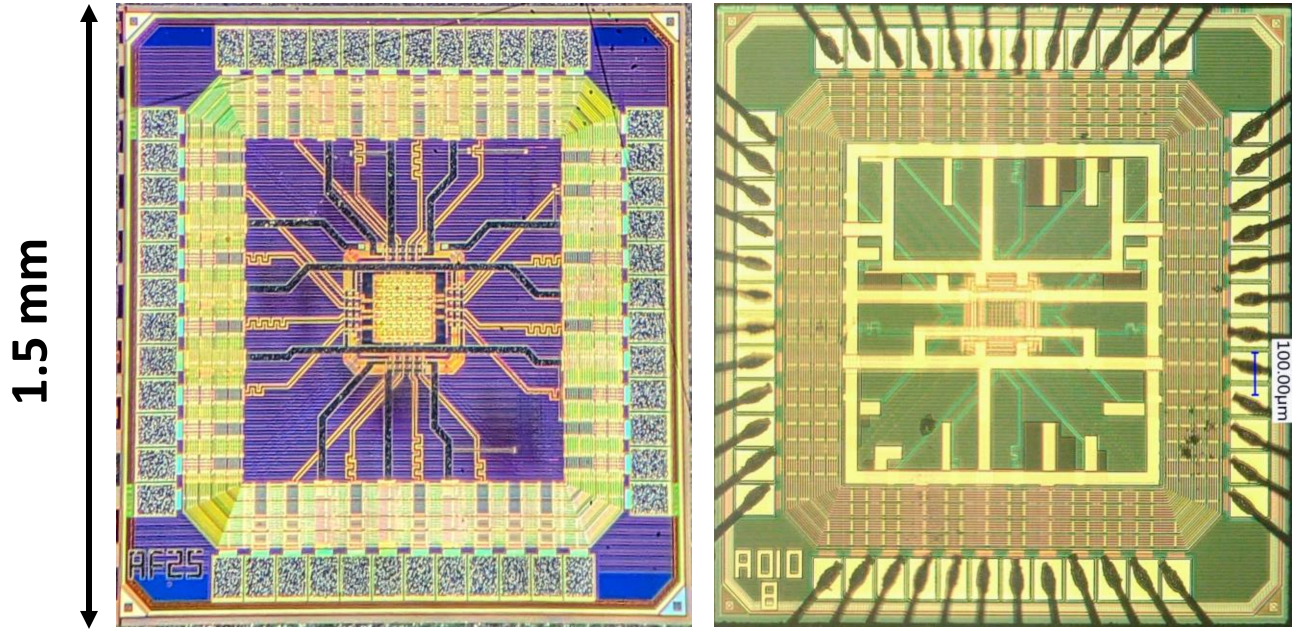
Analog Pixel Test Structure (APTS)

Pixel matrix and output buffer

- 6 × 6 pixel matrix
- Central 4 × 4 pixels directly read with analogue readout
- Pixel pitch: **10**, 15, 20, 25 µm
- Pixel output buffer variants:
  - ➢ Source follower (SF)
  - ➢ **Operational amplifier (OPAMP)**

APTS SF **APTS OPAMP**



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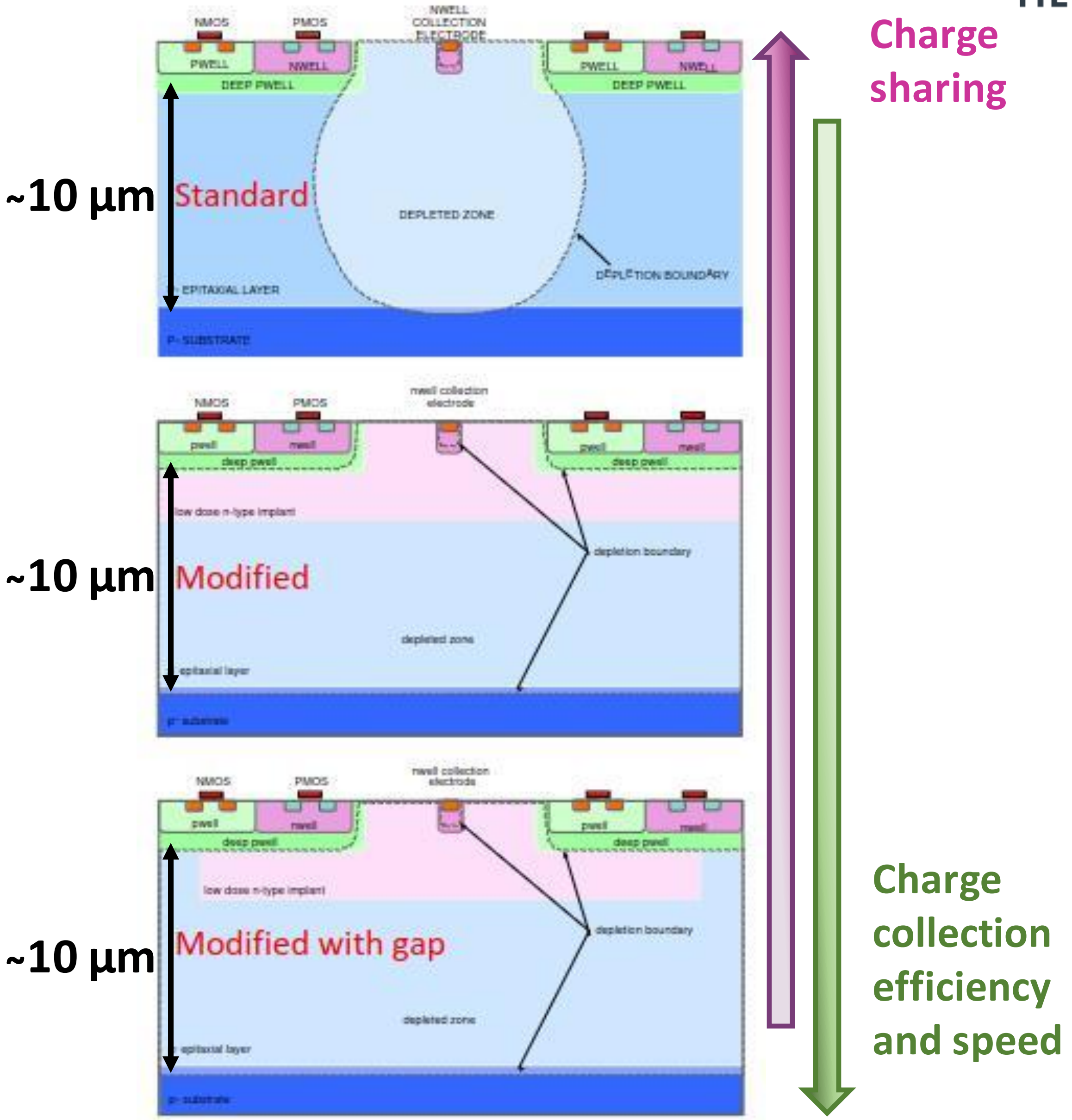
Sensor features

- Implemented in all three TPSCo 65 nm CMOS process variants
- ~ 10 µm high-resistivity p-type epitaxial layer
- R&D chip of general interest, for **applications** even **beyond ITS3**
- Aim: **qualification of the charge collection and timing properties of the new technology**

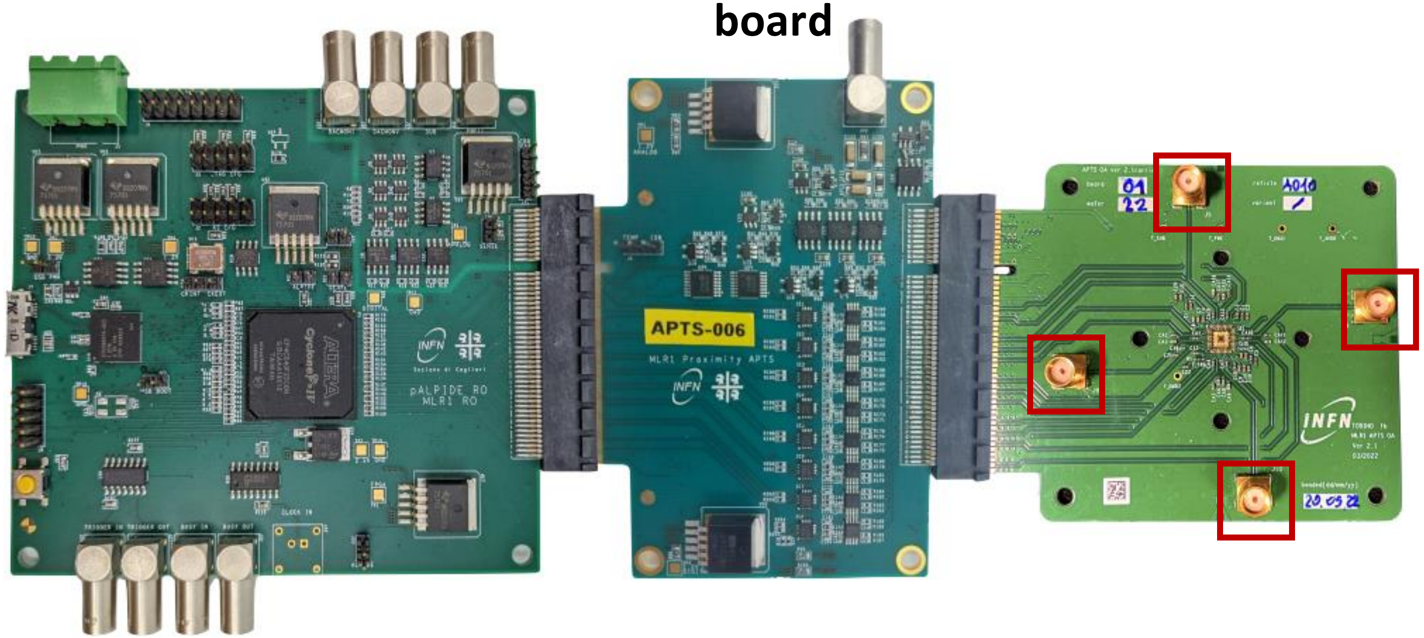


Readout system

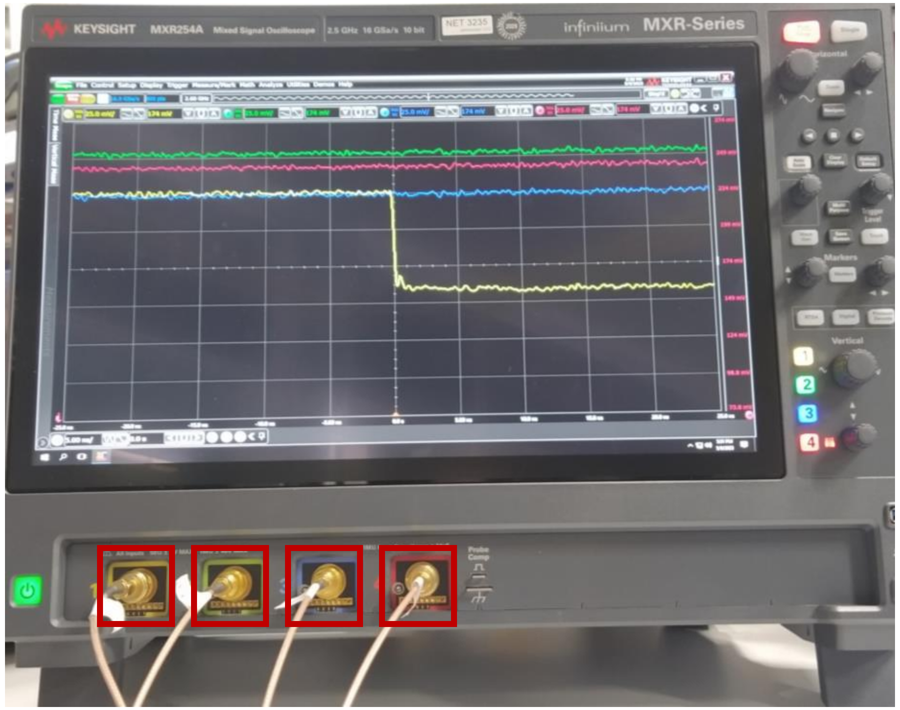
DAQ board

Proximity board

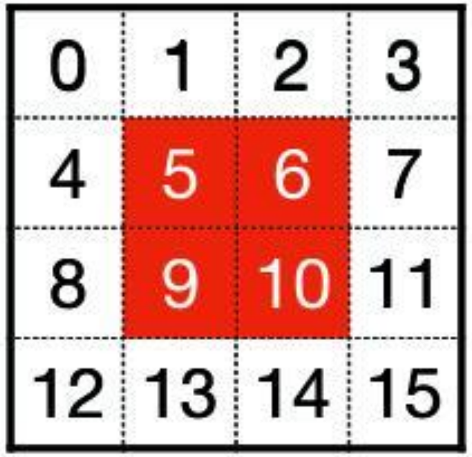
Chip board



Keysight Infiniium MXR404A
4 GHz – 4 × 16 GSa/s



- DAQ board
  - Single board to operate all the test structures
- Proximity board
  - Specific to the chip to be operated
  - DACs and ADCs
- Chip board
  - Provides 4 direct analog SMA outputs to the central pixels of the matrix
  - Other 12 pixels are readout via ADCs – 4 MSa/s sampling frequency



4 × 4 pixel matrix

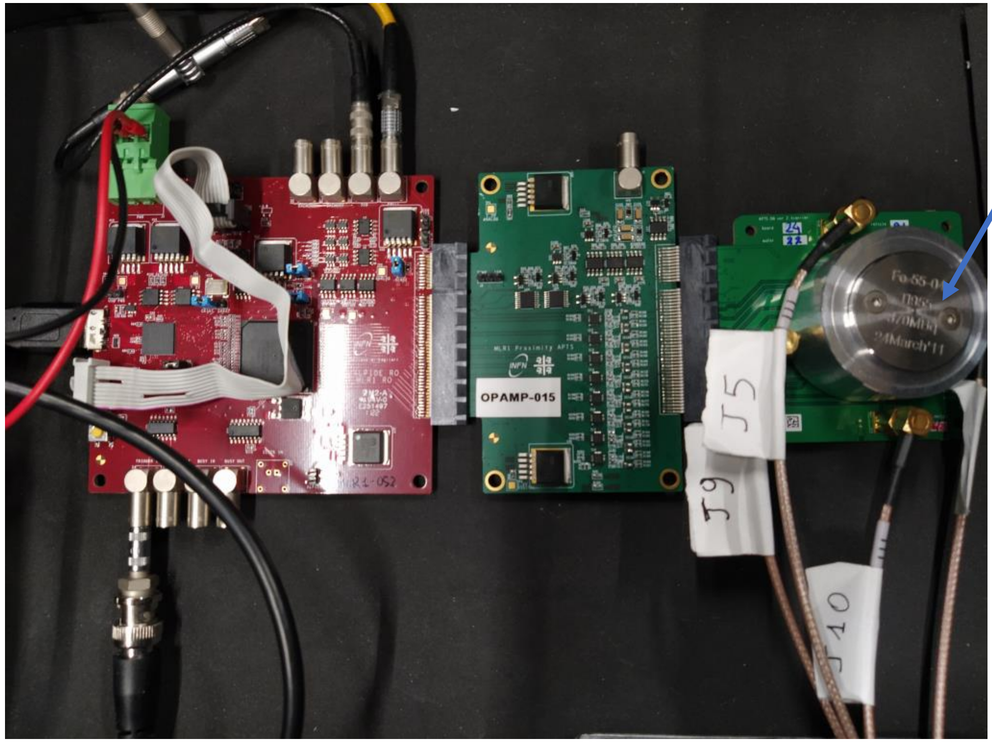
Characterisation measurements

Laboratory:

- Tuning operation parameters
- Test pulses and noise measurements
- Measurements with ^{55}Fe radioactive source:
  - **Signal calibration**
  - **Charge collection efficiency**

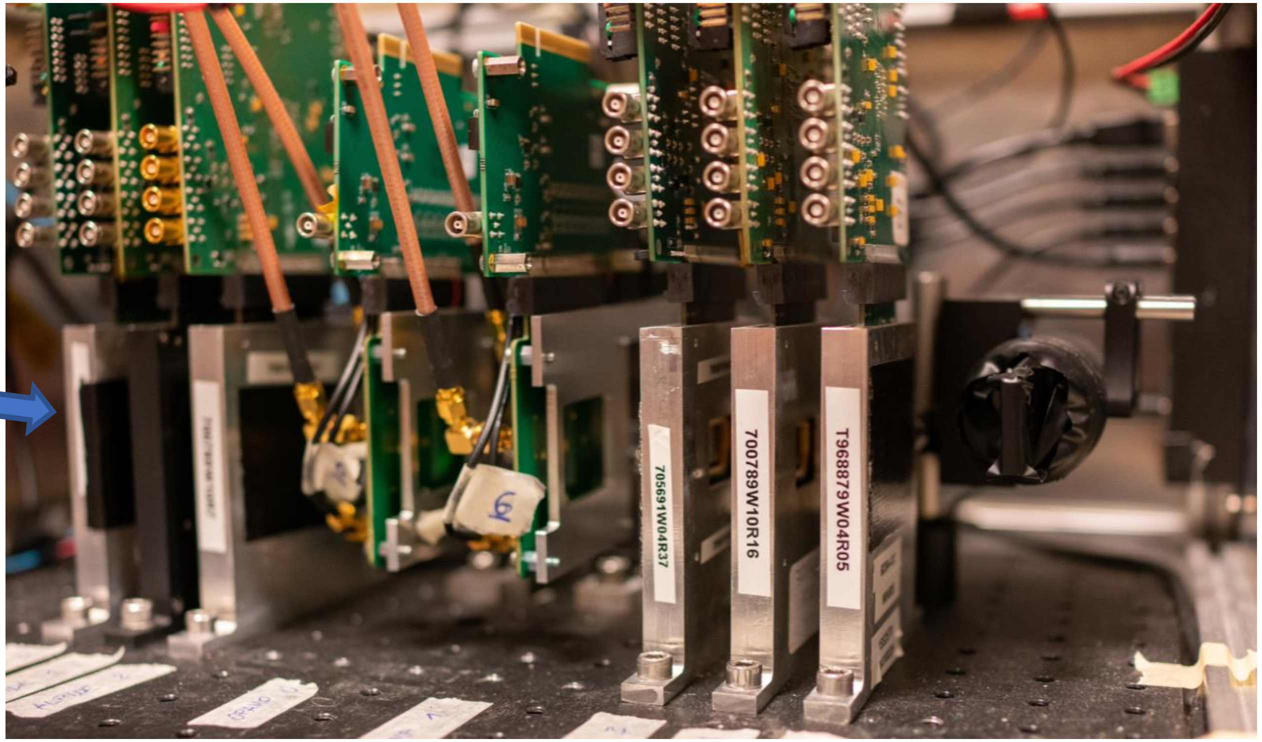
Beam test facilities:

- Sensor performance evaluated with MIPs (e^-, π)
- Tracks reconstructed with beam telescope
- Tracks associated with DUT clusters
  - Signal, SNR, detection efficiency
  - Spatial and **timing** resolution



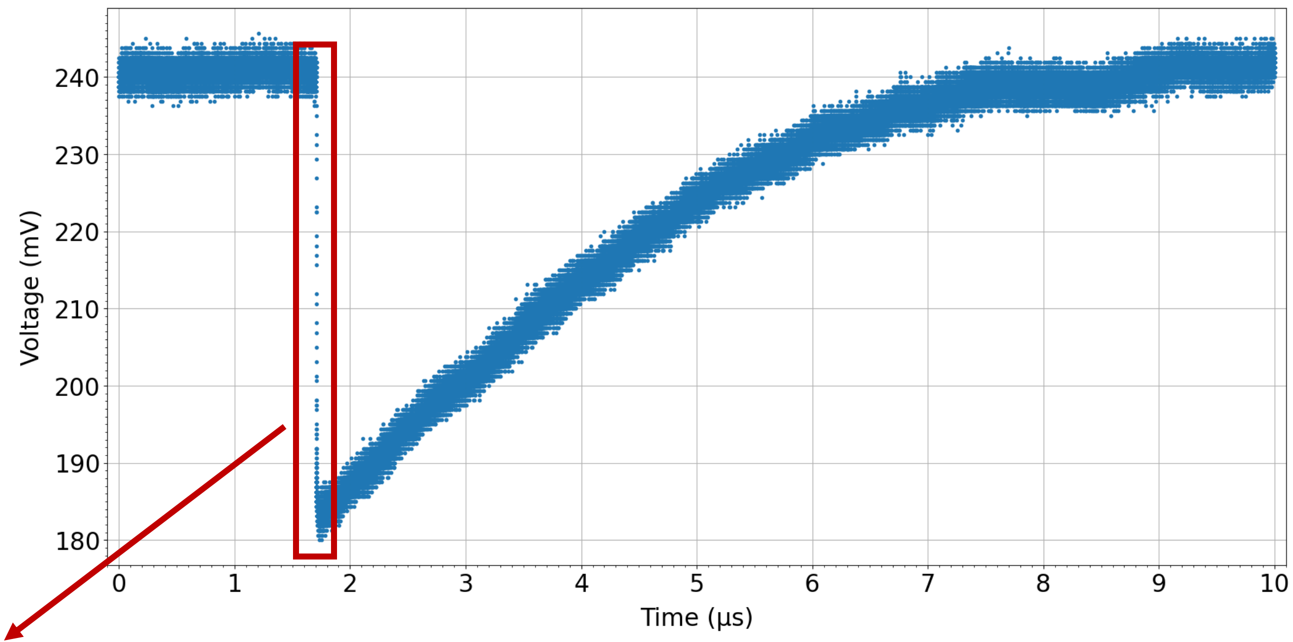
^{55}**Fe source**

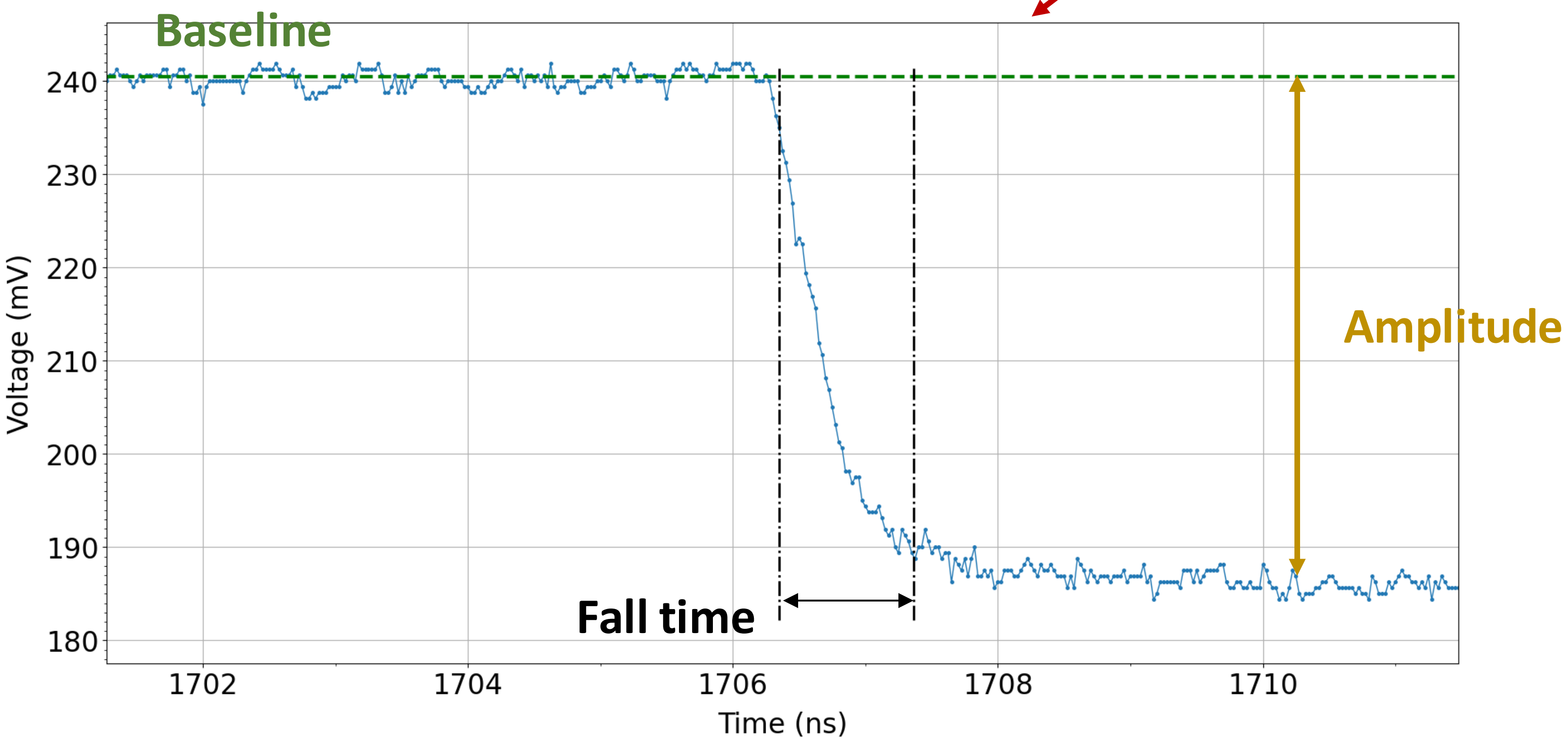
Beam



Waveform anatomy

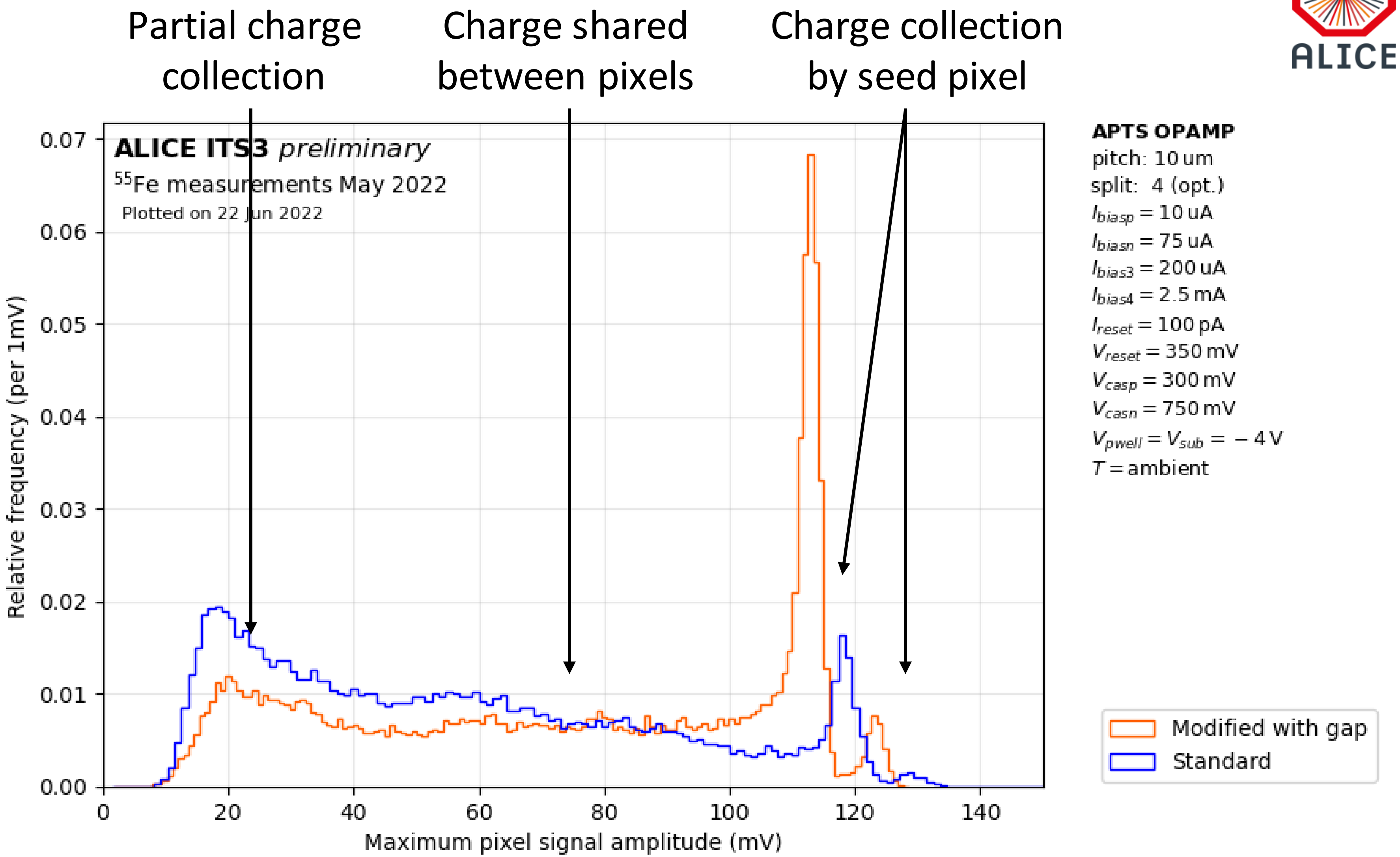
- **Baseline**: pixel reference voltage level
- **Amplitude**: difference between baseline and minimum signal voltage level
- **Fall time**: Time difference between 10% and 90% of signal amplitude





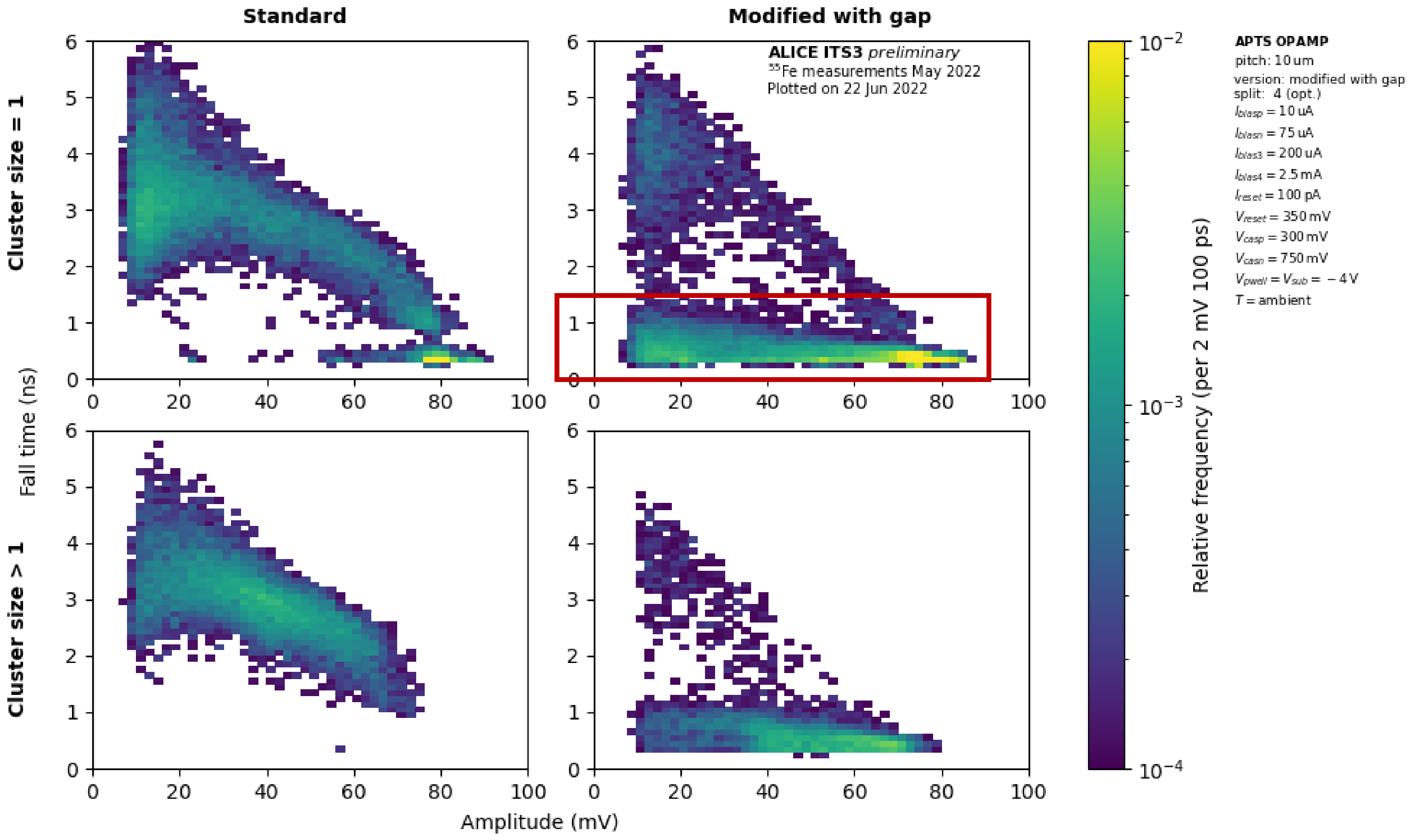
^{55}Fe measurement

- Standard process
  - Larger absolute signal
- Modified with gap process
  - Less charge sharing
  - Higher probability of single pixel cluster
- Sensor signal calibration based on Mn-K_α (1640 e^-) and Mn-K_β (1800 e^-) peaks



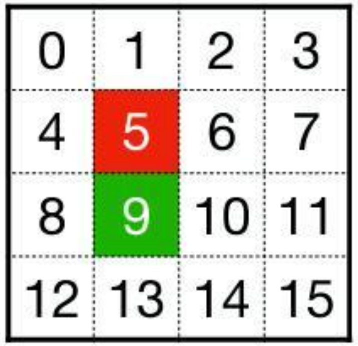
^{55}Fe measurement

- Clusters of various sizes show distinct time and charge distributions
- Modified with gap variant shows more events with high signal amplitude and low fall time
  - ➢ Suppression of charge sharing among neighbor pixels
  - ➢ Faster charge collection

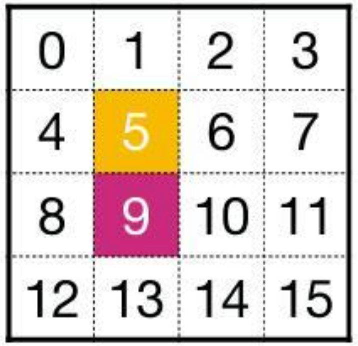


Beam test setup

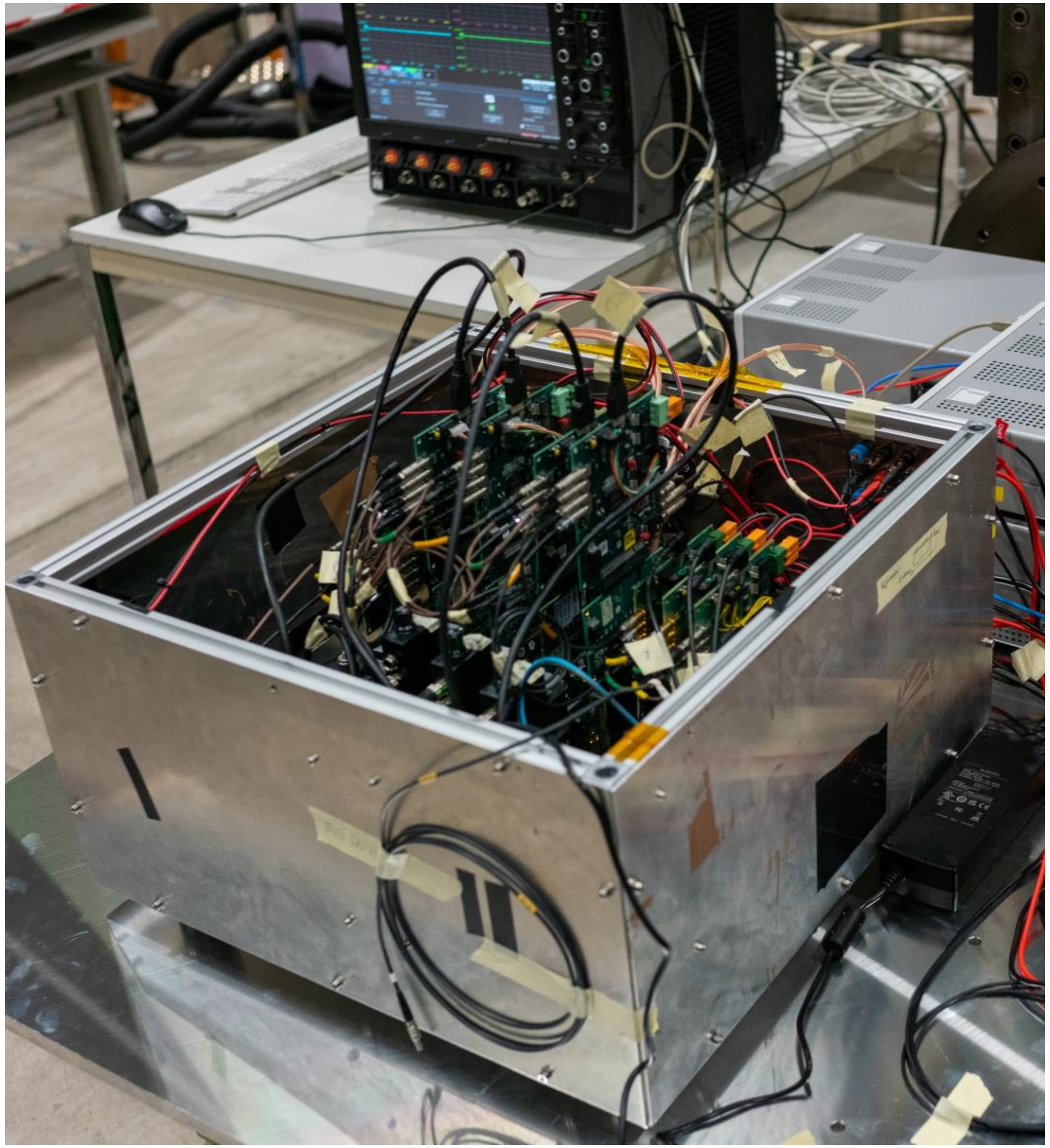
- **Goal**: Timing resolution measurement with MIPs
- **Beam**: SPS, CERN – 120 GeV/*c* hadron beam
- **Setup**
  - ➢ Beam telescope
    - ALPIDE telescope
  - ➢ DUT
    - 2 APTS OPAMP modified with gap variant (OPAMP0 and OPAMP1)
  - ➢ Oscilloscope
    - Teledyne LeCroy Wavemaster 820Zi-B
    - 13 GHz, 4 × 40 GSa/s
    - 2 channels for OPAMP0, 2 channels for OPAMP1



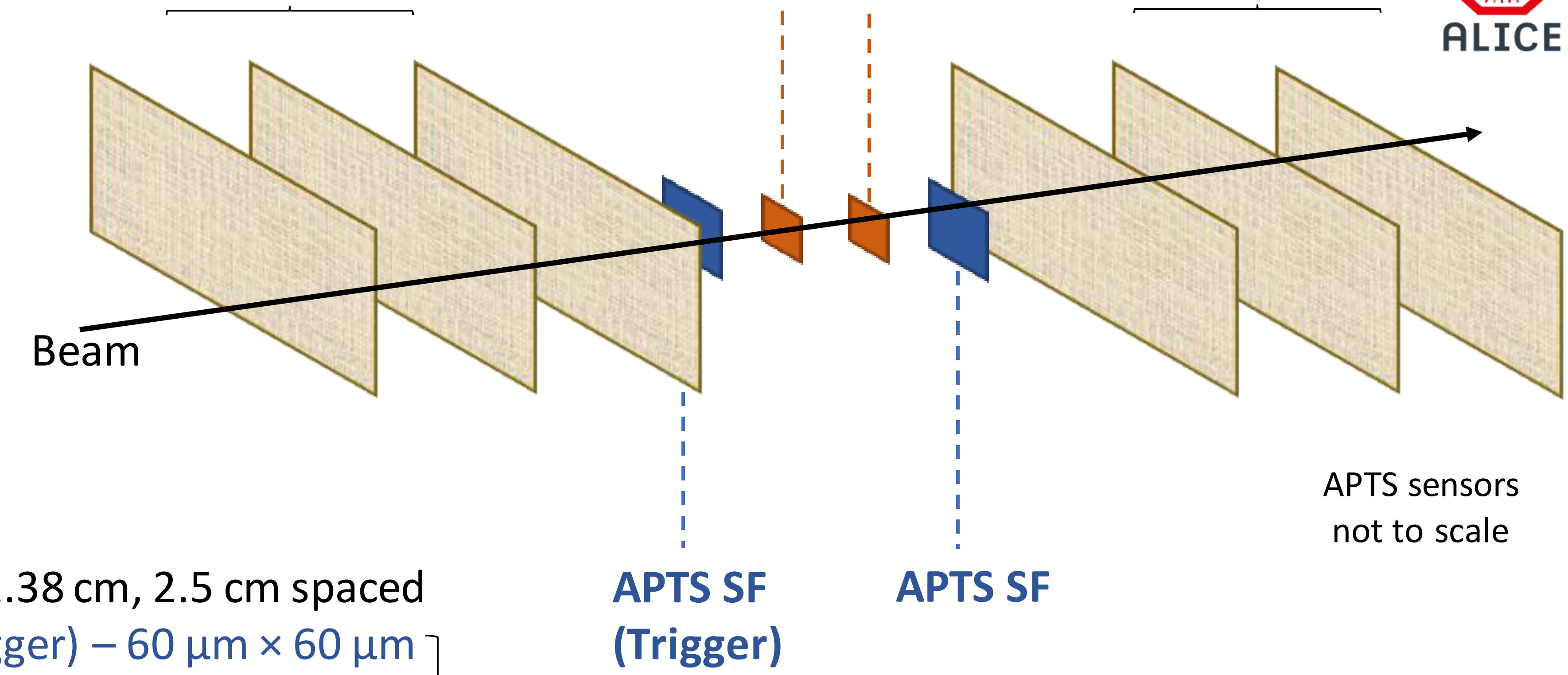
OPAMP1



OPAMP0



Beam test setup



- Planes
  - 3 ALPIDE planes – 3 cm × 1.38 cm, 2.5 cm spaced
  - APTS Source Follower (Trigger) – 60 µm × 60 µm
  - APTS OPAMP – 40 µm × 40 µm
  - APTS OPAMP – 40 µm × 40 µm
  - APTS Source Follower – 60 µm × 60 µm
  - 3 ALPIDE planes – 3 cm × 1.38 cm, 2.5 cm spaced

(APTS planes: 5 cm spaced)

- APTS SF (Trigger) and APTSs OPAMP mounted on µm-precision moving stages
- Tracking resolution on the DUT of the order of 1.8 µm with APTSs SF included in the track reconstruction

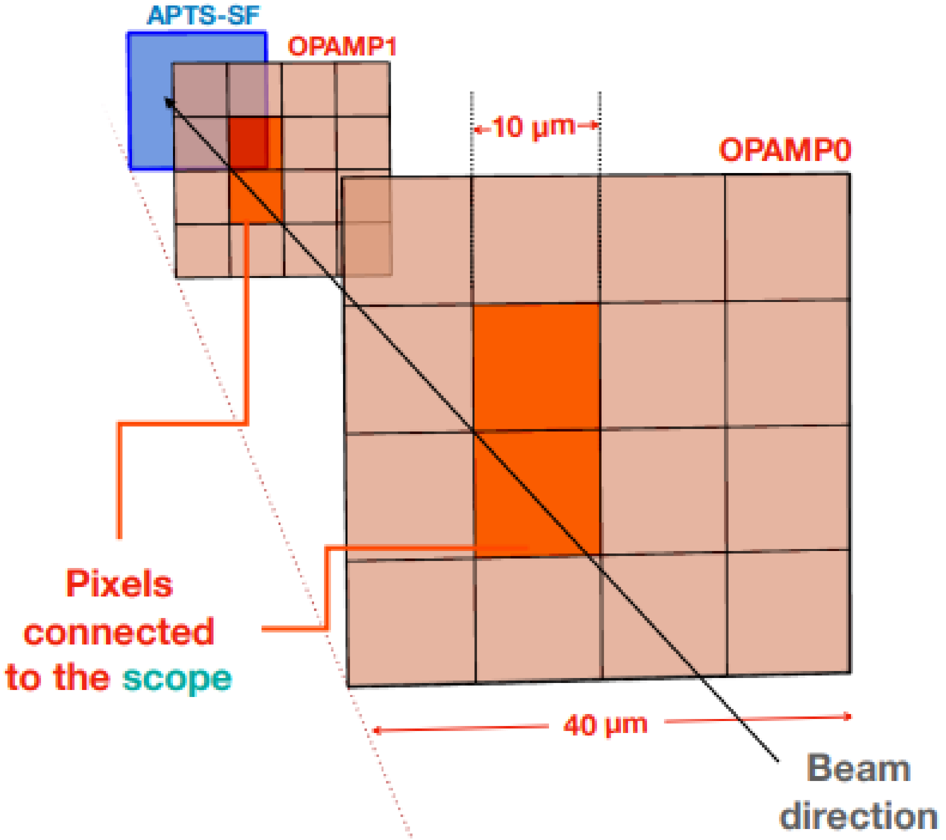
Beam test: measurement and alignment

Measurement strategy

- Time residuals Δt distribution of tracks associated to the pixels of both DUT measured with the oscilloscope

DUT alignment

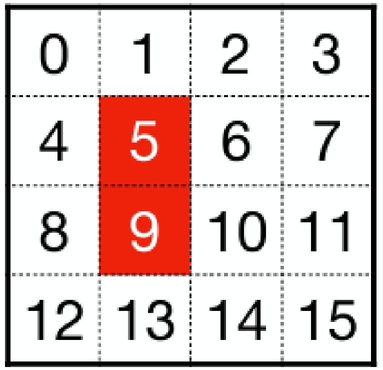
- Challenging alignment of < 5 µm accuracy
- Online analysis of alignment runs and position adjusted with moving stages



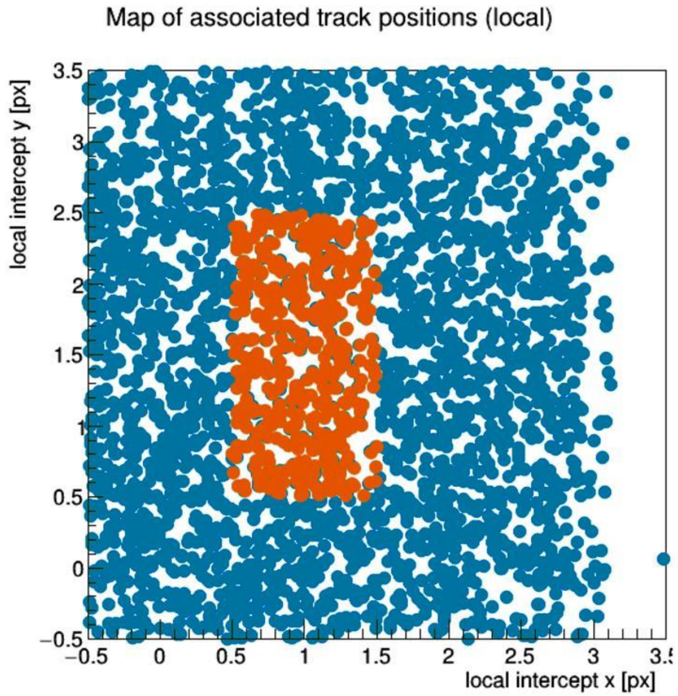
Beam test: tracking and waveform analysis

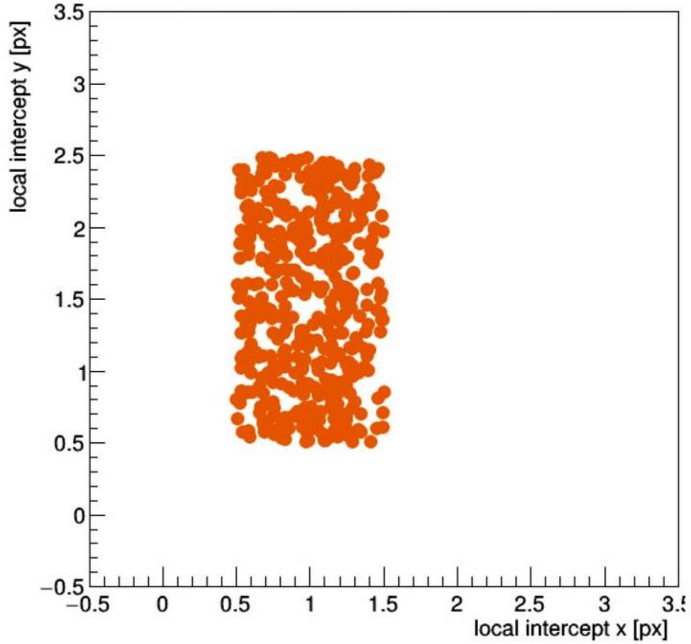
Track reconstruction

- Offline track reconstruction and association to DUTs with [Corryvreckan]() framework
- Reconstructed tracks filtered depending on the interpolated intercept on the DUT plane
- Accepted only tracks associated to the two pixels read out with the oscilloscope for each DUT



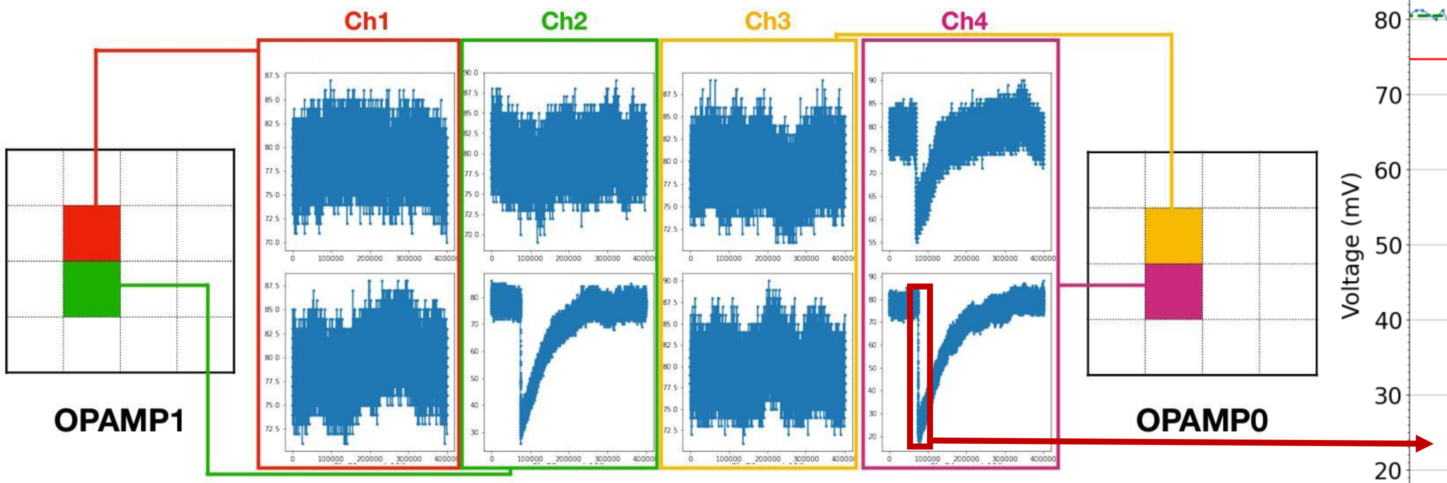
Map of the pixels connected to the oscilloscope for one of the DUTs

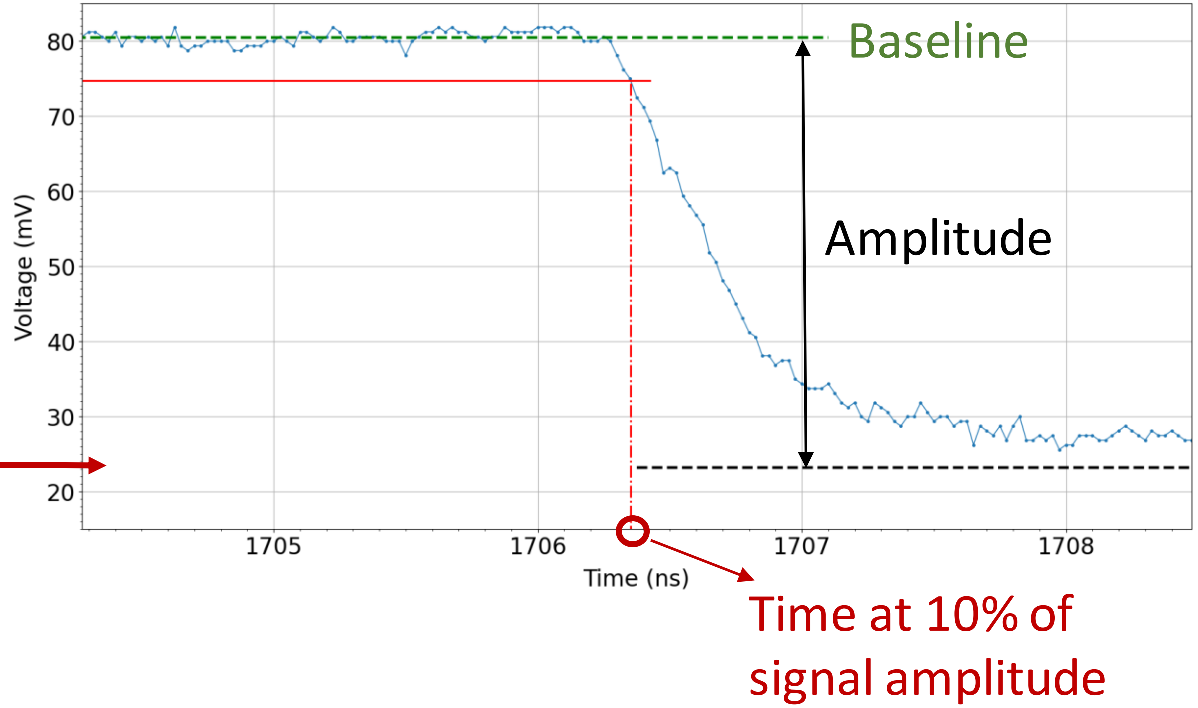




Corryvreckan: doi:10.1088/1748-0221/16/03/P03008

Beam test: tracking and waveform analysis





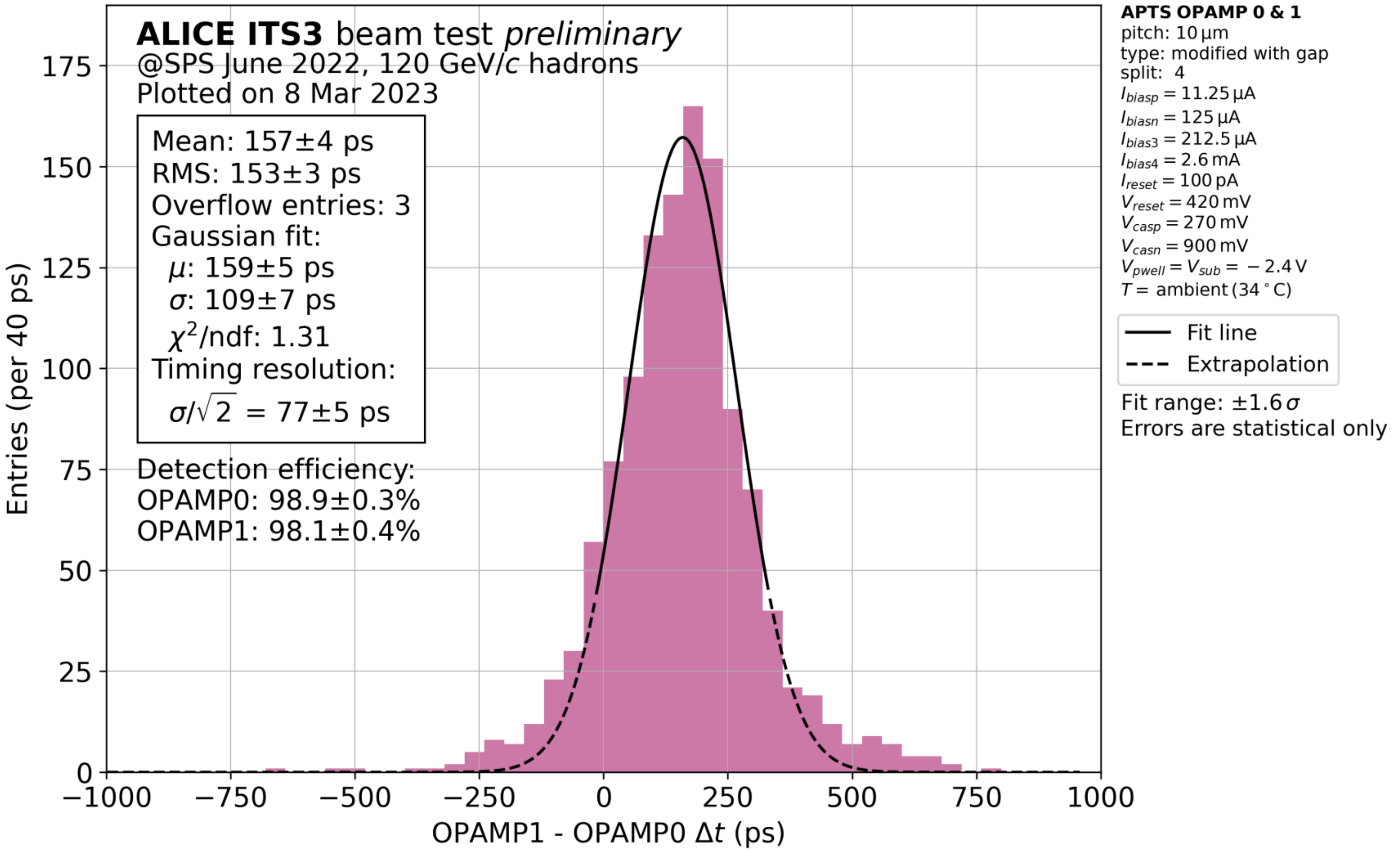
Top: not valid event for timing resolution measurement/
Bottom: valid event

Waveform analysis

- Selected waveforms with amplitude above 5.5 mV (~ 150 e^-)
- Valid event for timing resolution measurement must have the associated track to one of the two pixels measured with the oscilloscope of both the DUT planes
- Constant Fraction Discrimination (CFD) analysis of the waveforms
- Measured time residuals distributions at different CFD times (10% to 90%)

Beam test: timing resolution

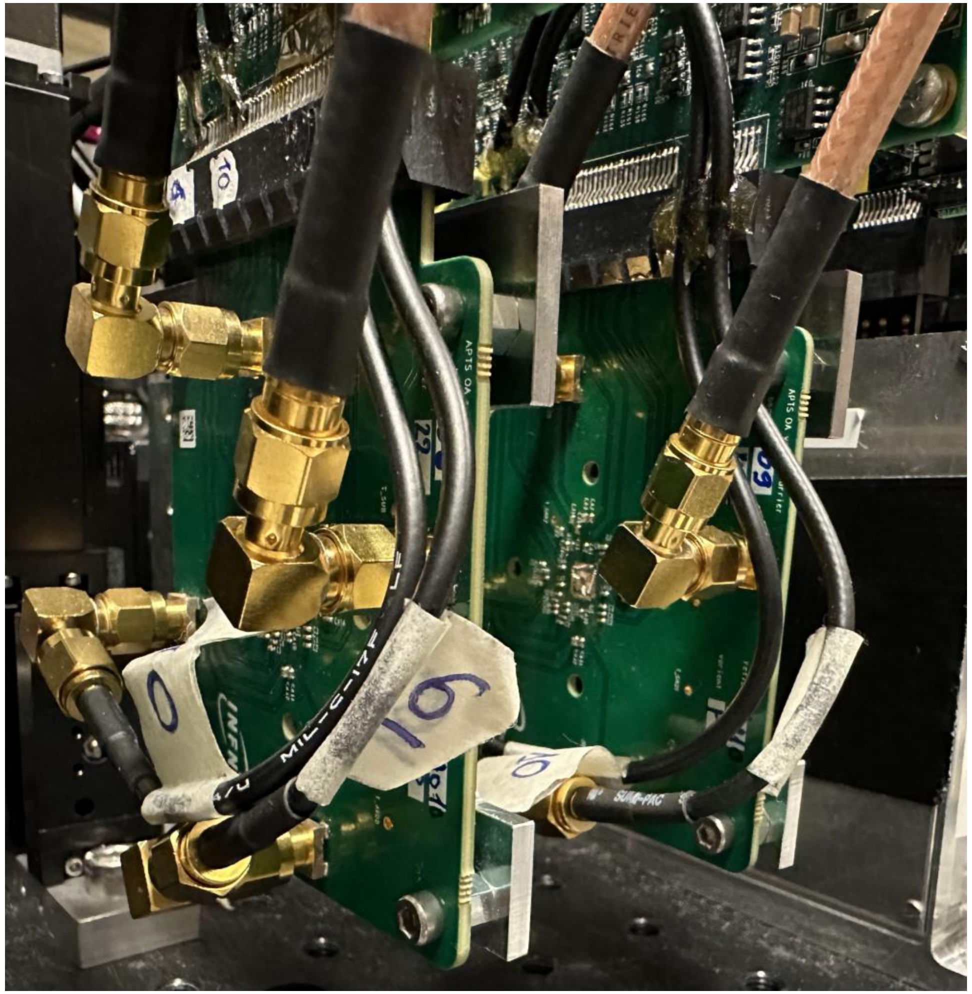
- Presented time residuals distribution at 10% of signal amplitude fraction
  - ➢ $\Delta t = t^1_{10\%CFD} - t^0_{10\%CFD}$
- DUTs operated at – 2.4 V reverse bias
- Efficiency of both DUTs of the order of 99%
- Time residuals distribution fitted with a gaussian function within ± 1.6 σ range (solid line)
- **Timing resolution of 77 ± 5 ps without jitter/time walk correction**



Summary & outlook

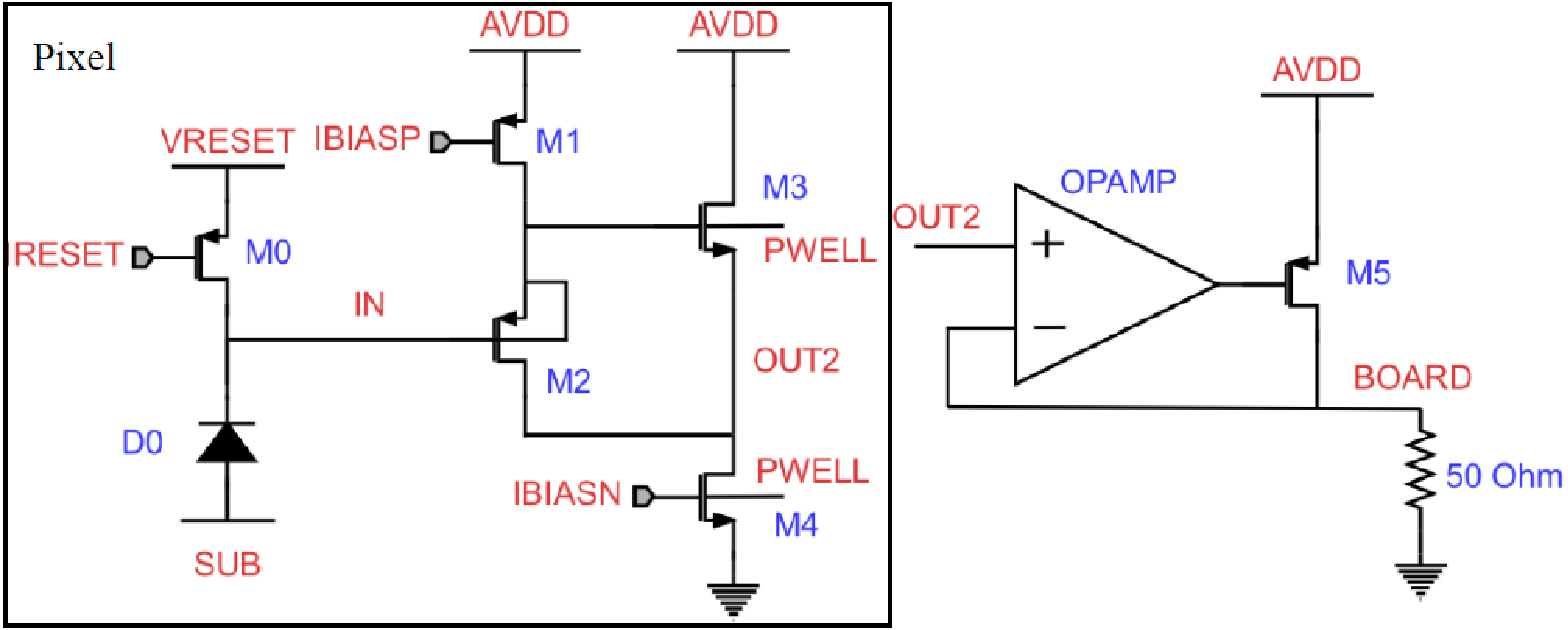
- CERN EP R&D and ALICE ITS3 developments:
  - Wafer-scale, bent MAPS
  - **TPSCo 65 nm CMOS process**
- APTS OPAMP to study the charge collection and the timing performance of the new technology
- ^{55}Fe source measurements:
  - reduced charge sharing and improved charge collection speed of modified with gap CMOS process
- Beam test measurement:
  - **Timing resolution of 77 ± 5 ps** at ~99% detection efficiency

- Ongoing studies and future plans:
  - Measurements at different operation conditions
  - In-pixel frontend jitter
  - Modified CMOS process variant with ^{55}Fe source
  - Characterization of irradiated samples
  - In-pixel position dependence of timing resolution



Additional slides

APTS OPAMP pixel analog frontend

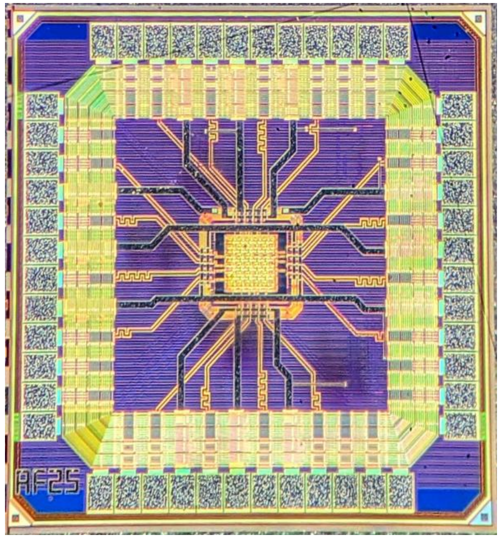


Test structures for the ALICE ITS3 upgrade

APTS

Analogue Pixel Test Structure

1.5 mm

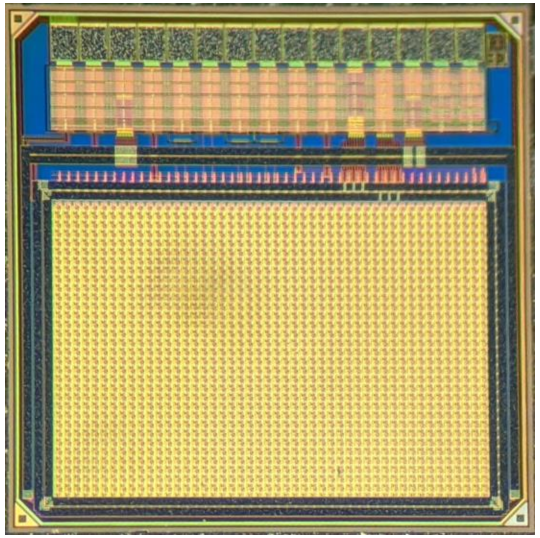


Matrix: 6 × 6 pixels
Readout: analogue readout of central 4 × 4 pixels
Pitch: **10**, 15, 20, 25 μm
Process: all 3 flavours
Variants: pixel buffers

- Source follower (SF)
- **Operational amplifier (OPAMP)**

CE65

Circuit Exploratoire 65 nm

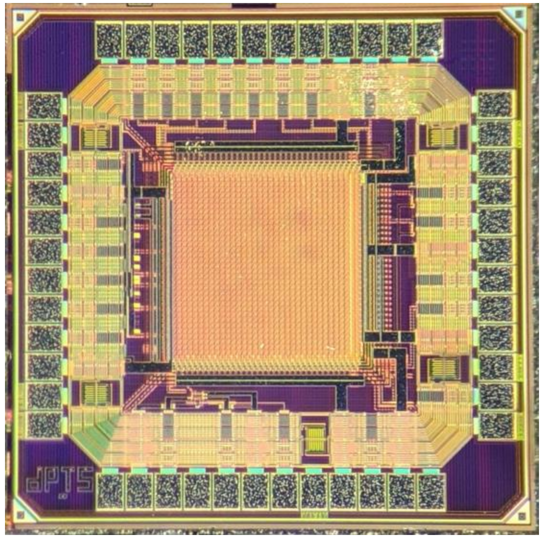


Matrix: 64 × 32/ 48 × 32 pixels
Readout: rolling shutter (50 μs integration time)
Pitch: 15, 20, 25 μm
Process: all 3 flavours
Variants: in-pixel architectures

- Source follower
- AC-coupled amplifier
- DC-coupled amplifier

DPTS

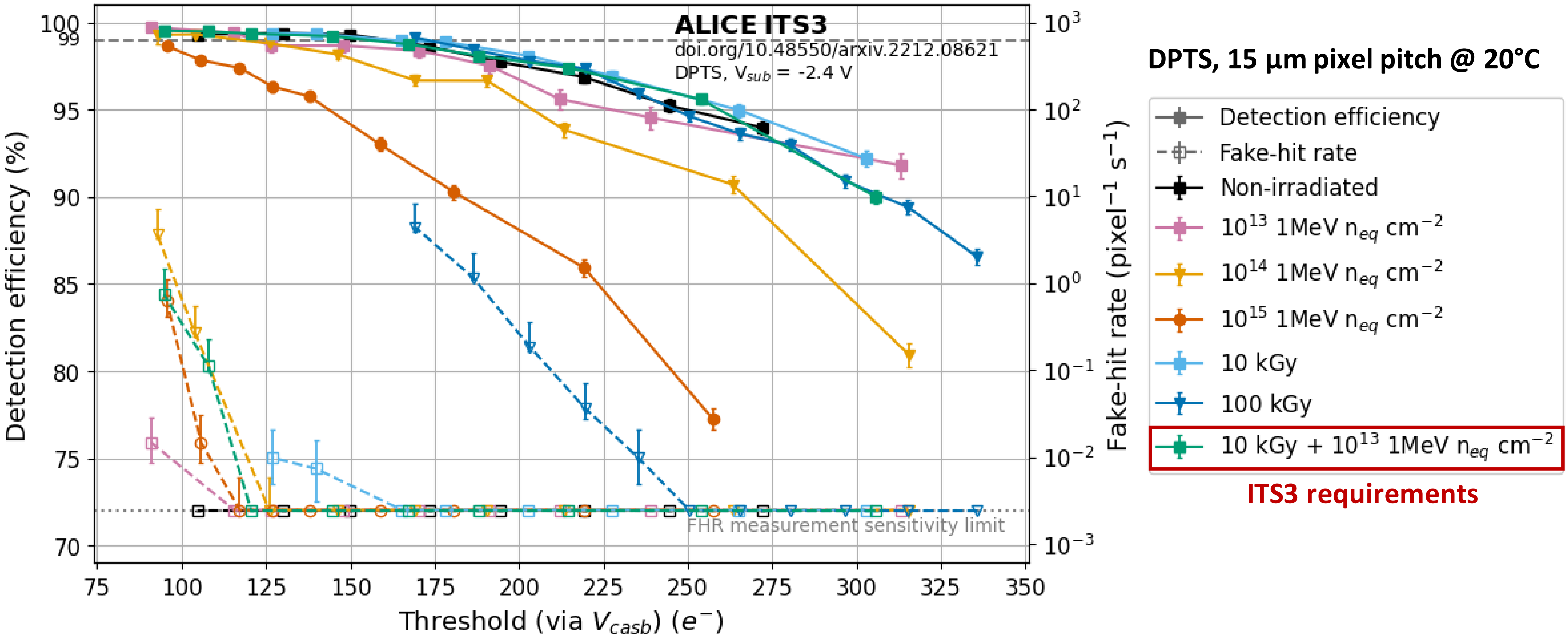
Digital Pixel Test Structure



Matrix: 32 × 32 pixels
Readout: Asynchronous digital readout
Pitch: 15 μm
Process: Modified with gap only
First results published:
doi:10.48550/arXiv.2212.08621

65 nm CMOS process – Radiation hardness

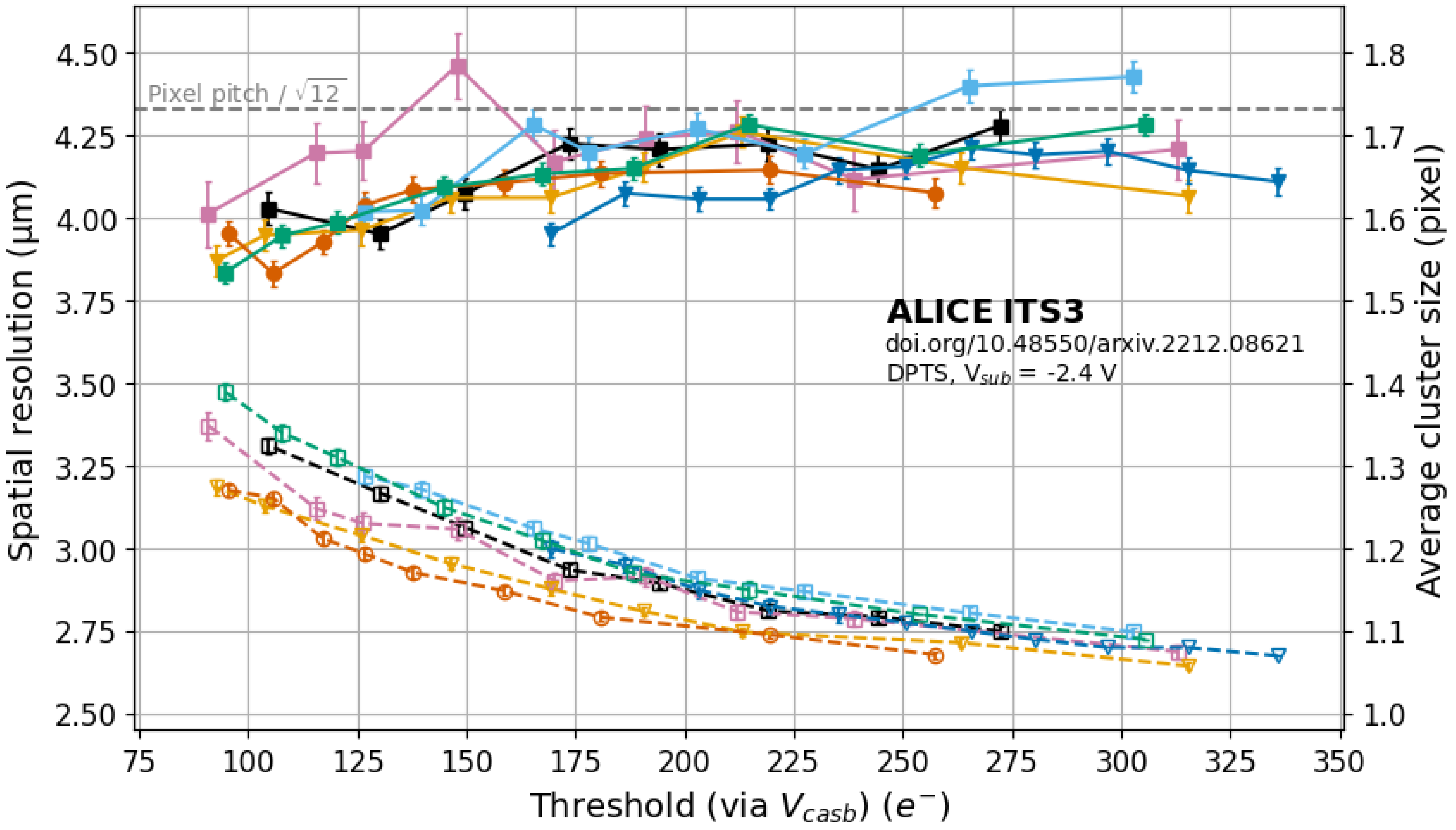
Detection efficiency and fake-hit rate (FHR)



ITS3 requirements

65 nm CMOS process – Radiation hardness

Spatial resolution and cluster size



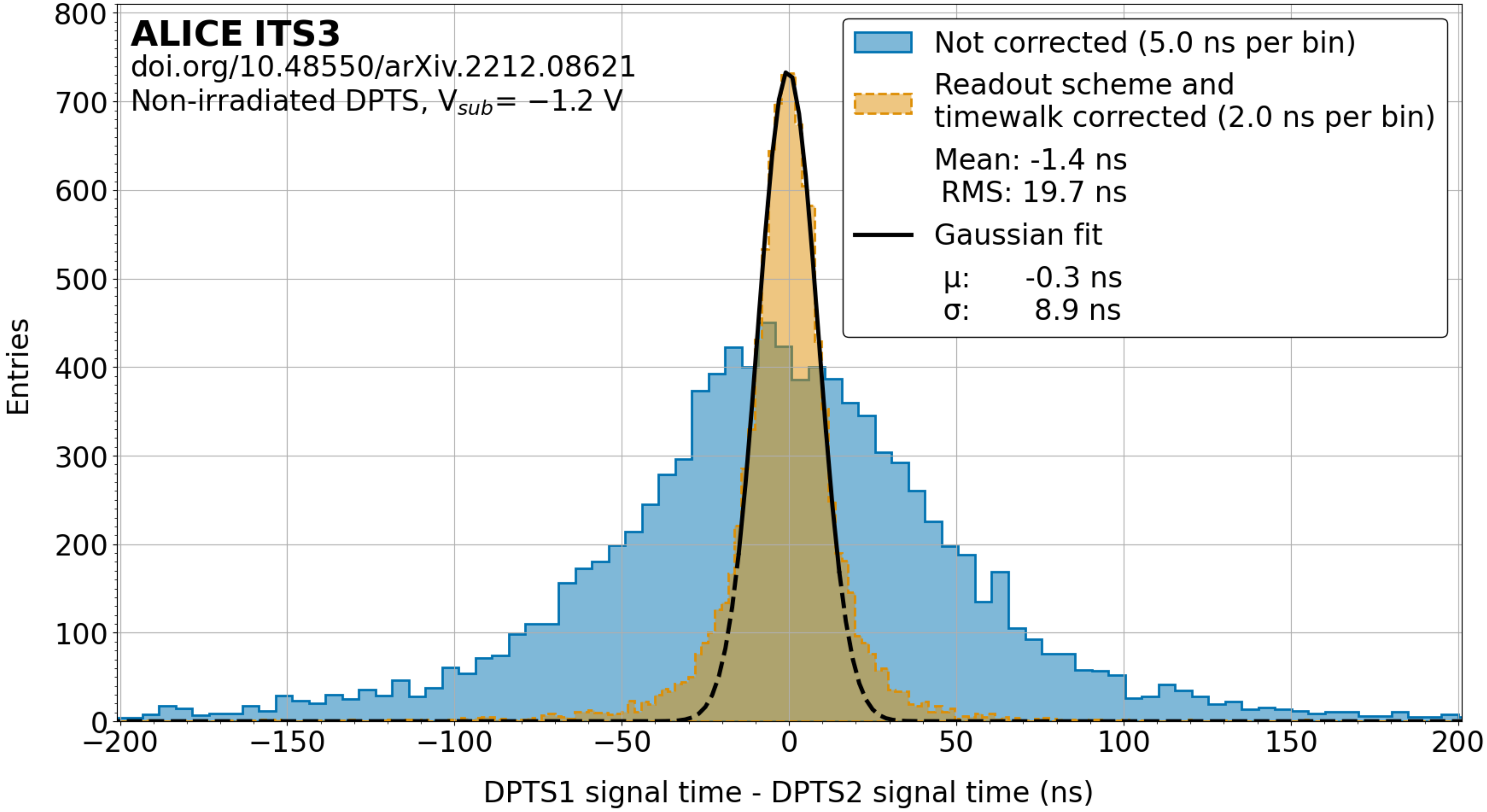
DPTS, 15 μm pixel pitch @ 20°C

- Spatial resolution
- Average cluster size
- Non-irradiated
- 10^{13} 1MeV n_{eq} cm^{-2}
- 10^{14} 1MeV n_{eq} cm^{-2}
- 10^{15} 1MeV n_{eq} cm^{-2}
- 10 kGy
- 100 kGy
- 10 kGy + 10^{13} 1MeV n_{eq} cm^{-2}

ITS3 requirements

65 nm CMOS process – Timing resolution

Sensor + full digital frontend



DPTS, 15 µm pixel pitch

~ 6 ns timing resolution

(~ 30 ns not corrected)

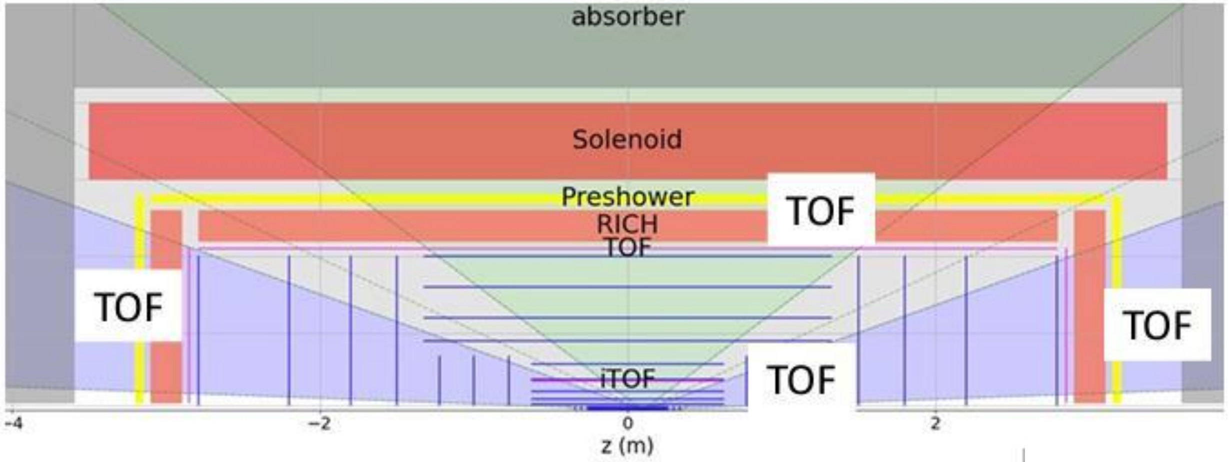
Power consumption:
~ 120 nW in-pixel

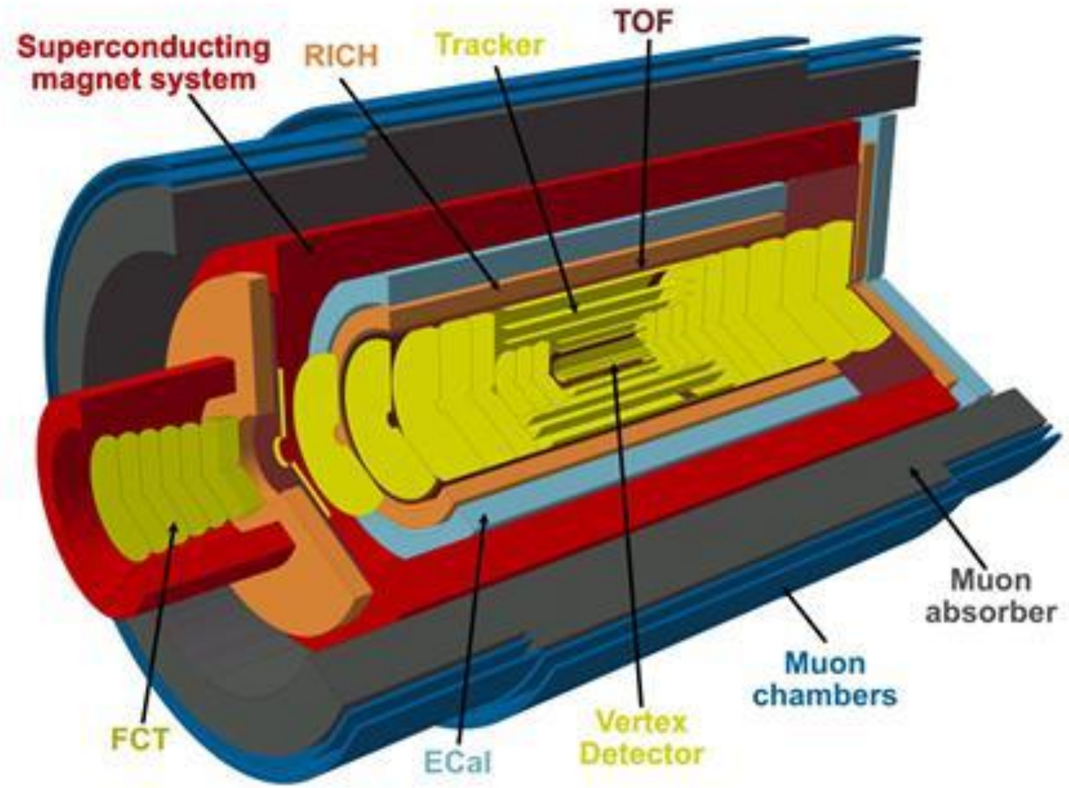
Perspectives for fast timing detectors

- R&D activities to explore new technologies for applications even beyond ITS3 needs
- New ALICE detector under design for data taking after LHC Run 4 (2034 and beyond)
- Full silicon-based vertex, tracker and Time of Flight (TOF) detectors
  - Silicon timing sensors requirements for TOF
    - **Timing resolution of 20 ps**
    - Material budget: 1-3% X/X_0
    - Power consumption below 50 mW/cm^2

TOF

- outer TOF at R ≈ 85 cm
- inner TOF at R ≈ 19 cm
- forward TOF at z ≈ 405 cm

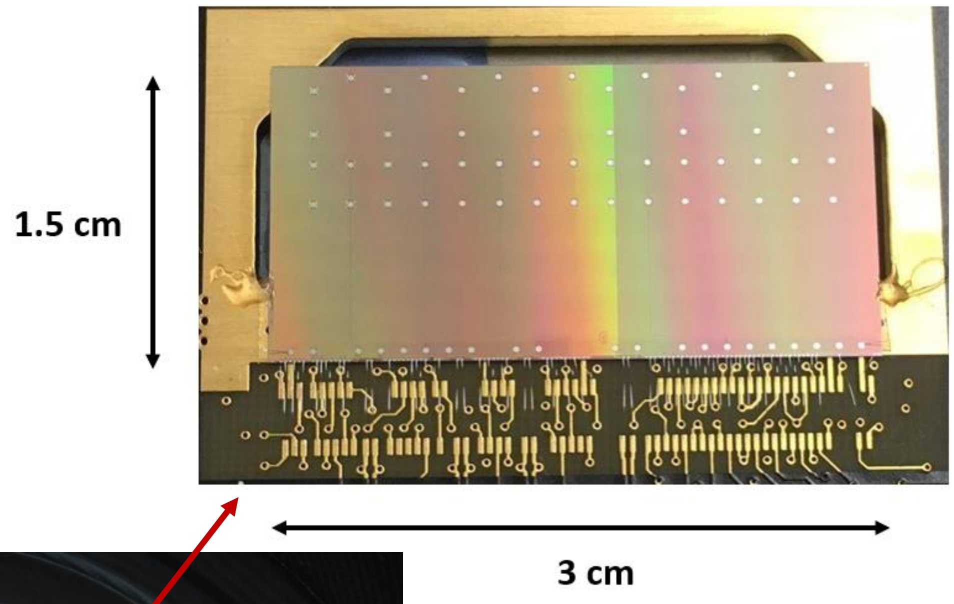


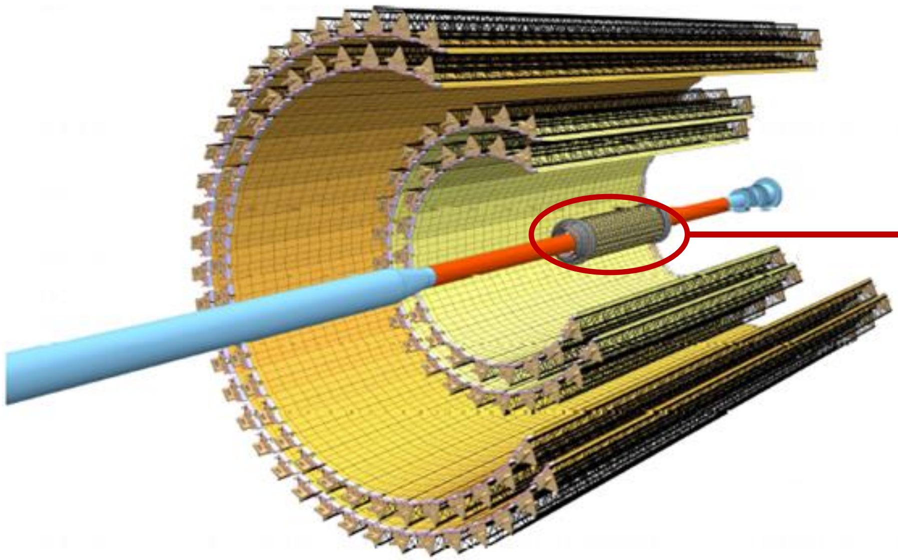


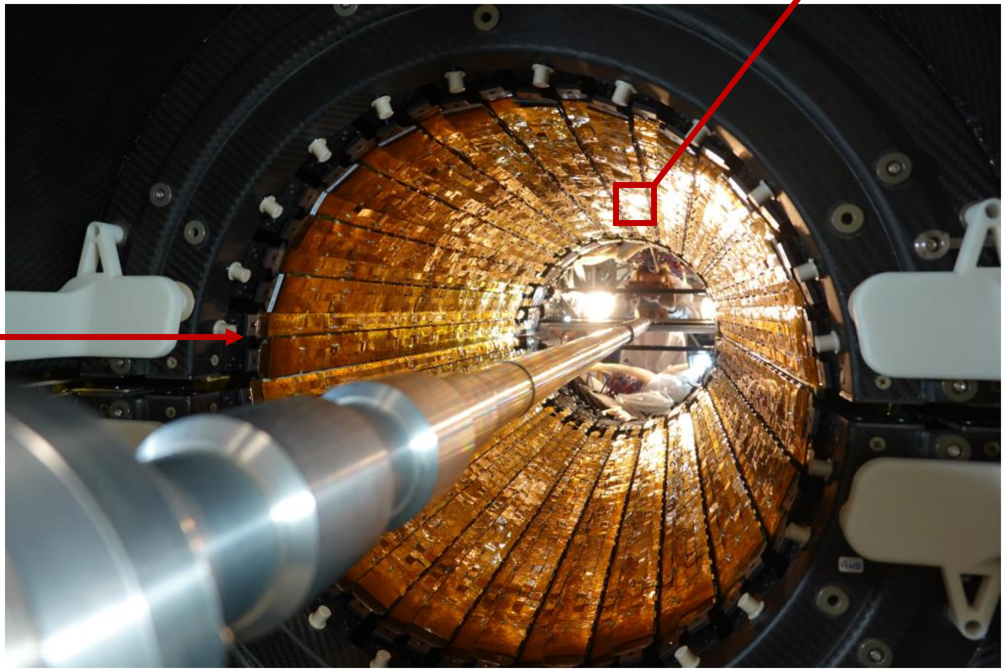
The ALICE Inner Tracking System: sensor

- ALice PIxel DEtector (**ALPIDE**) developed for the ITS2
- 1024 × 512 pixel matrix, 29 µm × 27 µm pixel size
- MAPS implemented in **TowerJazz 180 nm CMOS process**
- Thinned to 50 µm
- Detection efficiency >> 99%
- Spatial resolution of 5 µm

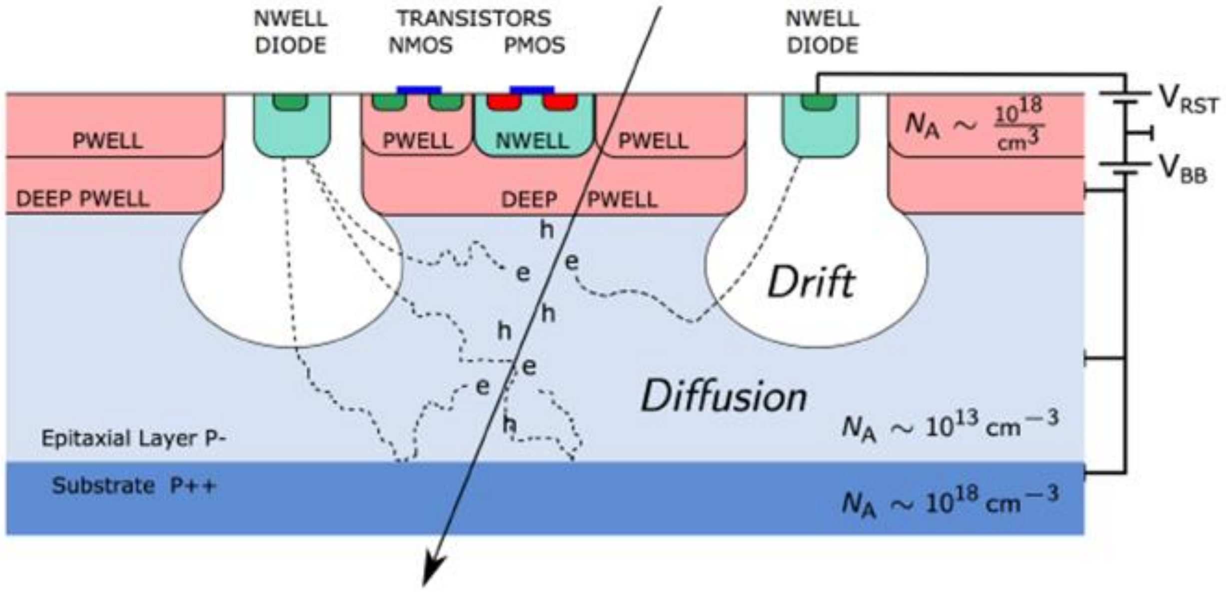
ALPIDE





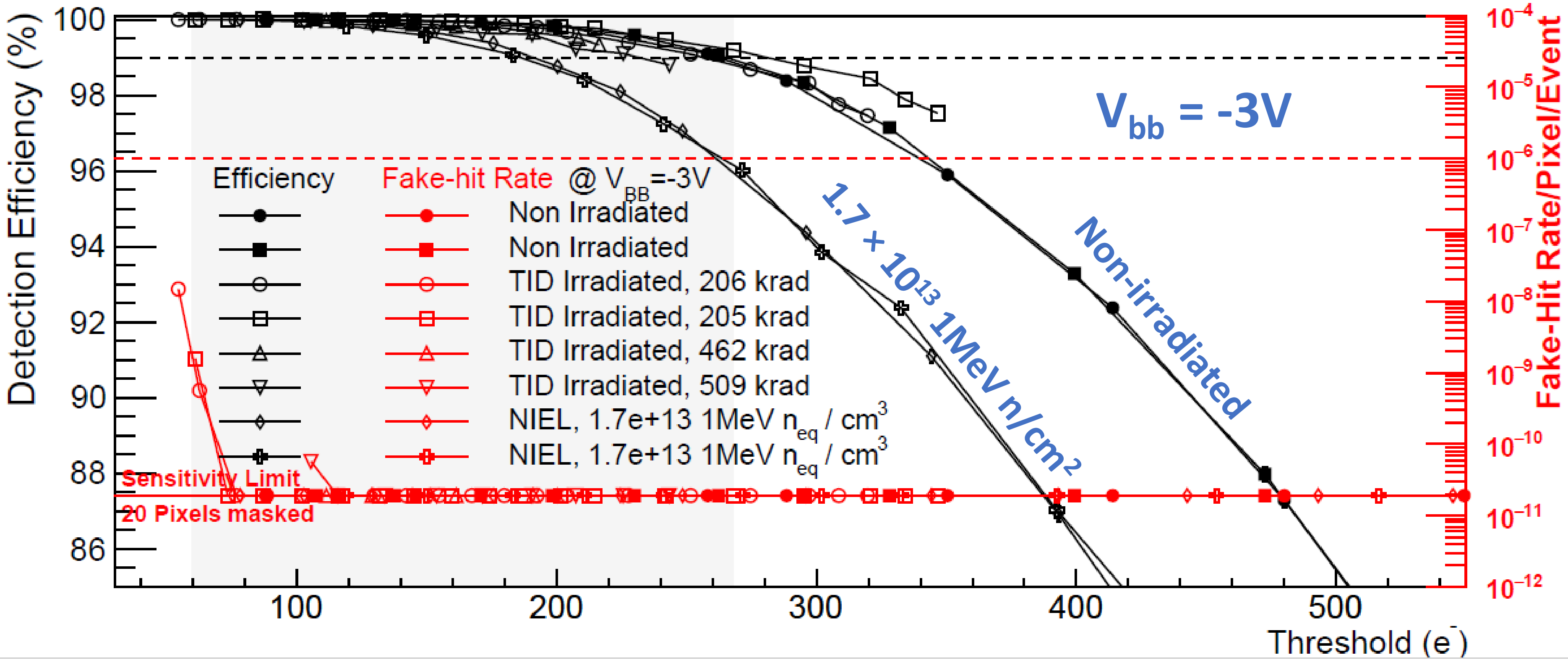


ALPIDE, the ALICE Pixel Detector



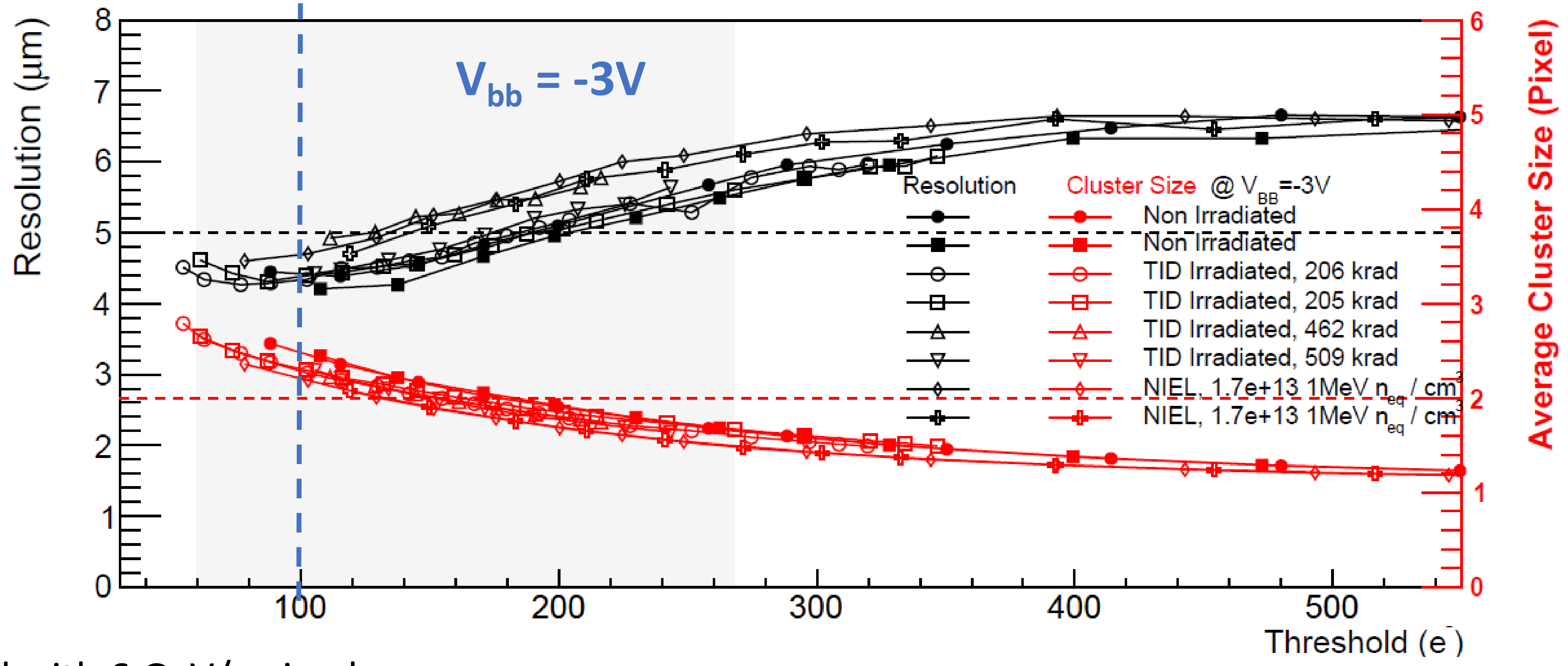
- TowerJazz 180 nm CMOS Standard Imaging Process pixel sensor:
  - High-resistivity (> 1 kΩ·cm) p-type epitaxial layer (25 µm) on p-type substrate
  - 2 µm diameter n-well electrode, ~ 5 fF input capacitance
  - **50 µm overall sensor thickness**
- Monolithic design:
  - In pixel amplification, discrimination, 3 hit storage registers
- Ultra-low power consumption:
  - **40 nW/pixel**
  - **20 mW/cm^2**
- High hit rate transmission:
  - **~6 MHz/cm^2 hit rate chip output data transfer**

ALPIDE performance figures



- Measured with 6 GeV/c pion beam
- At 100 e^- of operation threshold and V_{bb} = -3 V:
  - ➢ Detection efficiency above 99.99%
  - ➢ Fake hit rate < 2×10^{-11} pixel hits/event
  - ➢ Irradiated chips performance is comparable with not-irradiated chips

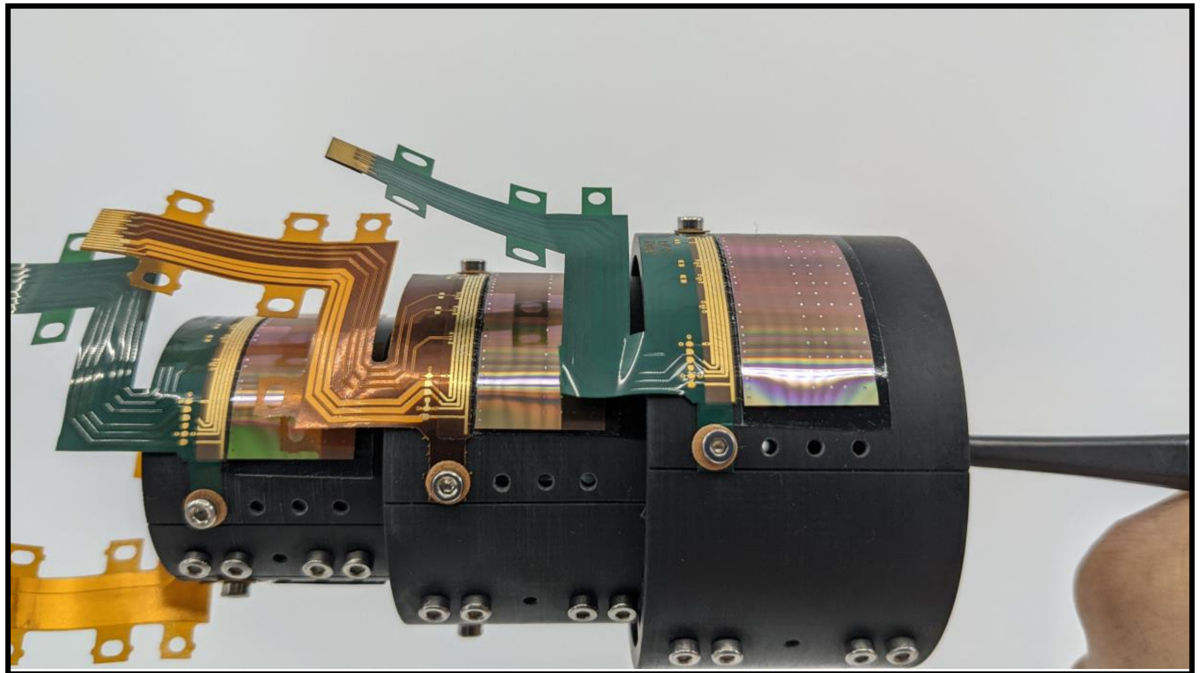
ALPIDE performance figures



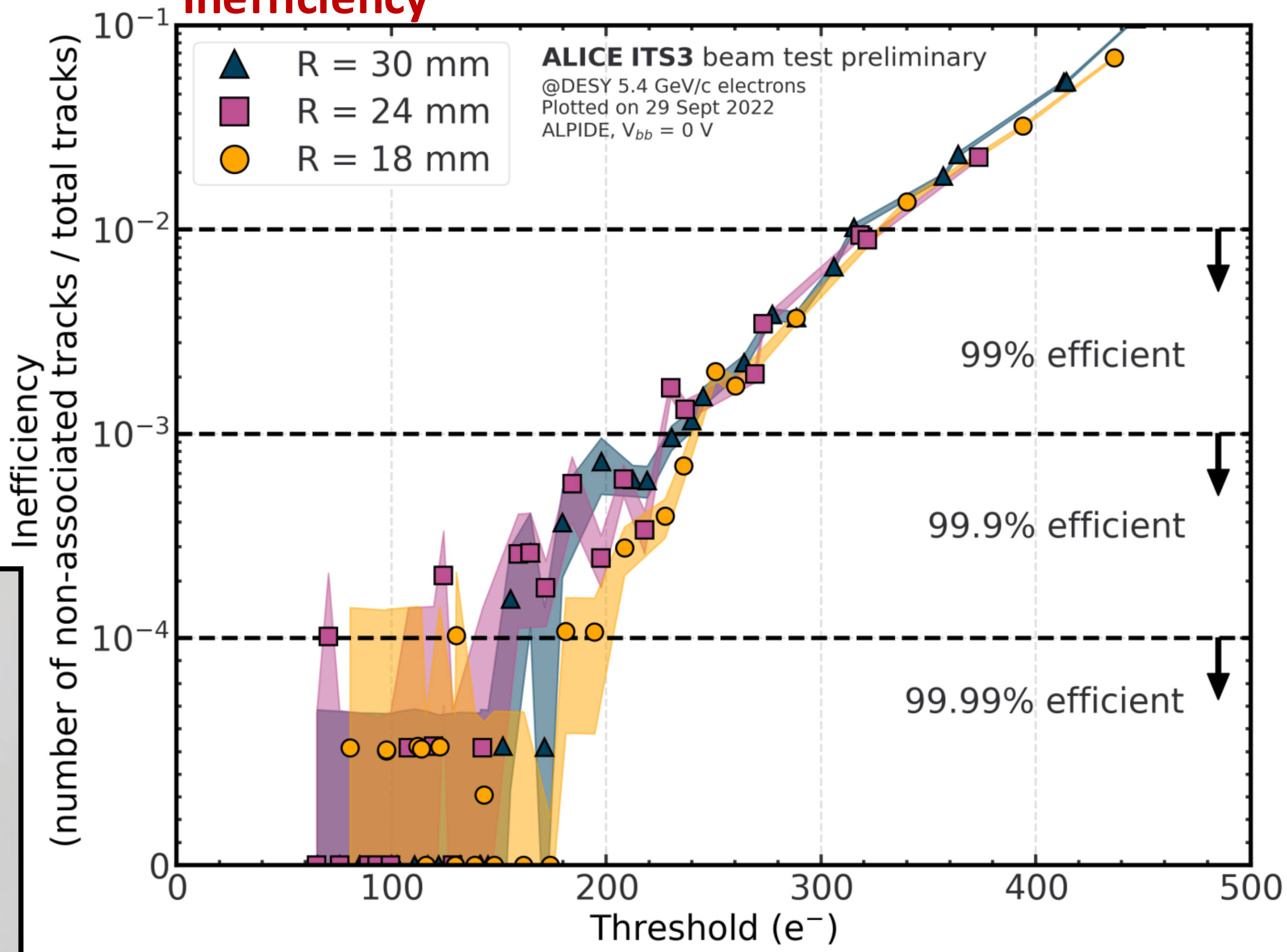
- Measured with 6 GeV/c pion beam
- At 100 e^- of operation threshold and V_{bb} = -3 V:
  - Spatial resolution below 5 μm
- Not irradiated and TID/NIEL chips show similar performance

Flexibility and bending of silicon sensors

- Full mock-up of the final ITS3 has been measured under charged particle beam
  - Realized with 6 bent ALPIDEs
  - Uniform spatial resolution among different radii
  - Efficiency and spatial resolution consistent with flat ALPIDEs



Inefficiency



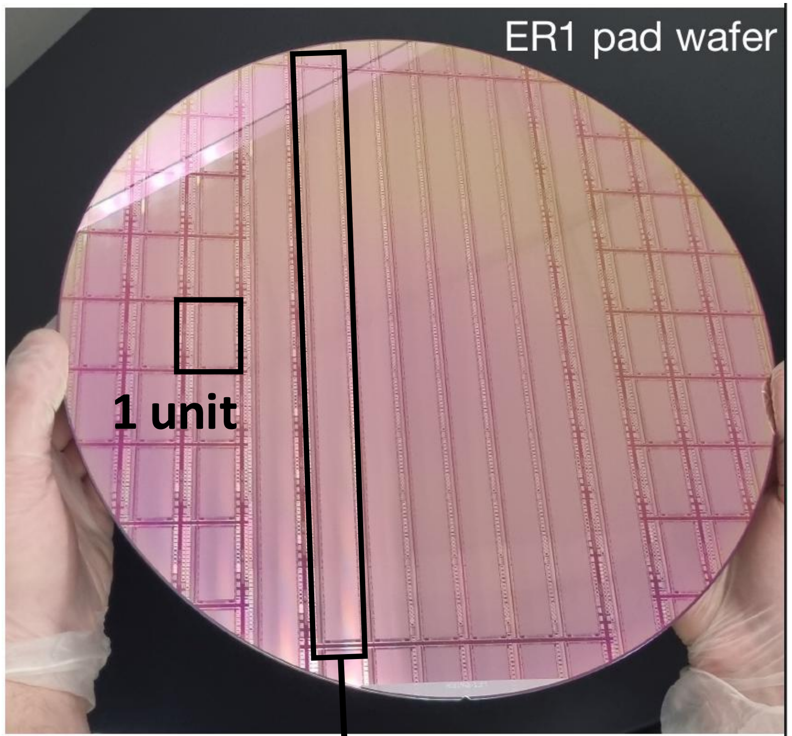
More results in doi:10.1016/j.nima.2021.166280

A wafer-scale sensor

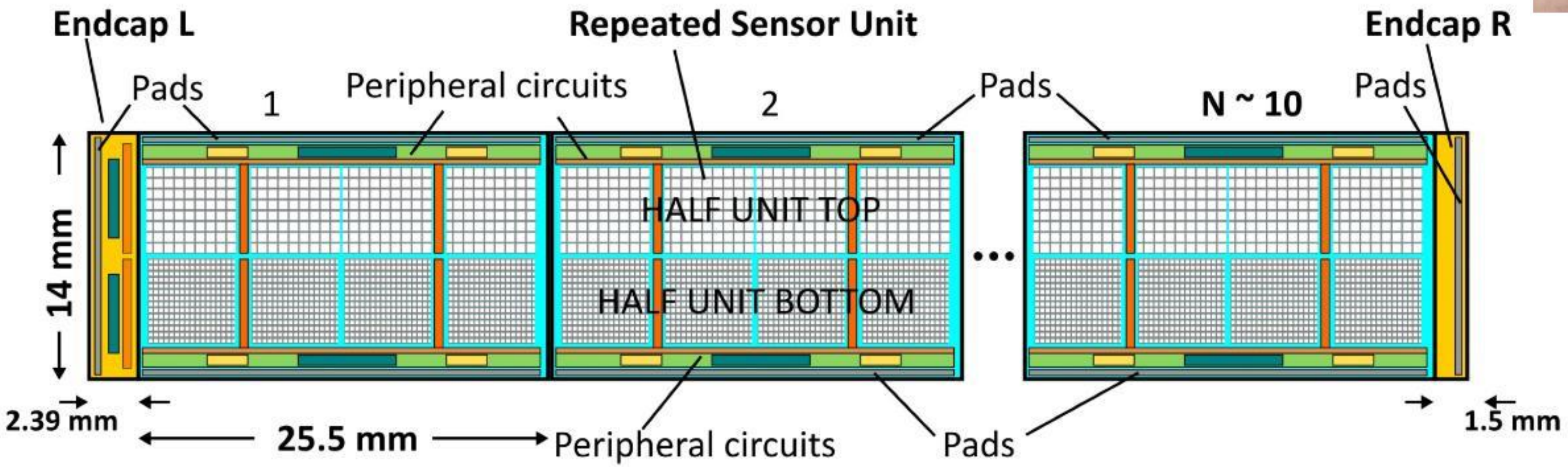
- CMOS sensor size is limited by manufacturing process ("reticle size")
- Typical sizes of the order of few cm^2

→ How to produce a 300 mm wafer-scale sensor?

- **Stitching**: merging multiple design structures on a wafer during the lithographic process
- A 300 mm wafer can house a sensor to equip a full half-layer
- First sensors to test expected soon

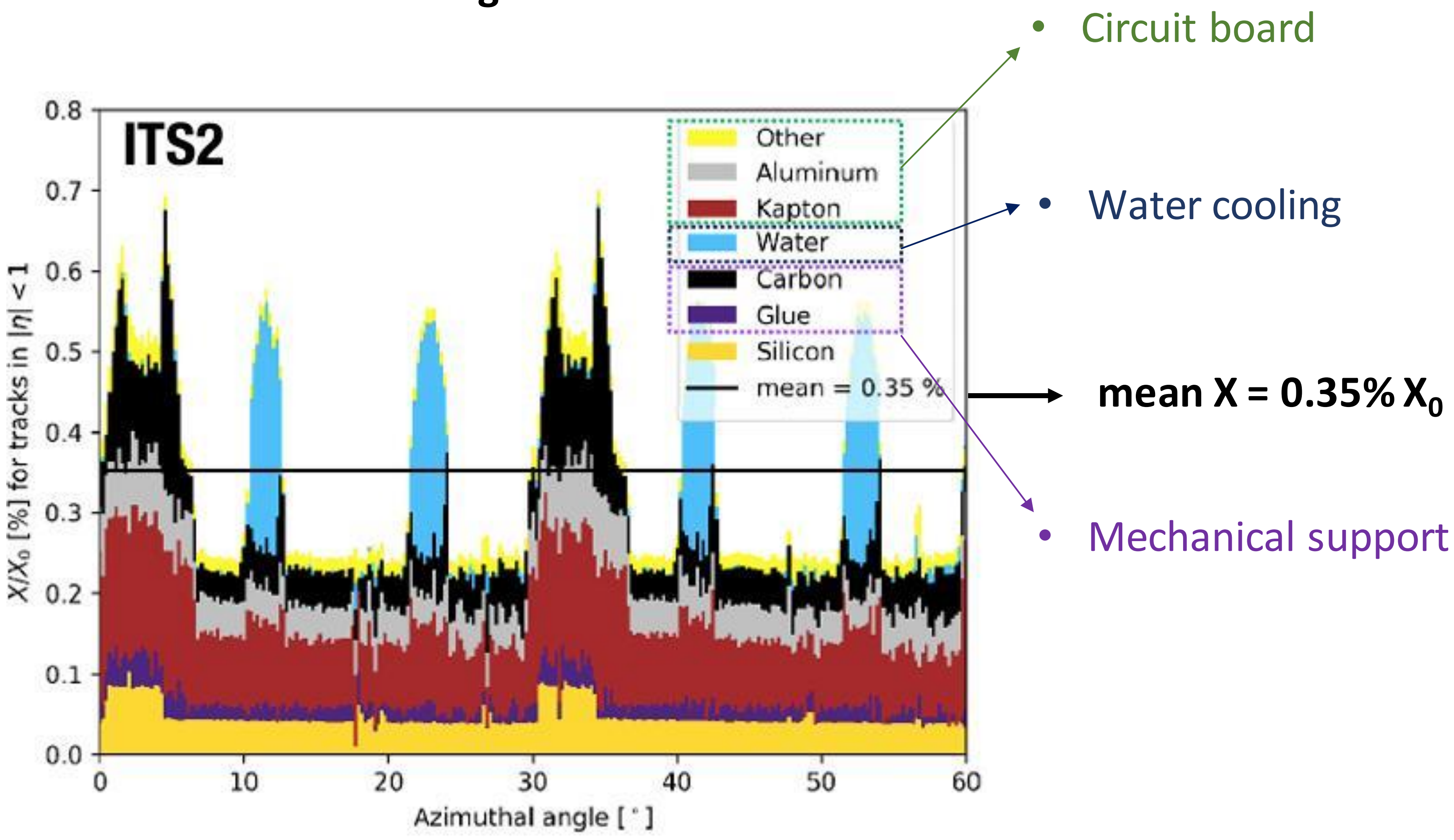


1 prototype sensor = 10 units



How to improve the ITS2 performance?

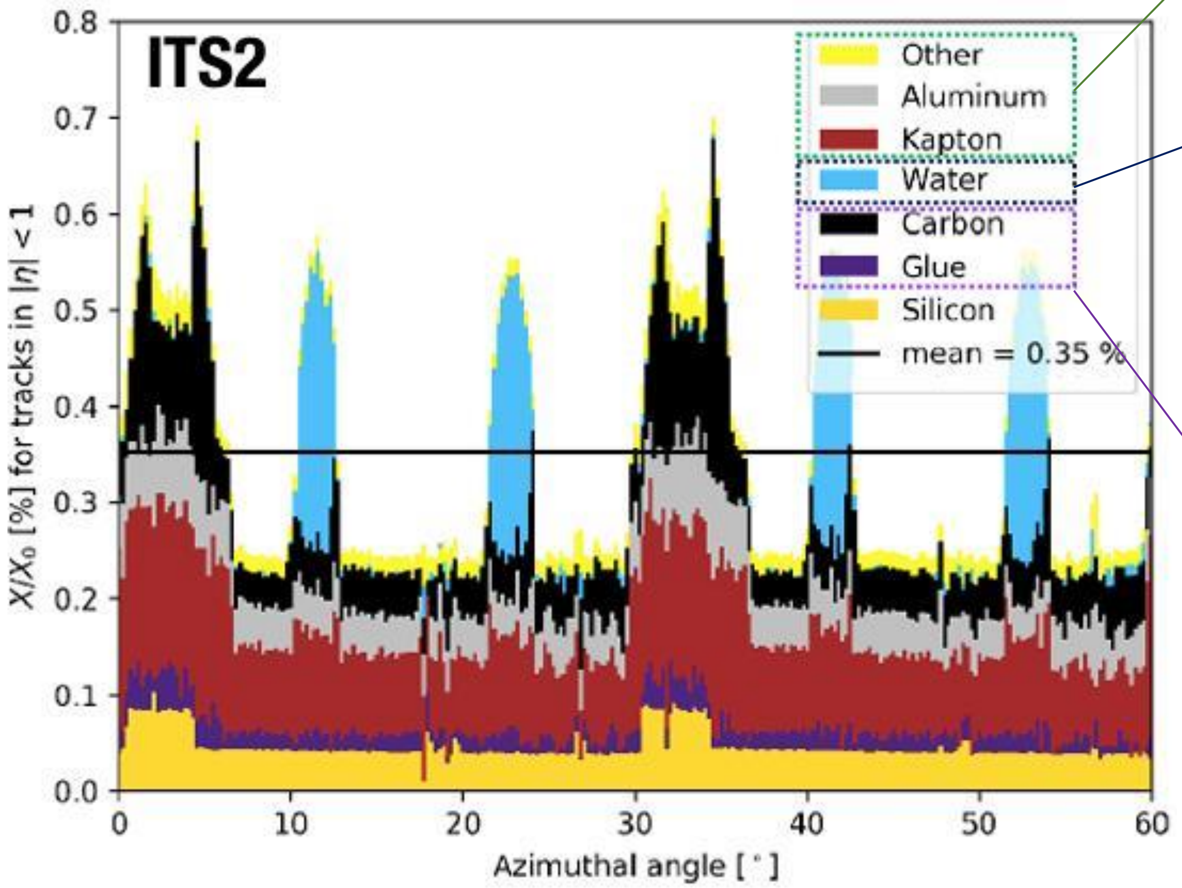
- Get closer to the interaction point
- **Reduce the material budget**



Material budget distribution of the innermost layer of the tracker

How to improve the ITS2 performance?

- Get closer to the interaction point
- **Reduce the material budget**

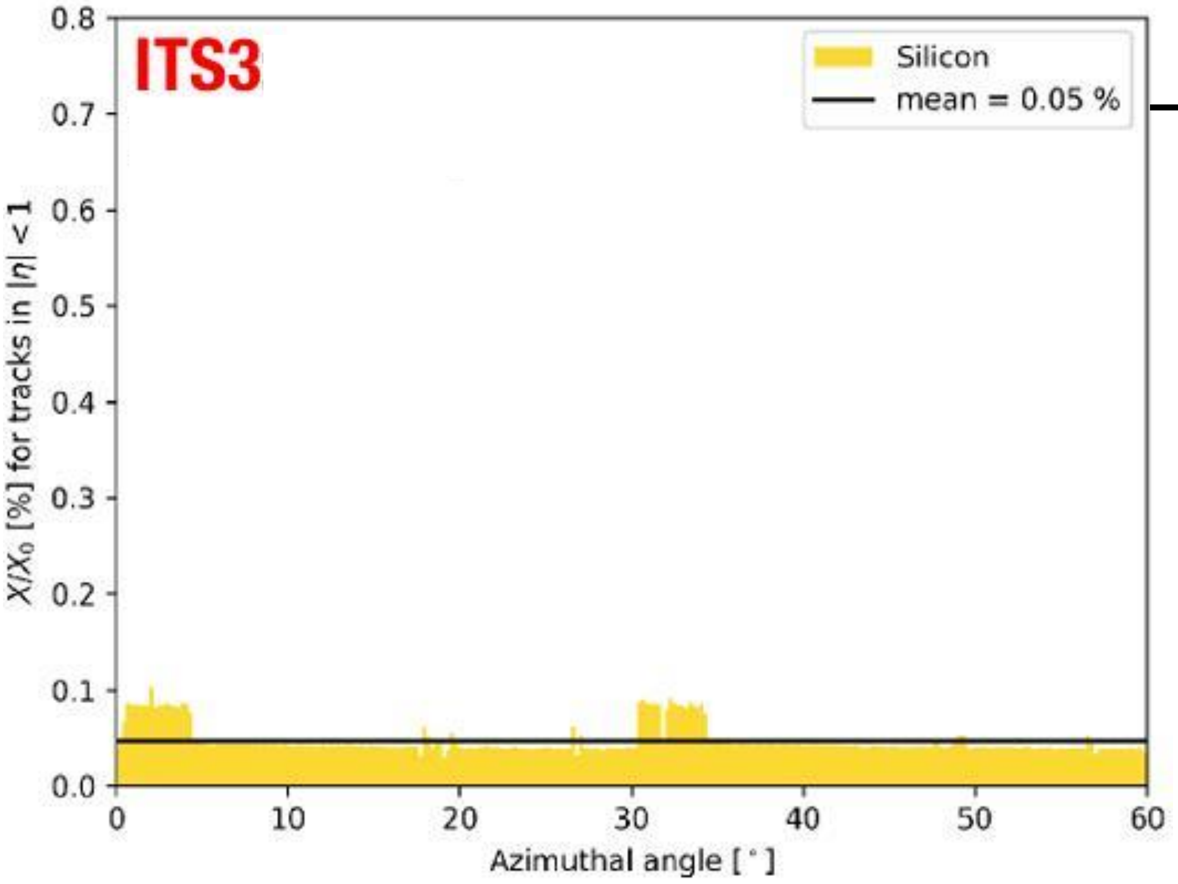


Material budget distribution of the innermost layer of the tracker

- Circuit board
  - ➢ Can be removed if power and data transmission are integrated into the chip
- Water cooling
  - ➢ Air cooling is enough if the chip power consumption is below 20 mW/cm^2
- Mechanical support
  - ➢ Not required if the detector has a self-supporting curved structure

How to improve the ITS2 performance?

- Get closer to the interaction point
- **Reduce the material budget**



mean X = 0.05% X_0

Ultra-light tracking detector!

Material budget distribution of the innermost layer of the tracker