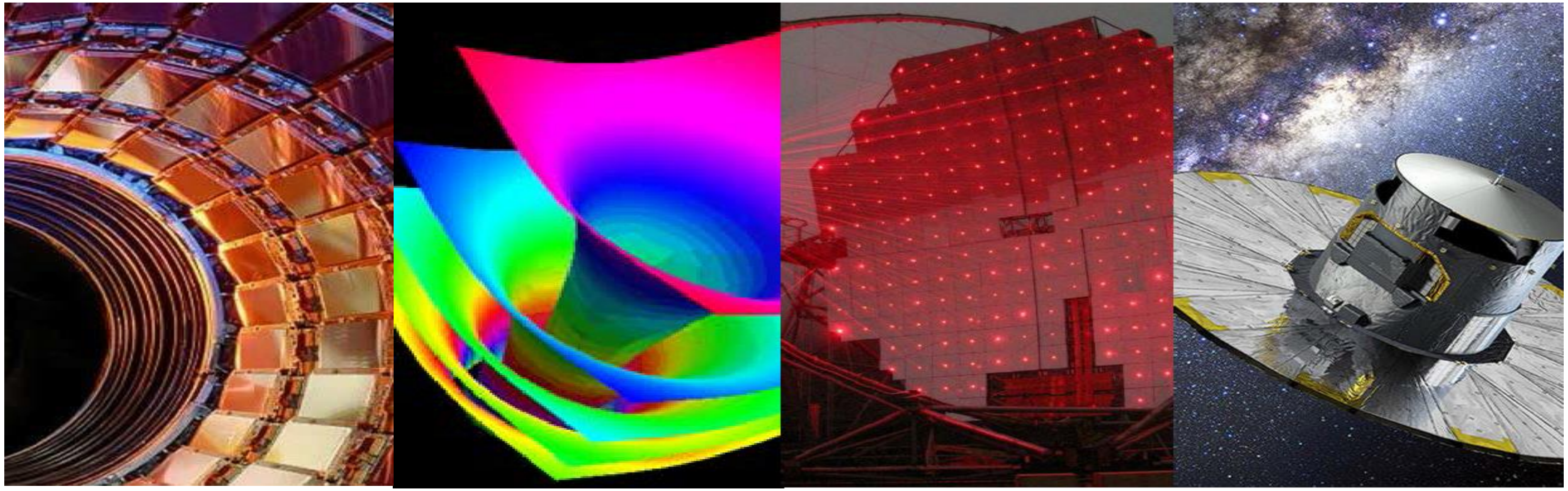
Institute of Cosmos Sciences



Status of FastIC developments

J. Alozy, E. Auffray, F. Bandi, R. Ballabriga, M. Campbell, J.M Fernández,
D. Gascon, S. Gomez, J. Kaplon, N. Kratochwil, A. Paterno, S.Portillo,
J. Mauricio, R. Manera, A. Mariscal, M. Piller, A. Pulli, A. Sanuy, J. Silva

ICCUB – Universitat de Barcelona

CERN microelectronics section (EP-ESE-ME)

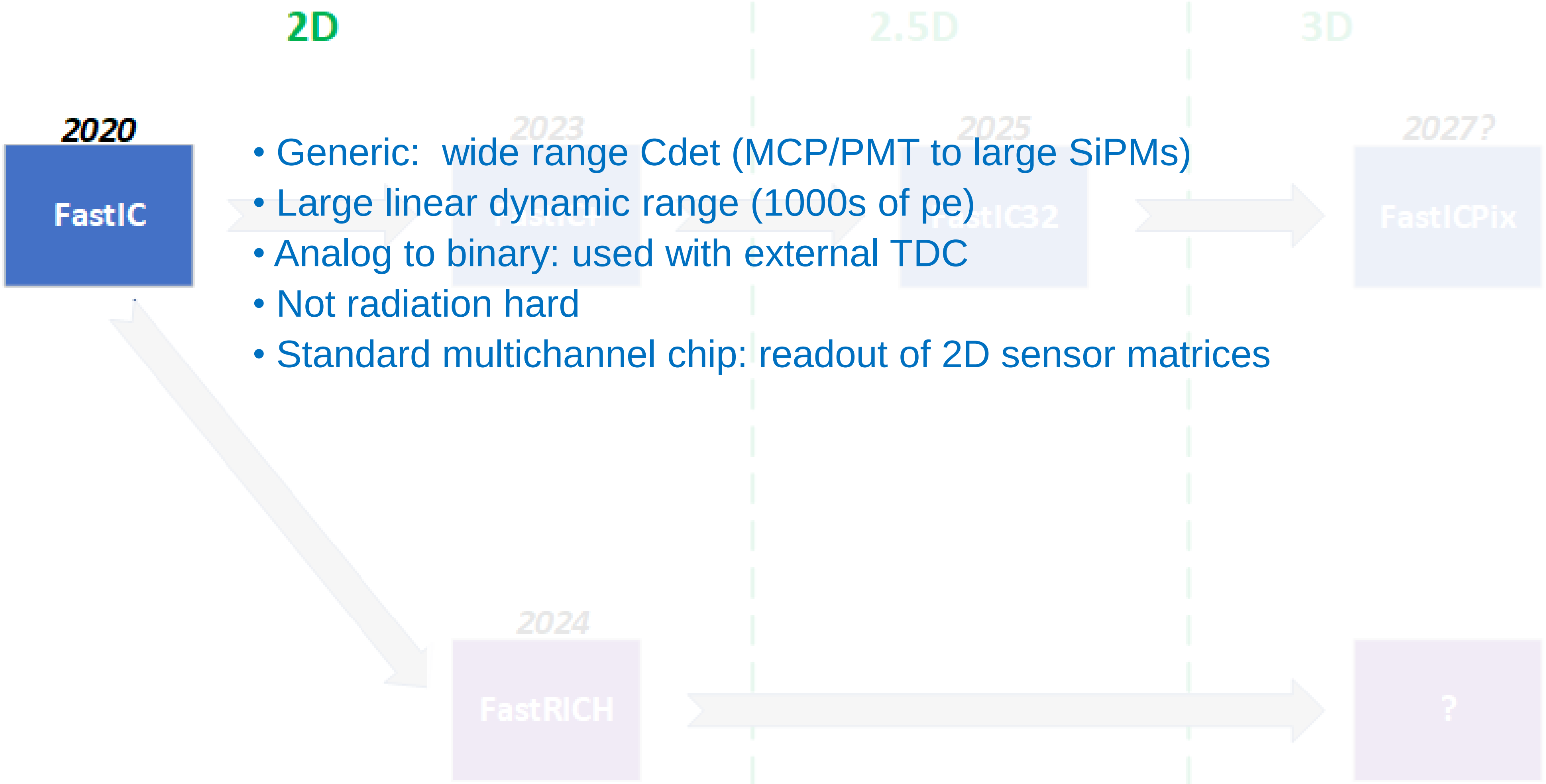
FAST23

30/05/2023

I. Introduction

- Collaboration: University of Barcelona (ICCUB) and CERN (EP-ESE-ME)
- Develop a *scalable* FE electronics for photosensors with intrinsic gain (PMTs, MCPs, SiPMs) to perform precise measurement of
  - Time: approach intrinsic single photon time resolution of the sensor: 10 - 100 ps
  - Energy: linear (< 3%) for 1000s p.e. range
    - Allows for precise time-walk correction
    - Optimal solution would be waveform sampling + digital signal processing (see D. Breton) but…
- What does scalable mean?
  - System on chip: input stage, comparators, TDC/ADC, digital back-end, serializer
  - Low power (<1 mW/mm^2) including everything
  - Compact:< 1 mm^2 per readout channel (or “pixel”)
  - Fabrication cost < 1 $/ch for volume production

II. FastIC

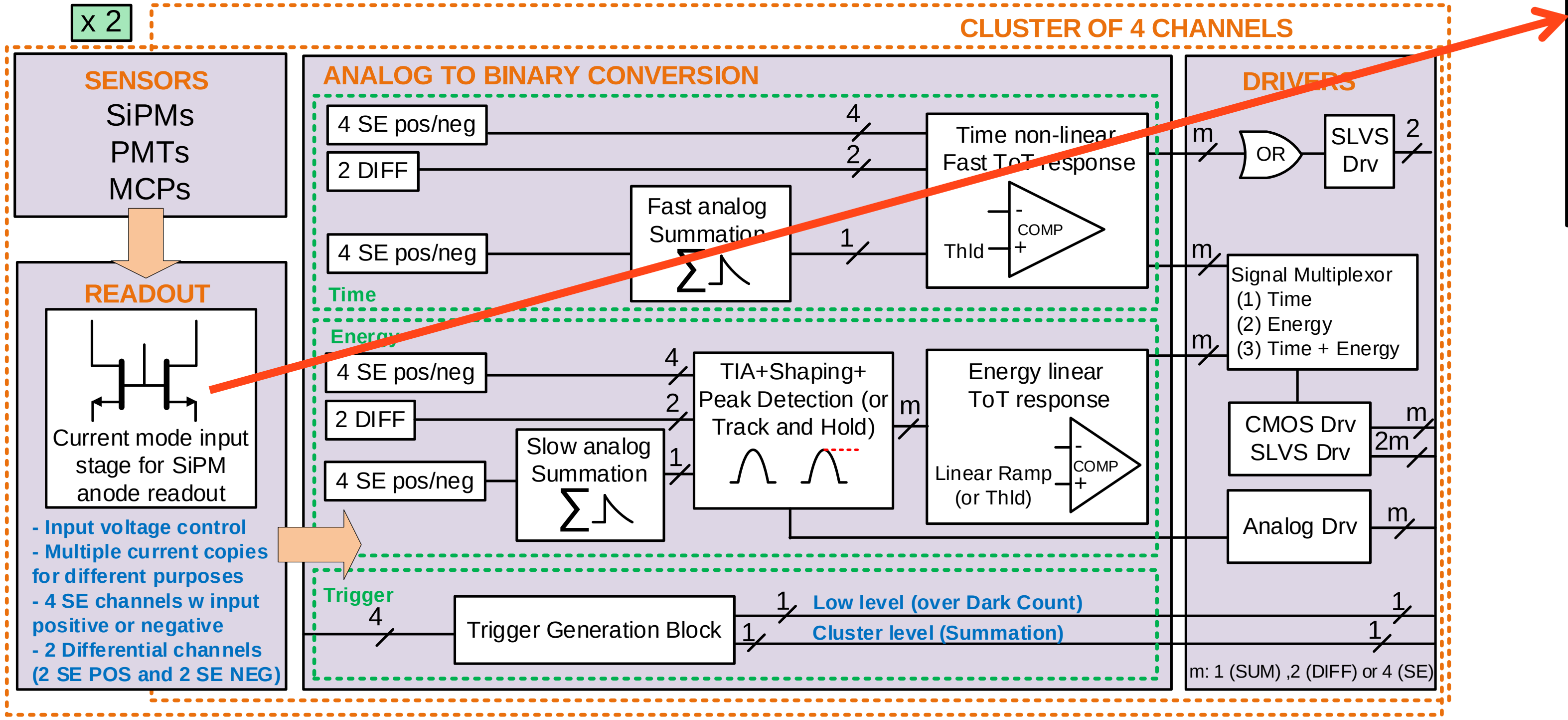


- Generic: wide range Cdet (MCP/PMT to large SiPMs)
- Large linear dynamic range (1000s of pe)
- Analog to binary: used with external TDC
- Not radiation hard
- Standard multichannel chip: readout of 2D sensor matrices

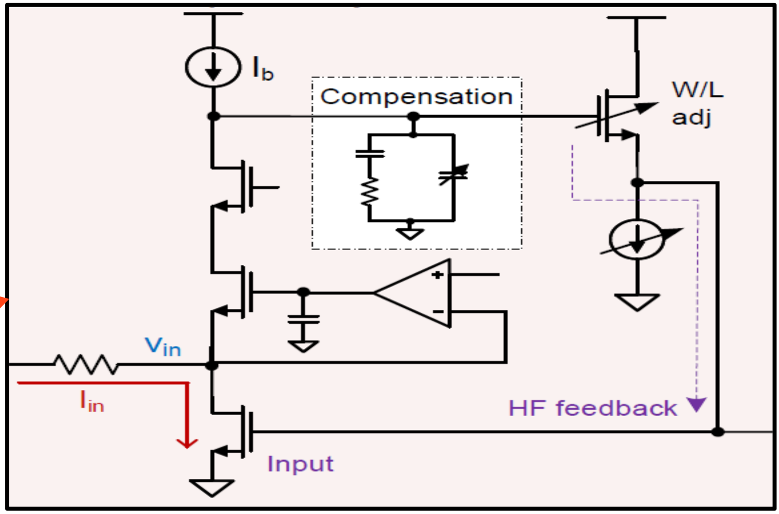
II. FastIC architecture

- **FASTIC** current mode ASIC.
  - **8 Inputs:** 8 Single Ended (POS/NEG), 4 differential and summation (POS/NEG) in 2 clusters of 4 channels.
  - **3 Output modes:** (1) SLVS; (2) CMOS; and (3) Analog.
  - Active analog summation of up to 4 SE channels to improve time resolution

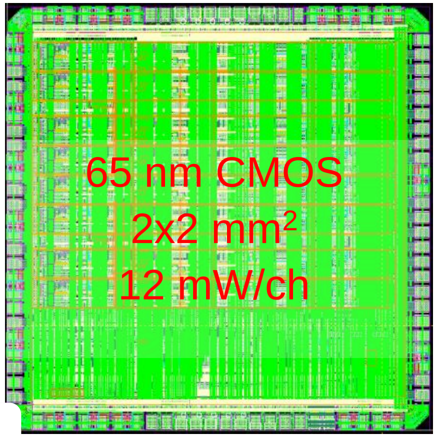
- **Fast current mode input stage**
- **Current mode comparator for timing**



Input stage "amplifier" < 3 mW/ch



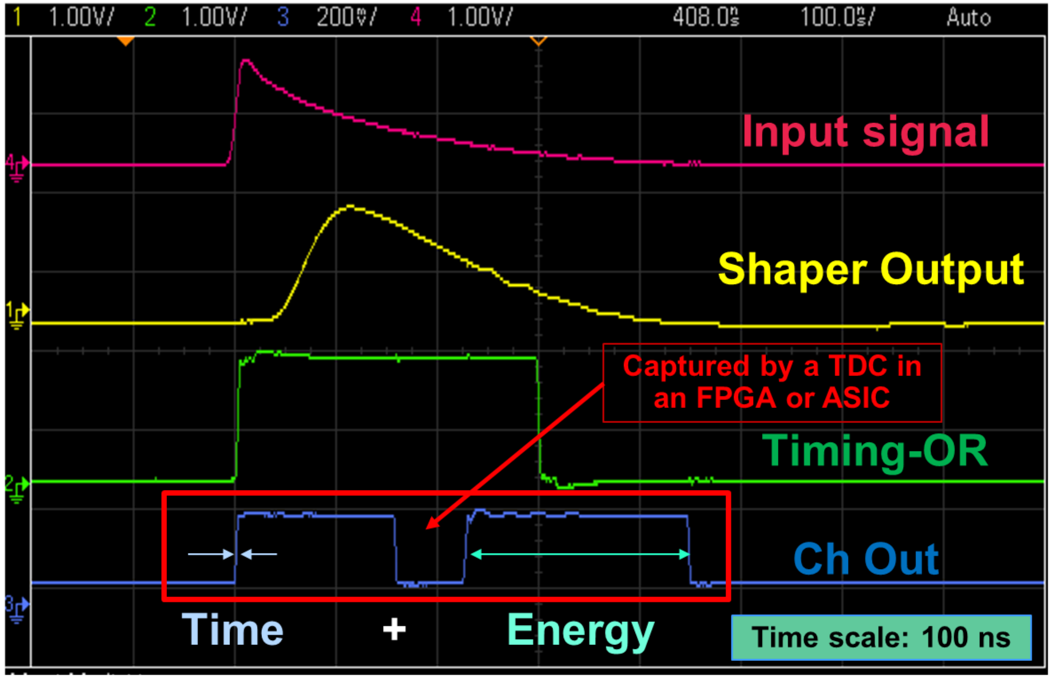
Based on HRFlexToT ASIC [1]



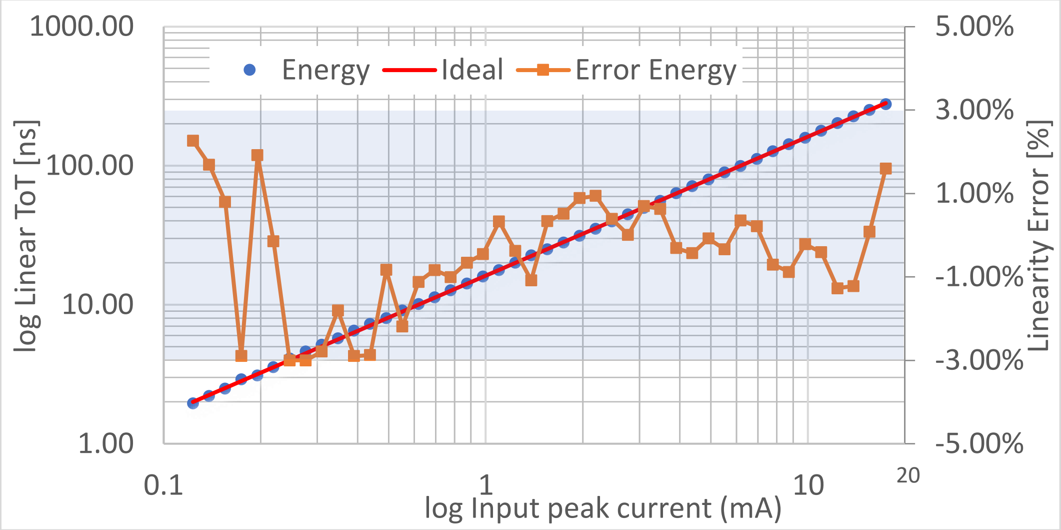
Collaboration of the ICCUB (Univ. Barcelona) and CERN-MIC

II. FastIC: Linearity of the Energy measurement

- **FastIC** provides a measurement of the **time** and **energy** per channel in two consecutive pulses
  - Based on HRFlexToT ASIC [1]
  - Linear energy by pulse width encoding
    - "Wilkinson ADC-like" conversion
    - Controlled by on-chip state machine



- Linearity error is **below 3%**
  - Saturation is reached at 25 mA of input current.
  - Other operating modes (negative, differential and summation) behaves similarly with a low linearity error.

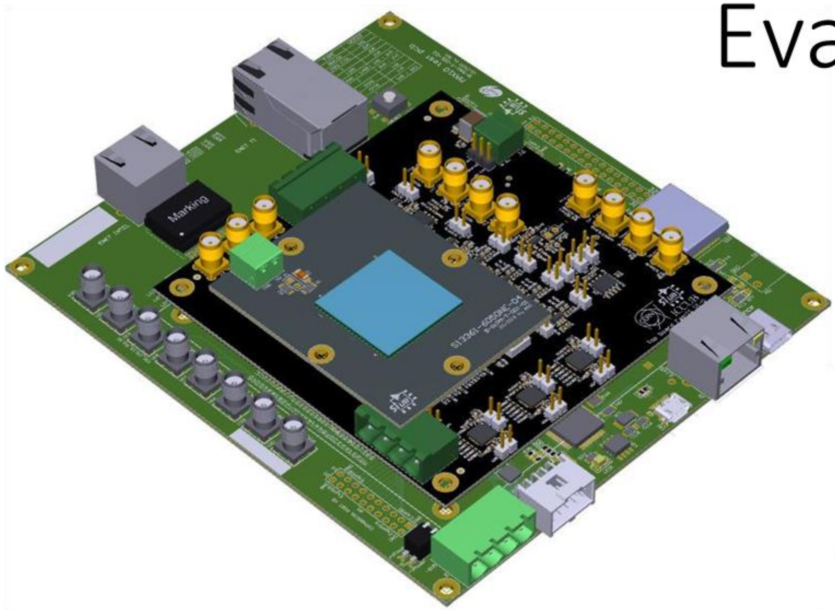


- **This makes FastIC suitable to different detectors: LYSO/LSO, BGO, Cherenkov, Monolithic, etc**
- Different trigger modes, including cluster trigger for monolithic

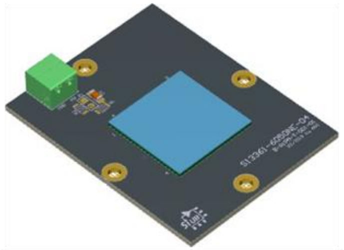
[1]: Sanchez, D., Gomez, S., et. al. HRFlexToT: A High Dynamic Range ASIC for Time-of-Flight Positron Emission Tomography, 2021, IEEE TRPMS, https://doi.org/10.1109/TRPMS.2021.3066426

II. FastIC evaluation system

Evaluation system



- Aims of the evaluation system:
  - Basic operational test & debug ASIC functionalities
  - Initial electrical characterization and linearity analysis.
  - Initial benchmark i.e. evaluate the FastIC chip by comparison
    - With respect previous designs (NINO, HRFlexTOT)
    - Using reference SiPM sensor:
      - Hamamatsu S13360-3050CS
      - FBK NUV-HD
  - Interface with other sensor based on adaptor board
  - Signal acquisition:
    - FPGA-based TDC (45ps time bin)
    - Differential sLVS link to external system



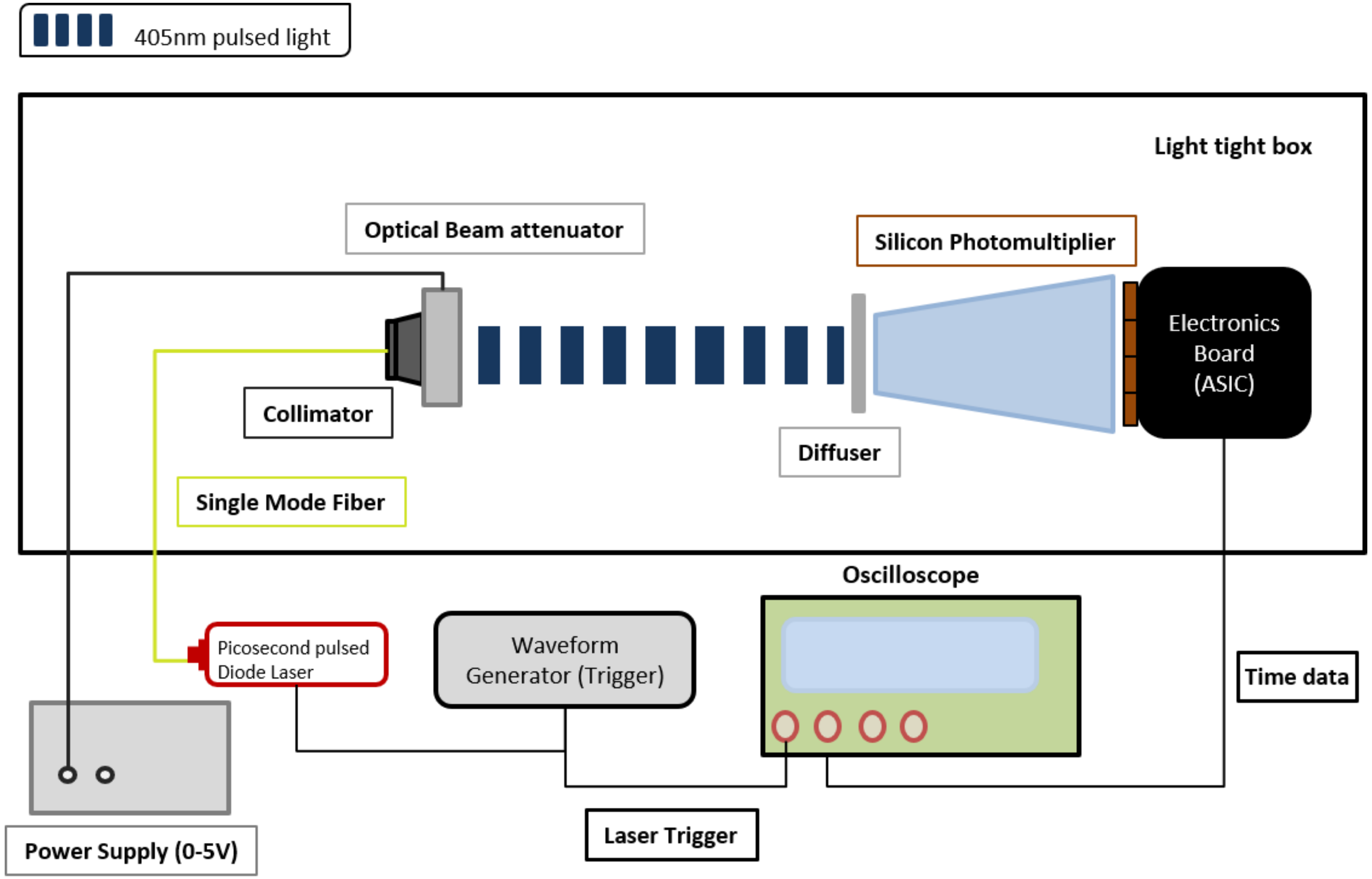
- Custom sensor board

- FastIC generic board
  - 2 FastICs on QFN64 (16 channels)
  - Reference SiPM sensors included
  - The board can be used stand alone

- FPGA board
  - FPGA board for slow control, acquisition and additional biasing.
  - Multichannel TDC is implemented in the FPGA (45ps time bin)

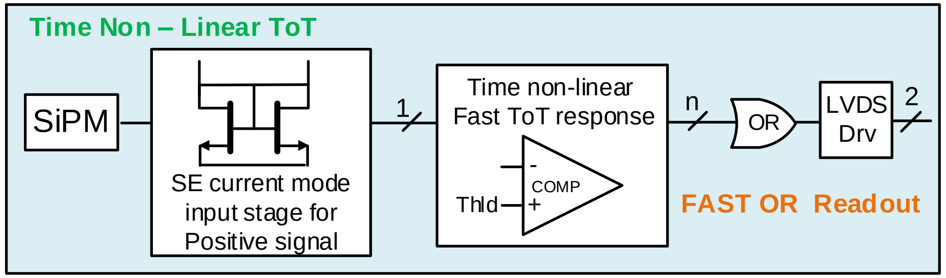
II. FastIC: SPTR measurements with SiPM and blue laser light

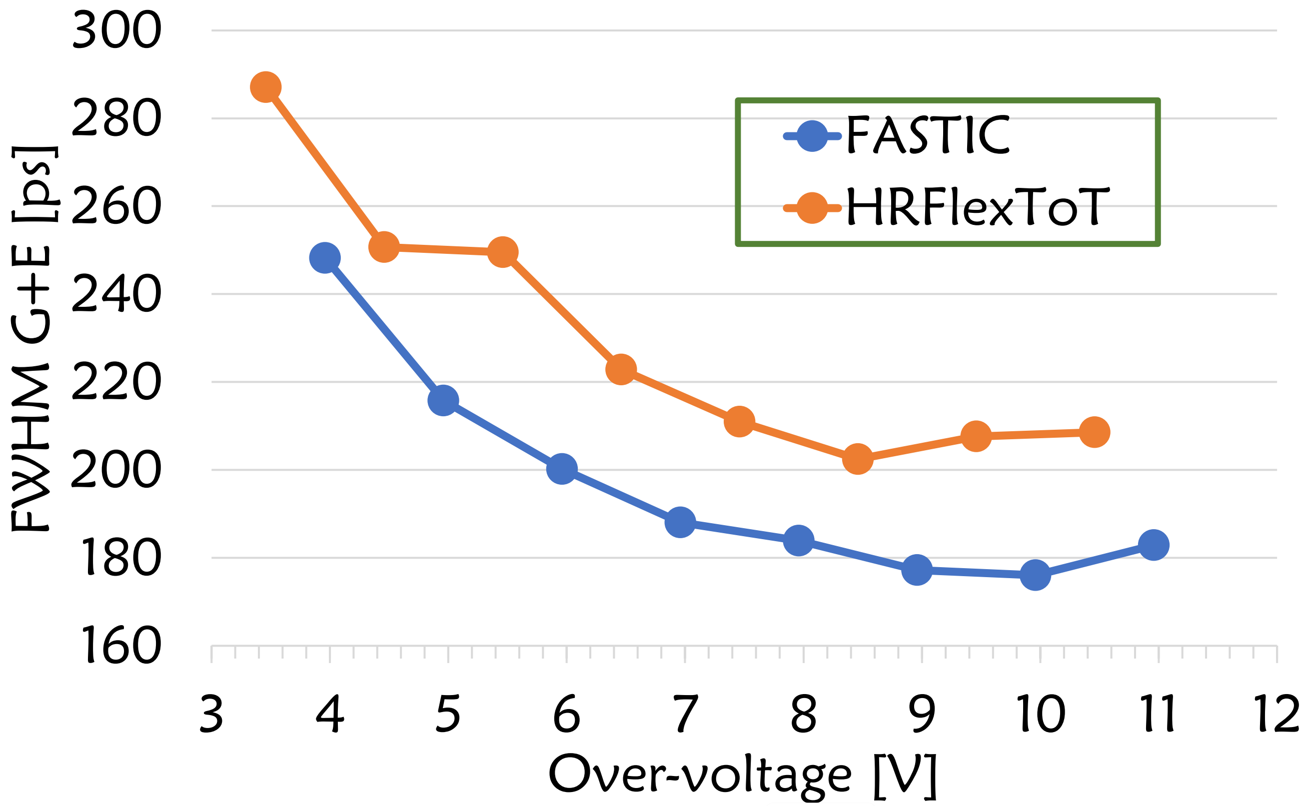
- **FASTIC** and **HRFlexToT** used for comparison.
- The setup is as follows:
  - Advanced Laser Diode Systems A.L.S. GmbH (PiL040X) at 405 nm and a tuned intensity level of 50%, jitter < 3 ps and < 45 ps pulse width .
  - **Sensor:** S13360-3050CS (Hamamatsu)
  - Agilent MSO 9404A 4 GHz oscilloscope (20 GS/s).
  - Several measurements are performed to identify the optimal threshold.



II. Performance: SPTR measurements with SiPM and blue laser light

- **Sensor:** HPK S13360-3050CS
- Results are obtained by performing a Gaussian plus an exponential fit of the delay histogram.
    - *Best SPTR **FASTIC**: 176,03 ps*
    - Best SPTR **HRFlexToT**: 202,05 ps





II. FastIC performance: CTR with scintillation light.

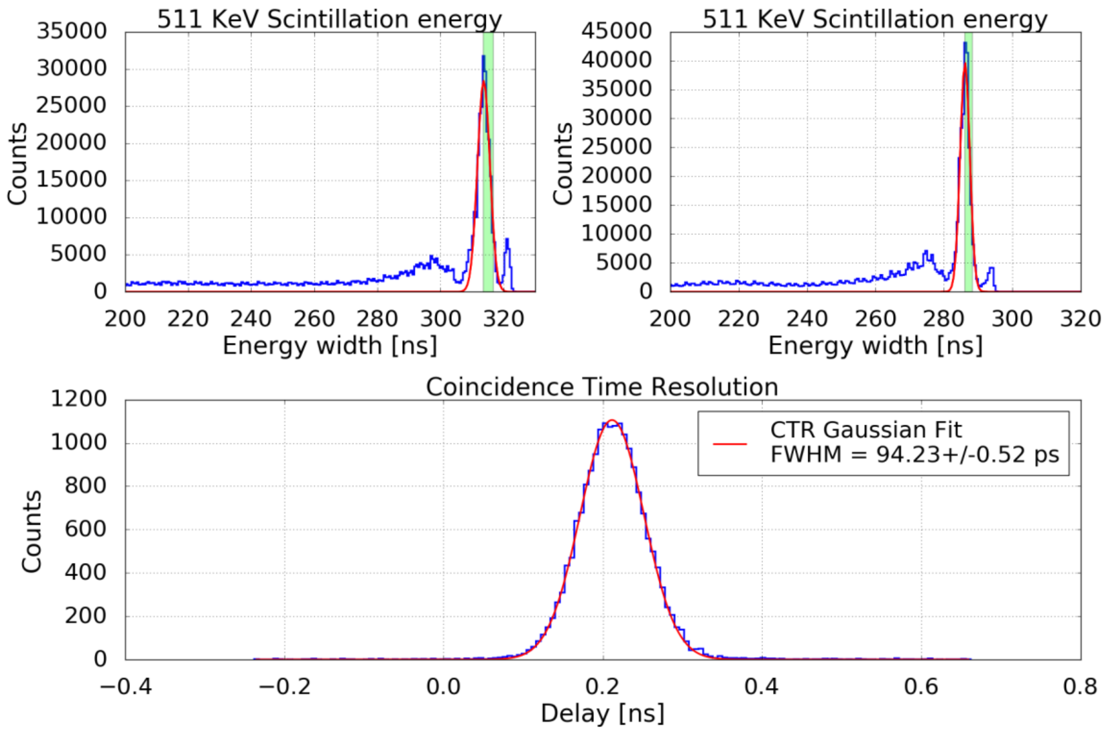
- **Sensor:** HPK S13360-3050PE 3x3mm^2, 50μm pixel pitch.
- **Crystal:** LSO:Ce Ca 0.2% of 2x2x3 mm³.
- **Coupling**: Melmount Glue
- Positive Readout.

FWHM = 94 ps

- Measurements using HPK S13360-3050VE and S14160-3050HS both of 3x3mm^2 and 50μm pixel pitch gives **similar** results

- Measurements using **HPK S14160-3050HS** 3x3mm^2, 50μm pixel pitch and the **negative** input polarity gives **similar** results

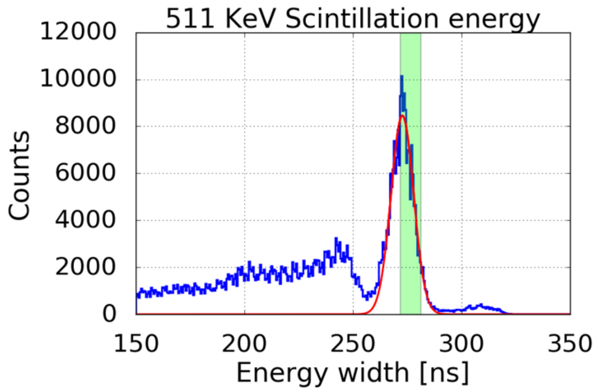
- For 1 sigma around 19 K events are selected.

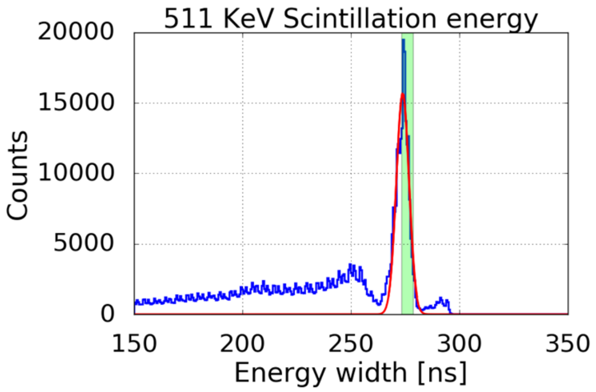


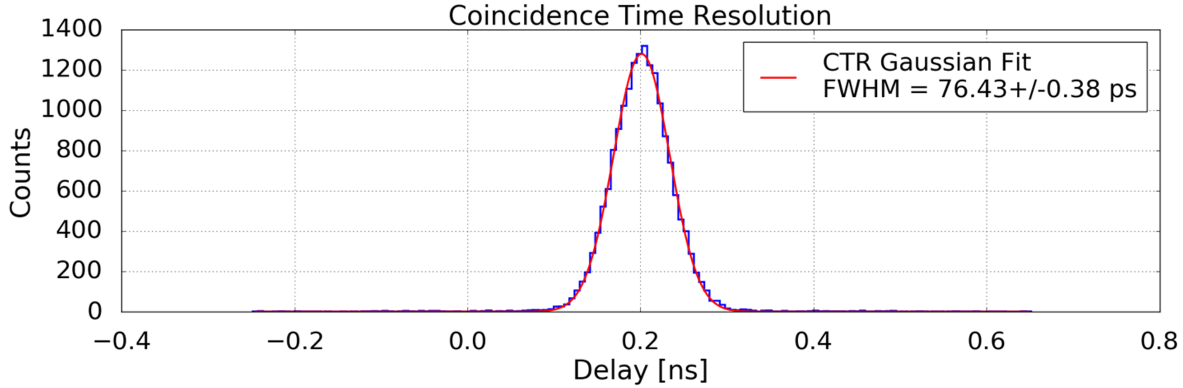
FastIC **Bias voltage 60.0 V (~7 V of Over-voltage)**

II. FastIC performance: CTR with scintillation light.

- **Sensor:** FBK-NUVHDLFv2b 3x3 mm², 40 pixel pitch.
- **Crystal:** LSO:Ce Ca 0.2% of 2x2x3 mm³.





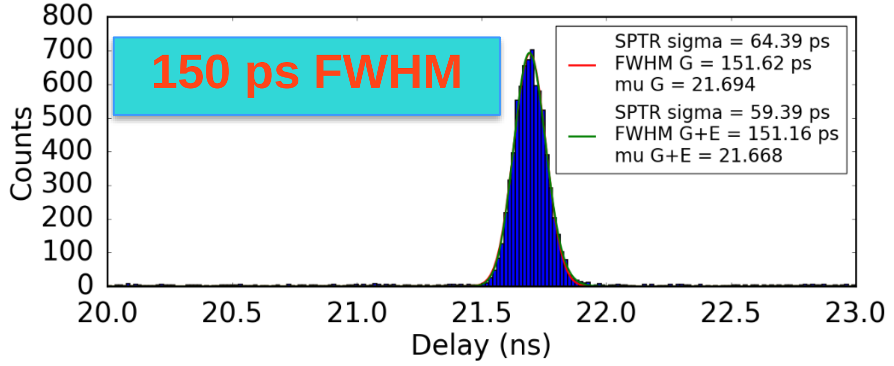


FWHM = 76 ps

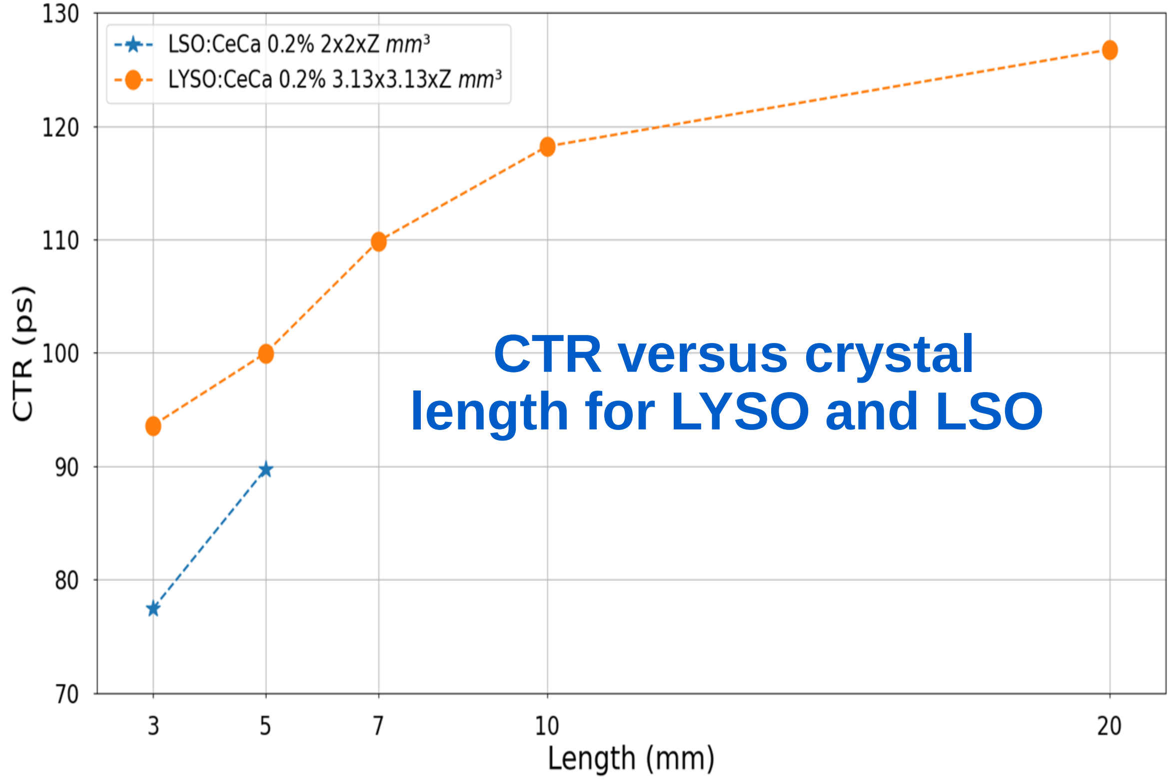
Input "amplifier" < 3 mW/ch

Complete signal processing < 12 mW/ch

- **SPTR with** FBK-NUVHDLFv2b 3x3 mm²



150 ps FWHM



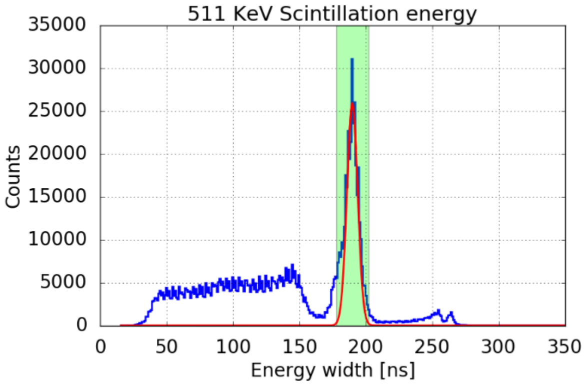
CTR versus crystal length for LYSO and LSO

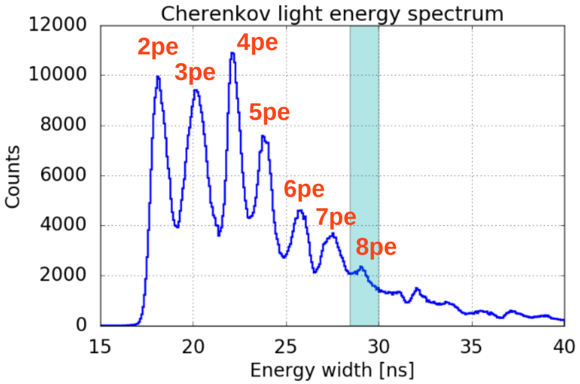
II. FastIC: CTR measurements with Cherenkov Light

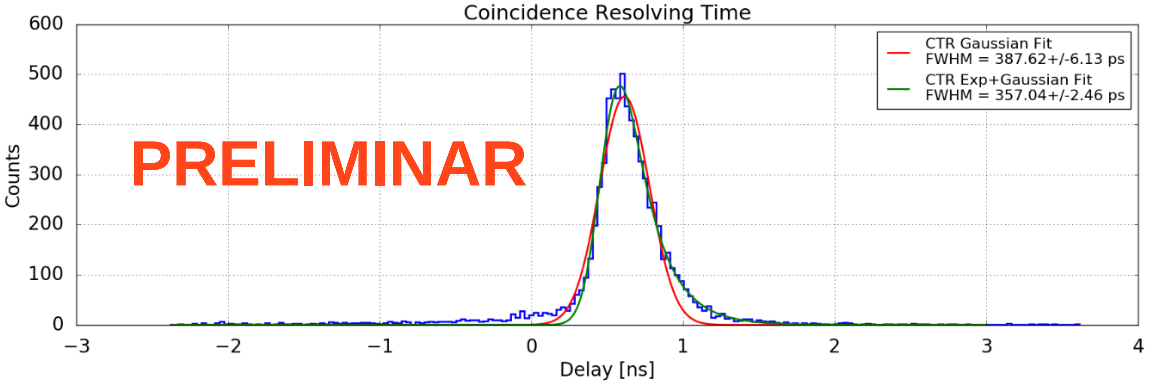
- Preliminary evaluation of the FastIC performance for Cherenkov radiation detection
  - **Sensor**: HPK S13360-3050CS 3x3mm^2, 50$\mu\mathrm{m}$ pixel pitch.
  - **Reference Crystal:** LSO:Ce Ca 0.2% of 2x2x5mm³ with a DTR of ~90 ps FWHM.
  - **Cherenkov Radiator:** TlBr of 3x3x5mm³.

- **Experimental setup is not optimized**. Coupling was done one month before the measurement and crystals were not properly aligned.
- Time resolution improves as we detect a larger number of photons.
- The CTR obtained is similar the one obtained in [2] but using a **feasible readout** for a scanner.

* Measurements done in collaboration with G. Ariño (UCDavis).







FASTIC **Bias voltage 58V (5V of Over-voltage)**

FWHM = ~357 ps

At least, 10 K events in coincidence are employed

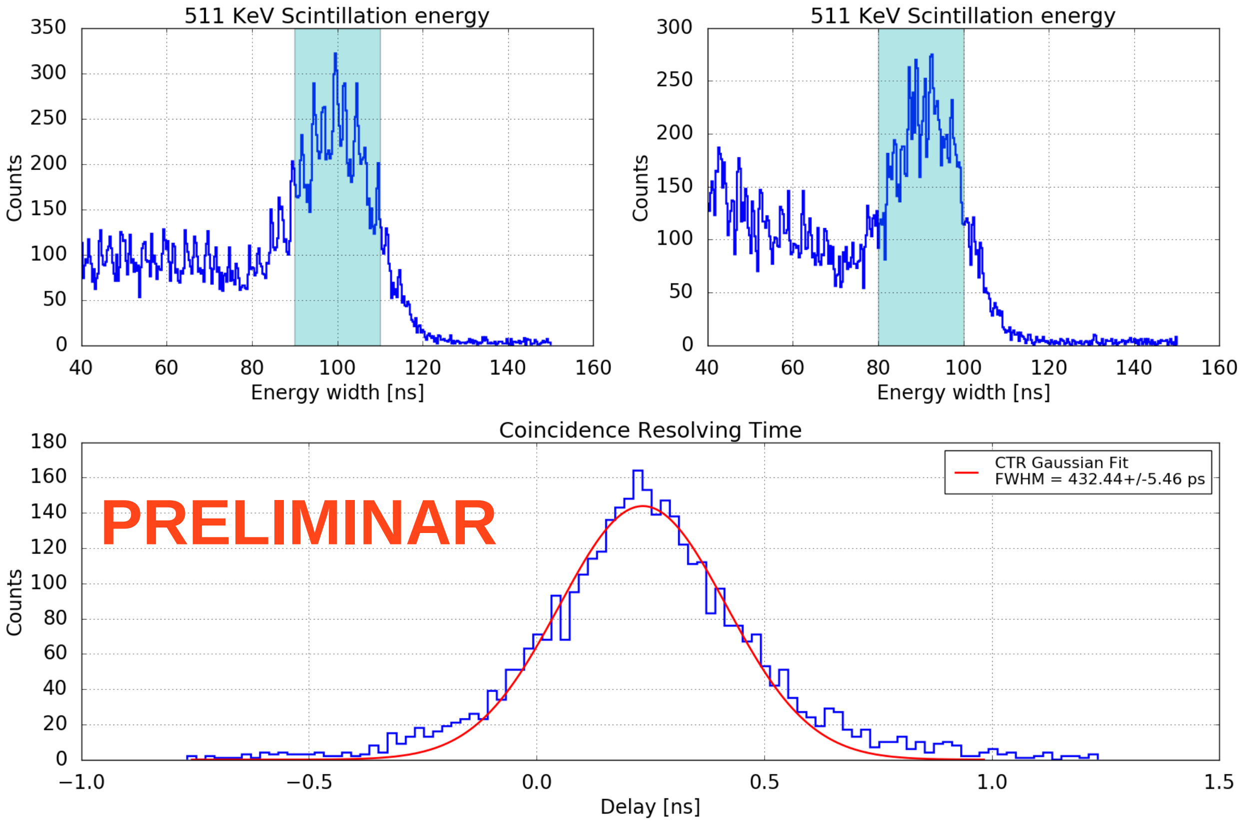
[2] Arino-Estrada, G., Roncali, E., et. al. Study of Čerenkov Light Emission in the Semiconductors TlBr and TlCl for TOF-PET. IEEE TRPMS. https://doi.org/10.1109/trpms.2020.3024032

II. FastIC performance: CTR with scintillation light: BGO

- **Sensor:** HPK S13360-3050PE 3x3mm^2, 50μm pixel pitch.
- **Crystal:** BGO of 2x2x3 mm³.

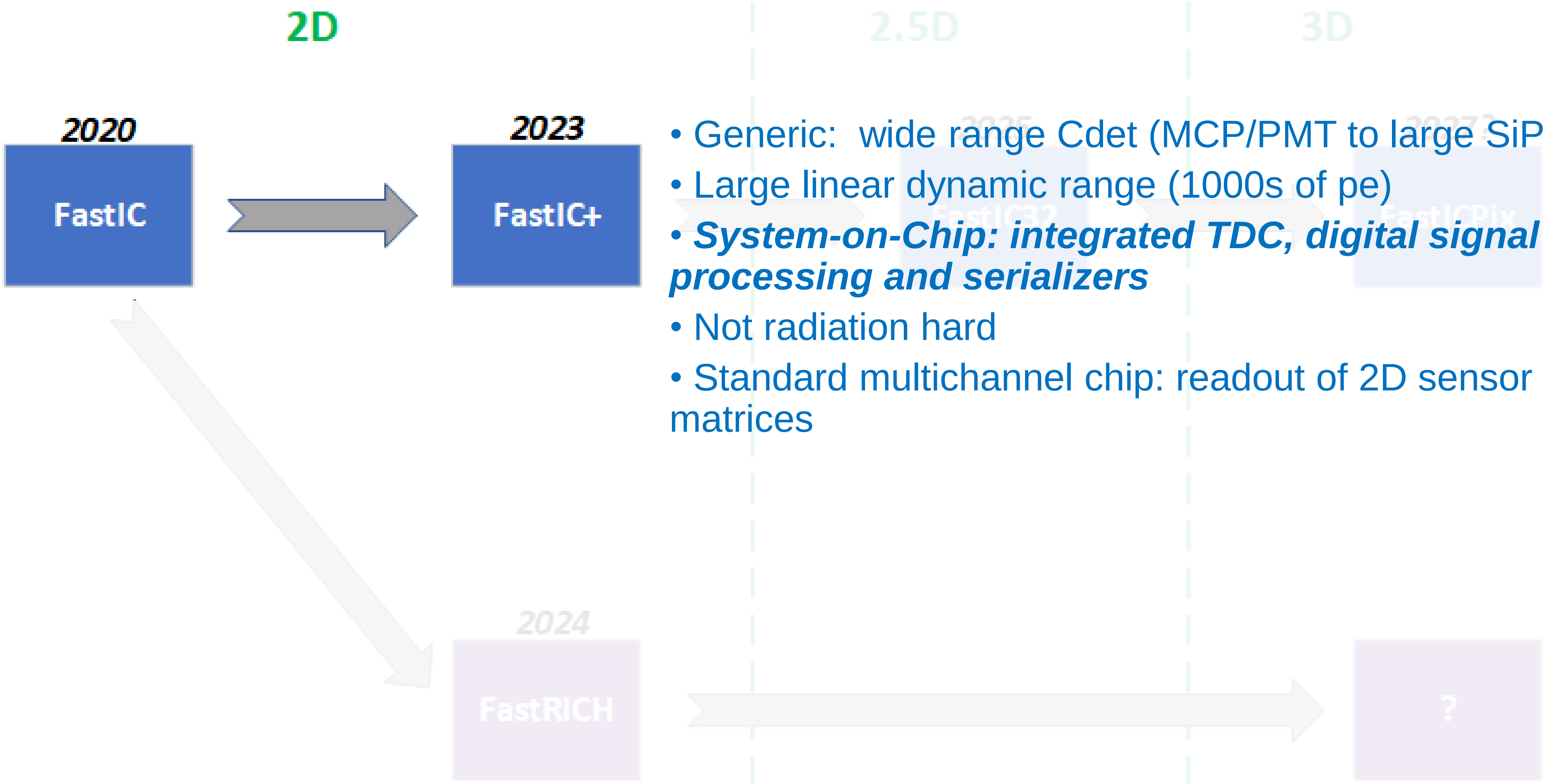
FWHM = 432.44 ps

FastIC Bias voltage 60.0 V (~7 V of Over-voltage)



- Ongoing measurements with FBK's NUV-HD-MT suggest that:
  - CTR < 300 ps for BGO of 2x2x3 mm³
  - CTR < 450 ps for BGO of 2x2x20 mm³

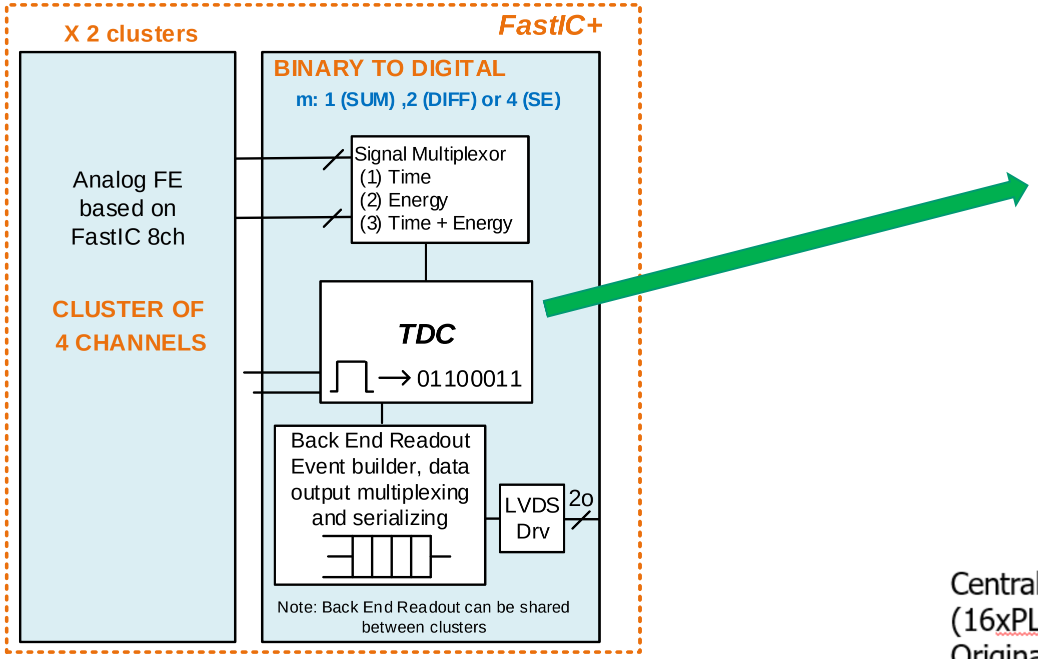
III. FastIC+



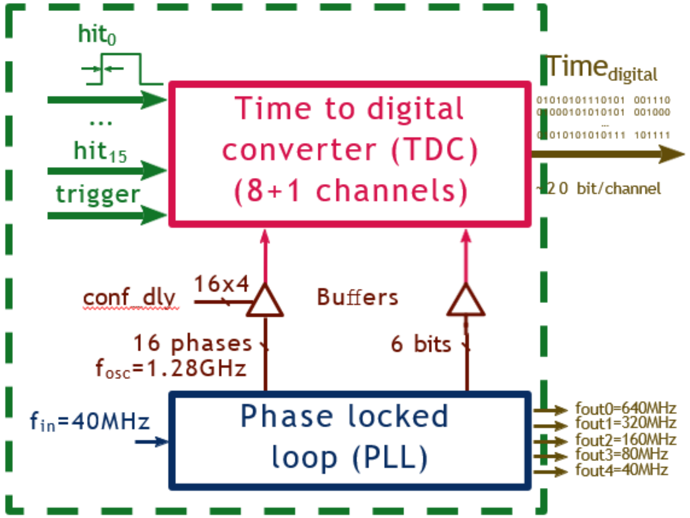
- Generic: wide range Cdet (MCP/PMT to large SiPMs)
- Large linear dynamic range (1000s of pe)
- ***System-on-Chip: integrated TDC, digital signal processing and serializers***
- Not radiation hard
- Standard multichannel chip: readout of 2D sensor matrices

III. FastIC+

- FastIC+: integration of 25 ps bin TDC on FastIC
  - Scheduled for Q3 2023
  - TDC readout core reads pulses from Time + Engergy multiplexer.
  - Digital ToA+ToT is captured, encoded and serialized.
  - Digitized data is sent through dedicated pads (SLVS).

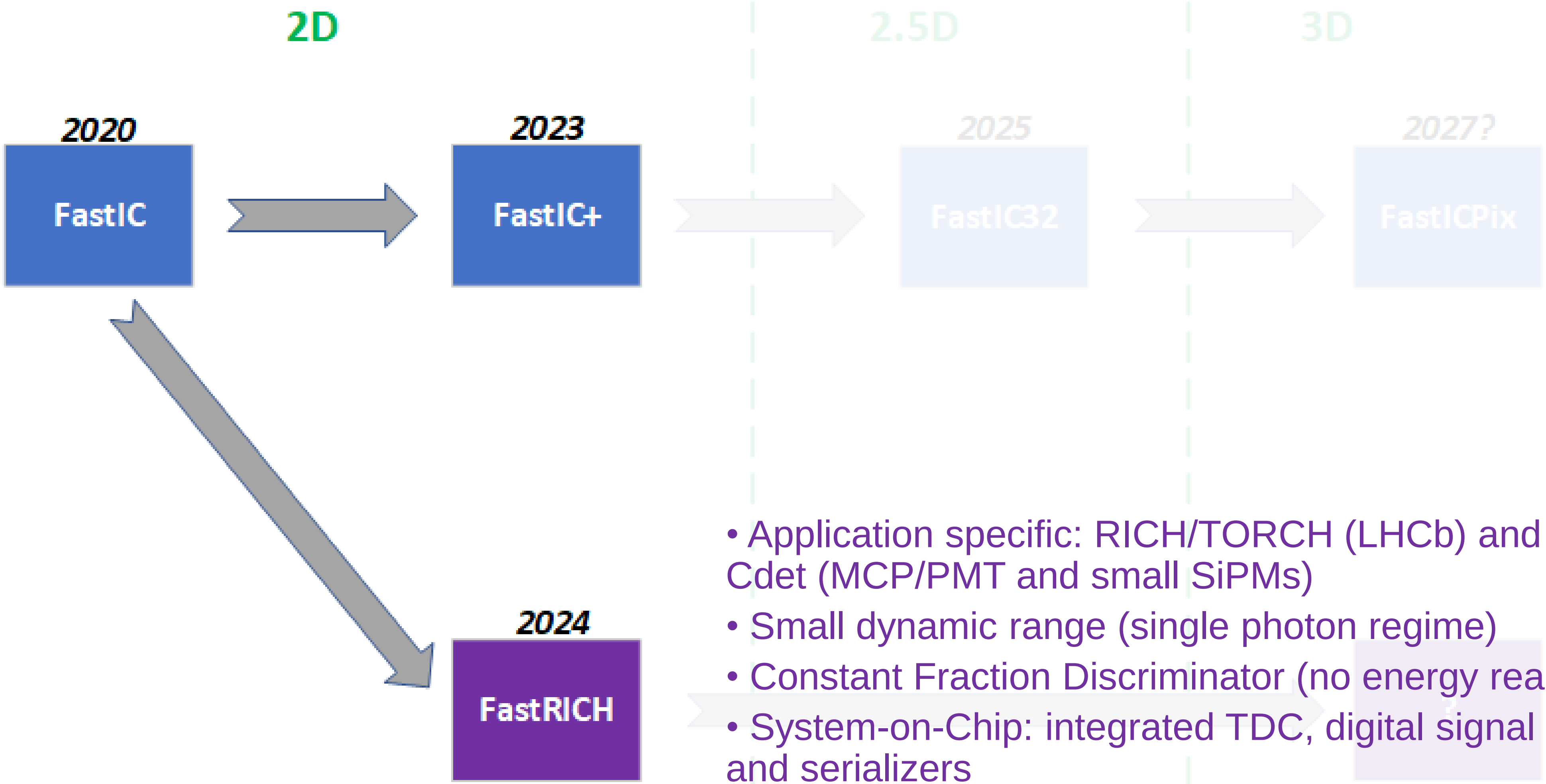


Central timing block



Central timing block diagram. The PLL provides the fine (16xPLL/VCO phases) and coarse (6xPLL/freq. div. phases) bits. Original idea: J. Christiansen (CERN).

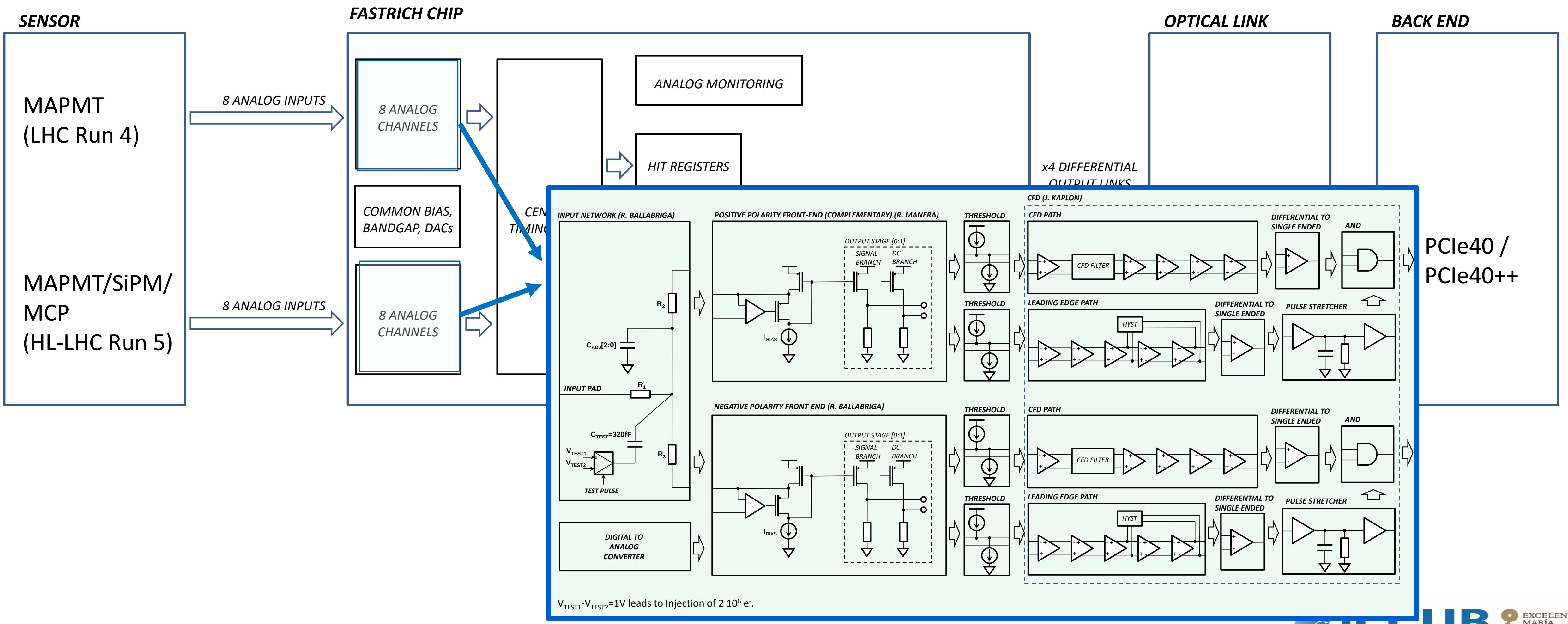
IV. FastRICH



- Application specific: RICH/TORCH (LHCb) and PID: small Cdet (MCP/PMT and small SiPMs)
- Small dynamic range (single photon regime)
- Constant Fraction Discriminator (no energy readout needed)
- System-on-Chip: integrated TDC, digital signal processing and serializers
- Radiation hard
- Standard multichannel chip: readout of 2D sensor matrices

IV. FastRICH

- FastRICH block diagram



SENSOR

MAPMT
(LHC Run 4)

MAPMT/SiPM/
MCP
(HL-LHC Run 5)

8 ANALOG INPUTS

8 ANALOG INPUTS

FASTRICH CHIP

8 ANALOG CHANNELS

COMMON BIAS, BANDGAP, DACs

8 ANALOG CHANNELS

CEN
TIMING

ANALOG MONITORING

HIT REGISTERS

x4 DIFFERENTIAL OUTPUT LINKS

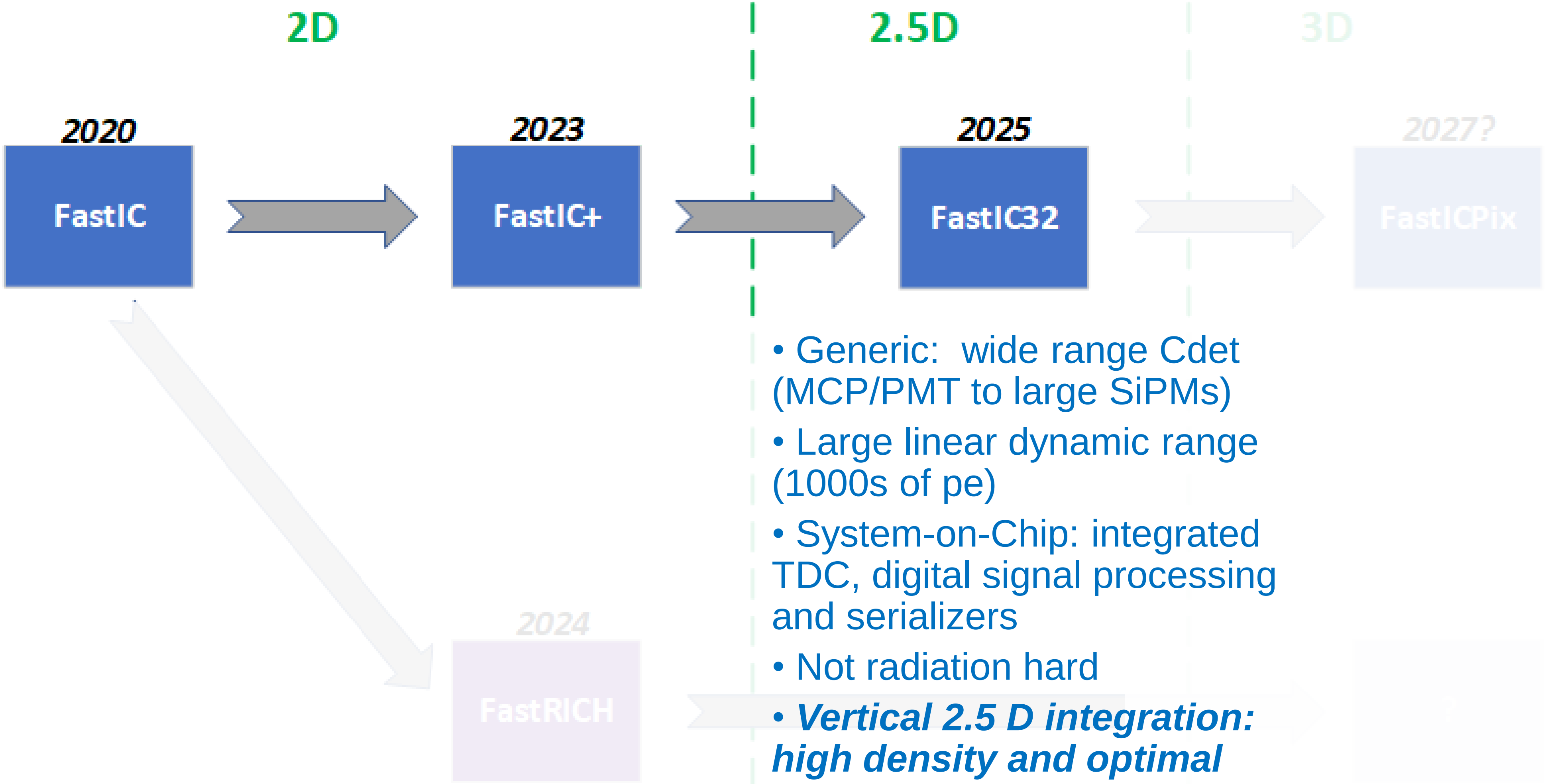
OPTICAL LINK

BACK END

PCIe40 /
PCIe40++

V_{TEST1}-V_{TEST2}=1V leads to Injection of 2 10^6 e^-.

V. FastIC32



2D | 2.5D | 3D

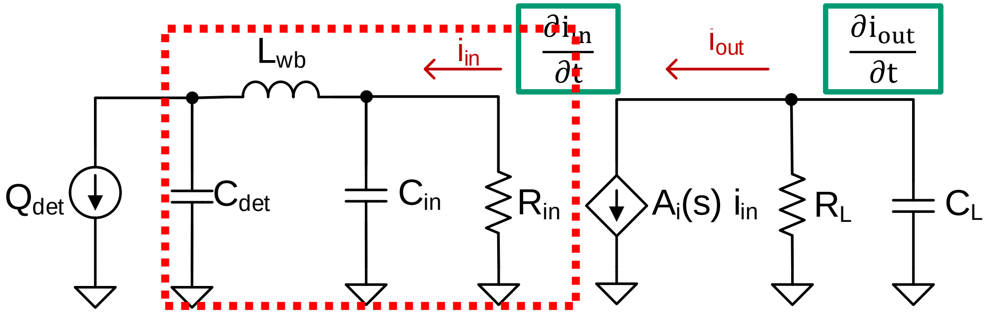
2020 FastIC → 2023 FastIC+ → 2025 FastIC32 → 2027? FastICPix

2024 FastRICH

- Generic: wide range Cdet (MCP/PMT to large SiPMs)
- Large linear dynamic range (1000s of pe)
- System-on-Chip: integrated TDC, digital signal processing and serializers
- Not radiation hard
- ***Vertical 2.5 D integration: high density and optimal interconnect***

V. FastIC32: Effect of interconnects (inductance)

Additional poles from parasitics $\approx \frac{3}{2\pi\sqrt{L\,C_{det}}}$



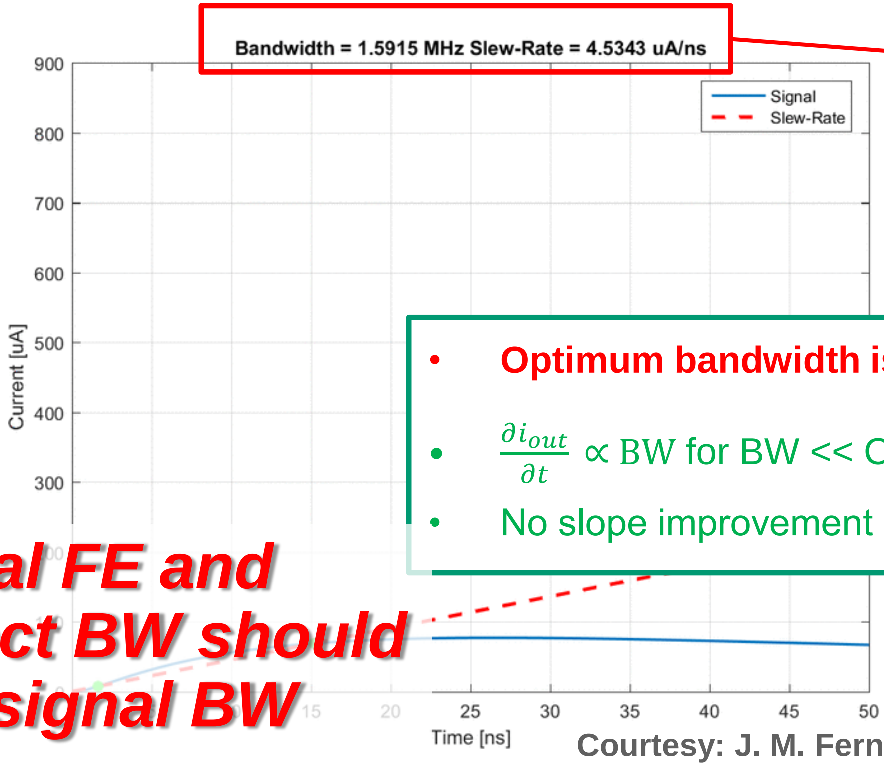
Optimum bandwidth for connecting inductances 5 nH – 25 nH and Cdet = 10 pF – 1 nF

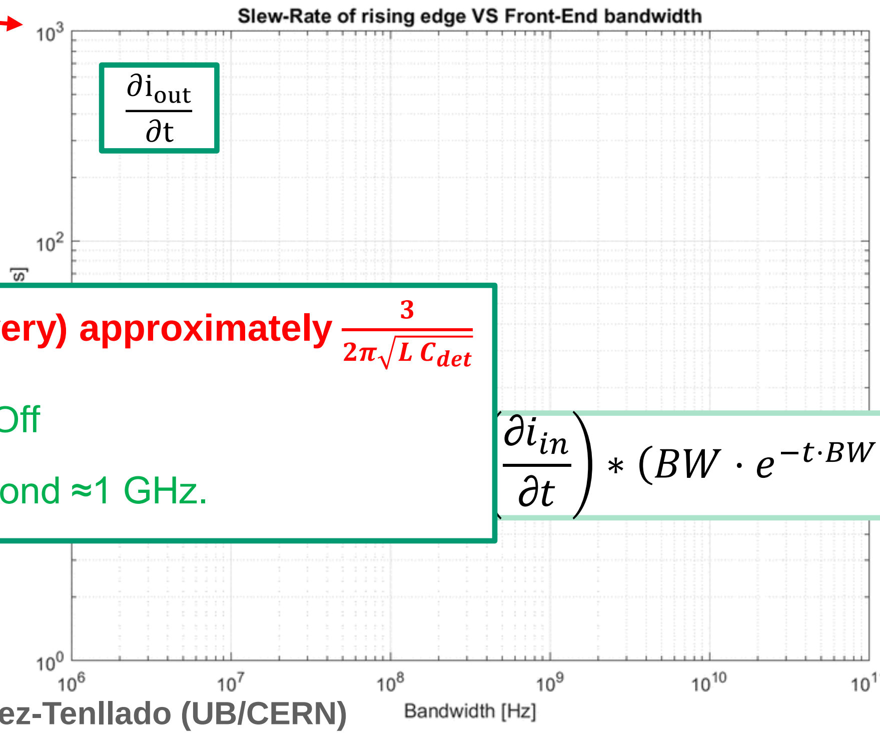
Lwb / Cdet

5 nH / 10 pF	5 nH / 1 nF	25 nH / 10 pF	25 nH / 1 nF
1.3 GHz	270 MHz	560 MHz	81 MHz

J. M. Fernández-Tenllado, et alt, "Optimal design of single-photon sensor front-end electronics for fast-timing applications," IEEE NSS/MIC 2019, doi: 10.1109/NSS/MIC42101.2019.9059805.

See also:Sensors 2020, 20(16), 4428; https://doi.org/10.3390/s20164428





- **Optimum bandwidth is (very) approximately $\frac{3}{2\pi\sqrt{L\,C_{det}}}$**
- $\frac{\partial i_{out}}{\partial t} \propto$ BW for BW << Cut-Off
- No slope improvement beyond ≈1 GHz.

$$\left(\frac{\partial i_{in}}{\partial t}\right) * \left(BW \cdot e^{-t\cdot BW}\right)$$

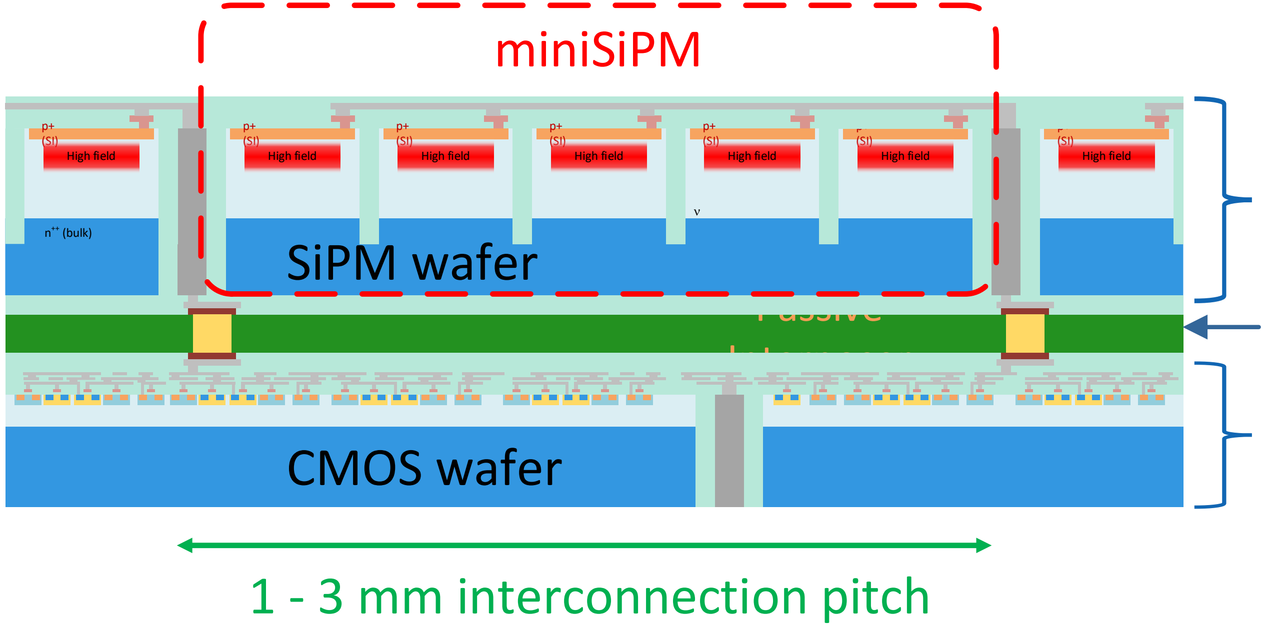
Optimal FE and interconnect BW should match signal BW

Courtesy: J. M. Fernandez-Tenllado (UB/CERN)

UB Sciences
EXCELENCIA MARÍA DE MAEZTU

V. FastIC32: a hybrid photosensor

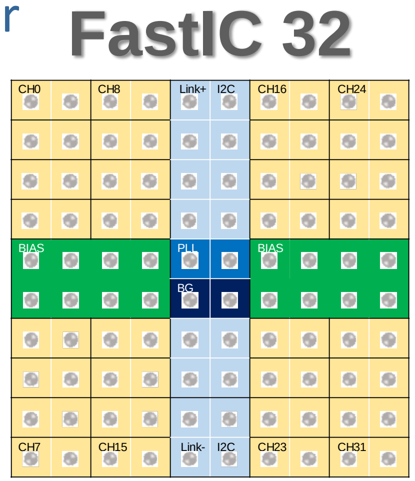
- 2.5D and 3D Integration
  - Photon Detection Module (PDM) in which SiPMs with TSVs down to 1 mm pitch
  - Connected to the readout ASIC on the opposite side of a passive interposer



SiPM array

PCB Interposer

FEE ASIC

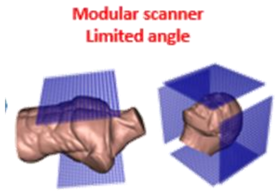


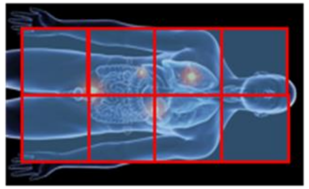
Integrated Photon Detection Module

Hybrid SiPM module being developed for ultimate timing performance in ToF-PET

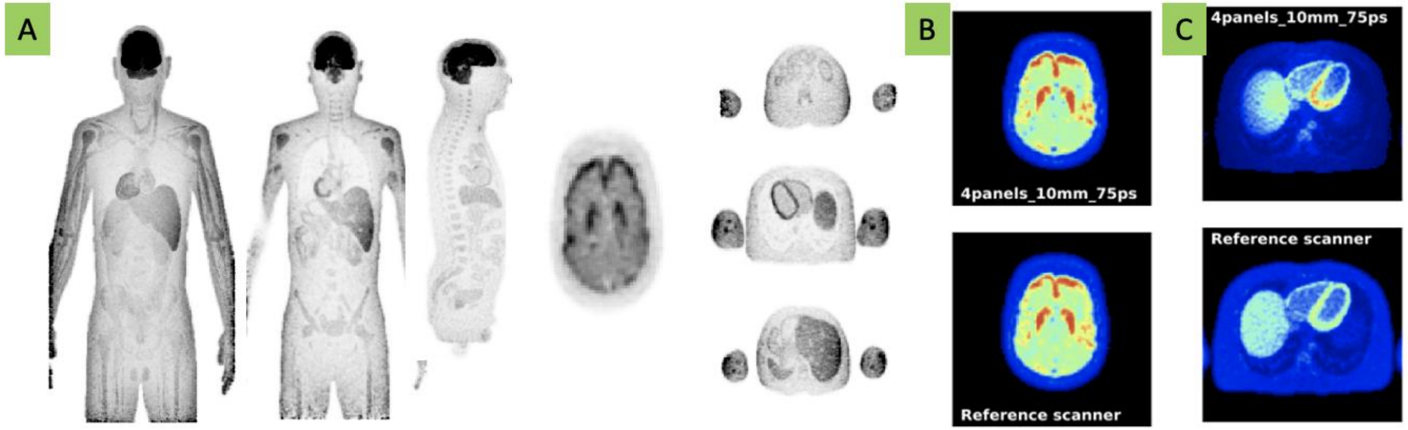
V. FastIC32: PETVision

- The **PETVision** Project was approved. Call: **Horizon EIC 2022 Pathfinder-open**.
    - 5-year project starting in September 2023
- The aim of PetVision is to leverage on 3D / 2.5D integration techniques to build a modular ToF-PET scanner, with next-generation performance and affordable cost.



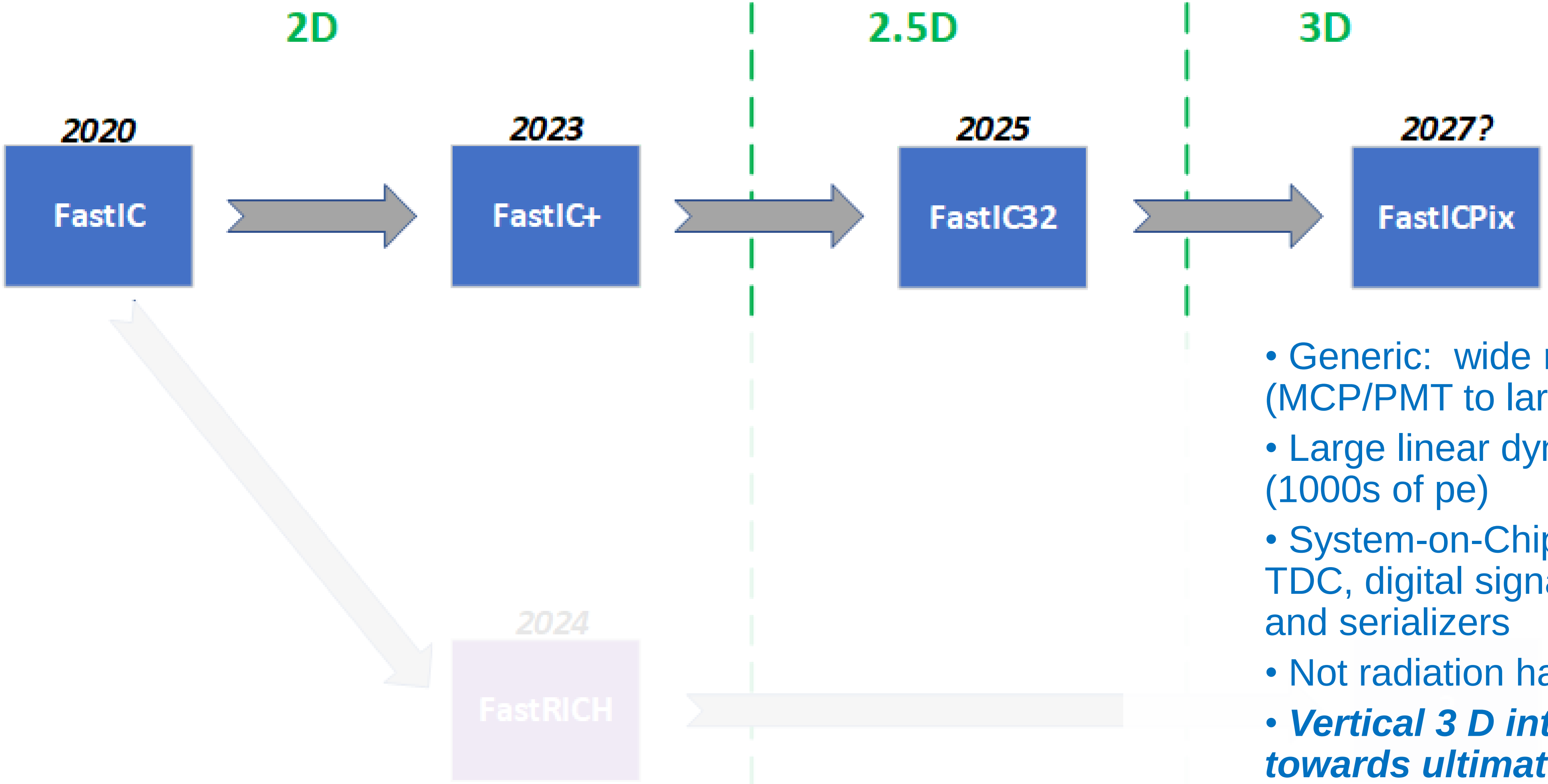


Partner	PI	Country
JSI	Rok Pestotnik	SI
FBK	Alberto Gola	IT
ICCUB	David Gascon	ES
Oncovision	Jorge Alamo	ES
CSIC	Jose Maria Bennloch	ES
TUM-MED	Wolfgang Weber	DE
MGH	Georges El Fakhri	USA



Simulation of the capability of the proposed planar TOF PET imager: Reconstructed Image (3mm slices) of an XCAT digital phantom acquired by two 120x60cm^2 panel detectors (above and below the patient) assuming 100 ps TOF resolution and 10 mm scintillator thickness (A) and with small 4 panel system used to image head (B) and torso (C)

VI. FastICPix

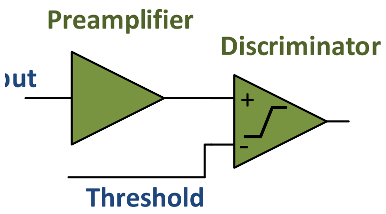


- Generic: wide range Cdet (MCP/PMT to large SiPMs)
- Large linear dynamic range (1000s of pe)
- System-on-Chip: integrated TDC, digital signal processing and serializers
- Not radiation hard
- ***Vertical 3 D integration: towards ultimate SPAD timing performance***

VI. How to improve the contribution of the electronics to the final timing?

- Contribution of the electronics to the timing resolution in a typical binary readout chain

$$\sigma_{t\_el}^{2} = \left(\sigma_{t\_el}^{TW}\right)^2 + \left(\sigma_{t\_el}^{Jit}\right)^2 + \left(\sigma_{t\_el}^{TDC}\right)^2 = \left(\left[\frac{t_r V_{th}}{S}\right]_{RMS}\right)^2 + \left(\frac{N}{dS/dt}\right)^2 + \left(\frac{TDC_{Bin}}{\sqrt{12}}\right)^2 + \ldots$$



- Electronic jitter $\boldsymbol{\sigma_{t\_el}^{Jit}}$ depends on noise and signal slew rate
- When the signal formation in the detector (t_d) is much fast than the detector time constant and the series noise (e_n) dominates and for the optimal FE BW

$$\boldsymbol{\sigma_{t\_el}^{Jit}} = \frac{N}{dS/dt} \approx \boldsymbol{\frac{e_n C_{DET}\sqrt{t_d}}{Q}}$$

C. De La Taille, Electronics Tutorial IEEE/NSS Manchester 2019

- Electronics noise e_n typically depends on transistor $g_m(I_d)$ → power

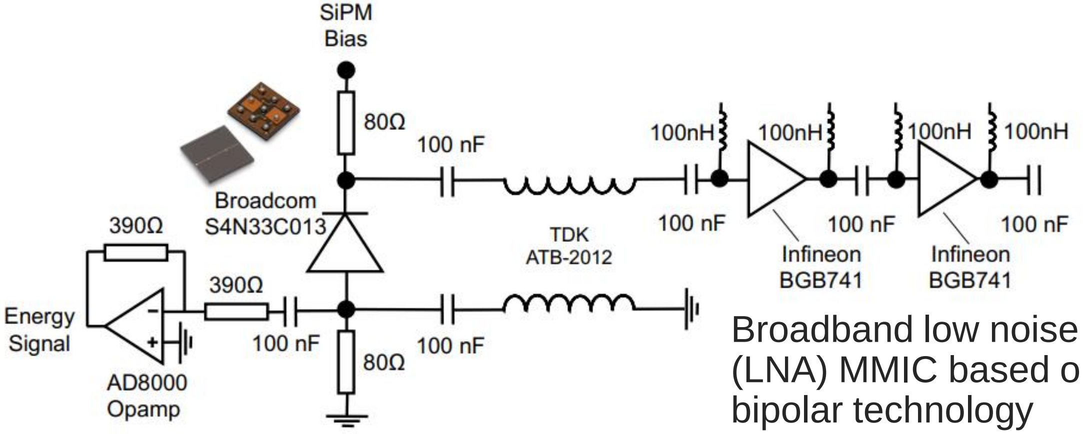
$$e_n = \sqrt{\frac{2kT}{g_m}} \approx \frac{2kT}{\sqrt{qI_d}}$$

- Therefore we can optimize electronics jitter contribution by:
  1) Increasing detector signal "temporal density" (increase $\boldsymbol{Q/\sqrt{t_d}}$): more signal and/or faster
  2) Burning more power (reduce e_n)
  3) Segmentation (reduce C_{DET})

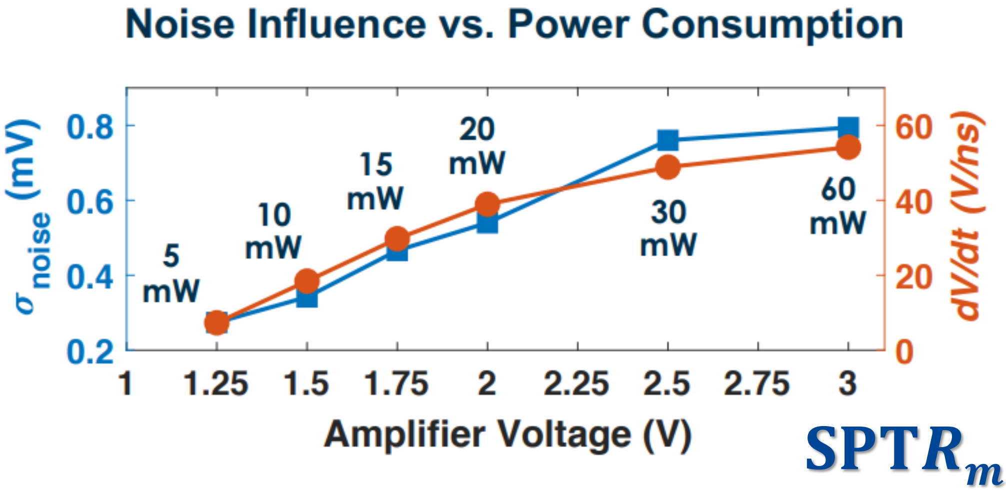
VI. How to improve timing? Power

Burning more power (improving FE) helps but has a limit…

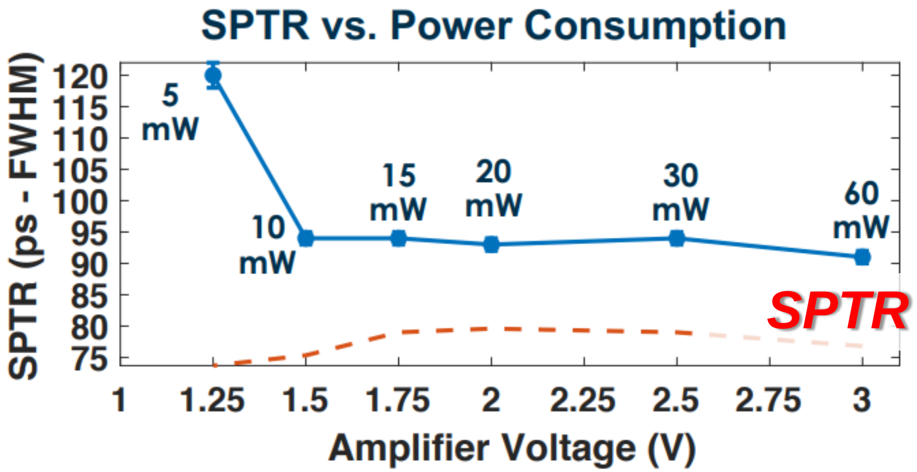
- 3x3 mm^2 SiPM readout by a discrete RF voltage amp
  - Path for timing with RF commercial components
  - Dedicated path for energy signal
  - SPTR versus power consumption



Broadband low noise amplifier (LNA) MMIC based on SiGe:C bipolar technology



$SPTR_{measured}$



SPTR > 90 ps

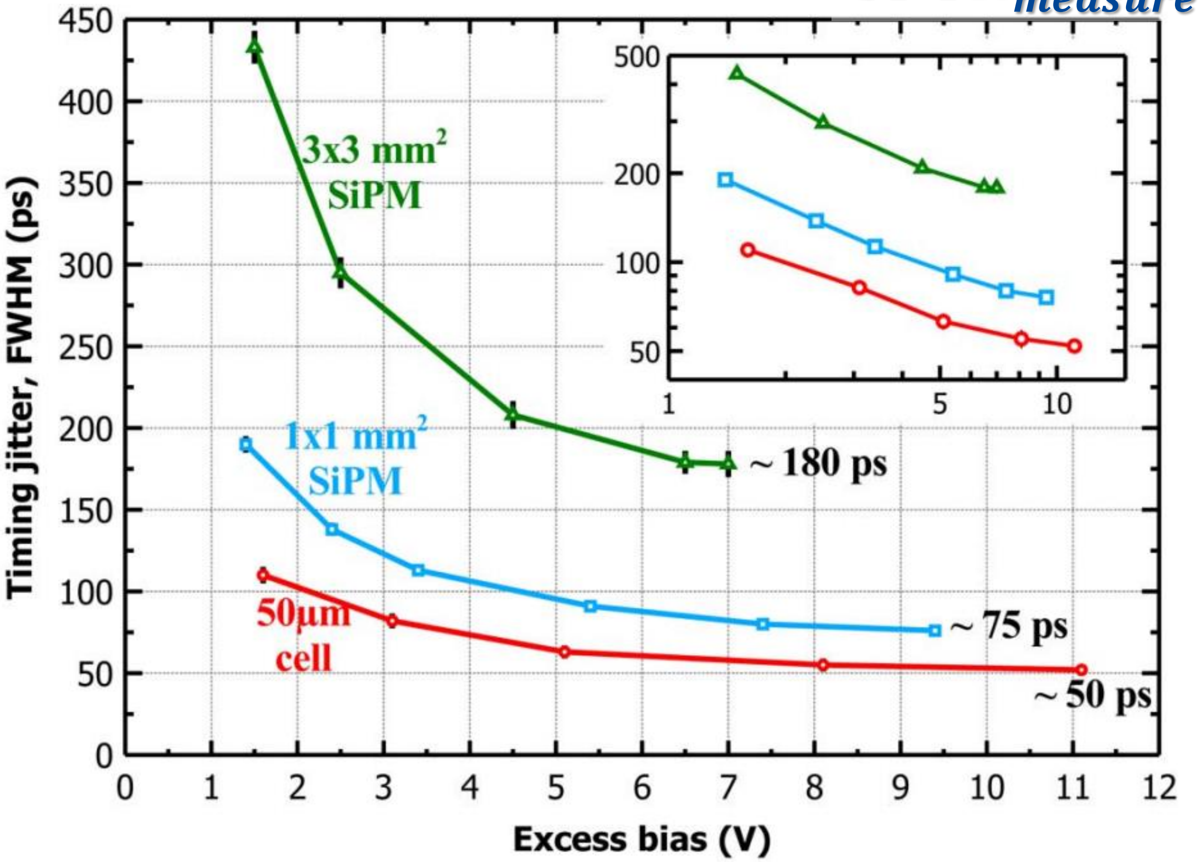
J. Cates, "Low Power Implementations of High Performance Electronic Readout to Advance TOF-PET Detector Module Performance", Fast Timing in Medical Imaging (FTMI) Workshop, Valencia, 2022

VI. How to reach the SPAD timing limit? Segmentation

SiPM technology is still far from the SPAD (microcell) SPTR limit

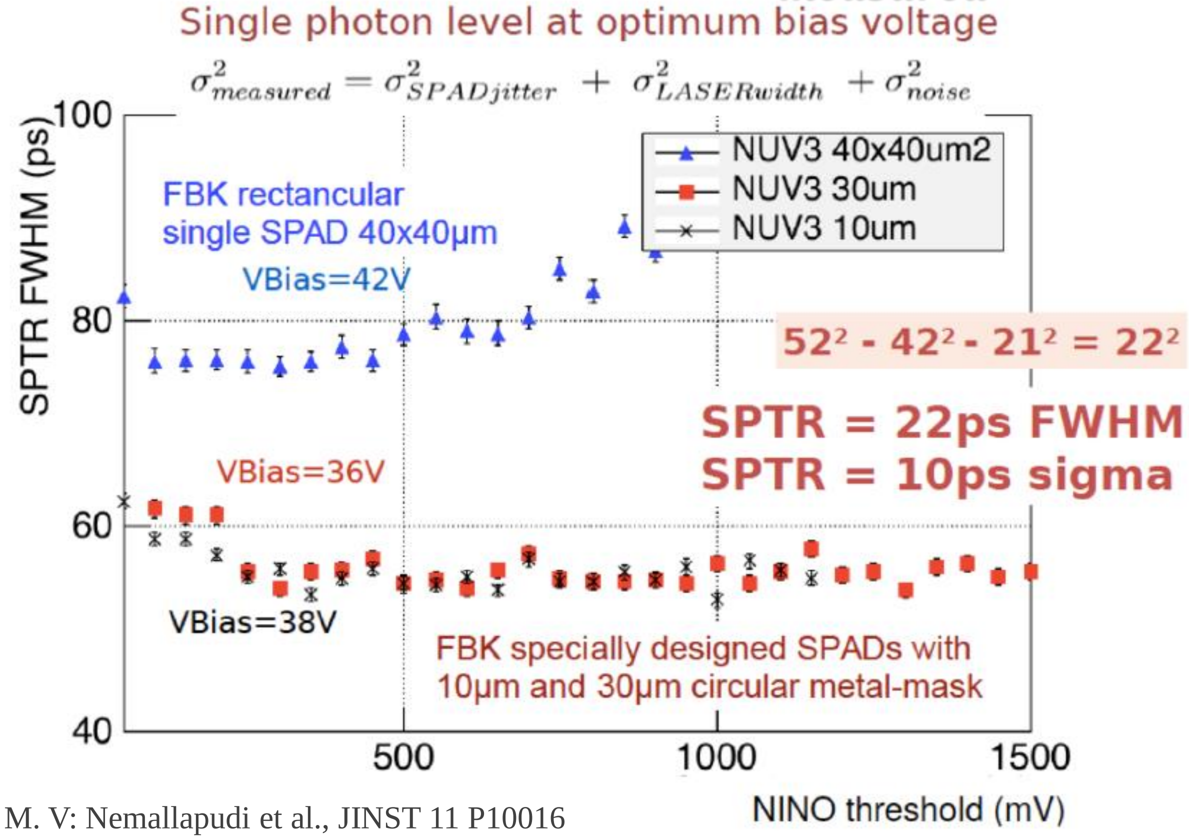
$$\mathrm{SPTR}_{measured} = \sqrt{SPTR^2_{sensor} + SPTR^2_{el} + Jit^2_{Laser}}$$

$\mathbf{SPTR}_{measured}$



F. Acerbi *et al.*, "Characterization of Single-Photon Time Resolution: From Single SPAD to Silicon Photomultiplier," in *IEEE Transactions on Nuclear Science*, vol. 61, no. 5, pp. 2678-2686, Oct. 2014.

$\mathbf{SPTR}_{measured}$



$52^2 - 42^2 - 21^2 = 22^2$

SPTR = 22ps FWHM
SPTR = 10ps sigma

M. V: Nemallapudi et al., JINST 11 P10016

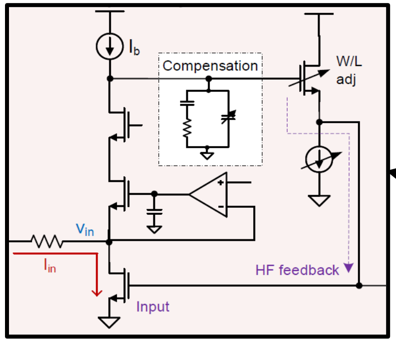
$$SPTR_{el} = \frac{e_n C_{DET}\sqrt{t_d}}{Q} \ll 1\,ps\ for\ single\ SPADs$$

VI. Segmentation

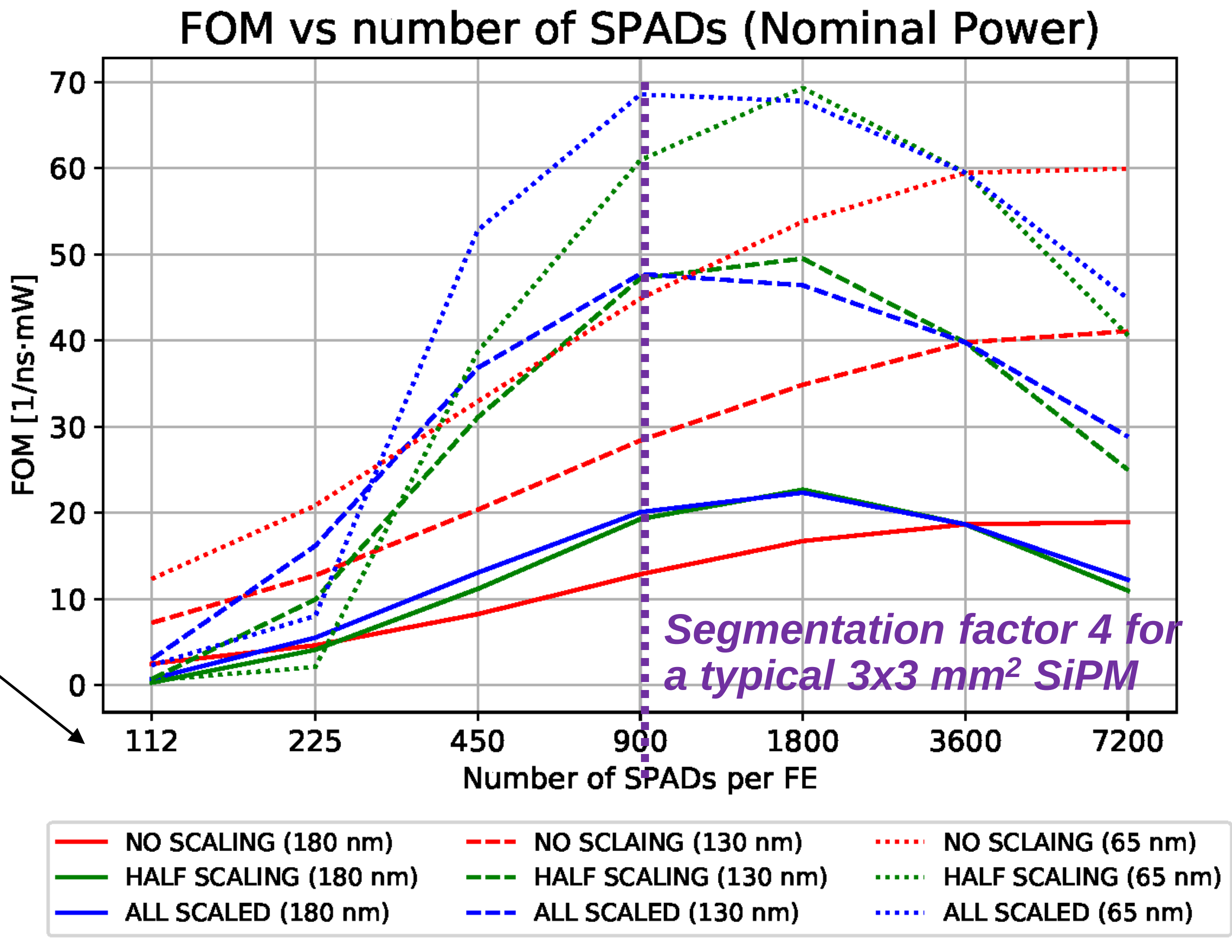
Segmentation is promising: but don't forget power !!!

1) What is the optimal segmentation for a given power budget?
   - $FOM = \frac{1}{Jitter \cdot Power \cdot 10^{12}} \left[\frac{1}{ns \cdot mW}\right]$
   - "Electronics noise" jitter for 1 firing cell

2) How does CMOS technology scaling impacts?
   - Compare: 180, 130 and 65 nm nodes



- *Typical 3x3 mm² SiPM*
- *3600 cells (50 um)*
- *Divided in groups of N SPADs*
- *Each group readout by FE*
- *Total power kept constant*



Segmentation factor 4 for a typical 3x3 mm² SiPM

Power required to achieve 10 ps "electronic noise" jitter with optimal segmentation for a 3x3 mm² SiPM?

- *180 nm: 10 mW*
- *130 nm: 3 mW*
- *65 nm: 2 mW*

R. Manera *et al*., "Study of Optimal Segmentation for Active Hybrid Single-Photon Sensors," *2021 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)*, Piscataway, NJ, USA, 2021, pp. 1-3, doi: 10.1109/NSS/MIC44867.2021.9875648.

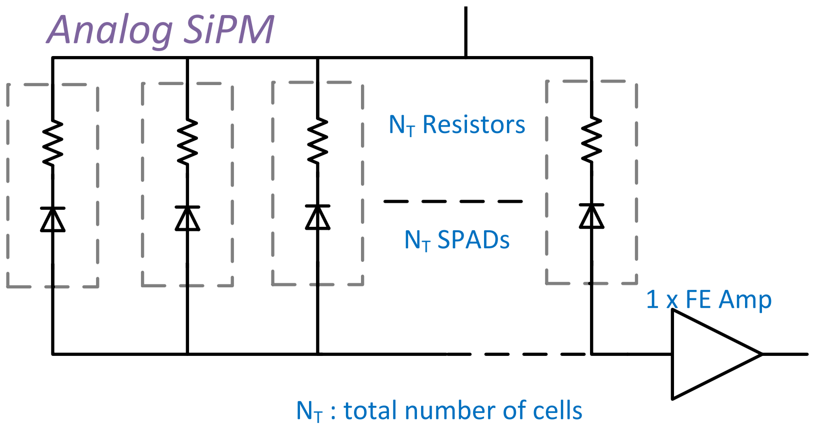
VI. FastICPix

- FastICpix: try to exploit optimal segmentation
  - Optimization for a given ***<u>power budget !</u>***
  - Investigation of new circuit topologies
  - 3D integration

Electronic noise jitter < 1 ps for next generation of detectors based on prompt light

Time tagging of first(s) photons

***Optimal** and **adaptable** **segmentation**: with **hybrid** detector*



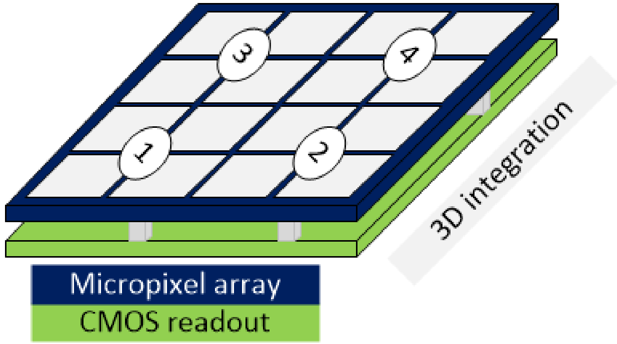
Pros

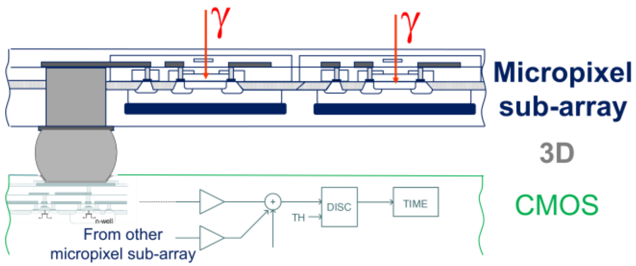
- Simplicity
- High Fill Factor (PDE)

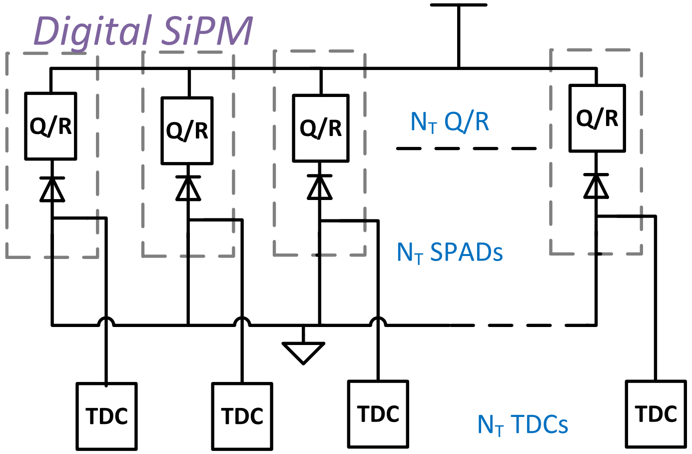
Cons

- Large capacitance degrades timing
- Xtalk deagrades timing

No segmentation







Q/R: Quenching and recharge circuit

Pros

- Individual photon timing available

Cons

- Complexity (cost and power)
- Fill factor degradation
- Xtalk degrades timing

Maximum segmentation

VII. Summary

- FastIC developments aim at optimize timing for “scalable” solutions
  - System on chip
  - Low power (<1 mW/mm^2)
  - Compact:< 1 mm^2 per readout channel (or “pixel”)
  - Fabrication cost < 1 $/ch for volume production
- Minimize electronics jitter
  - FE design in advanced nodes + + 2.5/3 D interconnects + segmentation
- Minimize digitization jitter
  - 25 ps bin TDC (<10 ps jitter)
- Time-walk correction
  - By precise and large dynamic range energy measurement

FastIC, FastIC+, FastRICH to readout “conventional” single photon sensors

50 ps rms SPTR

FastIC32 to readout pixelated single photon sensors (2.5 D integration)

< 50 ps rms SPTR

FastICPix: hybrid 3D sensor

< 20 ps rms SPTR

CERN ICCUB Institute of Cosmos Sciences EXCELENCIA MARÍA DE MAEZTU

Acknoledgments

Thanks a lot to our collaborators for contributions to this talk:

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- MGH (G. El Fakhri, S. Habet et al.)
- IJS (R. Pestotnik, R. Donelec, P. Krizan et al.)
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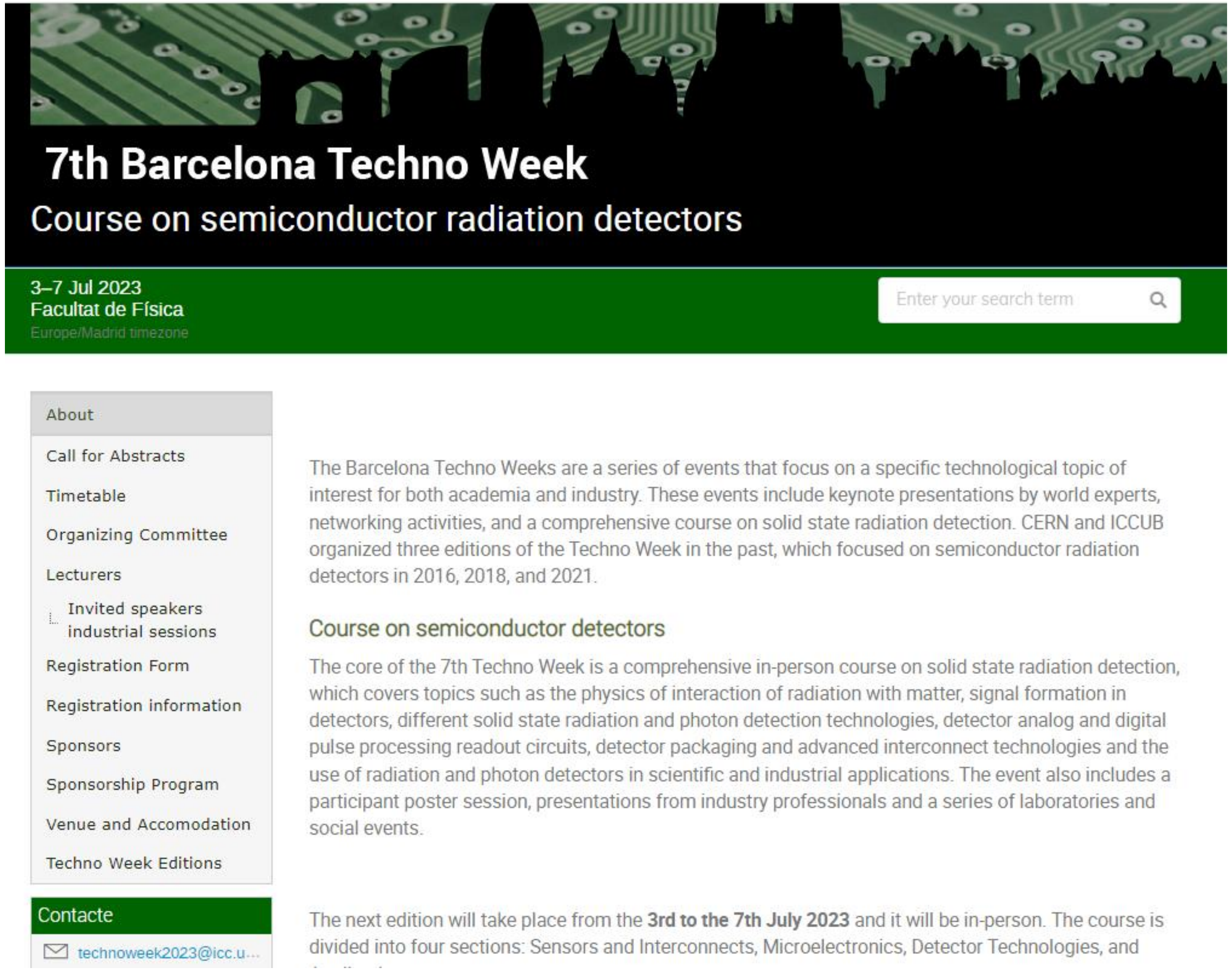
- I3M and Oncovision (J. M. Benlloch, A. Gonzalez, G. Pavon et al.)
- P. Lecoq, S. Gundacker, Y. Cates, E. Charbon, D. Breton and many others
- Hamamatsu Photonics

Barcelona Techno Week

- **Barcelona Techno Week:** a series of meeting point events between academia and industry, organized around a technological topic of interest for both worlds
  - The core is a semiconductor detector course
  - Organized by ICCUB and CERN
- Last edition on 2021 (online)
  - More than 100 students
  - Nearly 150 attendees in total
  - Industrial participation
- *July 2023: back to presential:*

You are welcome !


7th Barcelona Techno Week

Course on semiconductor radiation detectors

3–7 Jul 2023
Facultat de Física
Europe/Madrid timezone

The Barcelona Techno Weeks are a series of events that focus on a specific technological topic of interest for both academia and industry. These events include keynote presentations by world experts, networking activities, and a comprehensive course on solid state radiation detection. CERN and ICCUB organized three editions of the Techno Week in the past, which focused on semiconductor radiation detectors in 2016, 2018, and 2021.

Course on semiconductor detectors

The core of the 7th Techno Week is a comprehensive in-person course on solid state radiation detection, which covers topics such as the physics of interaction of radiation with matter, signal formation in detectors, different solid state radiation and photon detection technologies, detector analog and digital pulse processing readout circuits, detector packaging and advanced interconnect technologies and the use of radiation and photon detectors in scientific and industrial applications. The event also includes a participant poster session, presentations from industry professionals and a series of laboratories and social events.

The next edition will take place from the **3rd to the 7th July 2023** and it will be in-person. The course is divided into four sections: Sensors and Interconnects, Microelectronics, Detector Technologies, and

https://indico.icc.ub.edu/event/176/

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Thanks a lot for your attention !!!

Comments or questions ?

dgascon@fqa.ub.edu

UNIVERSITAT DE BARCELONA

30 May 2023

CERN ICCUB Institute of Cosmos Sciences EXCELENCIA MARÍA DE MAEZTU

I. Introduction

Institut de Ciències del Cosmos
UNIVERSITAT DE BARCELONA

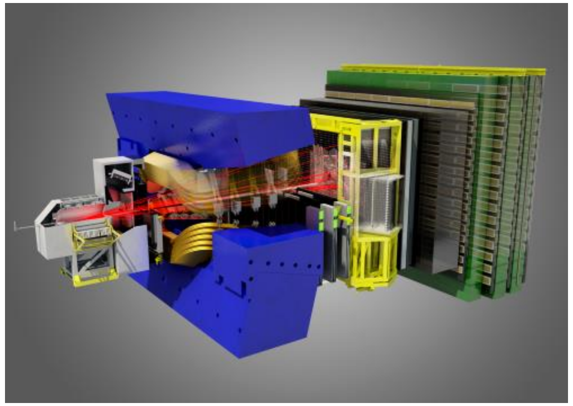
EXCELENCIA MARÍA DE MAEZTU 2020-2023

Applications

CTA

HERD

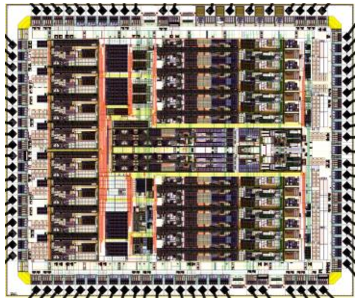
TOF-PET



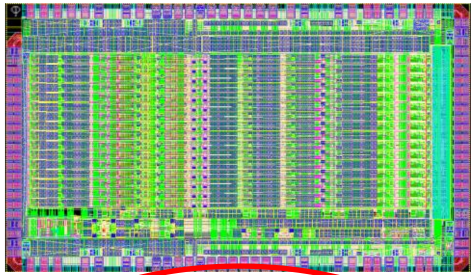
LHCb

Readout Electronics

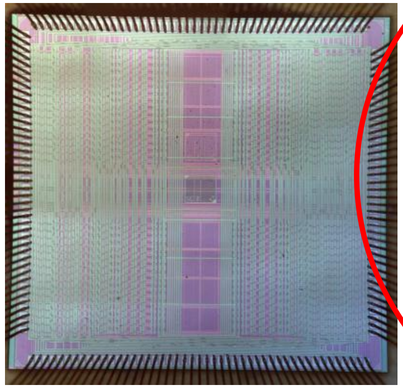
CTA: MUSIC



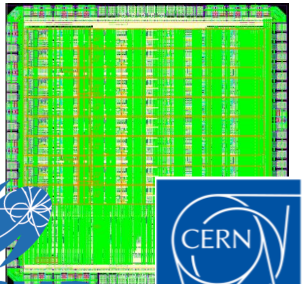
HERD: BETA



LHCb: Scifi - PACIFIC



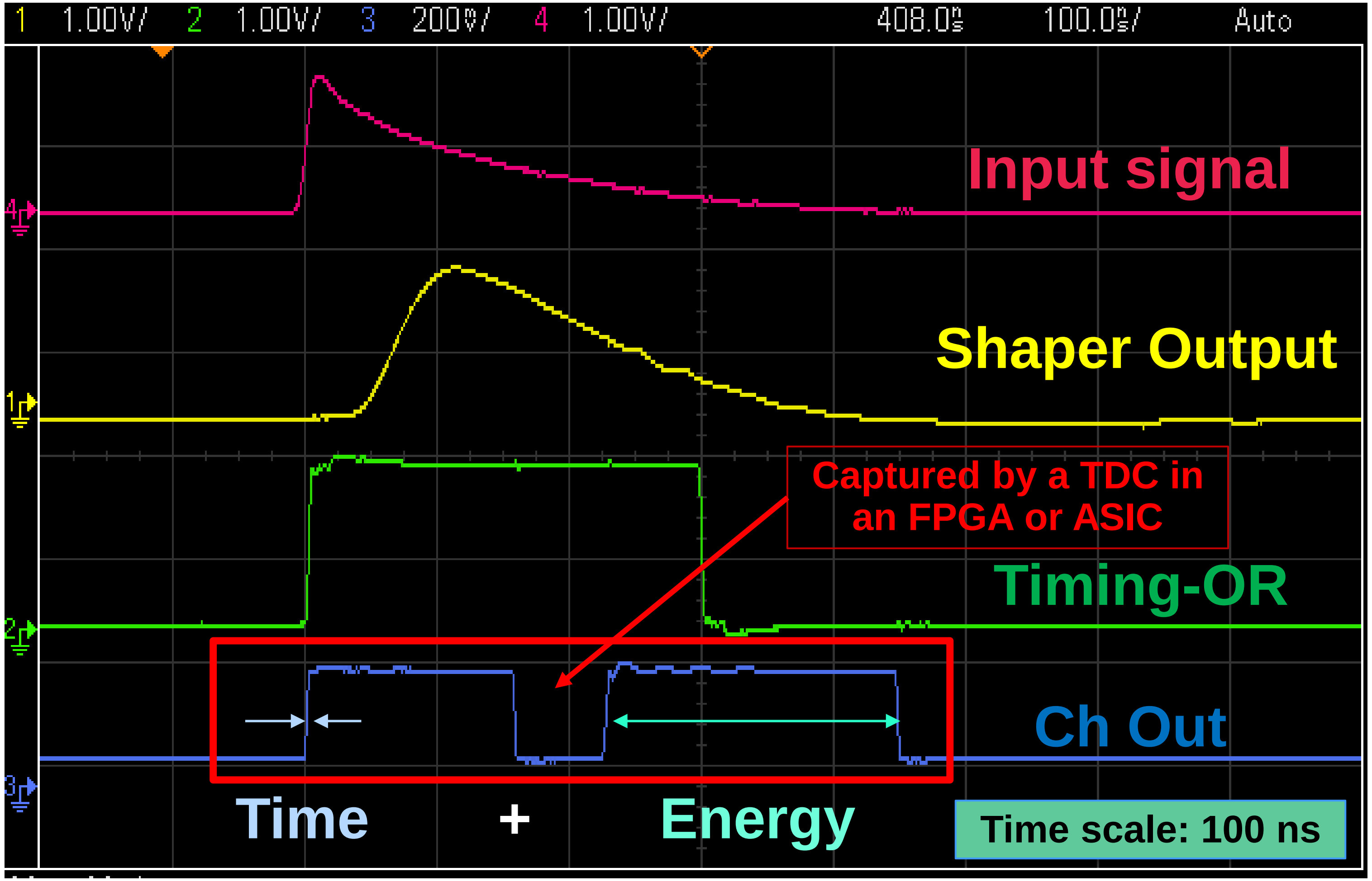
LHCb – TOF-PET: FastIC



CTA Observatory: http://observatorio-cta.es/; HERD Space mission http://herd.ihep.ac.cn/; PET scanner; https://en.wikipedia.org/wiki/Positron_emission_tomography; LHCb detector: https://visit.cern/node/611

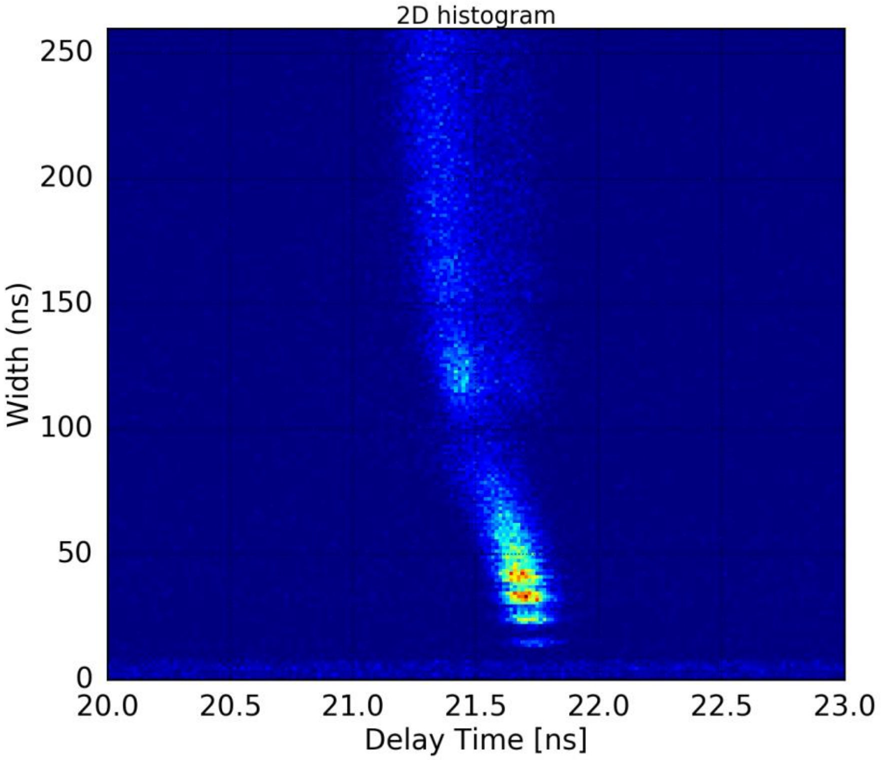
I. FastIC architecture: Time + Energy readout

- **FastIC** provides a measurement of the **time** and **energy** per channel in two consecutive pulses.

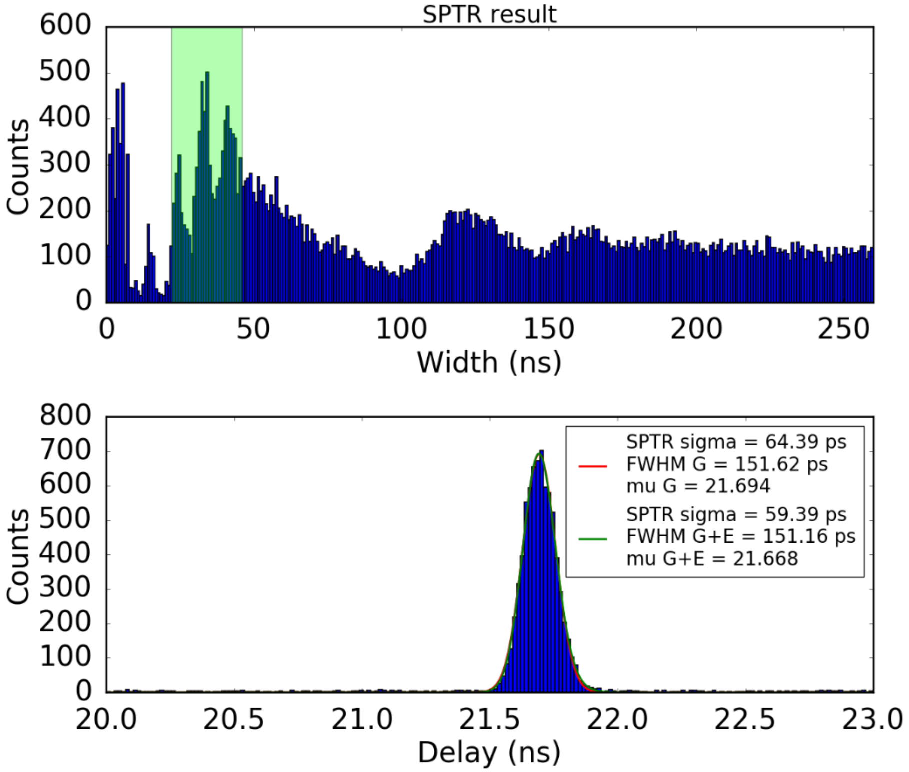


II. FastIC performance: SPTR with FBK-NUVHD technology

- **Sensor:** FBK-NUVHDLFv2b 3x3mm^2, 40μm pixel pitch.
- Room Temperature without stabilization.



- 8 K events used for the SPTR.

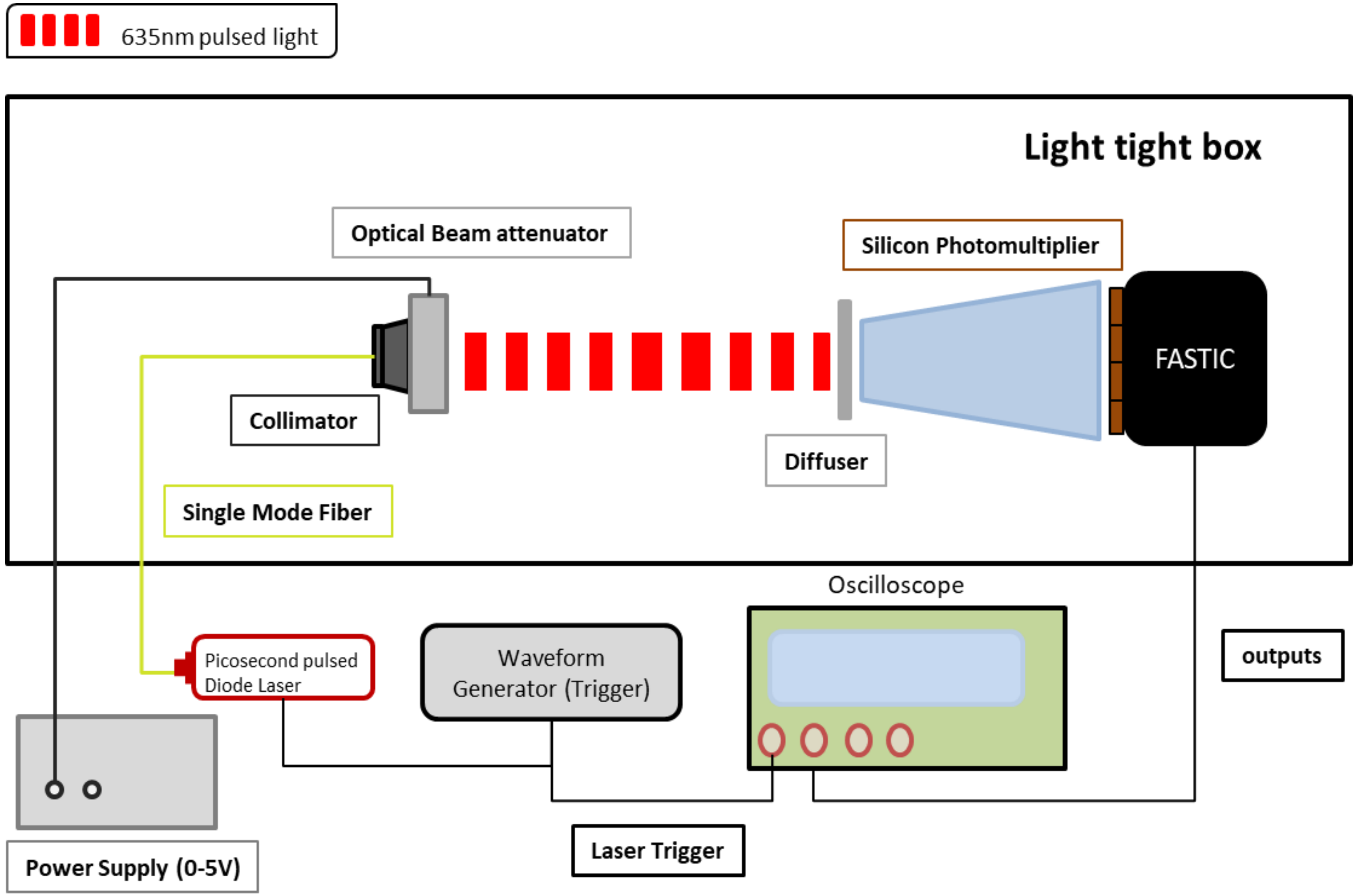


FWHM = 151.16 ps

FastIC Bias voltage 43.48 V (10.5 V of Over-voltage)

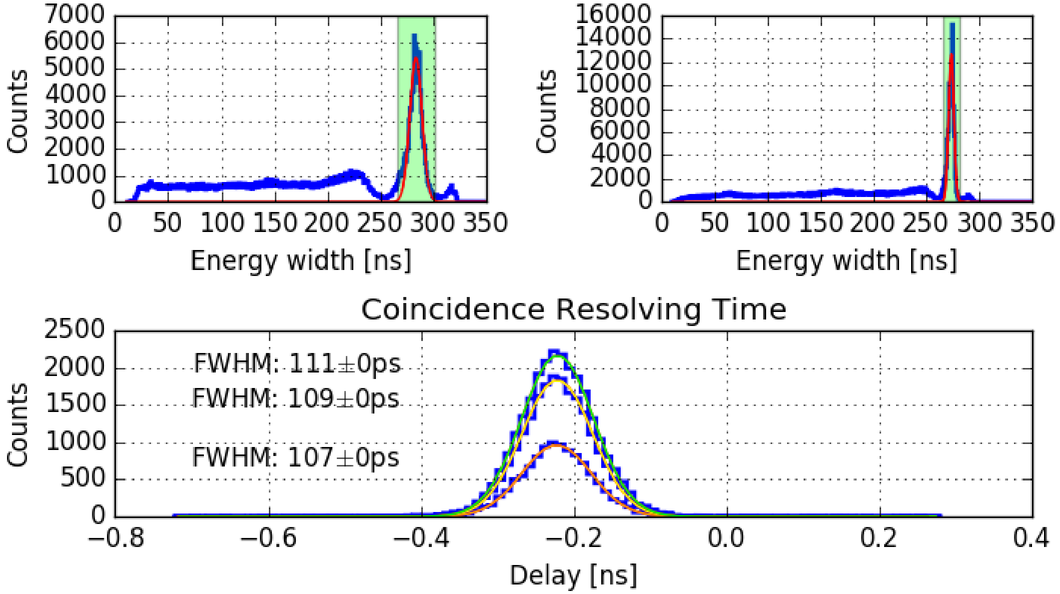
II. FastIC performance: SPTR measurements with SiPM and red light

- **FASTIC** and **HRFlexToT** used for comparison.
- The setup is as follows:
  - PicoQuant PDL 800-D laser at 635 nm and a tuned intensity level of 50%, jitter < 20 ps rms and 30 ps pulse width.
  - **Sensor**: S13360-3050CS (Hamamatsu).
  - Agilent MSO 9404A 4 GHz oscilloscope (20 GS/s).
  - Several measurements are performed to identify the optimal threshold.



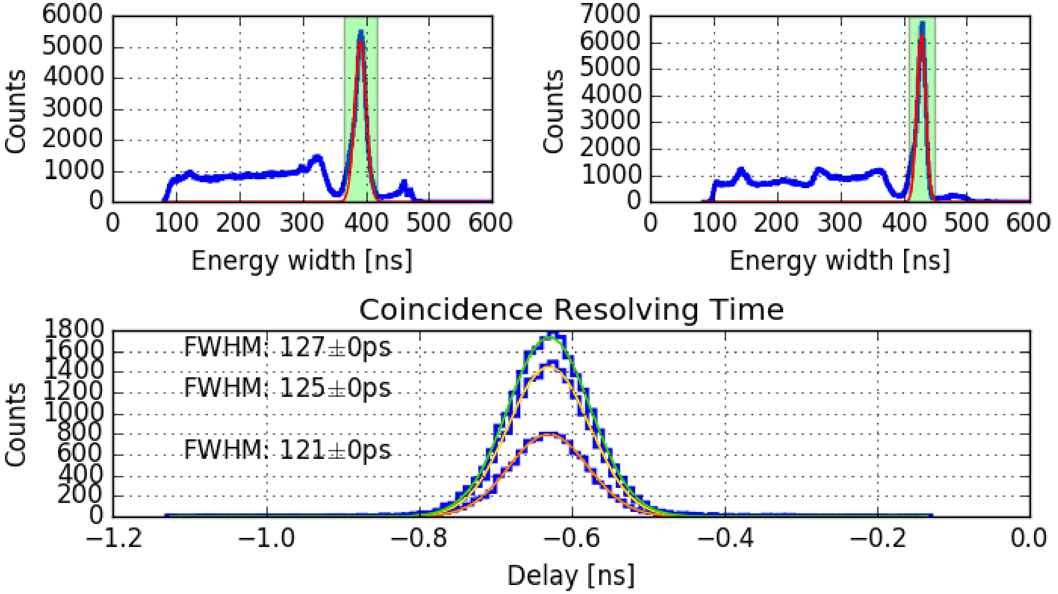
II. FastIC performance: CTR with scintillation light.

- **Sensor:** HPK S13360-3050CS 3x3mm^2, 50μm pixel pitch.
- **Crystal:** LSO:Ce Ca 0.2% of 2x2x5mm³.



FastIC **Bias voltage 60.0 V (7 V of Over-voltage)**

FWHM = 107 ps



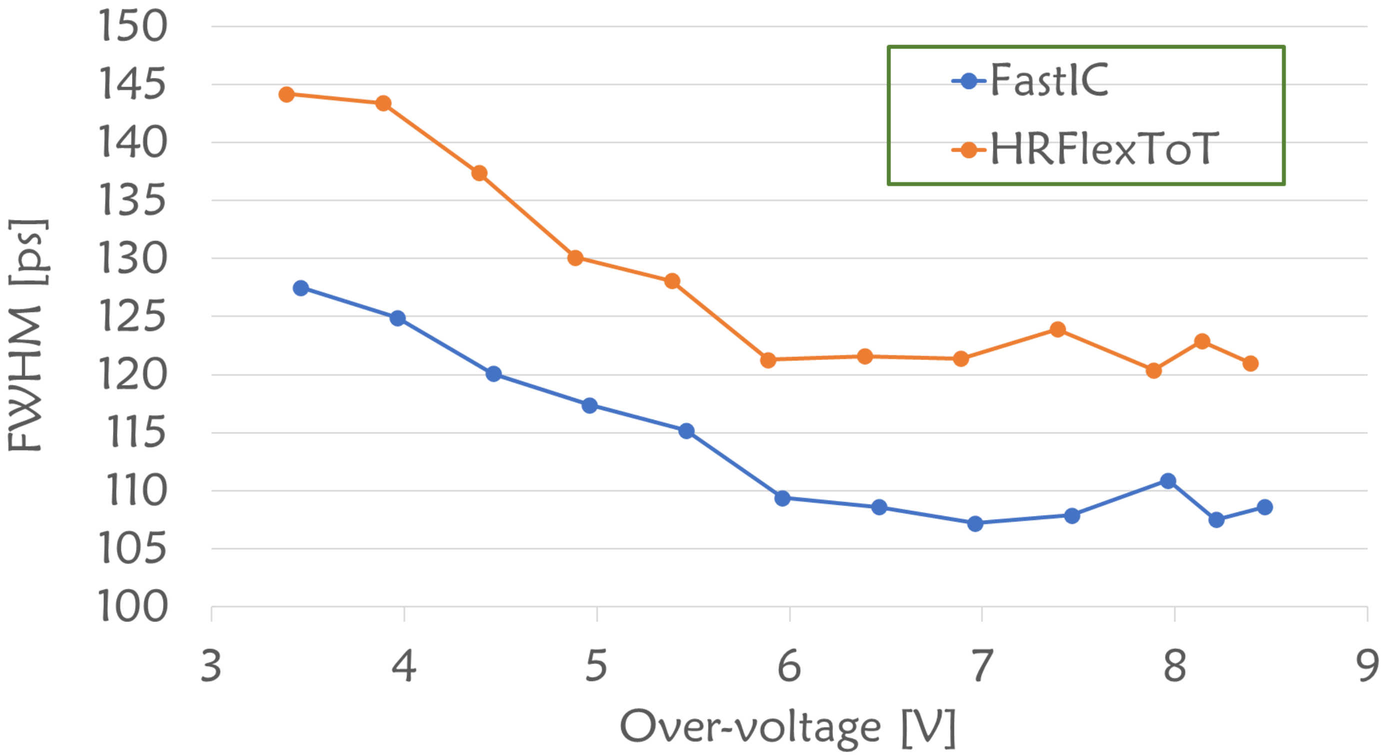
HRFlexToT **Bias voltage 60V (7V of Over-voltage)**

FWHM = 121 ps

- Different amount of events are selected in coincidence from the 511 keV energy peak.
- For 1 sigma around 13 K events are selected, and 25 K and 30 K for 2 and 3 sigma respectively.

II. FastIC vs HRFlexToT: CTR with scintillation light.

- **Sensor:** HPK S13360-3050CS 3x3mm², 50µm pixel pitch.
- **Crystal:** LSO:Ce Ca 0.2% of 2x2x5mm³



- Best CTR is achieved at over-voltages from 6 V to 8.5 V for both ASICs

HRFlexToT → **FWHM = 121 ps**

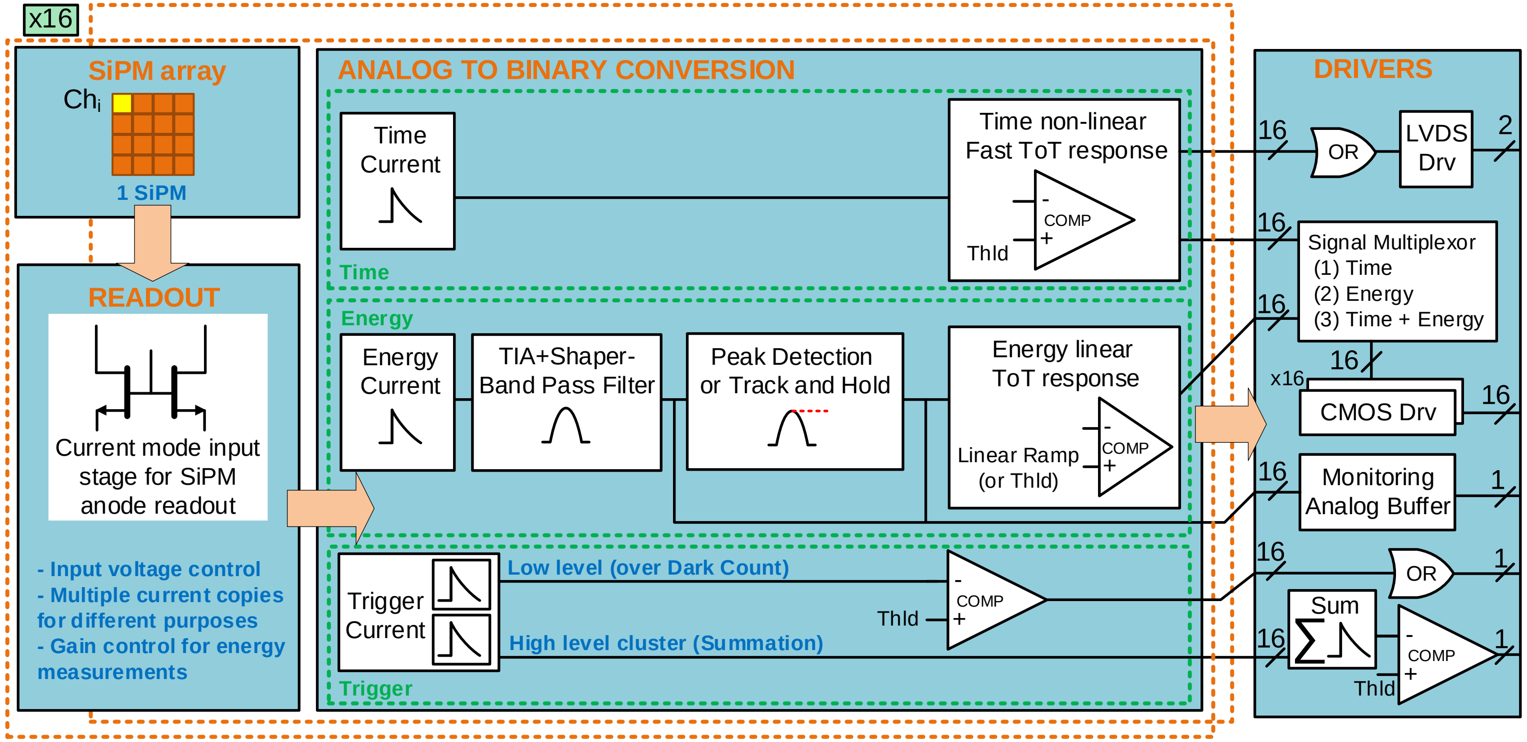
FastIC → **FWHM = 107 ps**

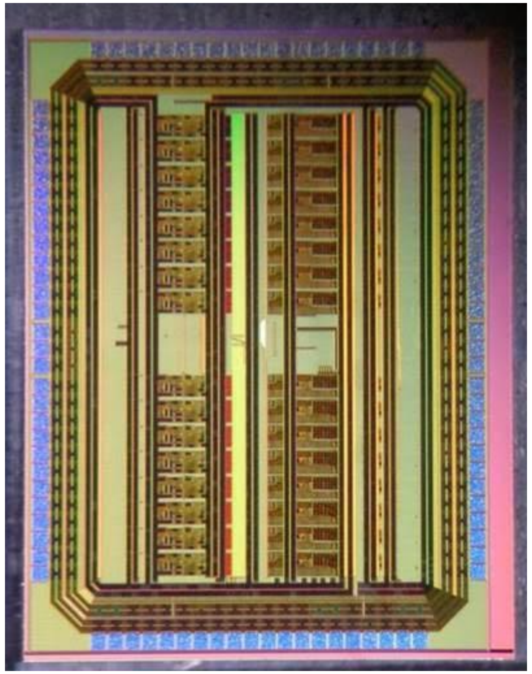
Improvement: 11,5%

- Different amount of events are selected in coincidence from the 511 keV energy peak.
- For 1 sigma around 13 K events are selected, and 25 K and 30 K for 2 and 3 sigma respectively.

I. Background: HRFlexToT architecture

- HRFlexToT[1] current mode ASIC.
  - 16 Inputs: 16 Single Ended Positive.
  - 16 Outputs in CMOS mode.
  - Lower power consumption (about 3.5 mW/ch).
  - Asynchronous FSM to control the energy response.
  - Arrival time as a fast OR and per channel.
  - Energy: Linear Time over Threshold with high dynamic range.
  - Different trigger levels and cluster trigger for monolithic crystals.



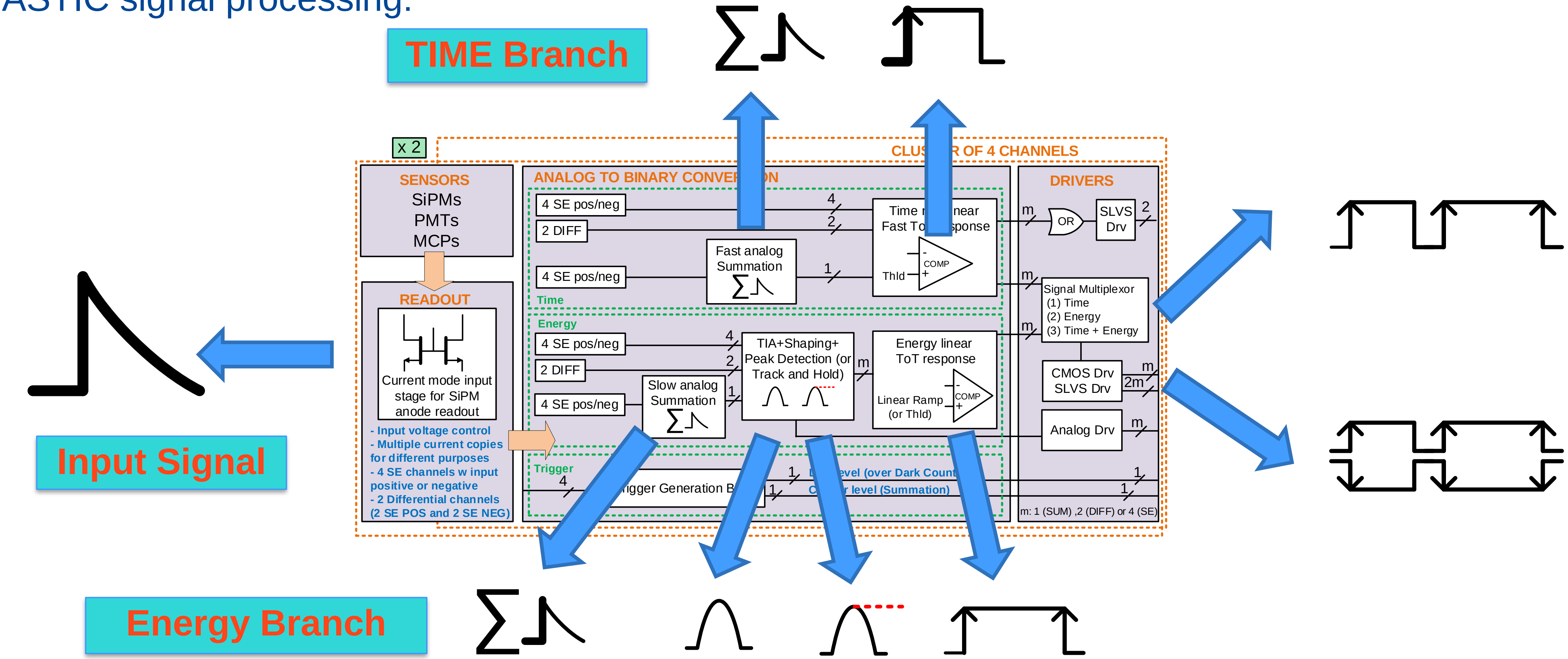


180 nm - 2,38 x 3,19 mm^2

[1]: Sanchez, D., Gomez, S., et. al. HRFlexToT: A High Dynamic Range ASIC for Time-of-Flight Positron Emission Tomography, 2021, IEEE TRPMS, https://doi.org/10.1109/TRPMS.2021.3066426

I. FastIC signal processing

- FASTIC signal processing:

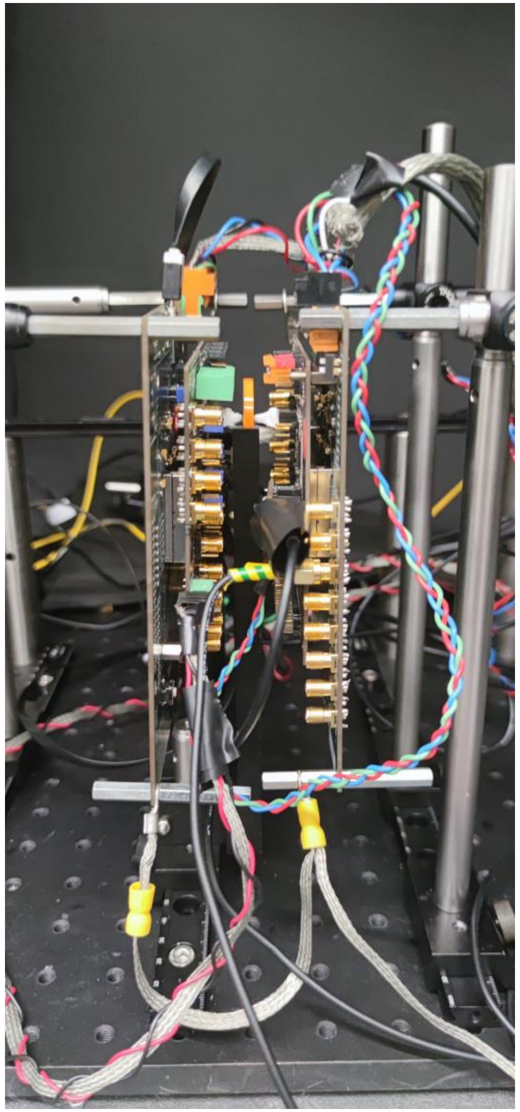


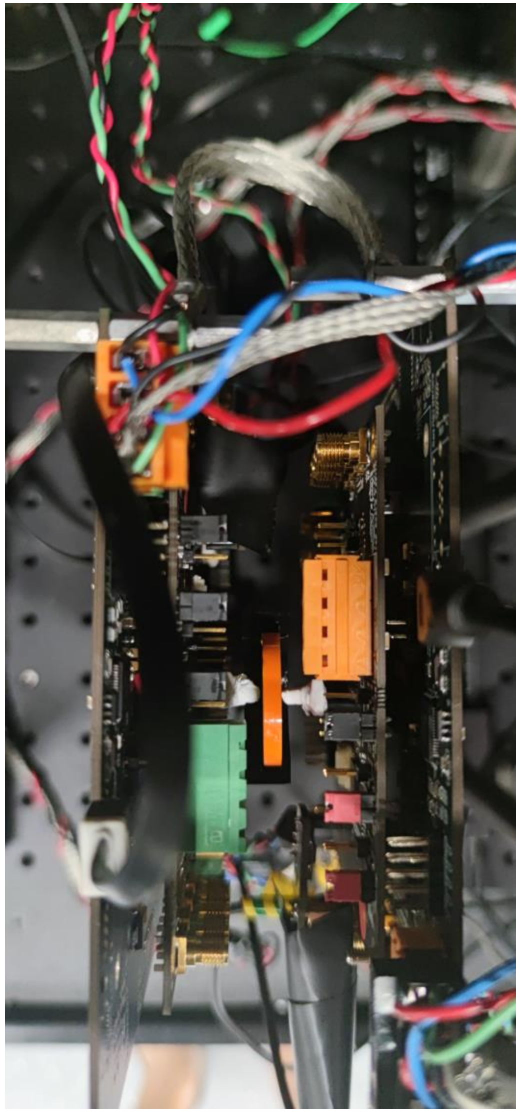
TIME Branch

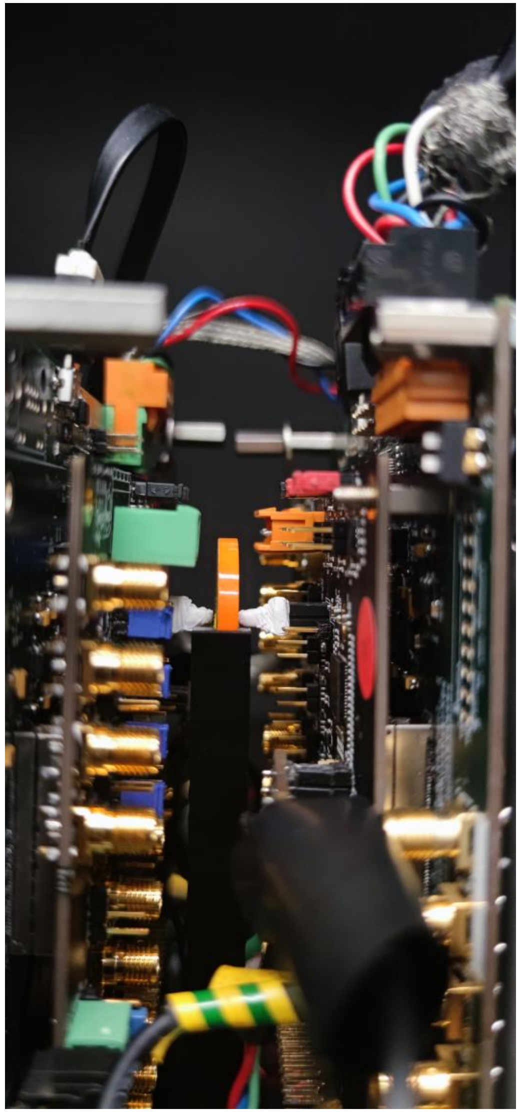
Input Signal

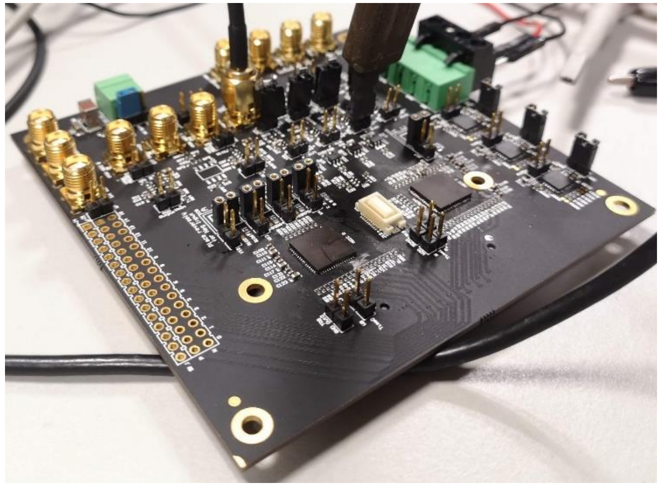
Energy Branch

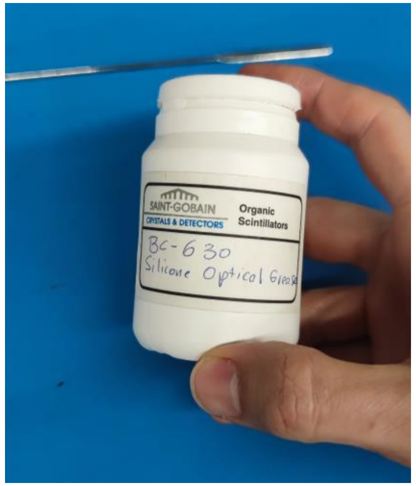
Methods: Setup CTR Na 22 Source



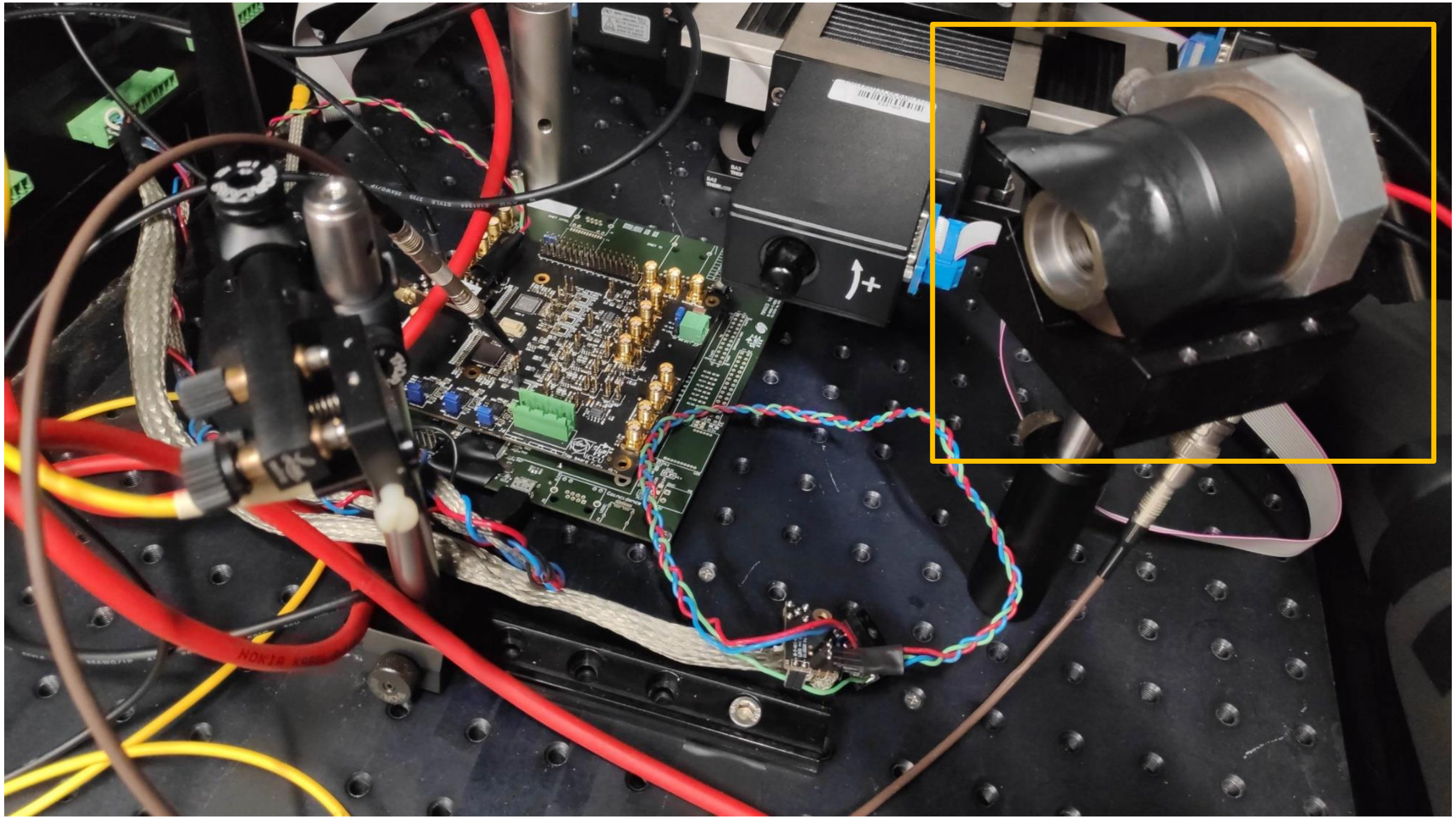








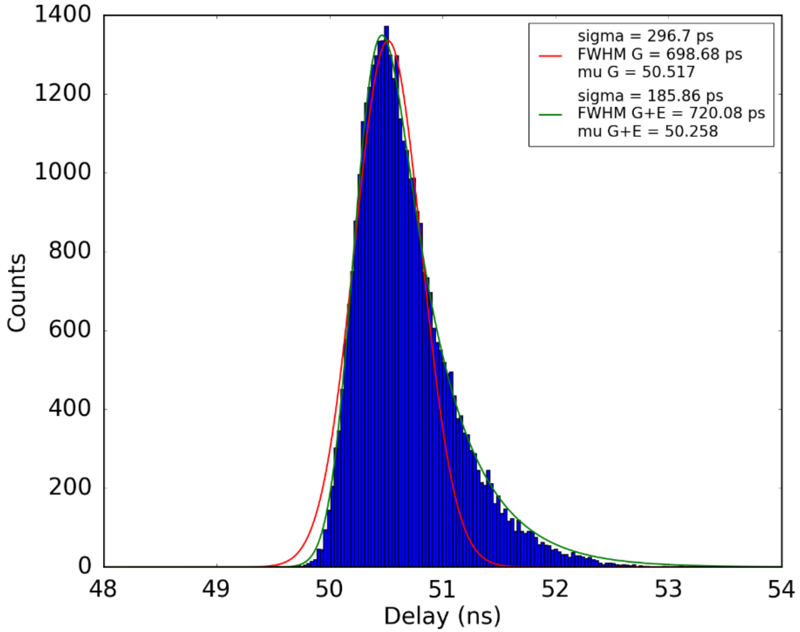
III. FastIC performance: Time resolution with a PMT.



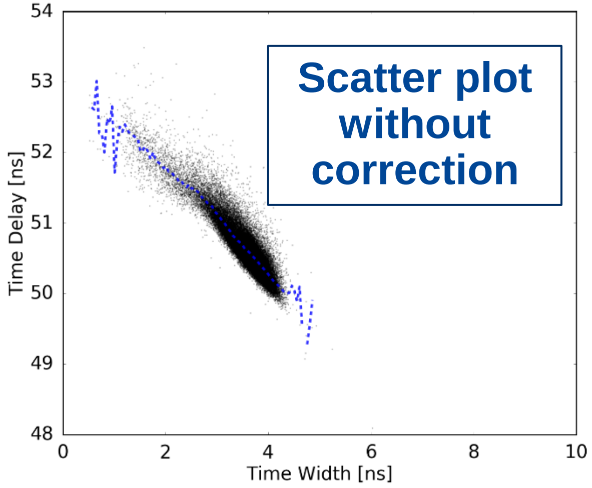
- FASTIC (Negative polarity)
- Blue laser (405 nm) – 40 ps FWHM pulse width
- ±Vcc = ±6.5V (Imax ≈ 2A)
- PMT: R5900 (Hamamatsu)
  - 800V power supply
  - $G = 6 \cdot 10^5$
  - $TTS = 340\ ps\ FWHM$

III. FastIC performance: Time resolution with a PMT.

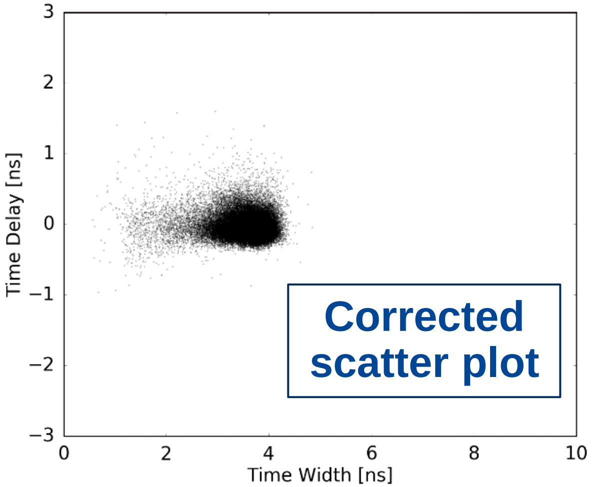
- Time-walk needs to be corrected for measurements at low light intensity with a PMT to improve the time performance.



Time histogram without TW correction

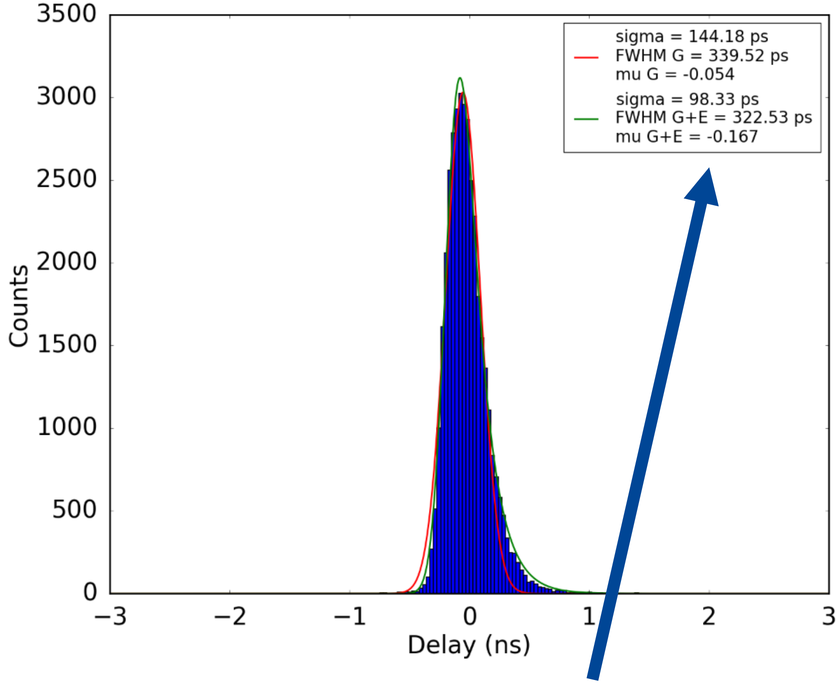


Scatter plot without correction



Corrected scatter plot

Time histogram with TW correction

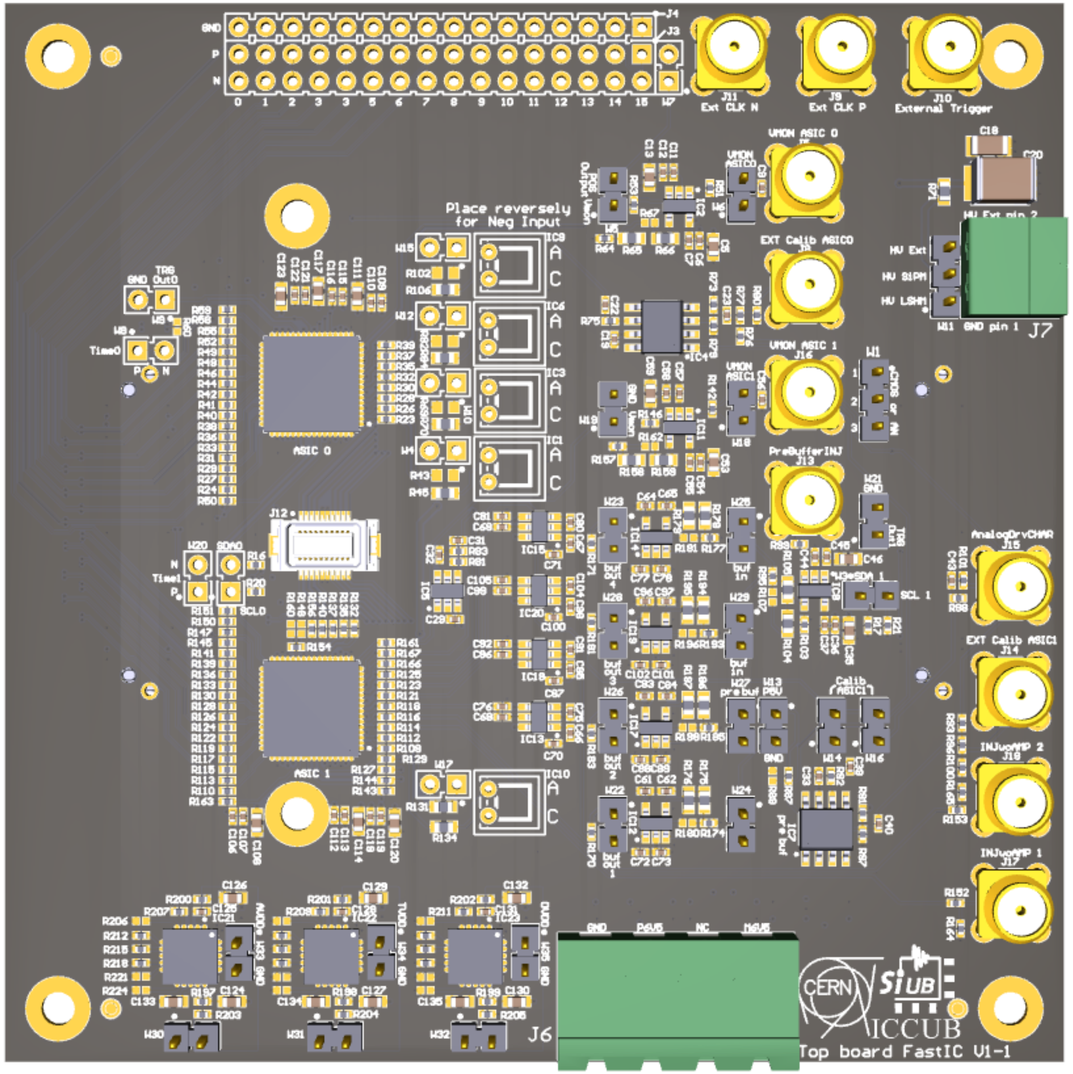


$340\ ps\ FWHM \sim TTS$

I. FastIC design specifications

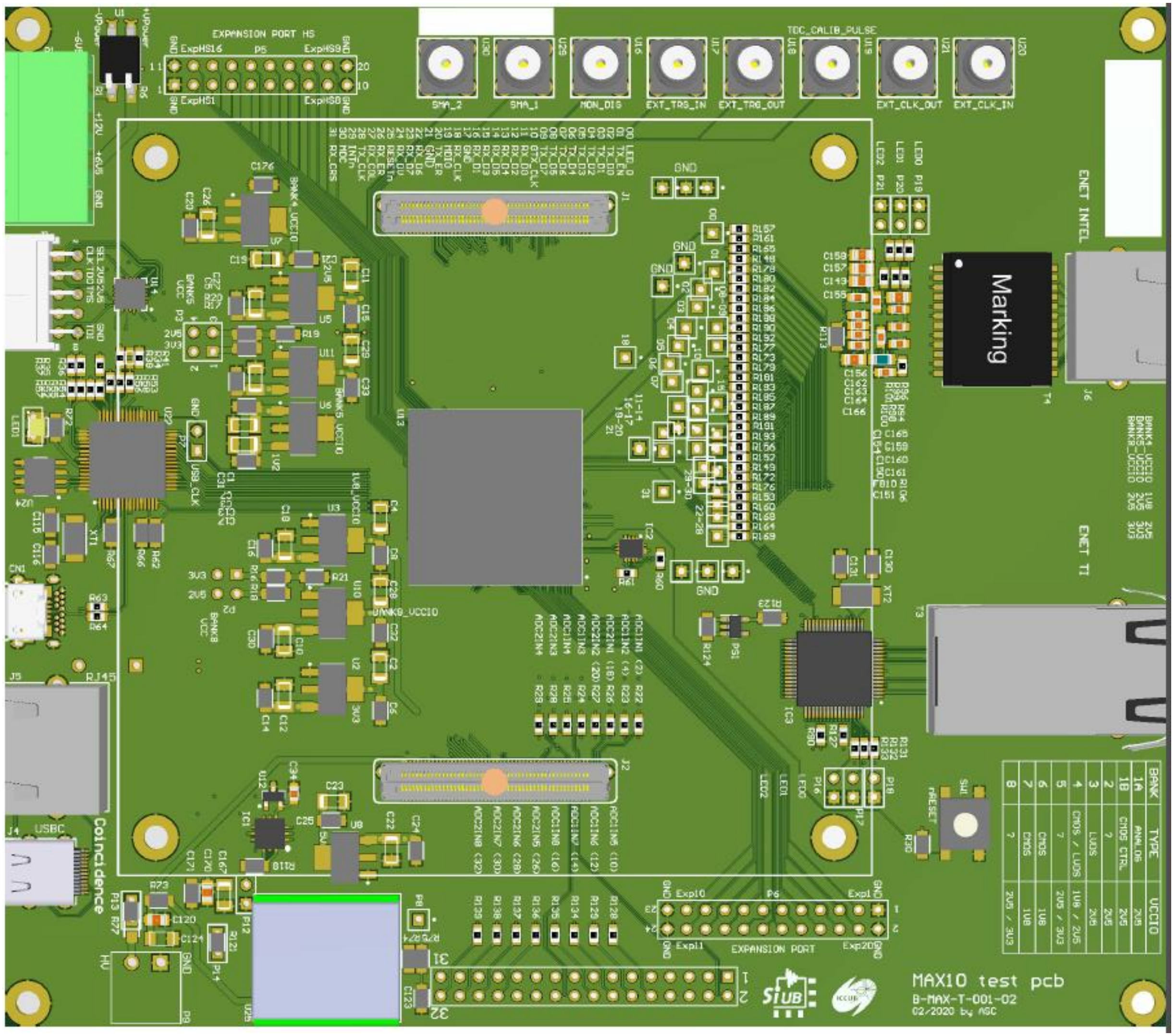
Parameter	Value
Technology	65 nm CMOS TSMC
Power consumption	~ 12 mW/ch in SE mode (V_{DD} = 1.2 V), depends on operation mode (~ 3 mW/Input Stage). Non-Linear ToT 6 mW/ch.
Input voltage	Adjustable input node DC voltage.
Number of channels	Input channel configuration (current mode processing): 8 Single Ended (SE) or 4 Differential (DIFF).
Connection Type	Configurable SE (Pos/Neg polarity), DIFF, Sum of 4 (Pos/Neg polarity)
Electronics Time Jitter	~ 30 ps_{rms} SPTR (330 pF 3x3 SiPM, LCT5 S13360 SiPM, Vov = 4.5 V, L = 1.2 nH)
Energy Resolution	Linear (~ 2.5 % Linearity error)
Dynamic Range	The linear energy measurement has 10-bit dynamic range up to ~25 mA of input current.
Maximum Rate	~ 2 MHz (Linear ToT readout) > 50 MHz (Non-linear ToT. Pulse-shape-dependent)
Testing and Calibration	Yes
Interface	I2C
Output	Configurable Digital (single-ended CMOS or differential SLVS) or Analog output (10 pF load).

I. Testing of FASTIC: Stacked PCBs. ASIC Board



- Test Board including two FASTIC chips.
- The board enables to inject electrical signal for characterization of any pulse shape.
- The board enables to connect SiPMs in POS, NEG and DIFF.
- External connector to be employed with any sensor.

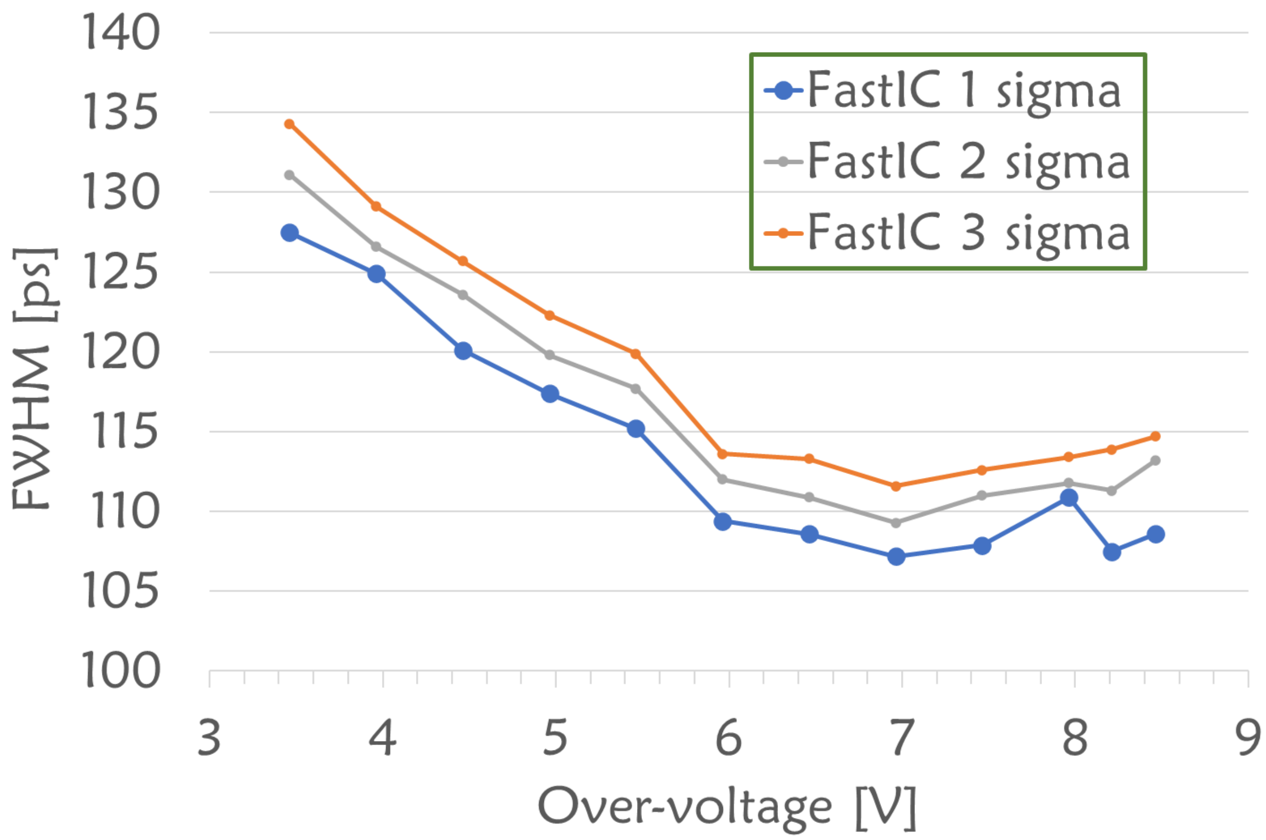
I. Testing of FASTIC: Stacked PCBs. Control Board



- Control board contaning an ALTERA MAX10 FPGA.
- The FPGA controls the ASIC through I2C
- It includes TDCs to digitize the Time + Energy response with 65 ps FWHM time bin resolution.

I. FASTIC: CTR with respect event selection

- Sensor: HPK S13360-3050PE 3x3mm^2, 50μm pixel pitch.
- Crystal: LSO:Ce Ca 0.2% of 2x2x5mm³



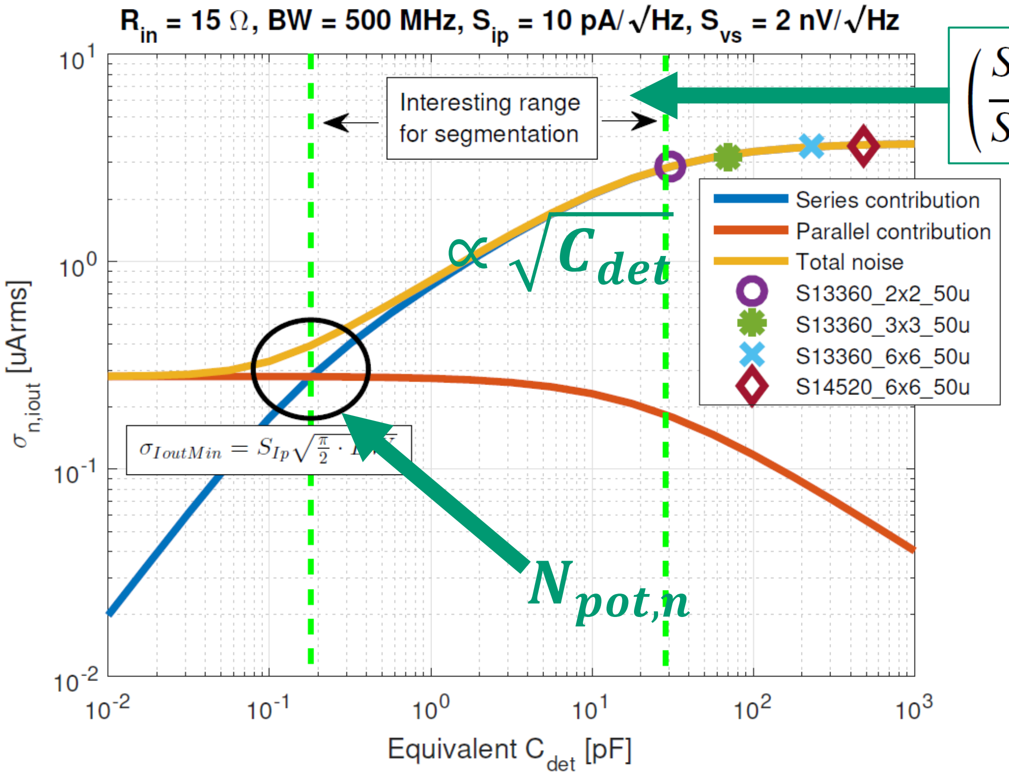
- 250K coincidence events were recorded.
- When selecting the 511 KeV events in coincidence, we can select events within 1, 2 or 3 sigma from the mean 511K Energy detected peak

	1 sigma	2 sigma	3 sigma
511 KeV events	5,13%	9,88%	12,07%
Best CTR	107,2	109,3	111,6
Improvement sensitivity		1,93	2,35
Worsening CTR		1,96 %	4,10 %

IV. Detector segmentation + active summation

- Not always series noise dominates
- Current noise
  - with series and parallel contributions
  - for simple detector capacitance and SiPMs models

J. M. Fernández-Tenllado, et alt, "Optimal design of single-photon sensor front-end electronics for fast-timing applications," IEEE NSS/MIC 2019, doi: 10.1109/NSS/MIC42101.2019.9059805.



$$\left(\frac{S_{I_P}}{S_{V_s}}\right)^2 \cdot \frac{R_{in}}{2\pi\ BW} < C_{det} < \frac{1}{2\pi\ R_{in}\ BW}$$

- Segmentation works for a C_{det} range:
  - Noise prop. $\sqrt{C_{det}}$
- That means there is a optimum/maximum segmentation factor $N_{opt,n}$
  - Beyond this factor noise will not improve

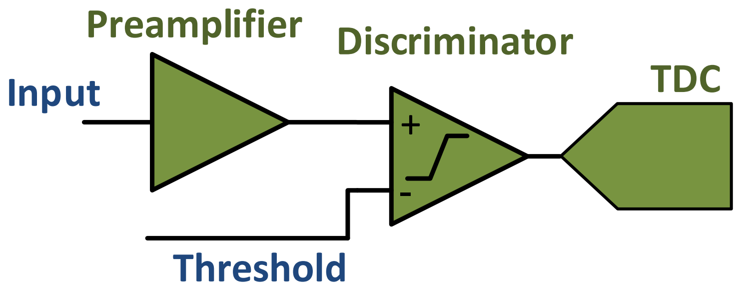
I. Introduction

- What is a fast detector?
  - ***"Prompt" signal generation***
    - *Timing measurements*
      - ***Many more factors involved !!***

- What is required to the electronics?
  - Low electronics jitter
  - Deal with time walk
  - **Accurate conversion**
    - **Adequate TDC resolution**
      - **Or waveform sampling…**

$$\sigma_{t\_el}^2 = \left(\sigma_{t\_el}^{TW}\right)^2 + \left(\sigma_{t\_el}^{Jit}\right)^2 + \left(\sigma_{t\_el}^{TDC}\right)^2 = \left(\left[\frac{t_r V_{th}}{S}\right]_{RMS}\right)^2 + \left(\frac{N}{dS/dt}\right)^2 + \left(\frac{TDC_{Bin}}{\sqrt{12}}\right)^2$$

Time-Walk ***Electronics Jitter*** ***Quantization error***



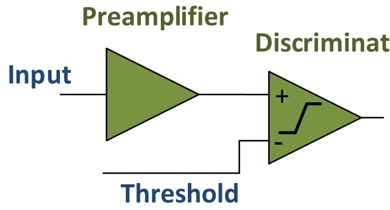
N. Cartiglia, "Ultra-Fast Silicon Detector"
https://www-physics.lbl.gov/seminars/Cartiglia.pdf

Different expression for waveform sampling systems (see section V)

III. Front end model: time measurement
Electronics jitter

- Electronic jitter depends on noise and signal slew rate

$$\sigma_{t\_el}^{Jit} = \frac{N}{dS/dt}$$



  - Noise is proportional to the square root of the BW ⟶ $N \propto \sqrt{f_{BW}} \; or \; {}^{1}\!/\!\sqrt{\tau_{BW}}$
  - Signal slew rate is inversely proportional to the rise time and thus proportional to the BW ⟶ $\frac{dS}{dt} \propto {}^{1}\!/t_{rFE} \rightarrow \frac{dS}{dt} \propto {}^{f_{BW}}\!/_{0.35}$

$t_{rFE} \approx {}^{0.35}\!/_{f_{BW}}$ rise time of a first order system for a step function

- So electronics jitter should be inversely proportional to the square root of the BW: ⟹ $\sigma_{t\_el}^{Jit} \propto {}^{1}\!/\!\sqrt{f_{BW}}$

- Then in principle we should maximize the BW of our electronics…

Is it completely correct?

III. Front end model: time measurement
Electronics jitter

- **No!**: the rise time of the signal at the output (t_{rS}) of the FE input stage depends ***both*** on its BW ***and the rise time of the input signal*** ($\boldsymbol{t_{r_{Iin}}}$)

$$t_{rS} \approx \sqrt{t_{r_{Iin}}^{2} + t_{rFE}^{2}}$$

The input signal rise time ($\boldsymbol{t_{r_{Iin}}}$) depends on detector/sensor signal formation (t_s) and/or on the detector capacitance time constant (τ_{DET})

- ***Optimal BW matches the input signal rise time***

$$\sigma_{t\_el}^{Jit} \propto \frac{\sqrt{t_{r_{Iin}}^{2}+\tau_{rFE}^{2}}}{\sqrt{\tau_{BW}}} \underset{\uparrow}{=} \frac{\sqrt{t_{r_{Iin}}^{2}+t_{rFE}^{2}}}{\sqrt{2t_{rFE}}} = \sqrt{2}\sqrt{\frac{t_{r_{Iin}}^{2}}{t_{rFE}} + t_{rFE}} \Longrightarrow$$

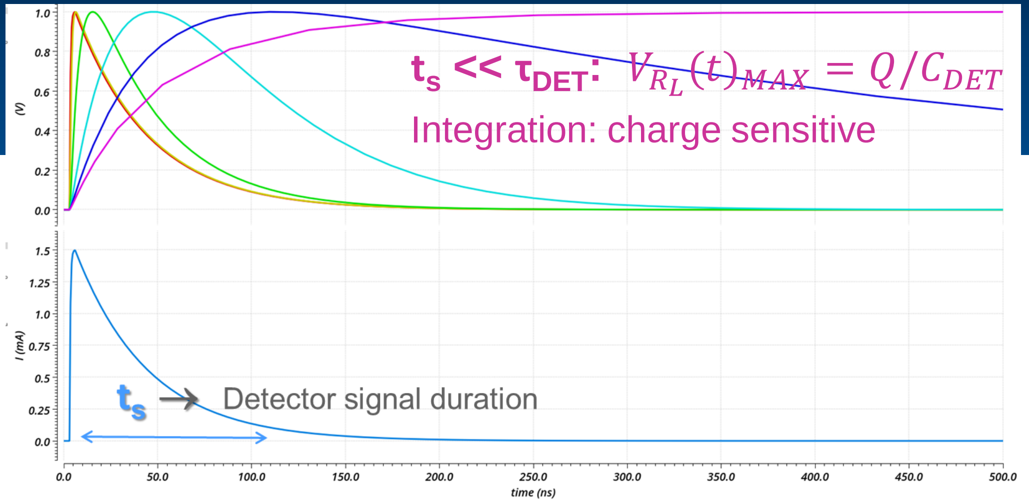
$$\tau_{BW} = \frac{1}{2\pi f_{BW}} = \frac{1}{2\pi}\frac{t_{rFE}}{0.35} \approx \frac{t_{rFE}}{2}$$

Minimum for:

$$\boldsymbol{t_{rFE} = t_{r_{Iin}}}$$

See also: A. Rivetti, «CMOS: Front-End Electronics for Radiation Sensors (Devices, Circuits, and Systems)» CRC Press; 1st edition, 2015

III. Front end model: time measurement
Electronics jitter



$t_s \ll \tau_{DET}$: $V_{R_L}(t)_{MAX} = Q/C_{DET}$

Integration: charge sensitive

t_s → Detector signal duration

- Jitter for highly capacitive detectors
  - When $t_s \ll \tau_{DET}$

$S = Q/C_{DET}$ Integration: charge sensitive $\Longrightarrow$ $\boldsymbol{t_{r_{Iin}} \approx t_s}$

- Slew rate can be approximated by $\frac{dS}{dt} \approx \frac{S}{t_{rS}} = \frac{Q/C_{DET}}{\sqrt{t_d^2+t_{rFE}^2}}$
- If $\tau_{DET} \gg \tau_{BW}$ noise is independent from C_{DET} : $N = e_n\sqrt{\pi/2\, f_{BW}} \approx e_n/\sqrt{2t_{rFE}}$
- Then $\boldsymbol{\sigma^{Jit}_{t\_el}} = \frac{N}{dS/dt} = \frac{e_n C_{DET}\sqrt{t_d^2+t_{rFE}^2}}{Q\sqrt{2t_{rFE}}} \underset{\uparrow}{=} \boldsymbol{\frac{e_n C_{DET}\sqrt{t_d}}{Q}}$

Minimum for: $t_{rFE} = t_{r_{Iin}} = t_d$

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Tutorial IEEE/NSS
Manchester 2019

- Electronics noise e_n typically depends on transistor $g_m(I_d)$ → power

$$e_n = \sqrt{\frac{2kT}{g_m}} \approx \frac{2kT}{\sqrt{qI_d}}$$

III. Front end model: time measurement
Electronics jitter

- Good initial approximation despite simplifications
  - And sensor intrinsic jitter contribution

$$SPTR_{el} = \frac{e_n C_{DET} \sqrt{t_d}}{Q}$$

Application	Sensor	C_{DET} (pF)	e_n (nV/√Hz)	T_d (ns)	Signal (fC)	$\sigma_{t\_el}^{Jit}$ (ps rms) estimated	σ_t^{Jit} (ps rms) measured
NA62 tracker	PIN diode	0.1	11	3	3 (1 MIP)	20	60
CMS HGCAL	PIN diode	8	1	3	3.8 (1 MIP)	110	200
ATLAS HGTD	LGAD (G=10)	2	2	0.5	5 (1 MIP)	10	40
Several	SiPM (G=10^6)	300	1	0.1	160 (1 pe)	20	60

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Parameter	FastRICH Analog
Technology	65 nm CMOS
Number of channels	16
Channel type / Connection	Linear layout / Single ended
Polarity	Negative (PMT, MCP, SiPM Cathode readout) and Positive (SiPM Anode readout) Front end optimized for small input capacitance detectors (PMT, MCP, ≤1x1mm^2 SiPMs)
Input Signal attenuation	Configurable per channel (1, 1/2, 1/4, 1/8)
Die dimensions/Number of pads	4x4 mm^2/ 80 pads
Power consumption Analog	Target ~4mW/channel
Electronics Time Jitter	~40 ps r.m.s. for 50 μA input pulse, <30 ps r.m.s. for pulses above 100 μA
Residual Time Walk	200ps pk-to-pk (after CFD, from 50 μA to 5 mA pulses) (Input PMT pulses are modelled with a Gaussian shape with σ=0.5 ns)
Energy Resolution	Non linear (Energy measurement not required due to single photon regime in experiment) (Possibility of an additional threshold to discriminate multiple photons on amplitude would be an asset for Upgrade 2. increasing the output bandwidth by 1bit/hit) (Feature currently under study)
Dynamic Range	5 μA to 5 mA (The timing performance is achieved for pulses >50 uA) Noise <2 μA r.m.s. (Typical PMT signal: Gaussian shape with σ=0.5 ns and 300 μA amplitude)
Front-End Hit Rate	Ability to detect signals on two consecutive beam crossings.
Testing and Calibration	Yes (With internal test charge generation by means of a test capacitance controlled by a digital signal)
Radiation hardness	Yes (TID (>100Mrad) and Triplication) (200 krad Run4, 2 Mrad Run5)