Exploring the limiting factors of PSEC4 resolution

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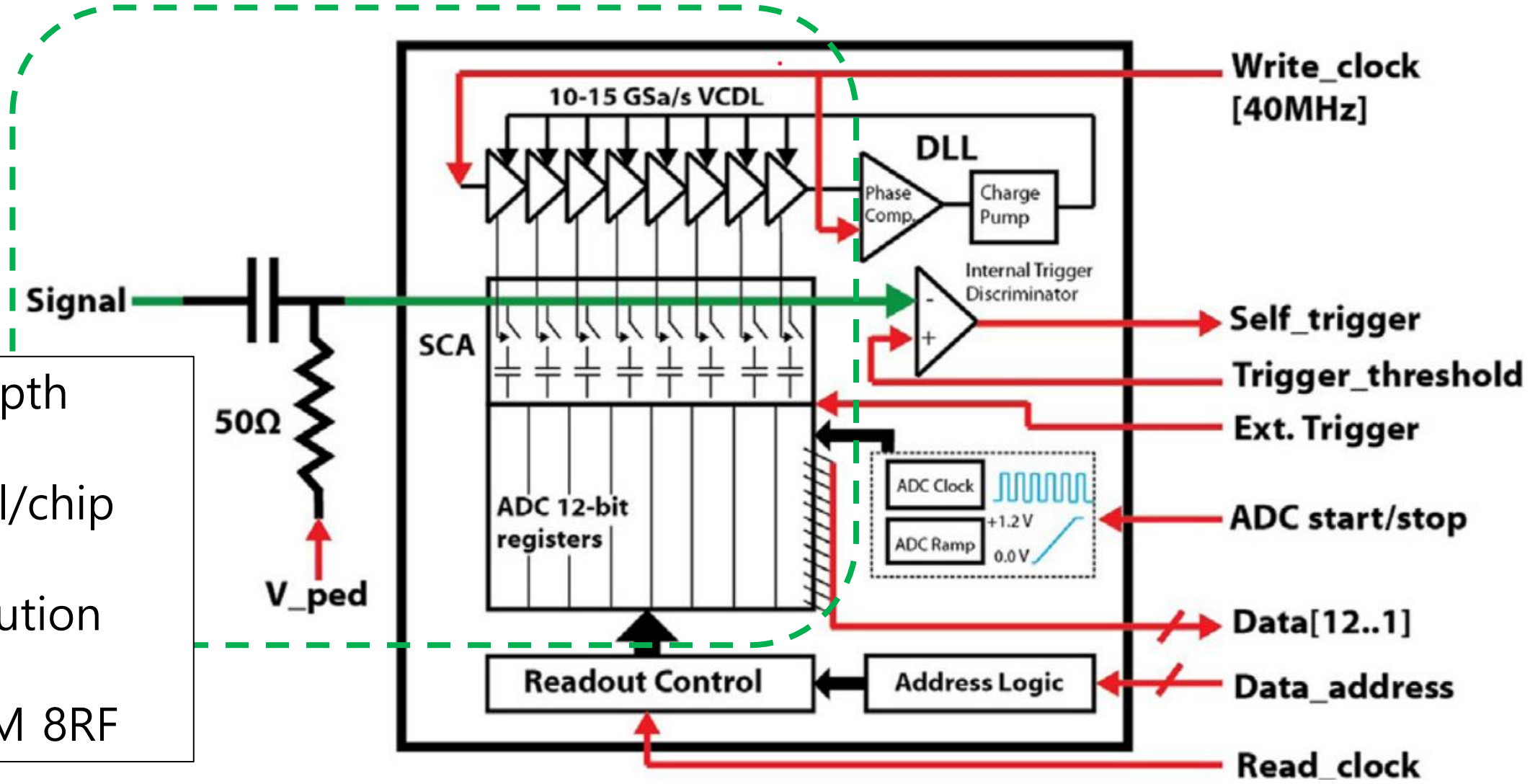
PSEC4 ASIC(2014)



- 12-bit depth
- 6 channel/chip
- 5ps resolution
- 130ns IBM 8RF

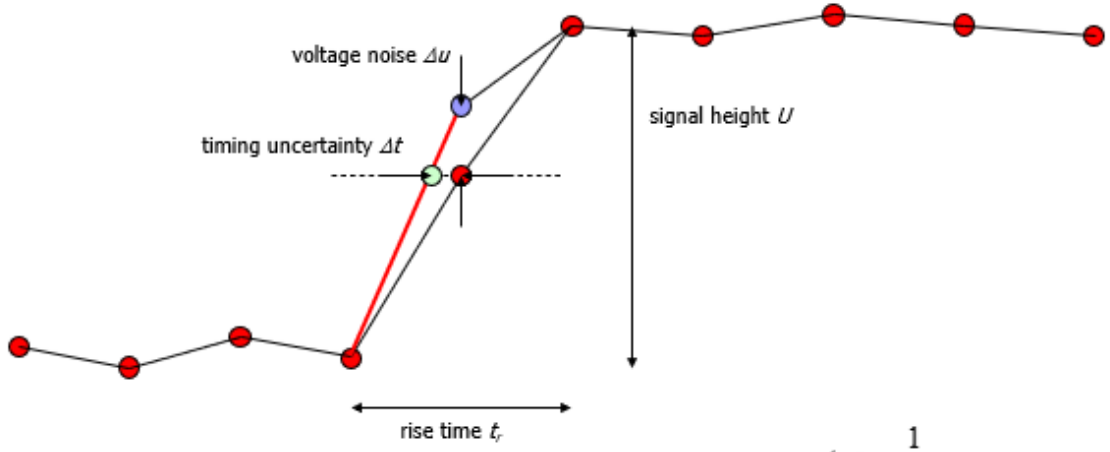
E. Oberla , J.-F. Genata, H. Grabasa, H. Frisch, K. Nishimura, G. Varner, arxiv.org/abs/1309.4397

Timing resolution factors – PSEC4 studies

- Must optimize four aspects:
  - **Signal rise time**
  - **voltage noise of samples**
  - **sampling time jitter/uncertainty**
  - **Nonlinearity**

Adopted from Stefan Ritt "**The role of analog bandwidth and signal-to-noise in timing for waveform digitizing**"

How is timing resolution affected?



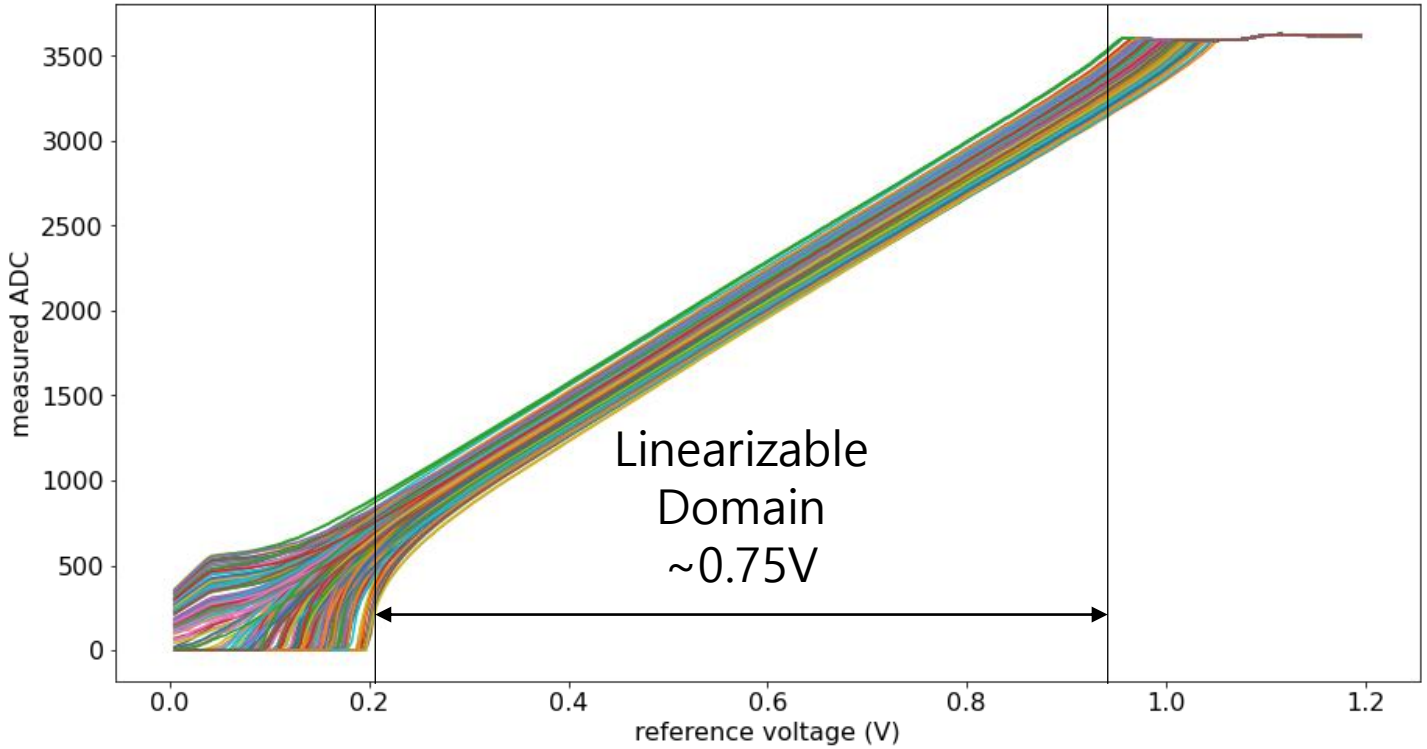
$$t_r \approx \frac{1}{3 f_{3dB}}$$

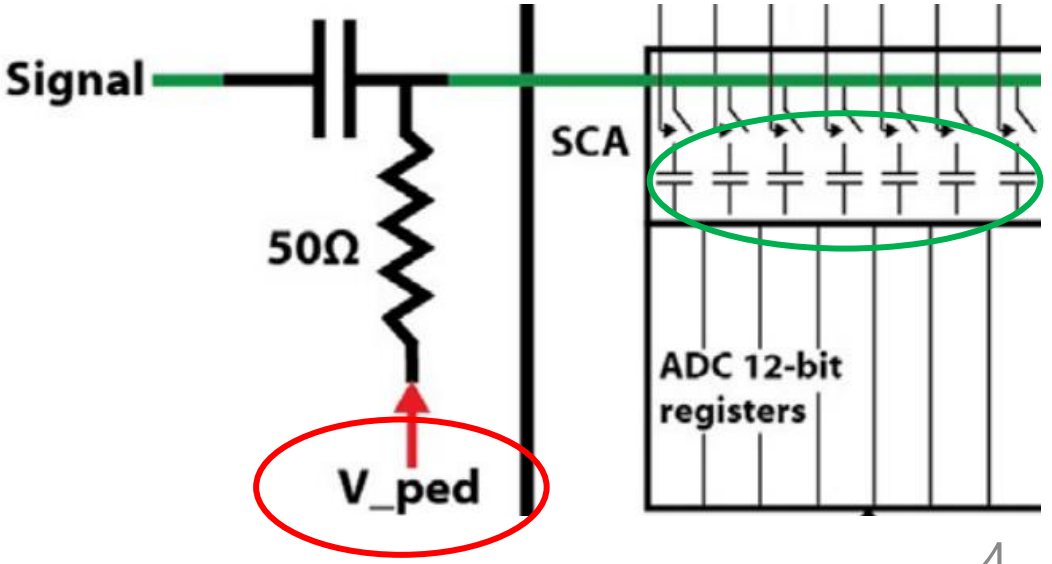
$$\Delta t = \frac{\Delta u}{U} \cdot t_r = \frac{\Delta u}{U\sqrt{n}} \cdot t_r = \frac{\Delta u}{U} \cdot \frac{t_r}{\sqrt{t_r \cdot f_s}} = \frac{\Delta u}{U} \cdot \frac{\sqrt{t_r}}{\sqrt{f_s}} = \frac{\Delta u}{U} \cdot \frac{1}{\sqrt{3 f_s \cdot f_{3dB}}}$$

Voltage linearization of PSEC4

It is necessary to reconstruct voltage from ADC value. The curve differs for each capacitor.

1. **V_ped** is set to a voltage of interest, 0.0v-1.2v
2. PSEC4 is left in sampling mode for a few cycles, so that all capacitors are set to **V_ped**. ($\sigma_V \approx 0.5mV$)
3. Each register is read. Each curve corresponds to a capacitor.

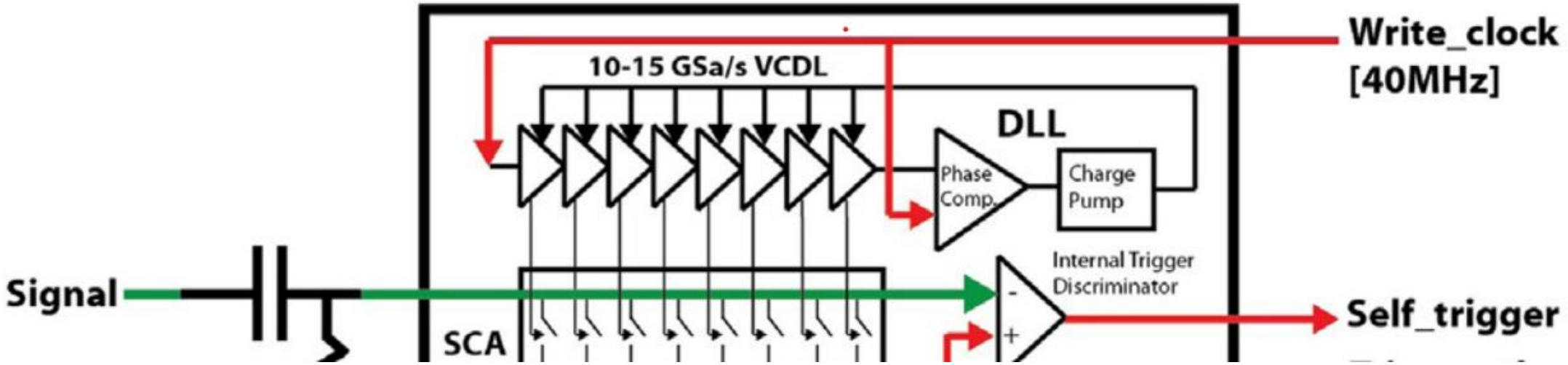




Sample time calibration – Ellipse method

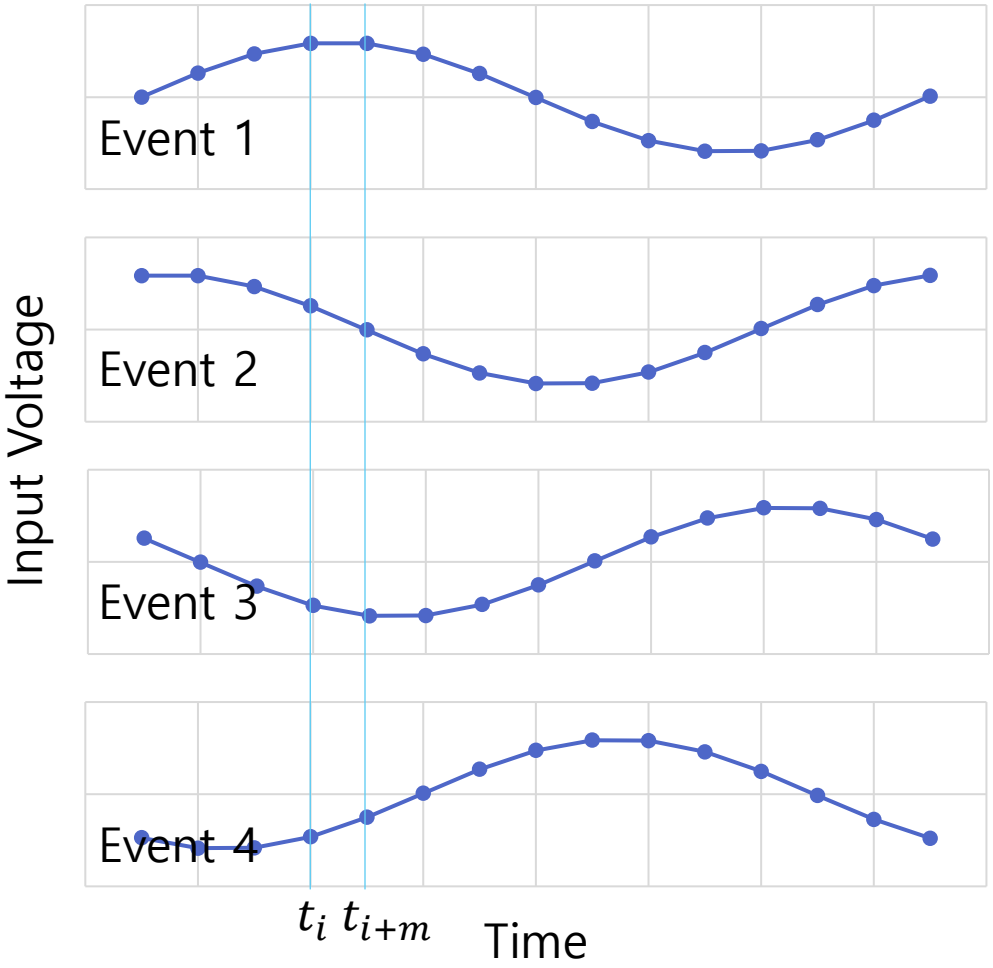
Time intervals between samples are determined by a VCDL.

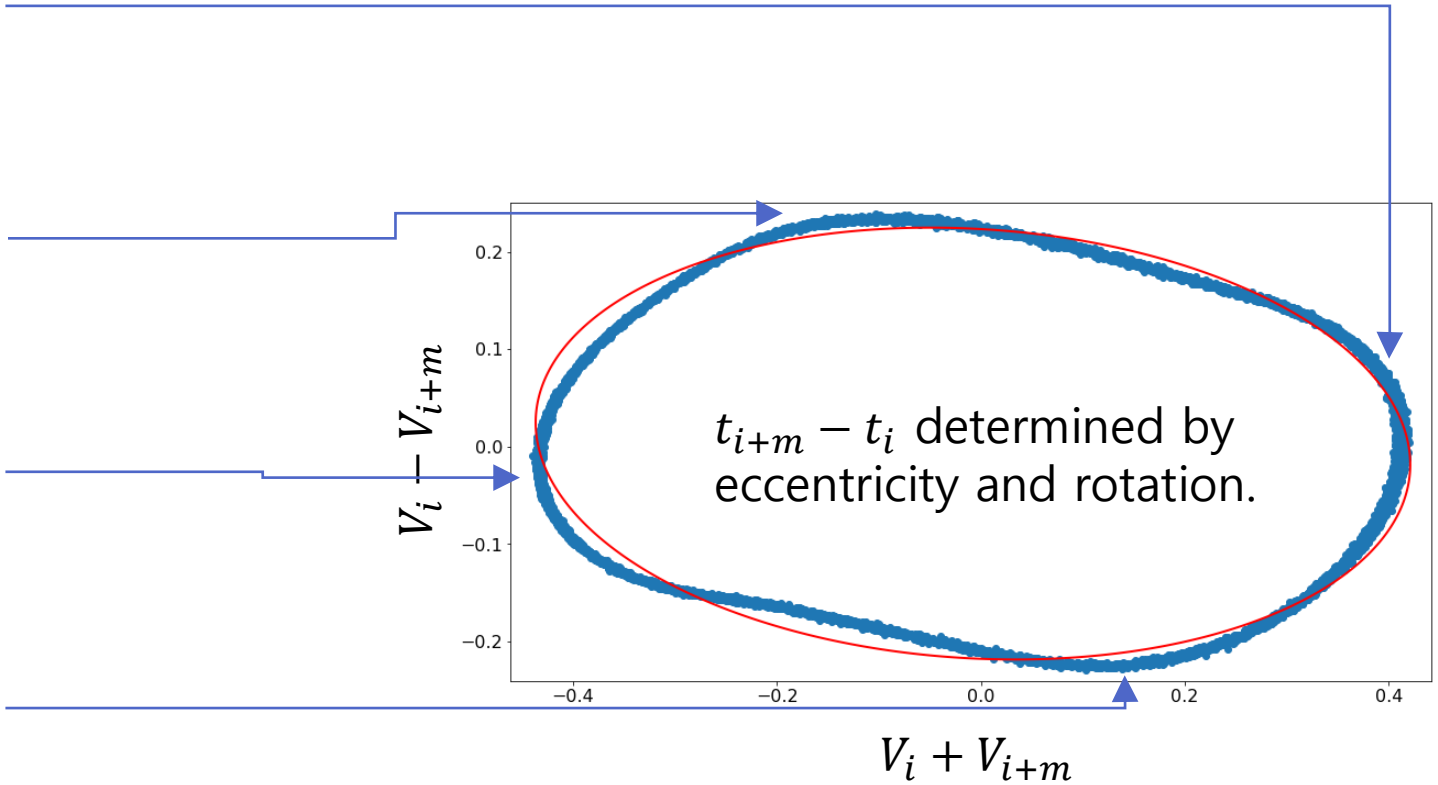
Each element of the VCDL has a different time offset.



K. Nishimura, A. Romero-Wolf, A correlation-based timing calibration and diagnostic technique for fast digitizing ASICs(2011)

1. Measure many events of a sine wave.
2. Sum vs. Difference of two adjacent samples, over all events, form an ellipse.
3. Time offsets can be determined from the ellipse coefficients.

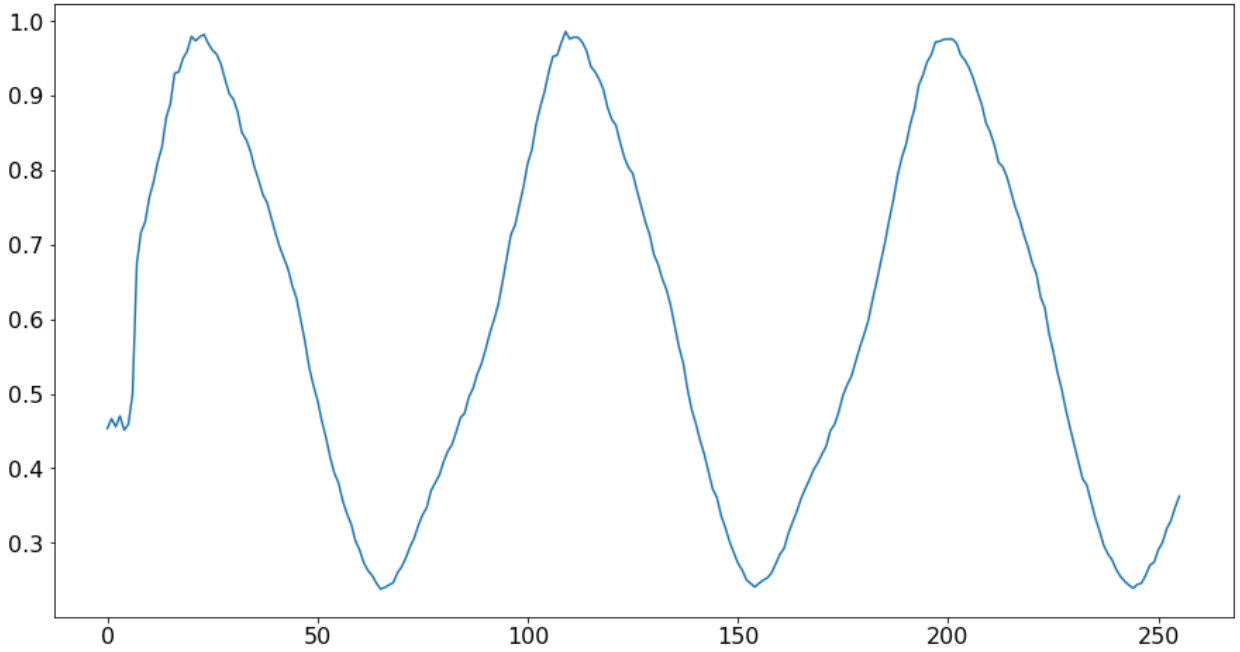


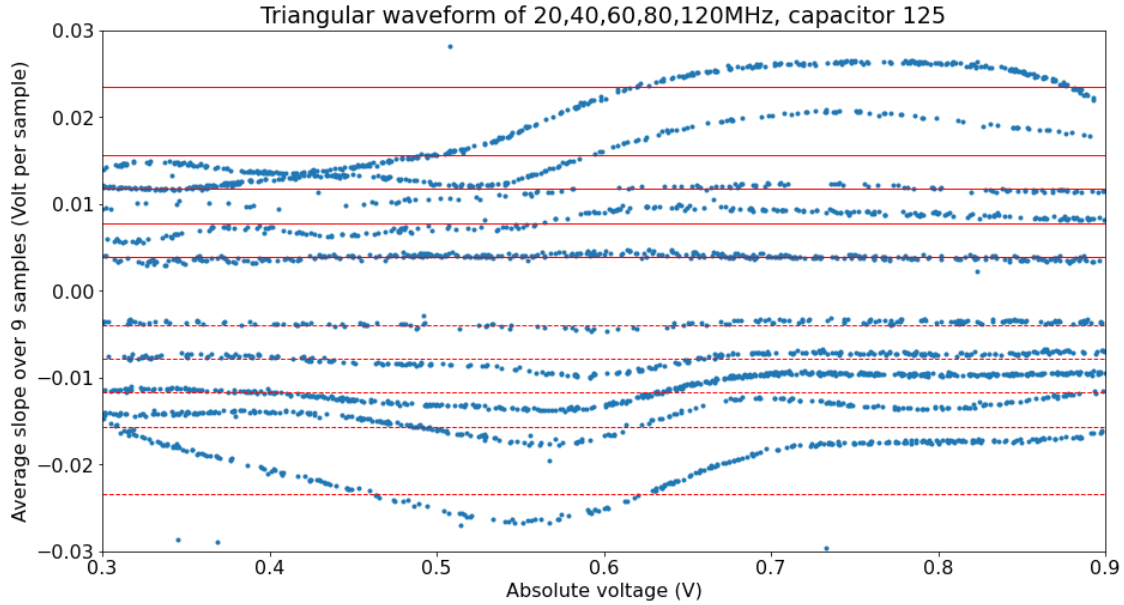


Noise → fainter, more spread curve.
Nonlinearity → distorted curve

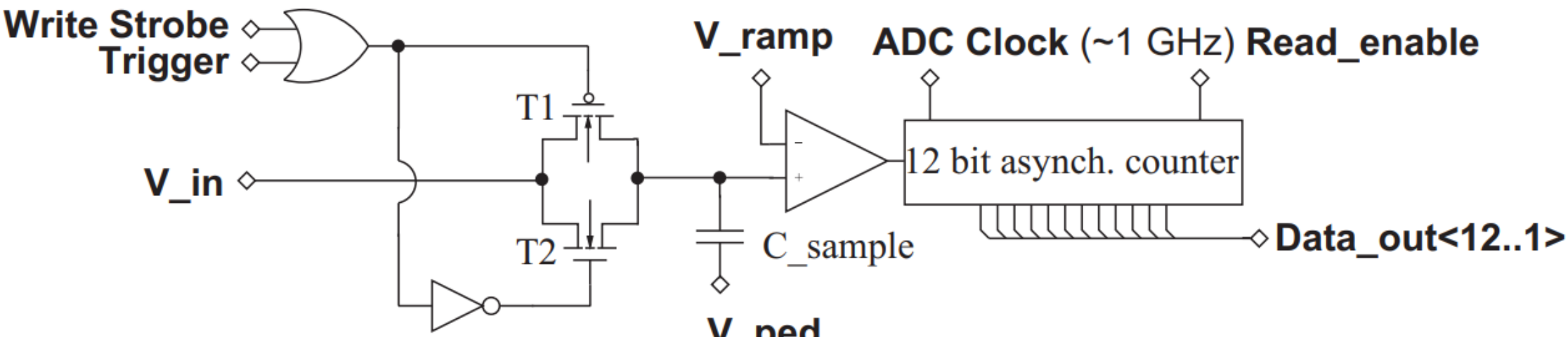
Nonlinearity - Measurement

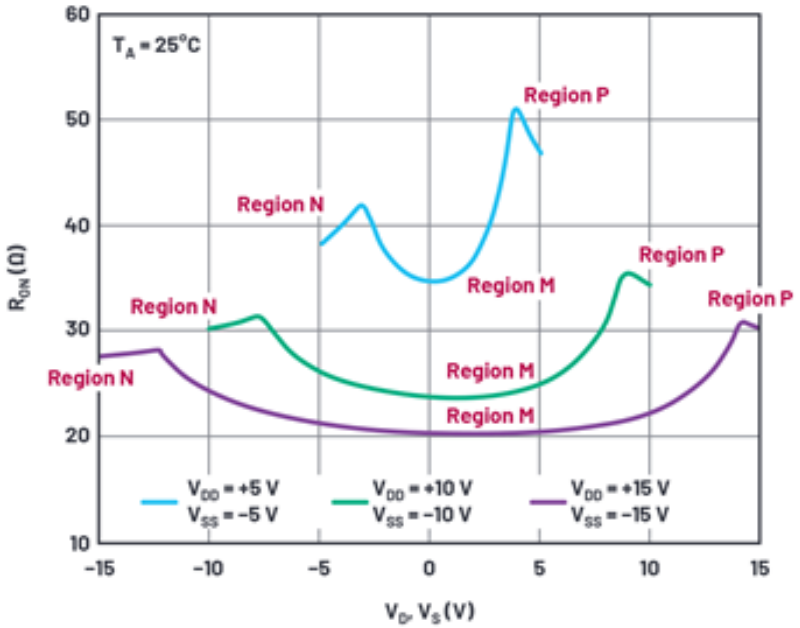
Nonlinearity distorts sine wave input, introducing systematic errors in the ellipse method.





Nonlinearity - Microscopic





Adapted from E. Oberla et al., A 15 GSa/s, 1.5 GHz bandwidth waveform digitizing ASIC(2013)

B. Harvey, On Building Physically Accurate Analog Switch Macromodels, https://www.analog.com/en/analog-dialogue/raqs/raq-issue-173.html

Weighted Least Squares Method

We want to estimate the following quantity:

$$T = \{t_0, \ldots, t_{N-1}\}$$

Where t_i is a time interval between ith and $i+1$th sample.

Conventional method of estimating T is the following:

$$\begin{pmatrix} a_{01} \\ a_{12} \\ \vdots \\ a_{(N-1)N} \end{pmatrix} = \hat{T} = \begin{pmatrix} 1 & 0 & 0 & \cdots & 0 & 0 & 0 \\ 0 & 1 & 0 & \cdots & 0 & 0 & 0 \\ 0 & 0 & 1 & \cdots & 0 & 0 & 0 \\ \vdots & \vdots & \vdots & & \vdots & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & 1 & 0 & 0 \\ 0 & 0 & 0 & \cdots & 0 & 1 & 0 \\ 0 & 0 & 0 & \cdots & 0 & 0 & 1 \end{pmatrix} \hat{T}$$

Where a_{ij} is a measured time interval between the ith and jth samples.

Weighted Least Squares Method

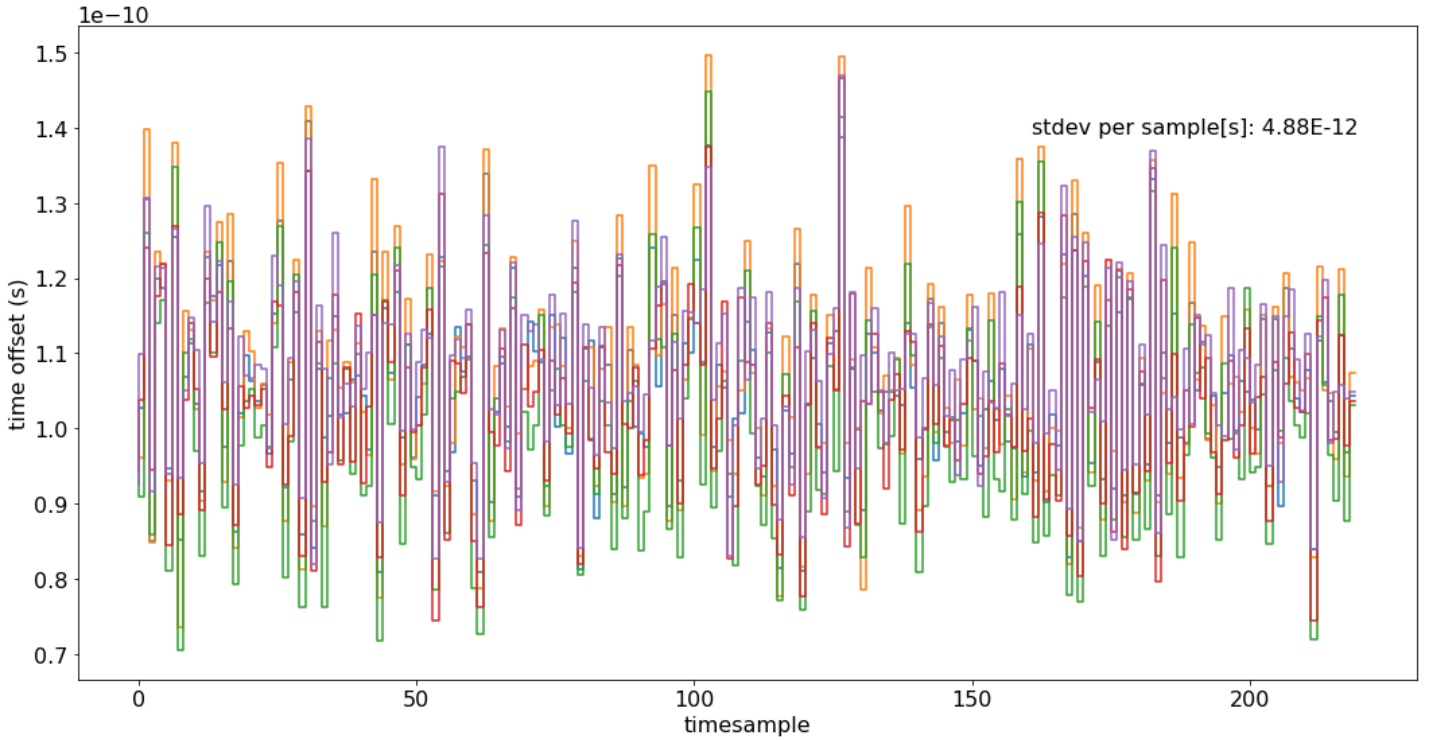
Consider measuring time intervals between ith and $i+2$th sample.

$$\begin{pmatrix} a_{02} \\ a_{13} \\ \vdots \\ a_{(N-2)N} \end{pmatrix} = \begin{pmatrix} 1 & 1 & 0 & \cdots & 0 & 0 & 0 \\ 0 & 1 & 1 & \cdots & 0 & 0 & 0 \\ \vdots & \vdots & \vdots & & \vdots & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & 1 & 1 & 0 \\ 0 & 0 & 0 & \cdots & 0 & 1 & 1 \end{pmatrix} \hat{T}(2)$$

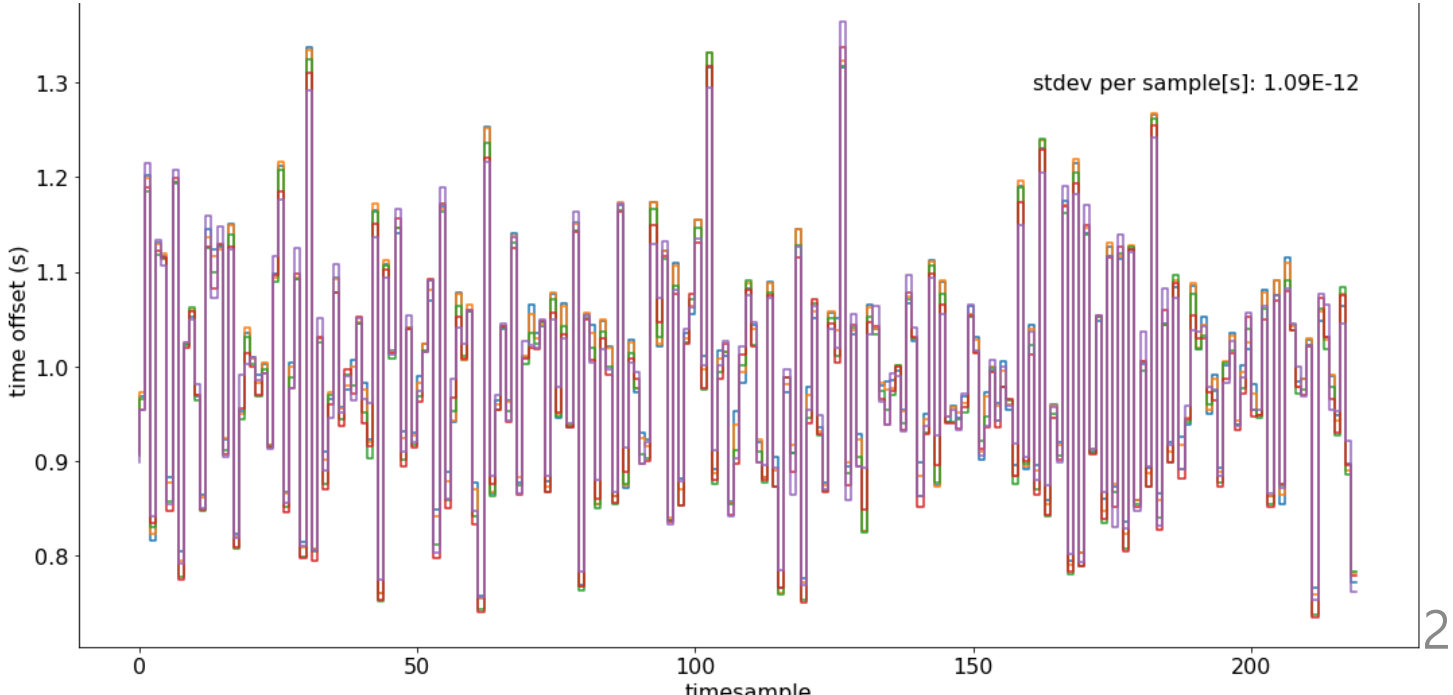
$$\begin{pmatrix} a_{02}/\sigma_{02}^2 \\ a_{13}/\sigma_{13}^2 \\ \vdots \\ a_{(N-2)N}/\sigma_{(N-2)N}^2 \end{pmatrix} = \begin{pmatrix} \sigma_{02}^{-2} & \sigma_{02}^{-2} & 0 & \cdots & 0 & 0 \\ 0 & \sigma_{13}^{-2} & \sigma_{13}^{-2} & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & \sigma_{(N-2)N}^{-2} & \sigma_{(N-2)N}^{-2} \end{pmatrix} \hat{T}(2) = A_2 \hat{T}(2) \qquad \left(a/\sigma^2\right) = \begin{pmatrix} A_1 \\ A_2 \\ \cdots \\ A_k \end{pmatrix} \hat{T}$$

We can use the least squares method to compute $\hat{T}$.

Only using N=1:

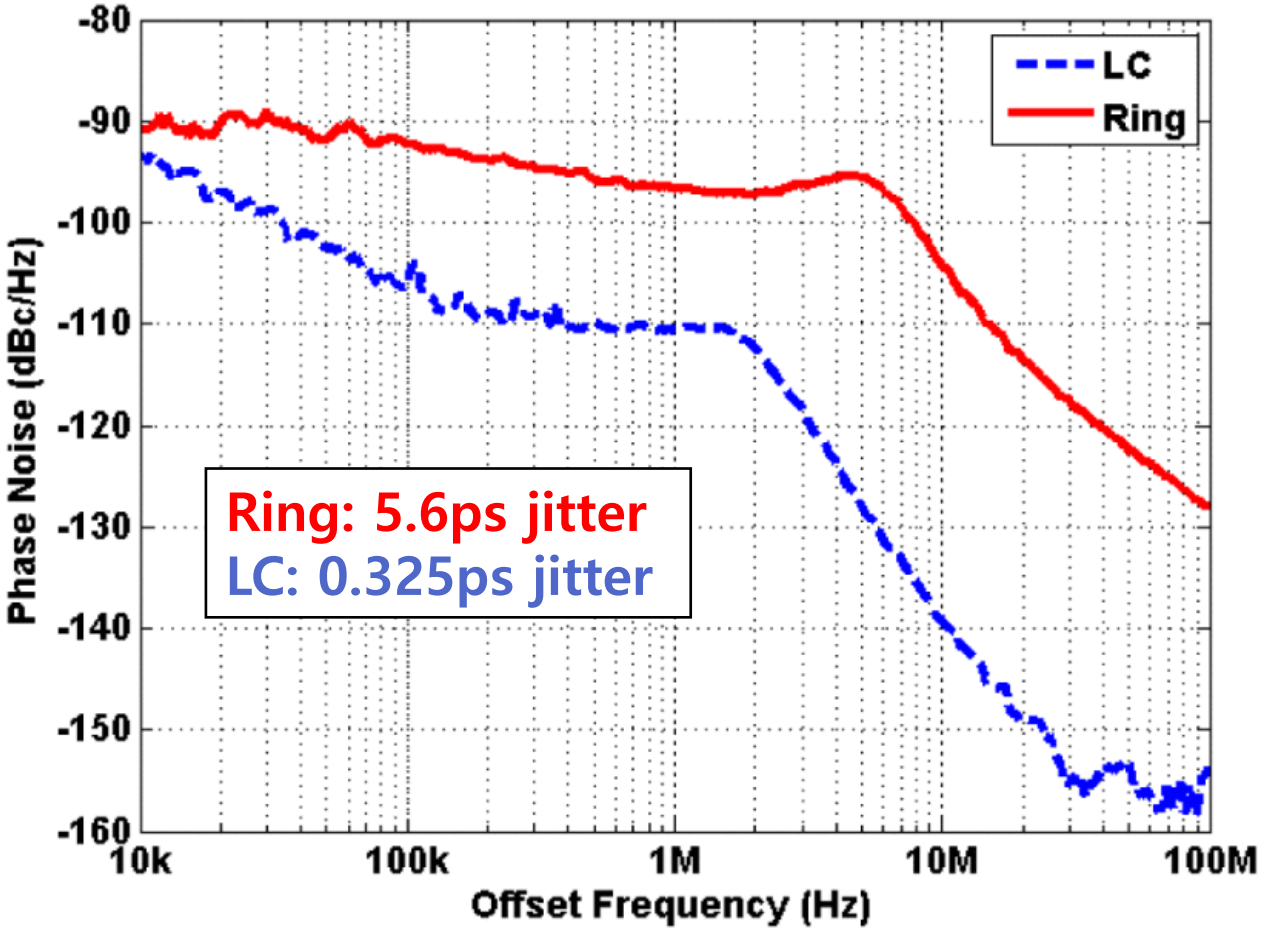


Weighted average N=1-6:



PSEC5 Design Philosophy

Timing uncertainty reduced by an optimized LC-oscillator based PLL



From abstract:
"Both independent PLLs have identical loop dynamics to allow a fair comparison …
Furthermore these circuits consume the same amount of power. The PLLs were processed in a commercial 65 nm CMOS technology."

J. Prinzie, J. Christiansen, P. Moreira, M. Steyaert and P. Leroux, "Comparison of a 65 nm CMOS Ring- and LC-Oscillator Based PLL in Terms of TID and SEU Sensitivity," in *IEEE Transactions on Nuclear Science*, vol. 64, no. 1, pp. 245-252, Jan. 2017.

Comparison to other ASICs

Project	Sampling Frequency (GHz)	Input Bandwidth (GHz)	Buffer Length (Samples)	Number of Channels	Timing Resolution (psec)
ASoC	3-5	0.8	16,000	4	35
SAMPIC	3-10	2.5	64	16	10
HDSoC	1-3	0.6	2000	64	80
AARDVARC	8-14	2.5	32,000	4	10
AODS	1-2	1.0	8000	4	100
UDC	8-10	1.5-2	4000	16/32	10
PSEC4	5-17	1.6	256	6	5
PSEC5	5-40	**3.0**	**4096/64**	**9**	**1**

H. Frisch et al., A High-Performance Multi-Channel Low-Power ASIC with One Pico-second Resolution for Emerging Detector Technologies in Positron-Emission Tomography, Particle Physics, and Astrophysics