LATEST DEVELOPMENTS ON & AROUND SAMPIC

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INTRODUCTION

- I would like to measure the time precisely …
- I have quite a lot of channels …
- I have a reasonable counting rate …
- I have limited money …
- …and I really would like to see the shape of my signals!

A trade-off would be **a TDC providing just the adequate slice of Waveform** …

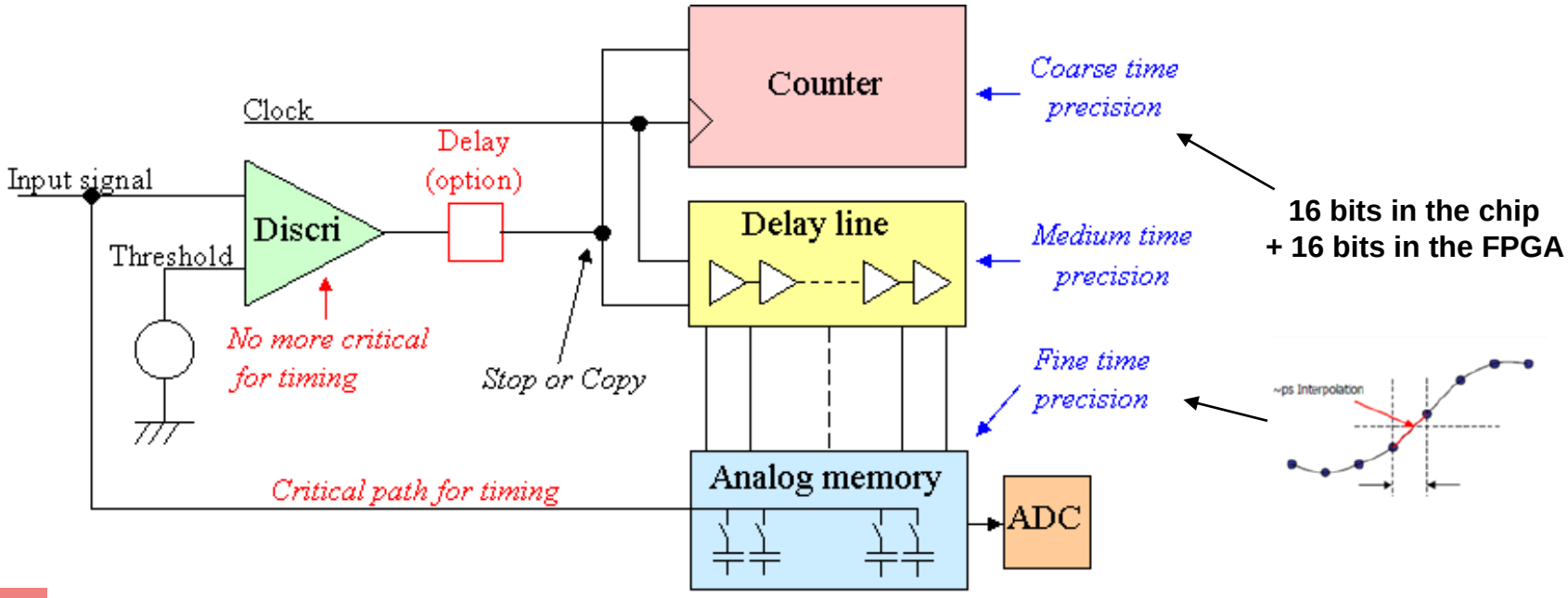
STRUCTURE OF THE WAVEFORM TDC

- **Mix of DLL-based TDC and of analog-memory based Waveform Digitizer**

- The TDC gives the time of the samples and the samples give the final time precision after **interpolation** => **resolution of a few ps rms**

- Digitized waveform gives **access to signal shape**…

- Conversely to TDC, discriminator is used only for triggering, **not for timing**

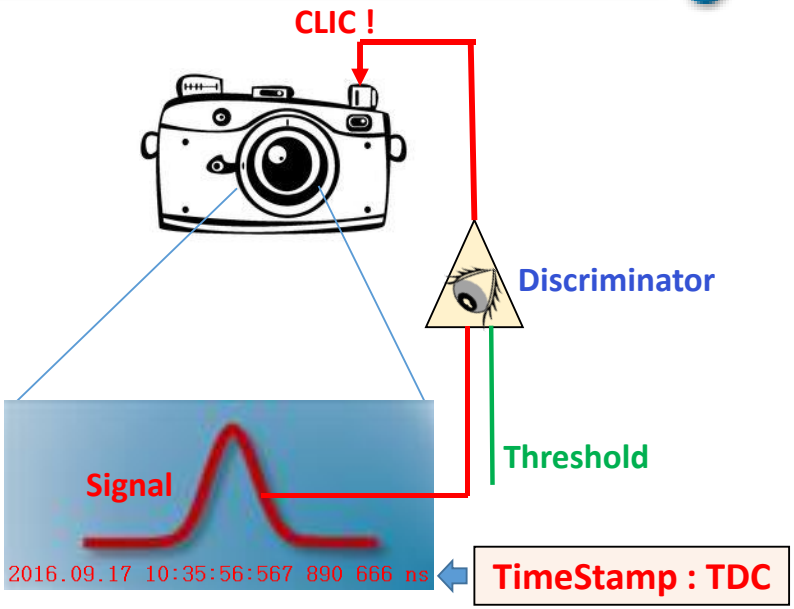


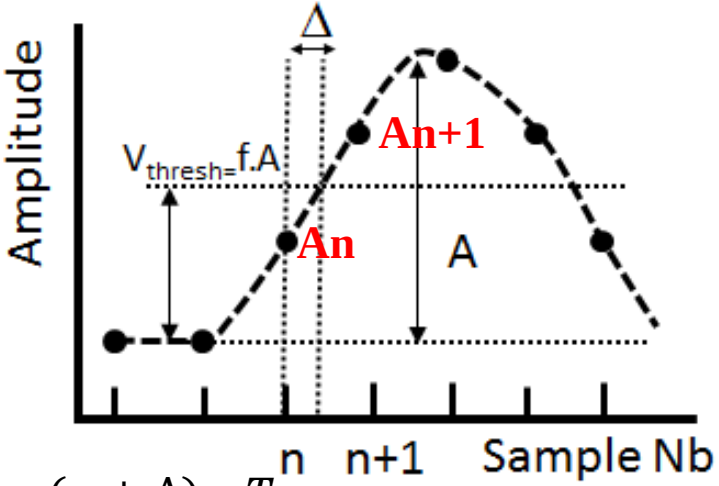
© Patented Structure

CONCEPT OF "WAVEFORM TDC"

WTDC: a TDC which also permits **taking a picture of the real signal**. This is done via sampling and digitizing only the interesting part of the signal.

Based on the digitized samples, making use of **interpolation** by a digital algorithm, fine time information will be extracted.





$$t_0 = (n + \Delta) * T_s$$

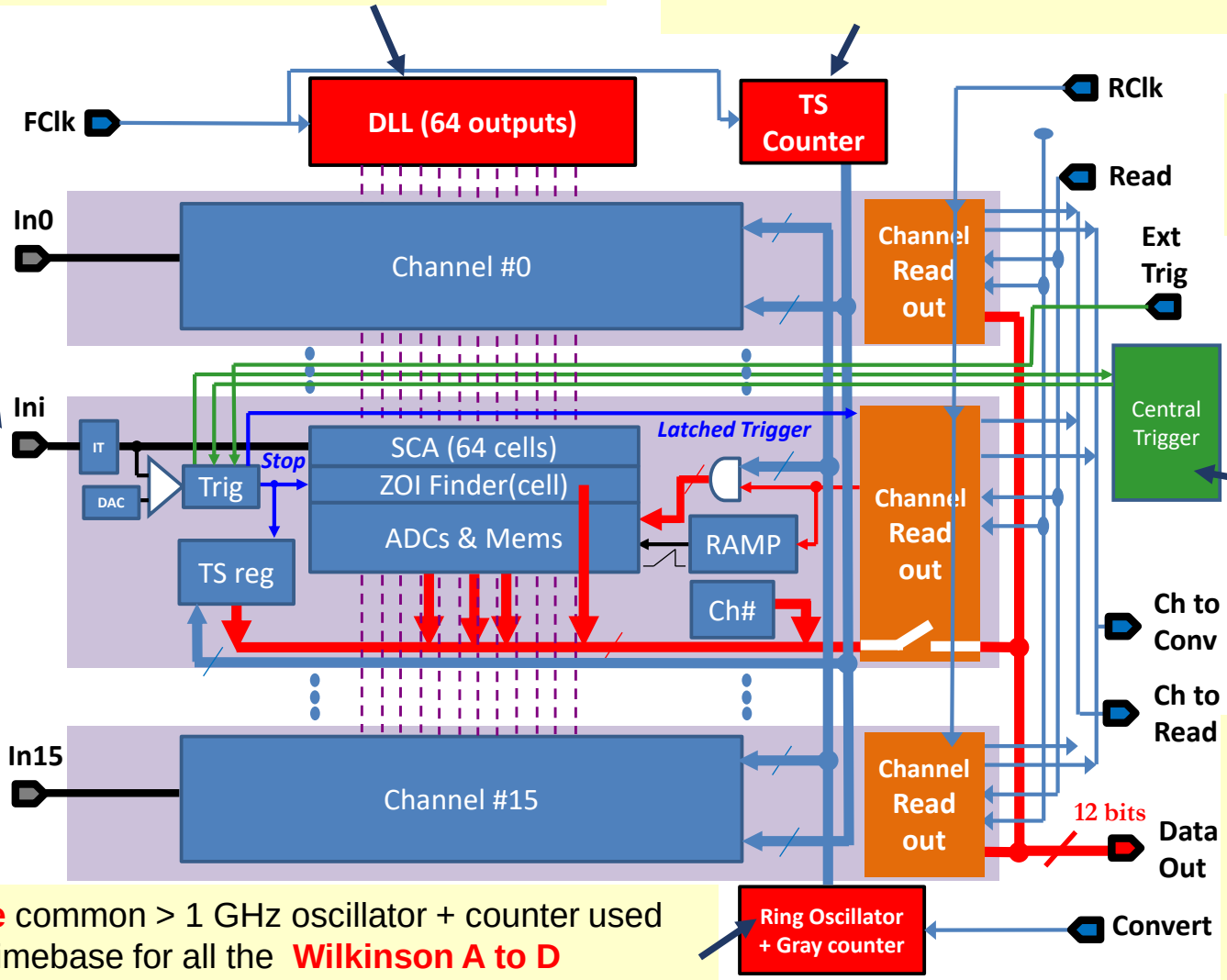
with $\Delta = \frac{f*A - A_n}{A_{n+1} - A_n}$

- Advantages:
  - Time resolution ~ **few ps rms**
  - **No "time walk" effect**
  - Possibility to extract other **signal features**: charge, amplitude…
  - **Reduced dead-time**…
- But:
  - waveform conversion (**200 ns to 1.6 µs**) and readout times are fast but don't permit counting rates as high as with a classical TDC

GLOBAL ARCHITECTURE OF SAMPIC

One Common servo-controlled DLL: (from 0.8 to 10,2 GS/s) used **for medium precision timing & analog sampling**

One Common 16-bit Gray Counter (FClk up to 160MHz) for **Coarse Time Stamping (TS)**.



16 Channels, each with:

-1 discriminator for self triggering

-Registers to store the timestamps

- 64-cell deep SCA analog memory

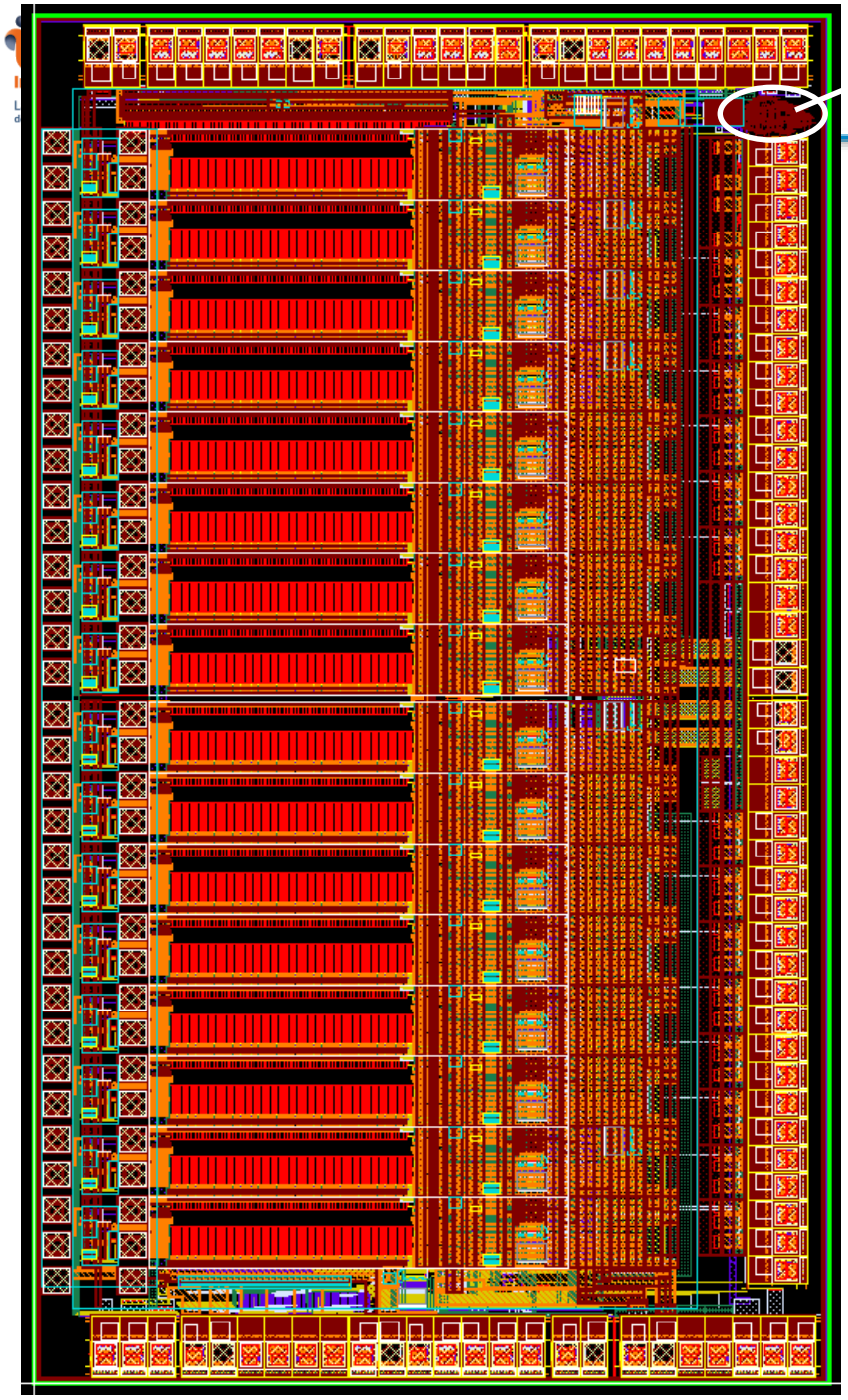
- 11-bit ADC/ cell
(Total : 1024 ADCs)

SPI Link for Slow Control

One Central Trigger block

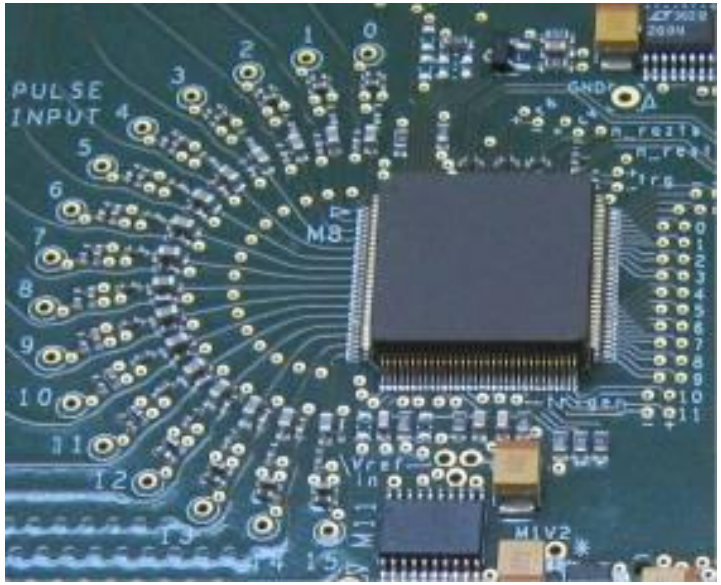
Read-Out interface: 12-bit LVDS bus running at > 160 MHz (> 2 Gbits/s)

One common > 1 GHz oscillator + counter used as timebase for all the **Wilkinson A to D converters**.



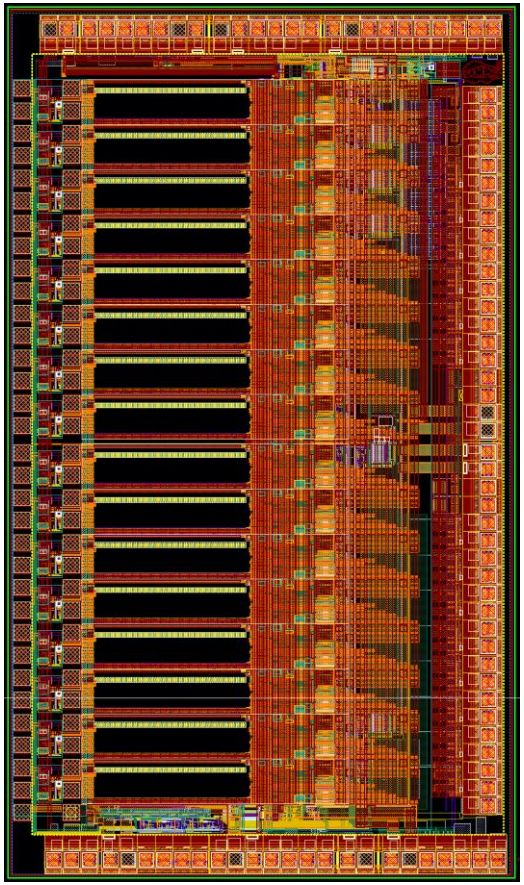
SAMPIC ASIC

- Most produced version is V3D (should have been called V4) submitted in December 2017 but received only in January 2019
- 1300 chips have been packaged in 128-pin plastic TQFP package



- Technology: **AMS CMOS 180nm**
- Surface: 8 mm^2
- Package: QFP 128 pins, pitch of 0.4mm

RECENT ASIC DEVELOPMENTS

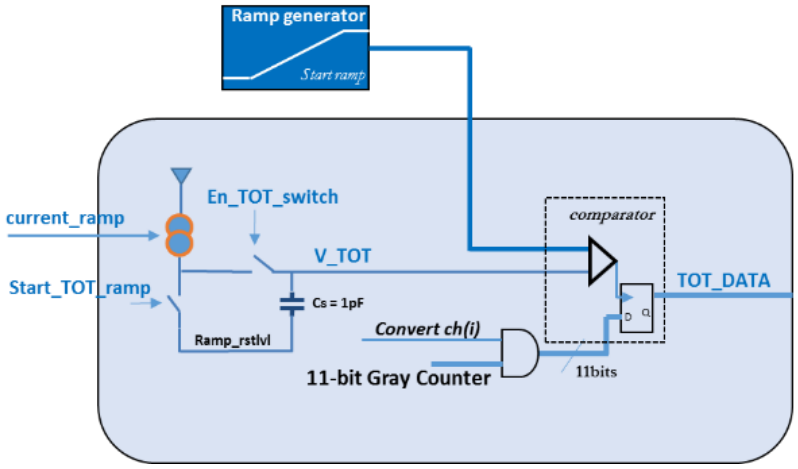


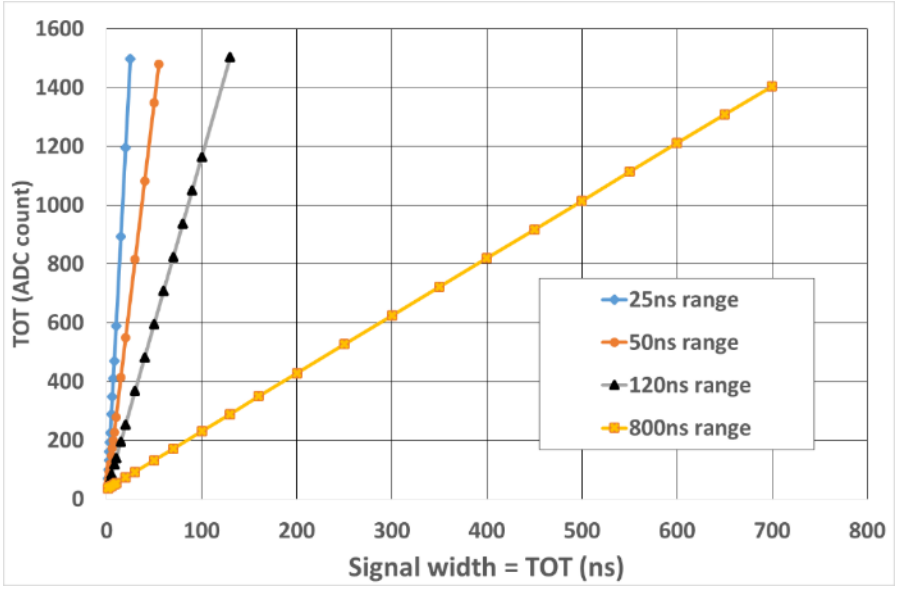
SAMPIC_V5
(TSI 0,18µm technology)

- Due to the (temporary ?) stop of the CMOS 0.18µm technology at AMS, we looked for equivalent ones.
- **TSI Microelectronics** is also proposing his own version of the former IBM CMOS 0.18µm technology, with some rule differences with AMS on the top metal layers.
- **We migrated** the design to TSI technology => **SAMPIC_V5**.
- We took benefit of this new submission for improving some historical weaknesses (sampling at **10.2 GS/s**, first sample, linearity of posttrig delays, internal calibration of ADC, …)
- We also designed **a second version dedicated to slower sampling,** covering the range **between 350MS/s and 2GS/s**.
  - Fully pin to pin compatible. Only difference is the main clock frequency.
- Both versions submitted in January 2021. Back in May (very effective work of TSI), packaged end of May 2021

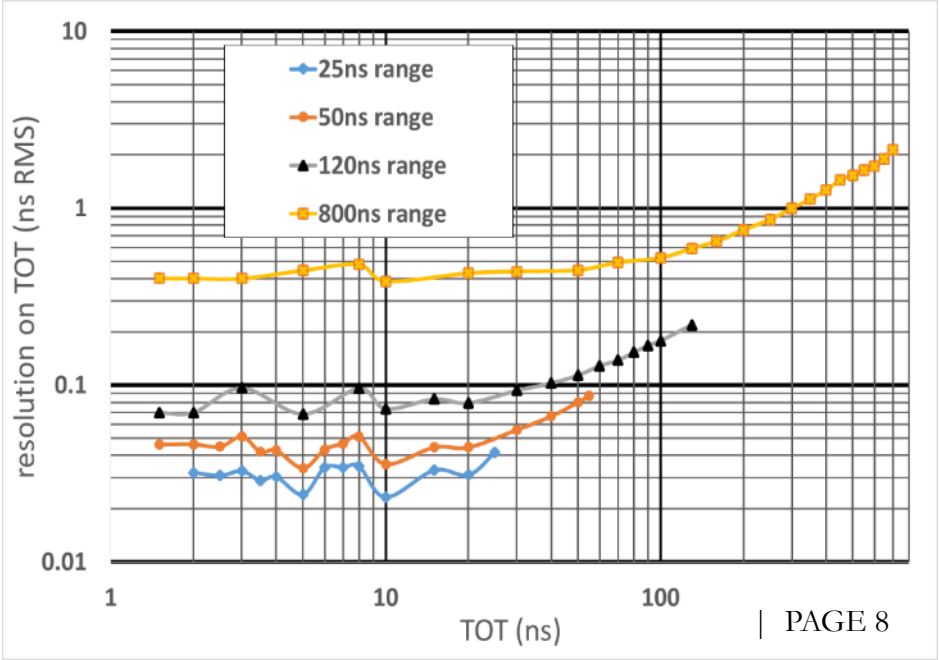
TOT MEASUREMENT

- SAMPIC is meant for **digitizing a short signal**, or only a **small part of a longer one** (eg rising edge) to extract the timing ➔ then **the other edge** is skipped
- Addition of a **ramp-based Time to Amplitude Converter** in each channel seen as a 65th memory cell during digitization → ~10bit TOT TDC
- A **TOT-based filter** is also integrated in the chip





Measurement ranges between 2 and 700 ns.



SAMPIC MAIN FUNCTIONALITIES (FROM V3)

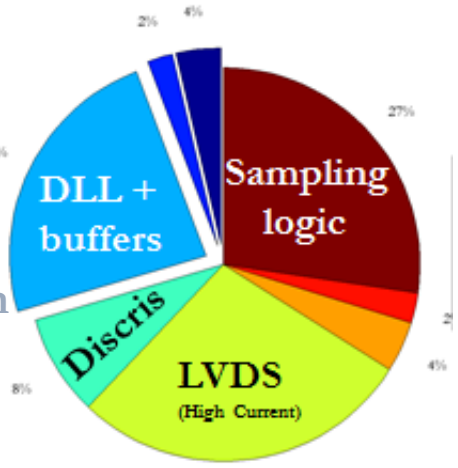
- **Waveform Sampling:**
  - Circular analog memory, sampling from **1.6 to 10 GS/s**
  - **64 samples** (memory depth) , possibility to read less samples => Smart Read mode of ROI
- **Triggering:**
  - **Self-Trigger :** individual on chip discriminators, channels are **independent.**
  - **Central Trigger:** (OR, **multiplicity of 2 & 3**) with possibility of **common deadtime or** selecting **only channels** participating in decision.
  - **Channel chained :** (to previous one)
  - **"Ping-Pong" or Toggling Mode:** channels work in pairs.
  - **PostTrig** (**8-step full window** very useful for low frequencies)
  - **TOT-Filter** : events are rejected based on the TOT value.
- **On-Chip Measurements:**
  - **ADC conversion** (selectable between 7 and 11 Bits)
    - **Auto-Conversion :** conversion automatically started when an event is detected, independently for each channel.
    - **Handshake with FPGA** : permits building 2nd and 3rdLevel triggers based on many chips or boards for a common event selection
  - **TOT :** based on the signal of the discriminator
- **AUTO Calibration** :
  - Dedicated signal sources are implemented in the chip in order to perform **time INL calibration** in standalone and **ADC calibration**.
- **Integrated DACS:**
  - all necessary DACs for controlling the chip are integrated

(current ramp for ADC, Ring Osc, TOT etc…)

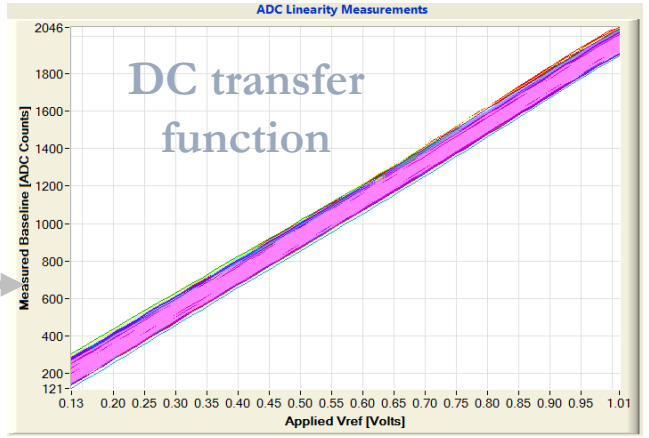
GLOBAL PERFORMANCES (V3 – V5)

- Power consumption: ~**10mW/channel**
- 3dB bandwidth > **1 GHz**
- **Sampling rate** up to **8,5 (10.2) GS/s**
- Discriminator noise **~ 2 mV rms**
- Counting rate **> 2 Mevts/s** (full chip, full waveform), up to 10 Mevts/s with Region Of Interest (ROI)

Power distribution

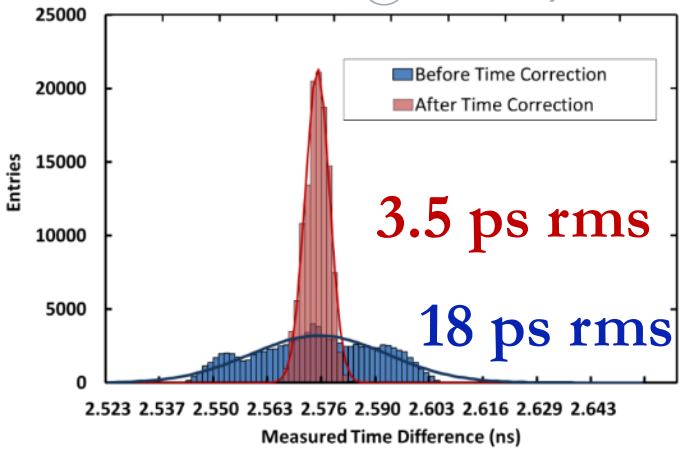


- Wilkinson **ADC conversion** @ ~**1 (1,45) GHz**
  - Dynamic range of **1V**
  - Gain dispersion between cells ~ **1%** rms
  - Non linearity **< 1.4 %** peak to peak
  - After correction of each cell (linear fit): noise = **0.7** (10GS/s) **to 1.3 mV rms** (1.6 GS/s)



- **Time Difference Resolution (TDR):**
  - Raw non-gaussian sampling time distribution due to DLL non-uniformities (TINL)
  - Easily **calibrated & corrected**
  - TDR goes from ~ **< 5** (10GS/s) **to ~18 ps rms** (1.6 GS/s)

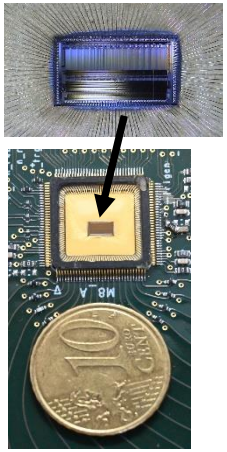
Ex: TDR @ 6.4 GS/s



SAMPIC: PERFORMANCE SUMMARY

		Unit
Technology	AMS CMOS 0.18µm	
Number of channels	16	
Power consumption (max)	180 (1.8V supply)	mW
Discriminator noise	2	mV rms
SCA depth	64	Cells
Sampling speed	0.8 to 10.2	GSPS
Bandwidth	> 1	GHz
Range (unipolar)	~ 1	V
ADC resolution	7 to 11 (trade-off time/resolution)	bits
SCA noise	~ 1	mV rms
Dynamic range	> 10	bits rms
Conversion time	0.1 (7 bits) to 1.6 (11 bits)	µs
Readout time / ch @ 2 Gbit/s (full waveform)	< 450	ns
Single Pulse Time precision before correction (4.2 to 10.2 GS/s)	< 15	ps rms
Single Pulse Time precision after time INL correction (4.2 to 10.2 GS/s)	< 3.5	ps rms

FROM THE CHIP TO THE SYSTEMS



BASIC QUESTIONS LINKED TO SYSTEMS DEVELOPMENT

- **Integration**
  - Connectors for fast and numerous analog signals, crosstalk
  - Number of components on board

- **Clock distribution and Synchronization :** inside module/crate, and between systems.

- **Data Acquisition**
  - Software/ Libraries ➔ plug and play for physicists!
  - Data Saving to disk

- **Calibration**
  - If available, self-calibration can be performed on-detector

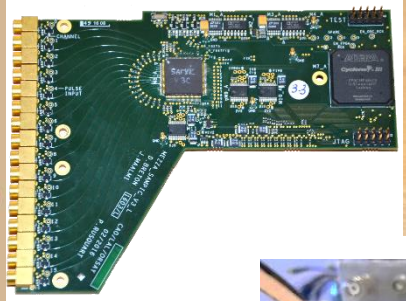
- **Triggering**
  - Coincidences, Combinatory logics, External Trig ➔ System Level
  - Self-triggering → buffers become full → potential loss of hit correlation

SAMPIC MODULES

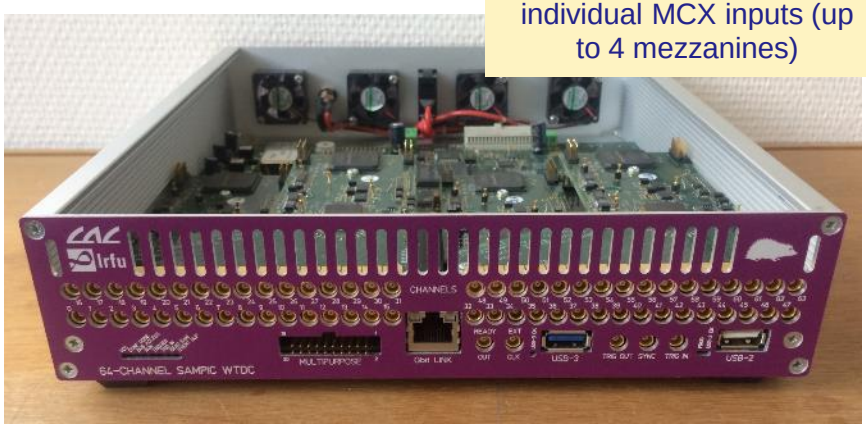
- Based on users requests, we developed **many different types of modules** in order to offer a wide range of channel number and connectivity options
- **16-, 32-, 48- and 64-channel** modules are available.
- Motherboard: synchronization, triggering, and acquisition.
- Daughter-board: Front-End Interface with SAMPIC
- Acquisition through **Gbit Ethernet UDP** (RJ45 or Optical), **USB2**

16 or 32-channel module (1 or 2 mezzanines)

16-channel mezzanine



64-channel module with individual MCX inputs (up to 4 mezzanines)

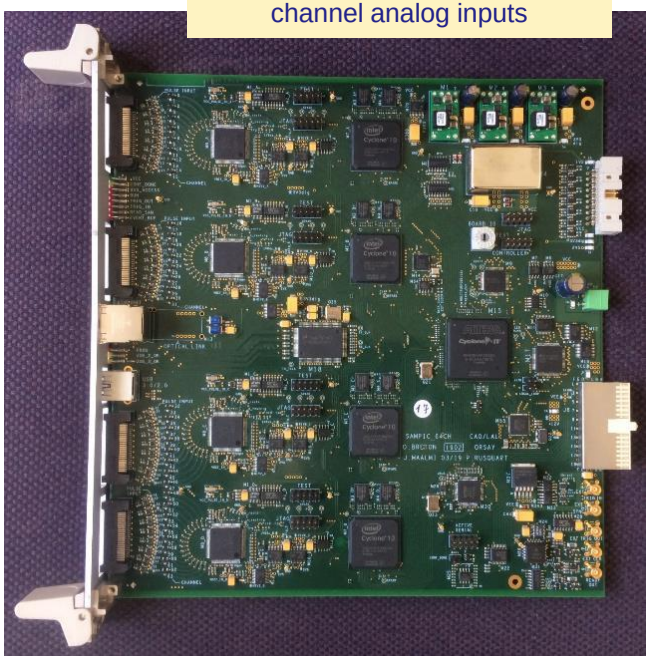


64-channel module with 16-channel input connectors (SAMTEC QRF8) (can be analog or differential digital) based on a **64-channel board**

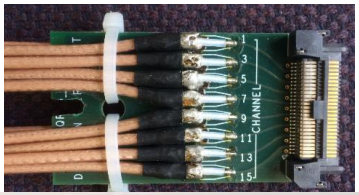
SAMPIC 256-CHANNEL CRATE

- **256-channel mini-crates** have also been developed based on the 64-ch board.
  - A **new control and DAQ software** has been developed together with a C library
- Central **Control Board** permits smart **3rd level triggering** and acquisition through **Gbit Ethernet UDP** (RJ45 or Optical), **USB2** **(USB3 requires fw/sw development)**
- Time difference resolution at crate level remains **of the order of 5ps rms**.
- **512-channel system**: synchronizing two crates one master & one slave crate
- **Mezza-Master boards** have been developed as mezzanines for running synchronously **up to 8 crates** (**2048 channels**) making use of the 6U, 4-slots motherboard (needs fw/sw developments)

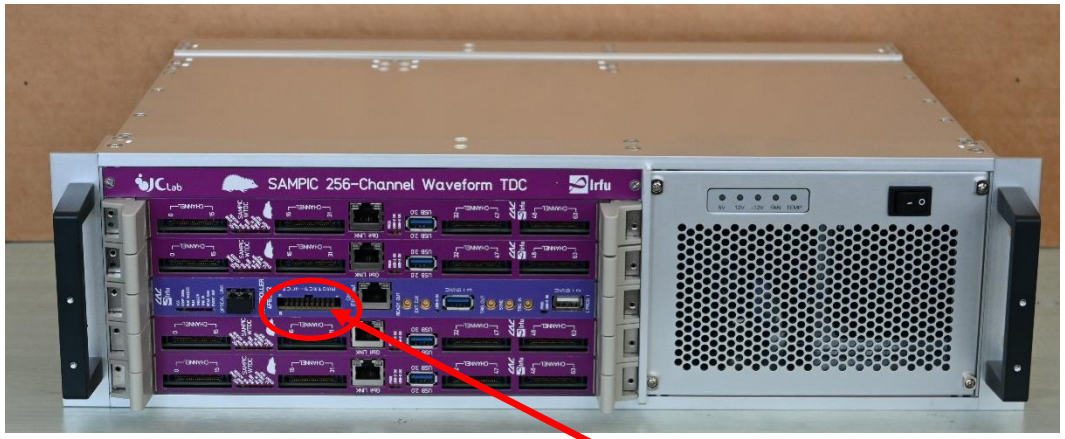
64-channel board with 16-channel analog inputs



16-channel coaxial to SAMTEC QRM8 interface board



Master boards for multi-crate synchronization

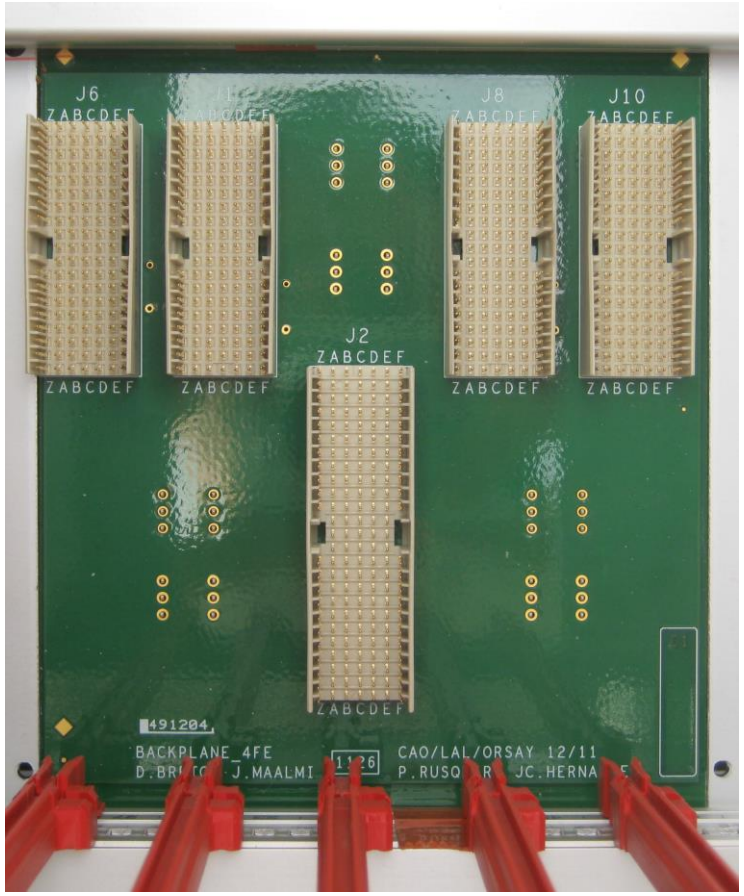


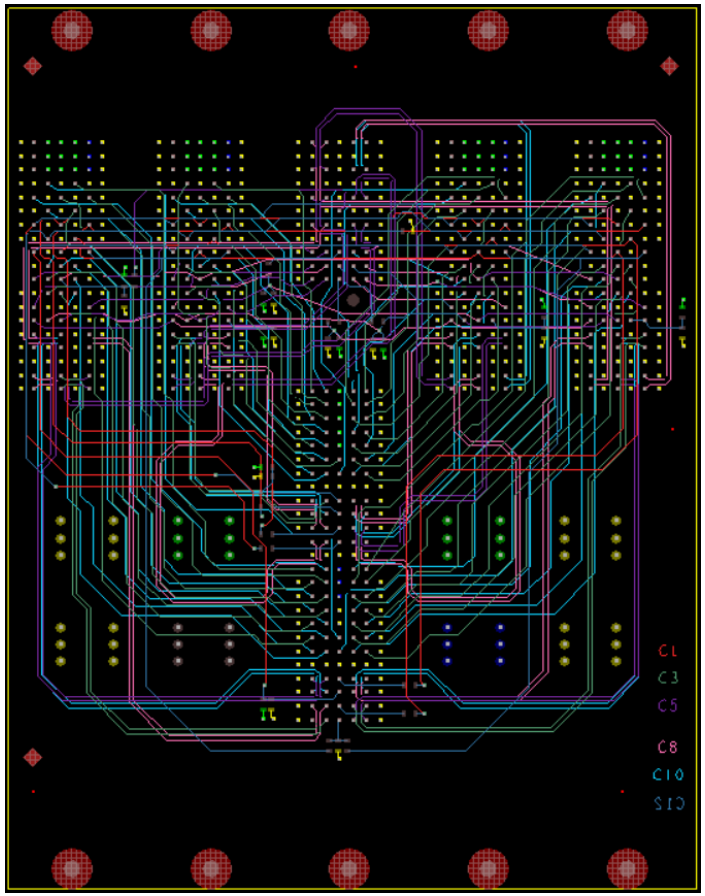
256-channel crate

Multipurpose IO connector

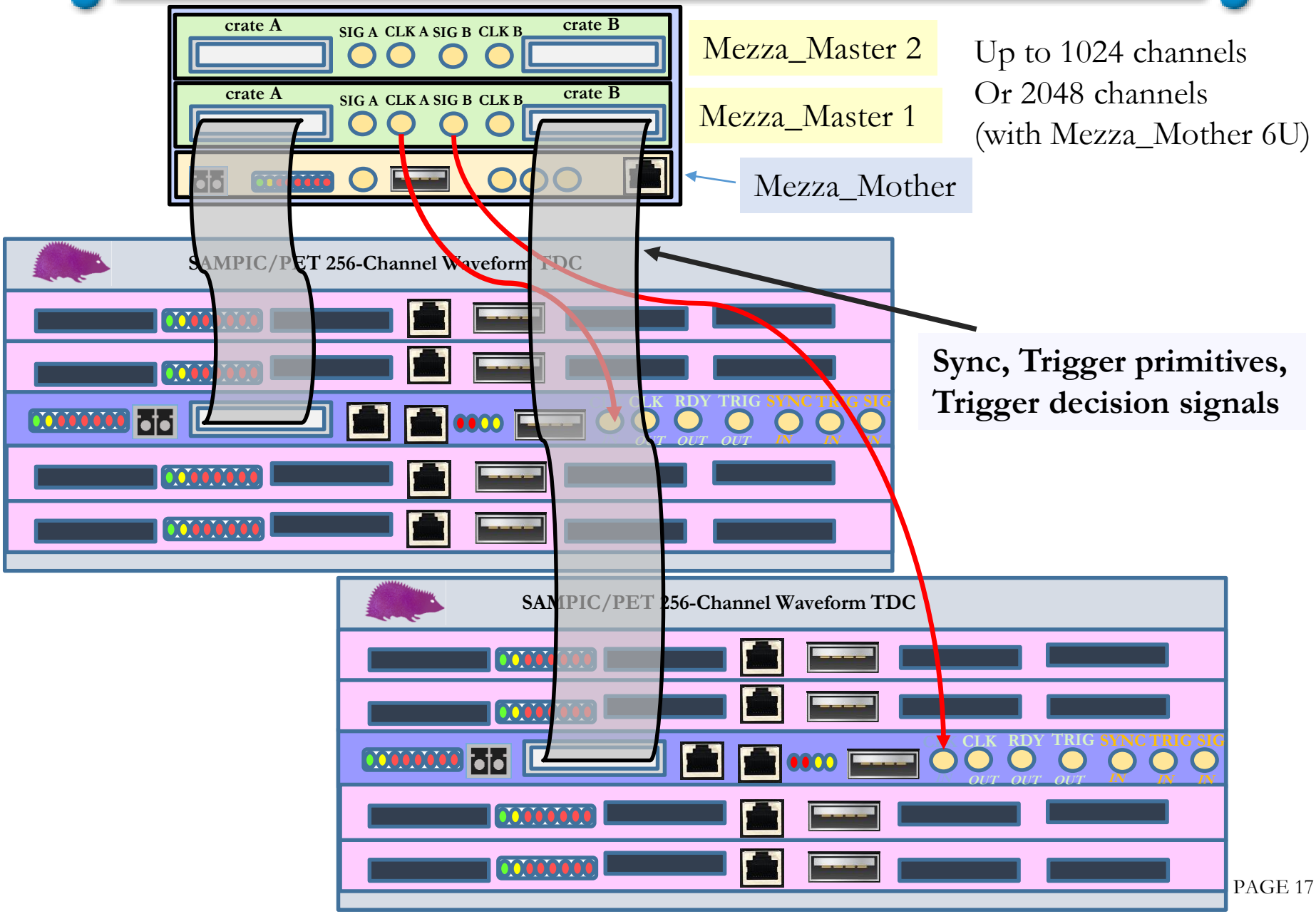
ZOOM ON CRATE BACKPLANE

- We have developed our own backplane housing : **clock** and **sync distribution** (LVDS diff), **smart trigger** construction and distribution, **buffer saturation management**, and **data readout** (choice between parallel and series links).





MULTIPLE CRATES SYSTEMS :
NEW CONTROL BOARD & NEW MASTER BOARD

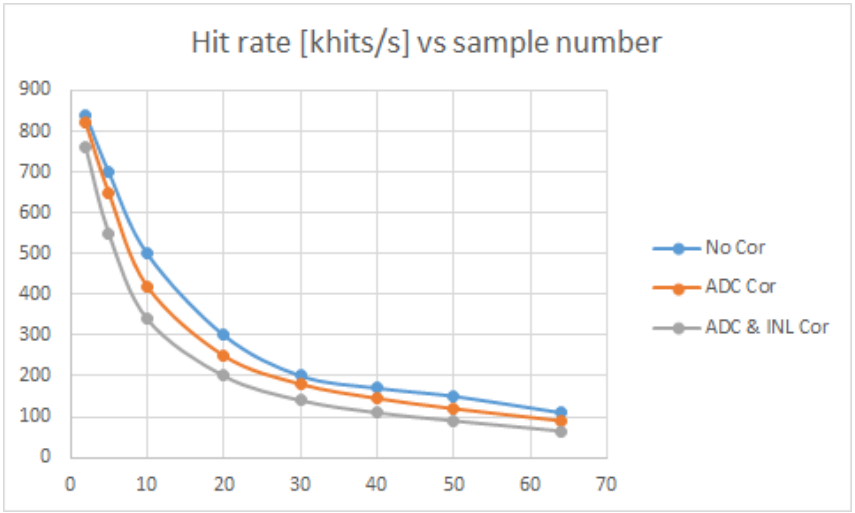


ACQUISITION SOFTWARE + C- LIBRAY

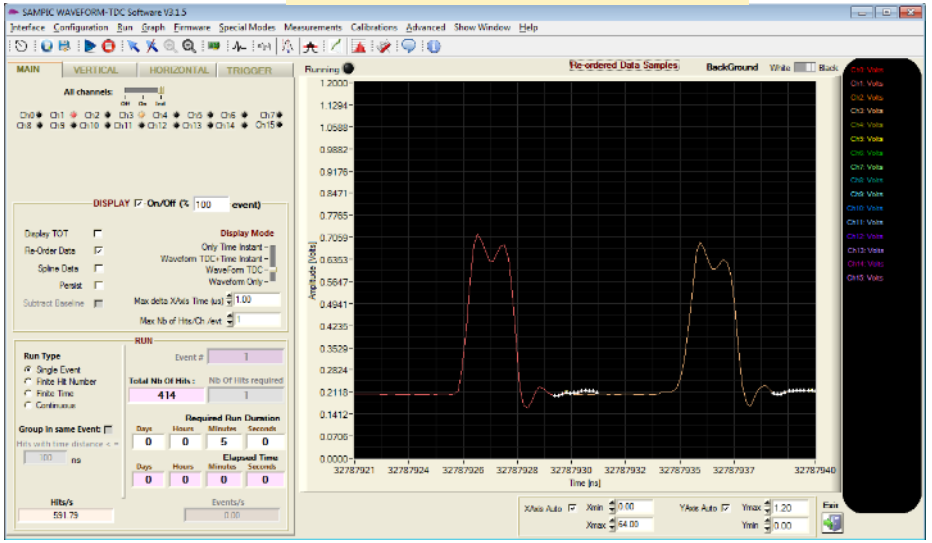
- **An acquisition software** has been developed up to 64 or 256 channels (also C libraries for the 256ch Crate) ➔ LabWindows CVI

=> full characterization of the chip & modules

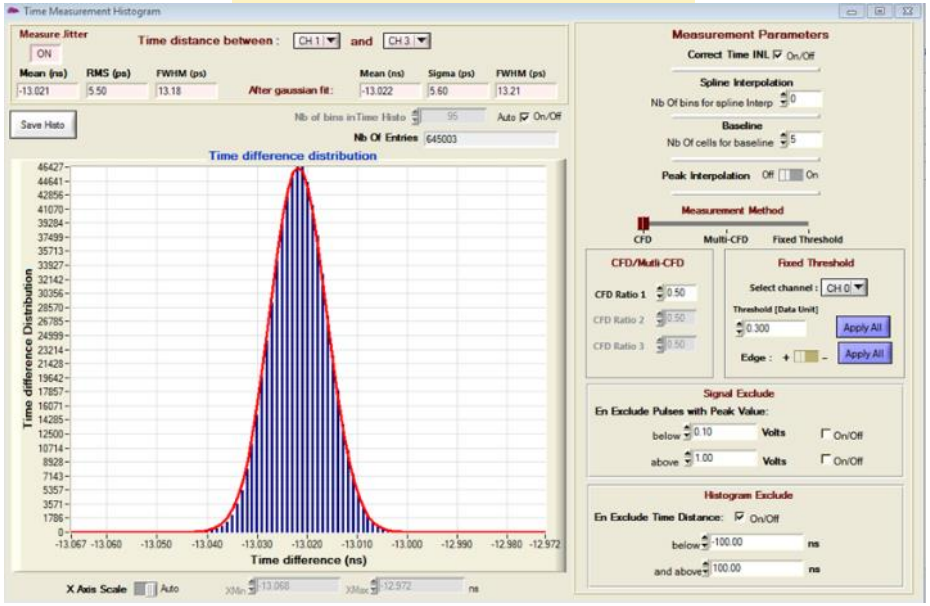
- Data saving on disk.
- Currently used by all SAMPIC users.
- Time measurement panel that permits selecting the parameters used for t**ime extraction**
- **New: TCP-IP Server** (available on the 256-ch software, soon on the 64-ch one): permits system configuration, start/stop and **data streaming**
- **Recorded hit rate** (vs nb of samples)



Main panel



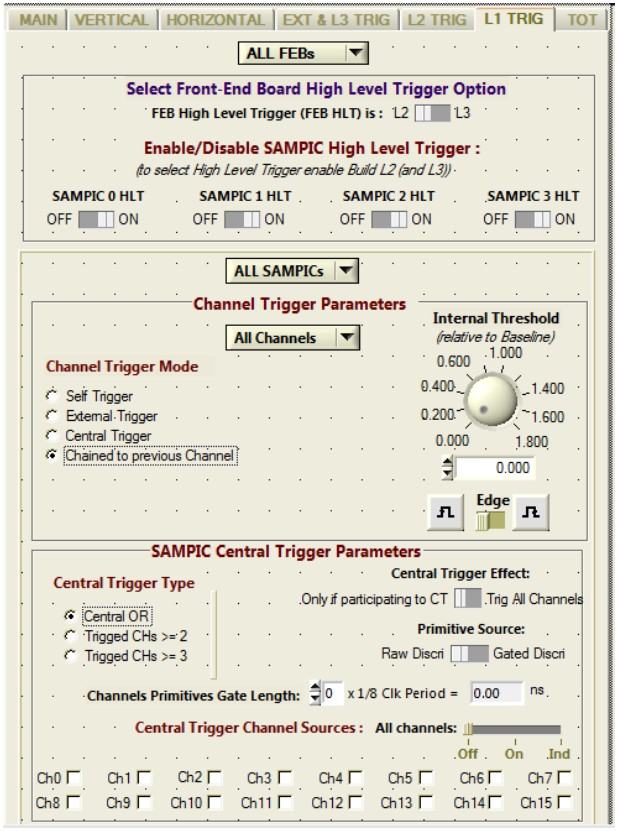
Time Measurement panel



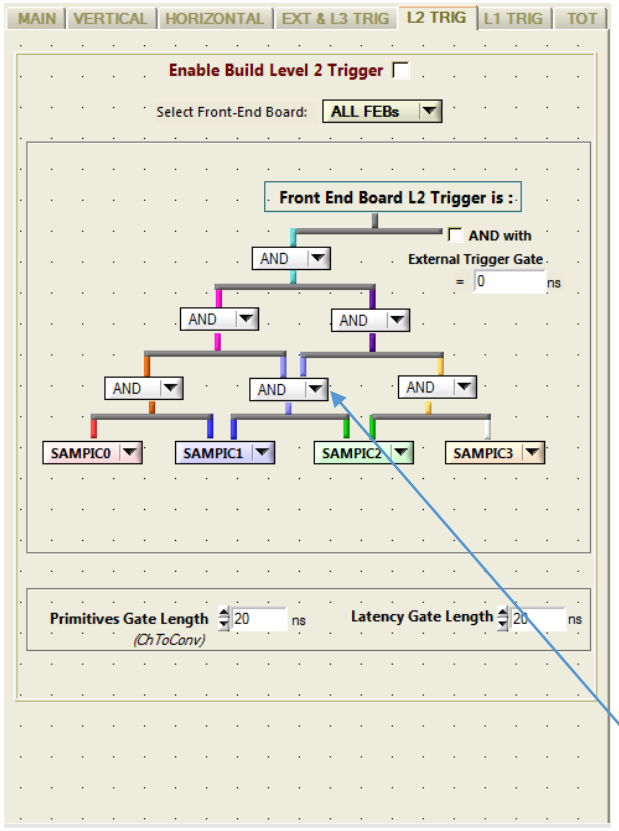
TRIGGER IN 256-CHANNEL SYSTEM

A powerful and fully configurable trigger scheme has been implemented in the 256-channel system:

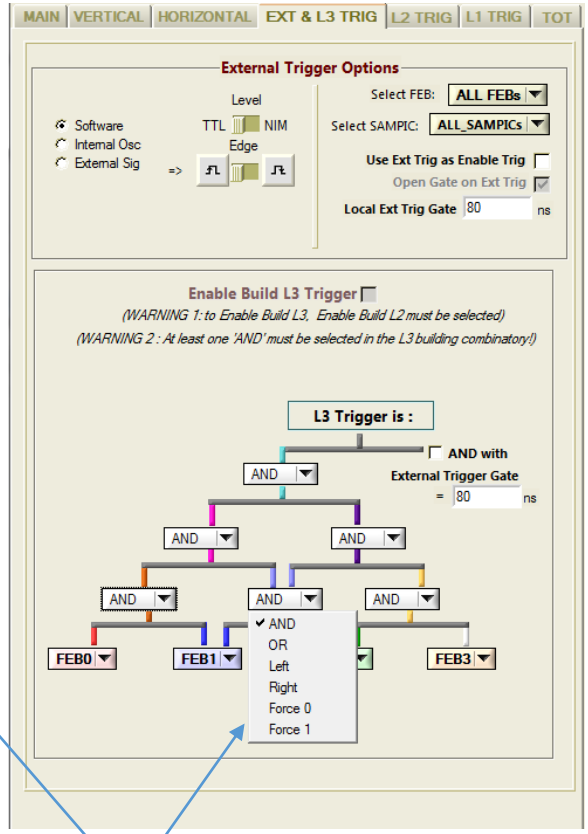
Panel for L1 TRIGGER (each FE board)



Panel for L2 TRIGGER (each FE board)



Panel for L3 TRIGGER (Controller board)



6-option menu

CALIBRATIONS

Different Calibrations are needed for SAMPIC :

- **ADC calibration**:
  - Voltage ramp: DAC inside the chip ➔ automated calibration.
    ➔ based on **number of bits** chosen for the conversion (7 to 11 Bits).
  - Transfer function: **gain** and **offset** of each Wilkinson ADC converter
    - Need to **vary input signal**
    - External DAC for the Baseline on the board
    - **Internal DAC** for internal calibration injected on the input

- **Trigger Threshold Offsets**: DAC inside the chip ➔ automated calibration (ramp fit or for fixed baseline)

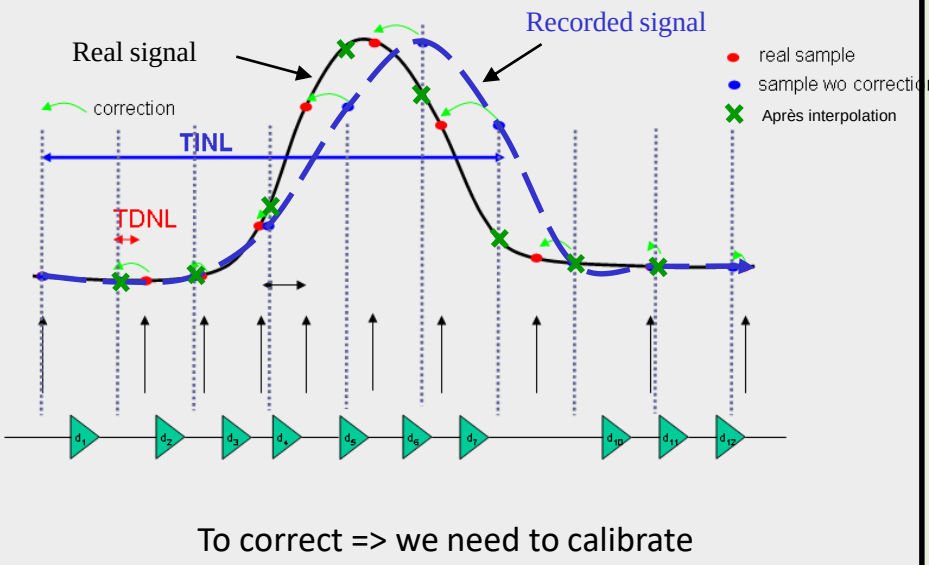
- **Time INL** calibration:
  - Need external sinewave generator : best results but fastidious
  - **Internal Oscillator** for time INL calibration ➔ automated calib

- **TOT measurement** calibration : needs external **pulse** with **variable width**.

Dedicated **Input Block**, with **Bypass Switch** to inject DAC for **internal ADC calibration** or asynchronous oscillator for **internal Time INL calibration**.

TIME INL CALIBRATION: SEGMENT METHOD

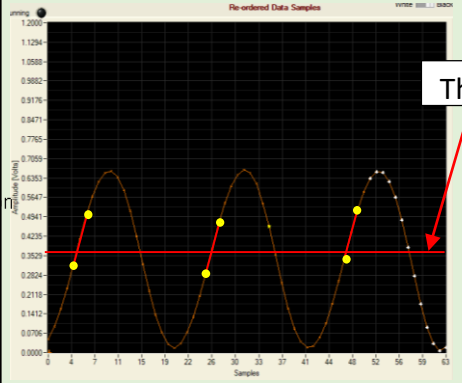
Effet on INL on the waveform sampling



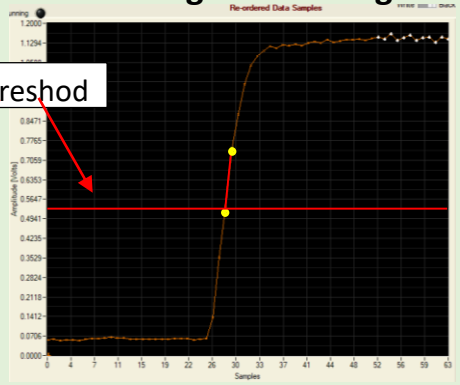
To correct => we need to calibrate

INL Calibration:

External SineWave

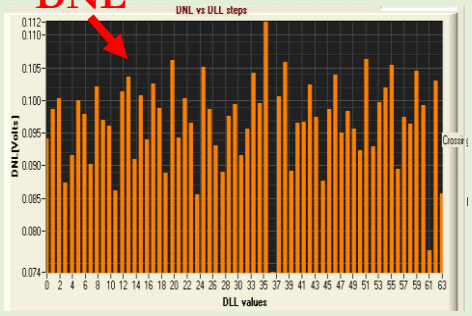


Internal generated signal

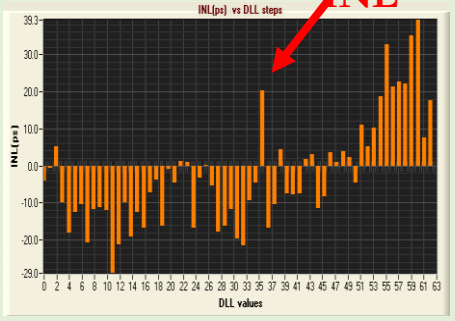


Calibration Result

DNL

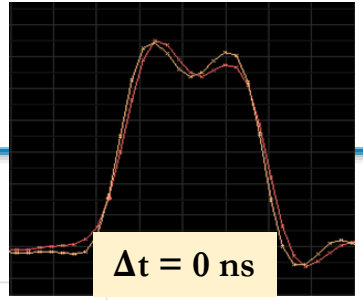


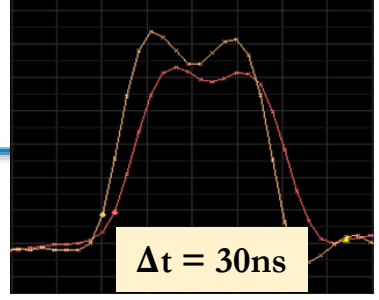
INL

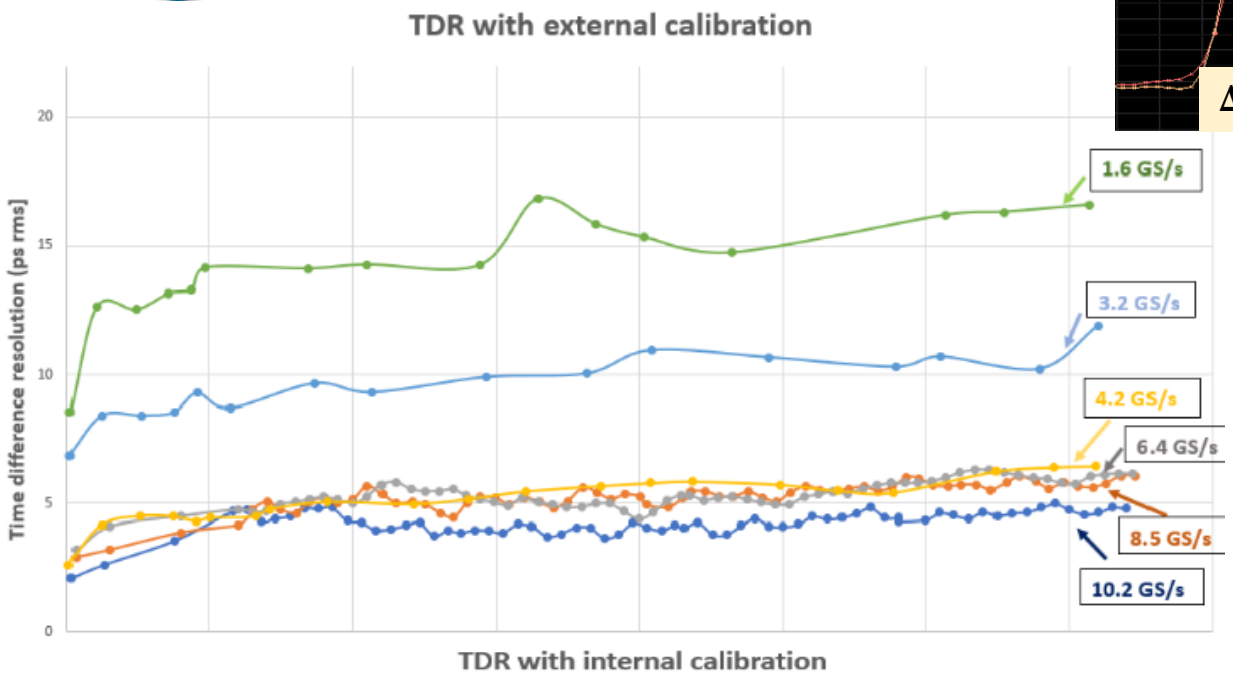


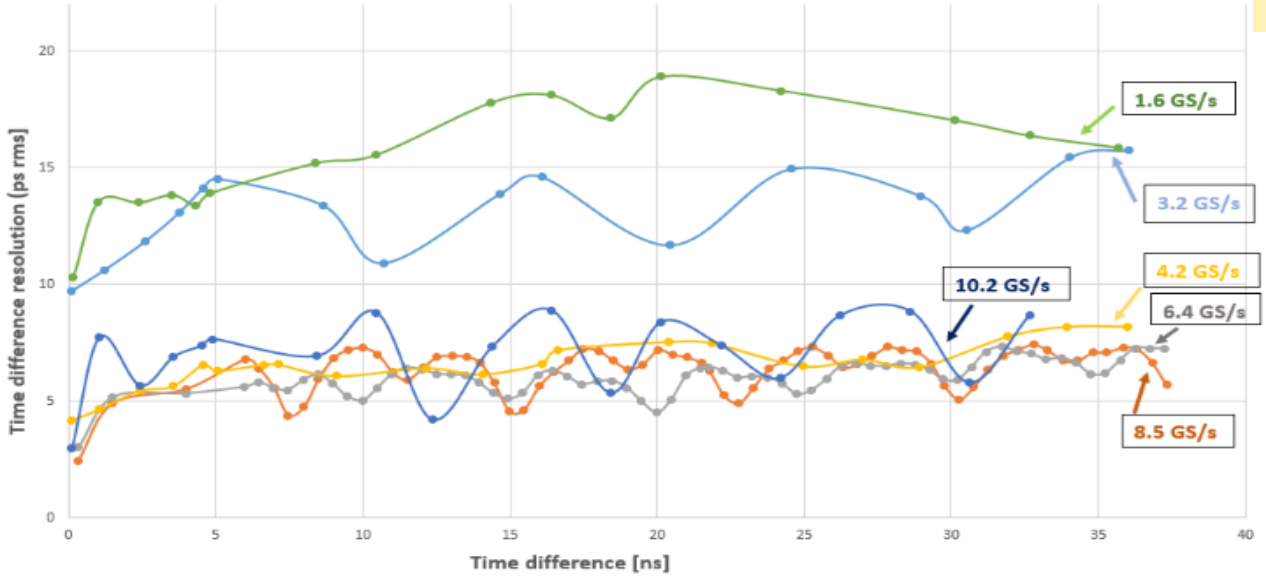
External Calibration: - very good results but fastidious : not envisageable at large scale.
Internal Calibration: - less good but can be perfomed automatically with the software, permits also to build integrated systems

TIME RESOLUTION
external vs internal calibration









Delays for measurement made by a **cable box:** rise time degrades with delay

With **external time-calibration** :

- **TDR of ~5 ps rms** for **4.2< Fs<8.5 (10,2) GS/s**
- **TDR < 10 ps rms** for **3.2 GS/s**
- **TDR < 18 ps rms** for **1.6 GS/s**

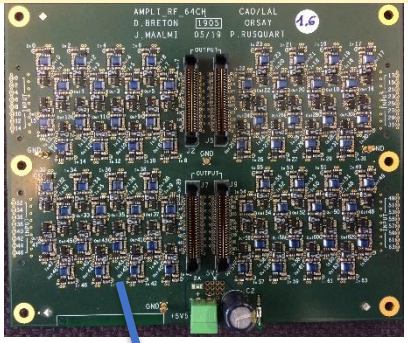
With **self-calibration**

- Limited jitter degradation (~20%)
- Permits **full integration** in **compact detection systems**

TAKING DATA WITH DETECORS

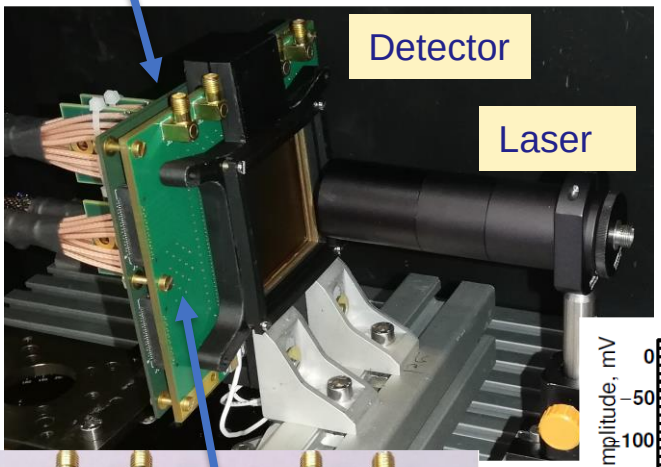
TEST OF MCP-PMT FOR BOLD-PET/CLEARMIND (CEA/IRFU)

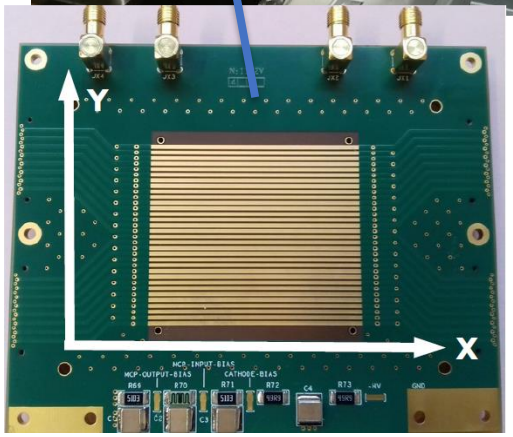
64-channel 20dB amplifier board (IJCLab) x 2



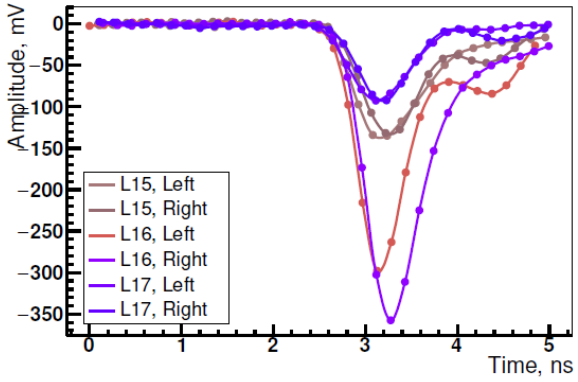
Coaxial cables

128-channel SAMPIC crate



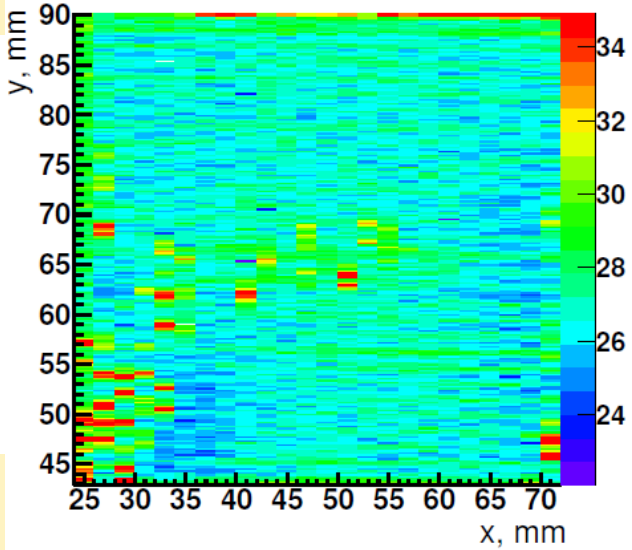


Signals read @ 6,25 GS/s



Stripline board for MCP-PMT: permits reading the **1024 (32x32) pixels** with only **64** (32x2) electronics **channels**

Time resolution (wrt laser trigger)



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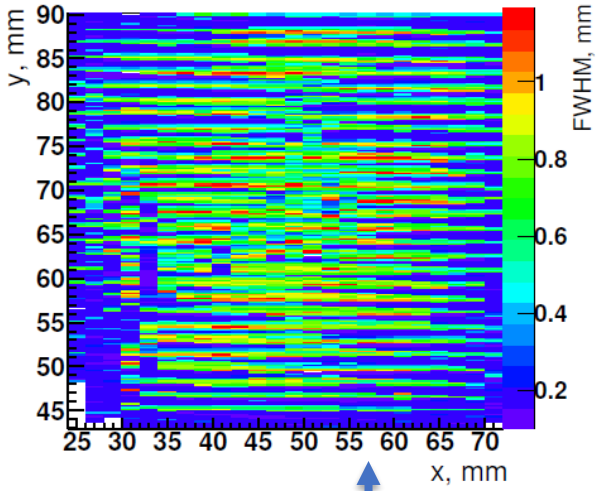
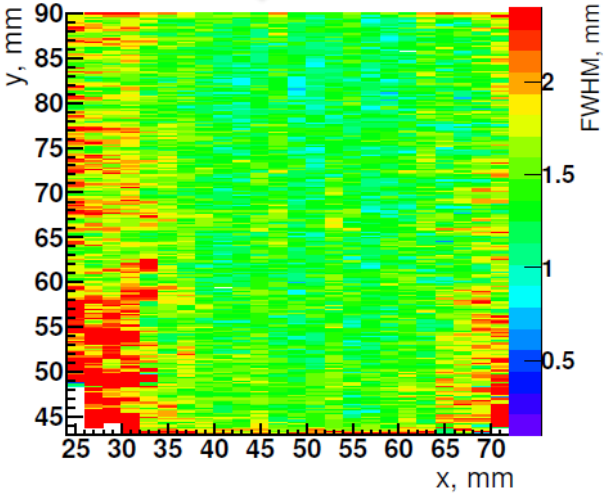
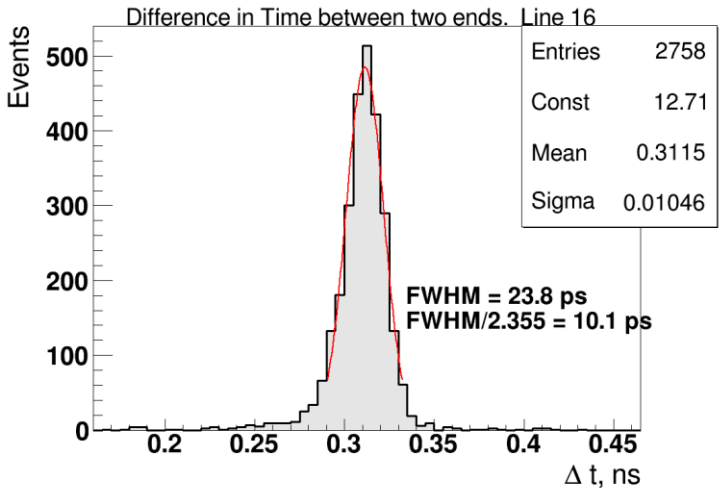
BOLD-PET/CLEARMIND: SPATIAL RESOLUTION



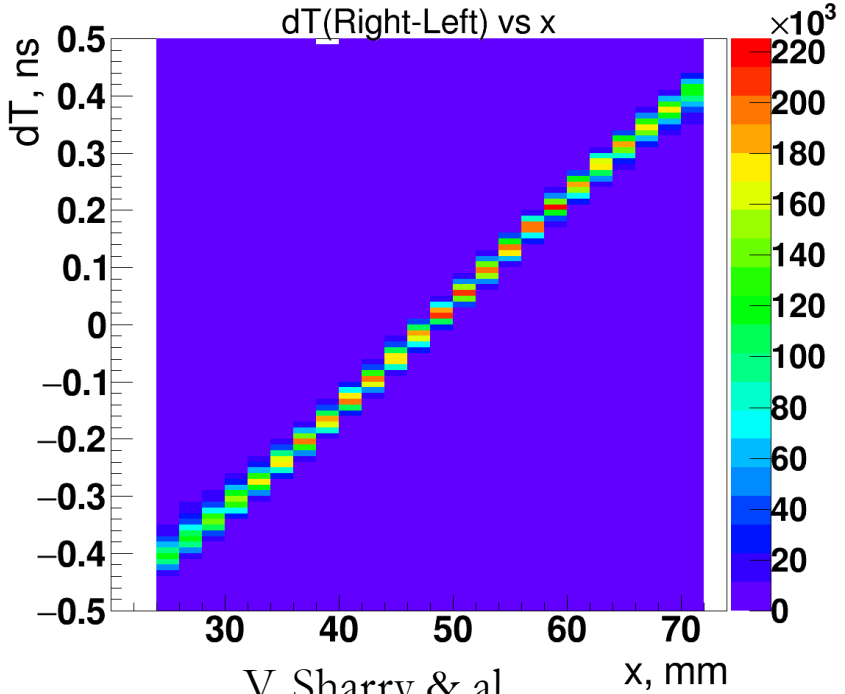
Spatial resolution:
Y (accross lines)
X (along lines)



TDR for a given location between the two extremities of a strip => gives the resolution in X



Scan of successive locations between the two extremities of a strip => gives the global resolution in X: **same order as the pixel** …



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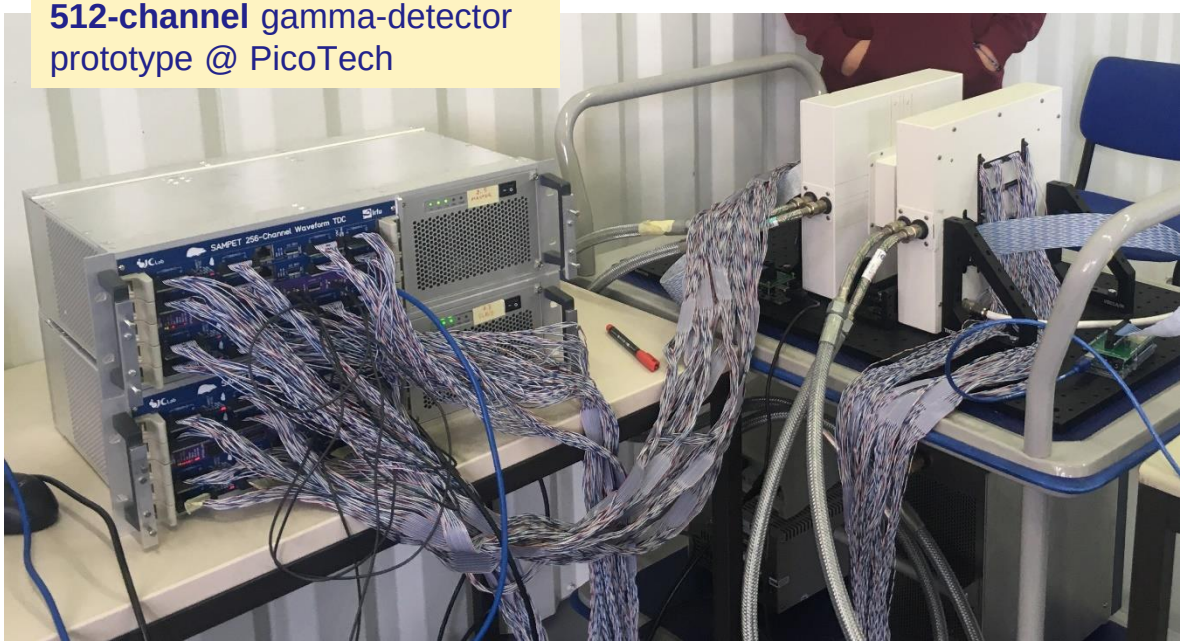
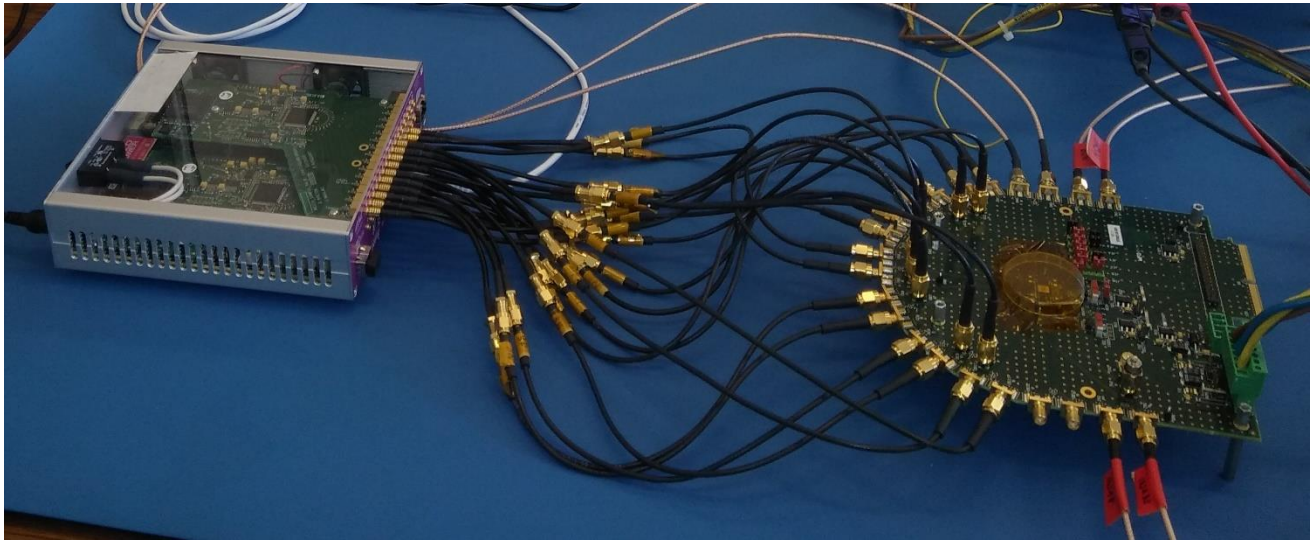
PICOTECH & RAFAEL

512-channel gamma-detector prototype @ PicoTech

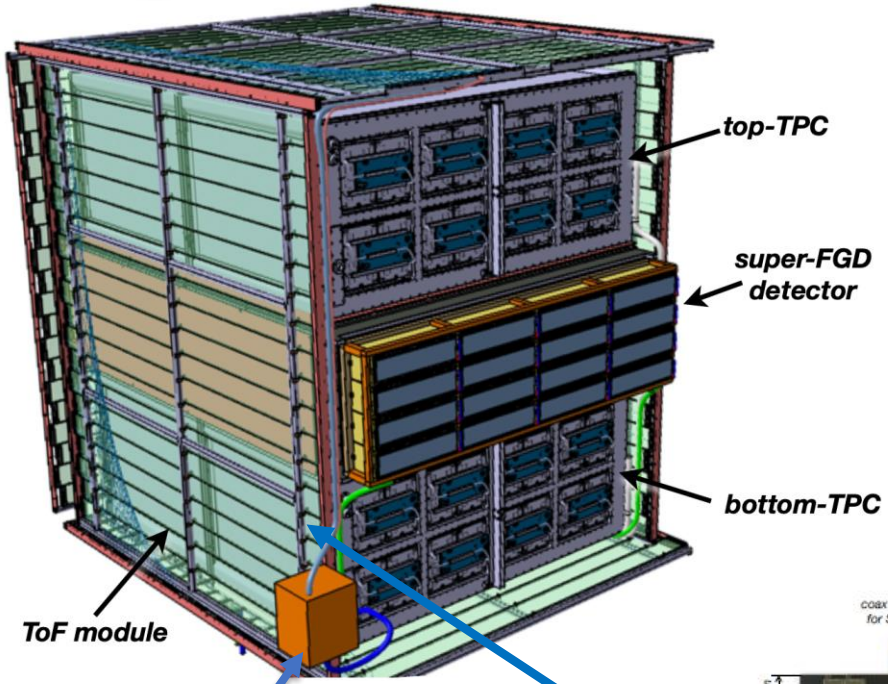


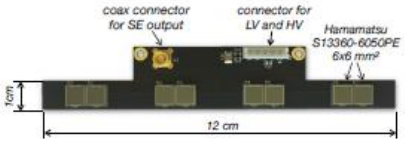
PicoTech TOF-PET prostate scanner

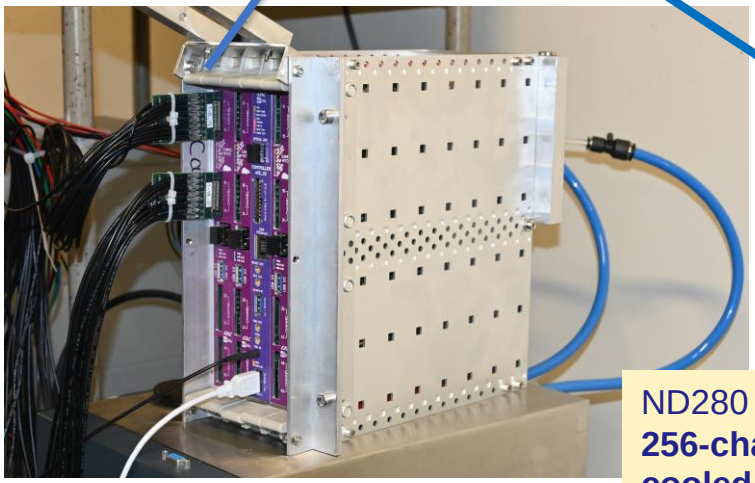
- Test bench (robotized since) for the production and characterization of the **100,000 RAFAEL ASICs** (**Clock Buffer** for **CMS**) at **IRFU**
- Readout @ **8,5 GS/s** by 32-channel SAMPIC module.
- Channel time resolution measured is **< 3 ps rms** !

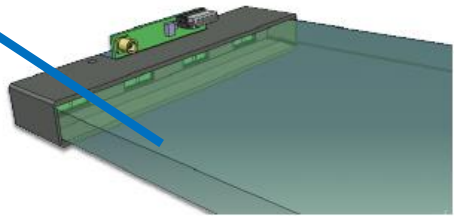


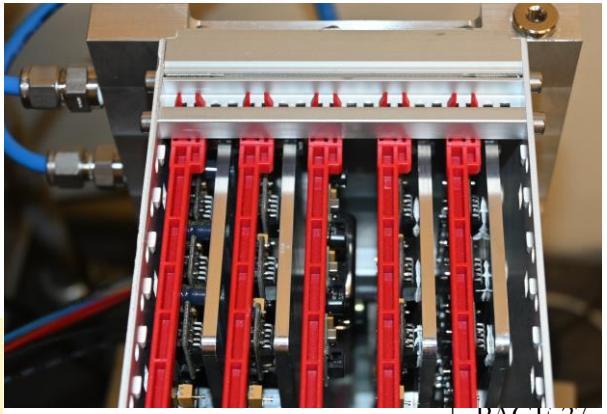
T2K ND280 UPGRADE







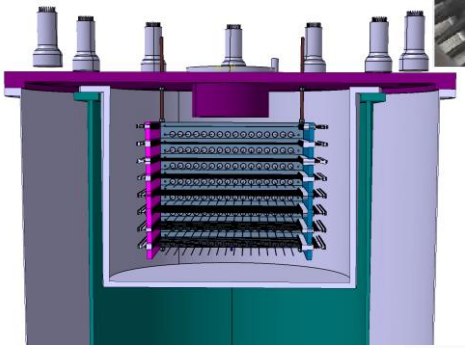


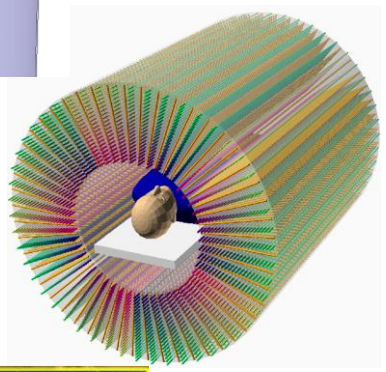


ND280 Timing Detector:
256-channel customized water-cooled SAMPIC crate

TOWARDS LARGE SCALE IMPLEMENTATION

- SAMPIC is the baseline digitizer ASIC for new experiments based on the **opaque scintillator technology** "**LiquidO**"
  - Matrix of WLS fibers immersed in opaque liquid scintillator and readout by SiPMs
- 3 detectors are currently in the design phase:
  - A technology demonstrator called **Mini-Gamma** at IJCLab in Orsay **(512 channels)**
  - A prototype for a PET-SCAN called **LPET-Otech** (ANR project) at IJCLab **(2000 channels)**
  - A **neutrino detector** called **AM-Otech** which will be built at IJCLab, then moved to Chooz Nuclear Powerplant next to the reactor, with both physics and technology goals (ERC project, **20000 channels).**
- In all cases, a **smart triggering** architecture is required for **dark noise rejection**, and **readout** will be **optimized** depending on **physics event rates**.



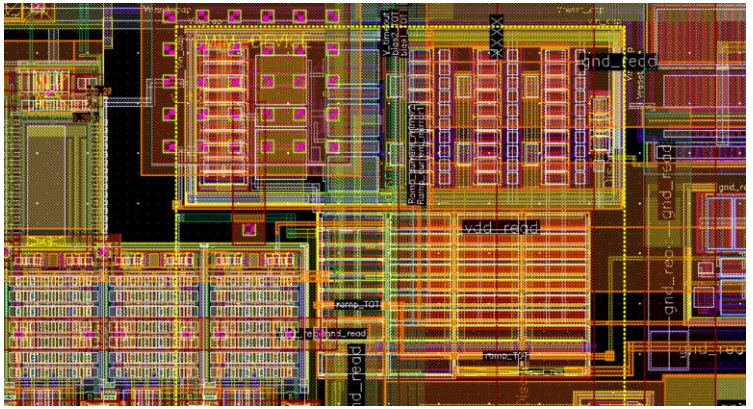


ABOUT MPW RUNS …

- We need to launch a production in order to address the needs of the projects
  - But before, we need a new (hopefully last) prototype.
  - **TSI,** which successfully produced our last version in 2021, announced end of November 2022, when IN2P3 wanted to renew the NDA: "TSI is a small foundry company and can not support and afford research & institution using MPW shuttle only and no production possibility for the last 10 years. It is only large foundry companies like TSMC, UMC, Globalfoundries and SMIC can afford. Also, TSI has new management team change and will not support MPW shuttle program anymore. Thanks for your understanding."
- Good news is that Europractice re-scheduled AMS 180nm CMOS runs, starting in **November 2023.**
- Other good news is that French **CMP** is back to life (now as **CIME-P**) and should soon also give access to all **AMS** technologies, including 180nm CMOS.
- So we should return to "normal" life …

NEW VERSION (V6)

- The idea here is to try to get an “as perfect as possible” chip wrt its current specifications before launching the production
  - A lot of work performed on the **routing of the power supplies** to gain on IR-drops and potential crosstalks.
  - Redesign of the **trigger comparator** to improve its linearity for low baselines
  - Modifications in the **internal signal generator used for time INL calibration** (especially targeting the calibration above 8 GS/s)
  - Optimization of the **routing of the write pointers**
  - Rework on the **Wilkinson ADC current generator** to reduce the noise during conversion
  - And many other details …



CONCLUSION

SAMPIC is a **10-year project** with 7 versions up to now.

- 4 with major evolutions, partly driven by users
- 3 mainly with bug corrections

- The **few ps resolution** was achieved from the first prototype
  - No major improvement on this side since
  - Most of the evolutions target new features or **system dedicated integration**
- Technology is a **tortuous path in 180 nm**
  - Already 3 different ones have been used, fortunately **new possible runs at least with Europractice** (nov 2023)
  - ➔ we hope it will be the last prototype (V6) before **engineering run.**

- **Development of systems** : years of work …
  - **Hardware, firmware, software**
  - Still lot of possible improvements
  - Starting large scale experiments (> 2000 channels) developments with SAMPIC
- **Technology transfer to CAEN**: 16, 32 and 64-ch desktops are in development.

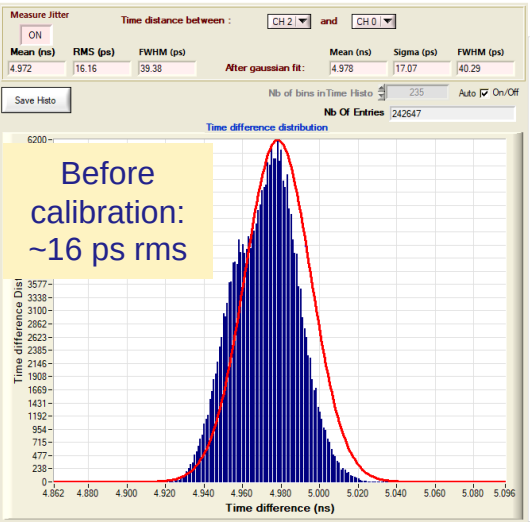
THANK YOU FOR YOUR ATTENTION

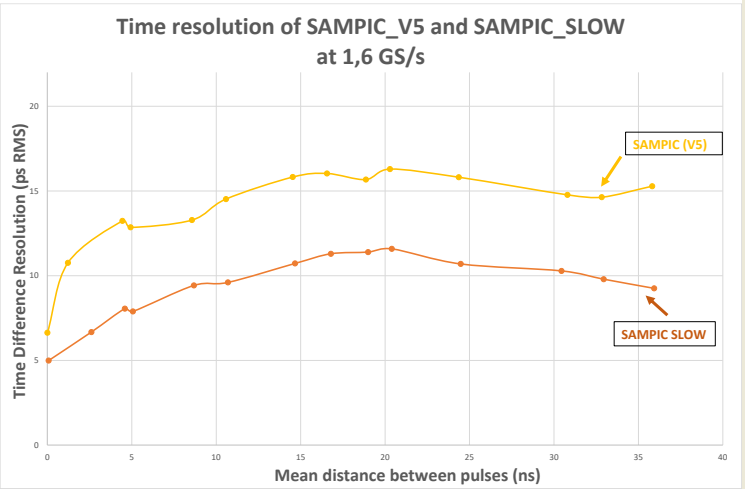
SAMPIC_SLOW : sampling rate < 1.6 GS/s

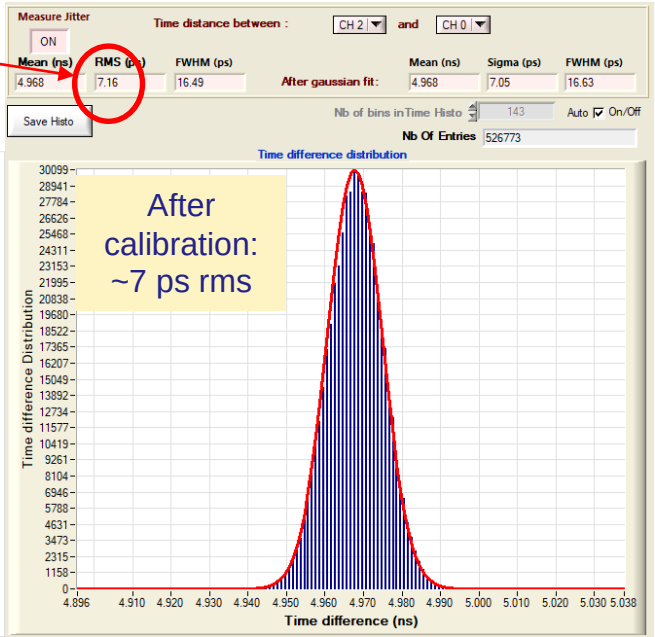
- A second version dedicated to slower sampling has been developed.
  - **Wider time window** should permit effective multi-sample offline reconstruction
  - Pin to pin compatible with standard version. Only difference is the main clock frequency.
  - DLL delays modified for running between 350MS/s and 2GS/s
  - All delays servo-controlled to main clock have been adapted
  - Analog memory cell has been enlarged (as much as easily possible but not yet optimum)

Time resolution measurements:

- TDR @ 1.6 GS/s < 10ps rms ! (**mainly limited by SNR**, already very good without calibration)
- Noise @ 1.6 GS/s ~ 1.05 mV rms







TIME RESOLUTION (DIGITAL CFD) VS SIGNAL AMPLITUDE

- ADC conversion time can be reduced (by decreasing the resolution): factor 2 for 10 bits (800 ns), 4 for 9 bits (400 ns), 8 for 8 bits (200 ns), 16 for 7 bits (100 ns).

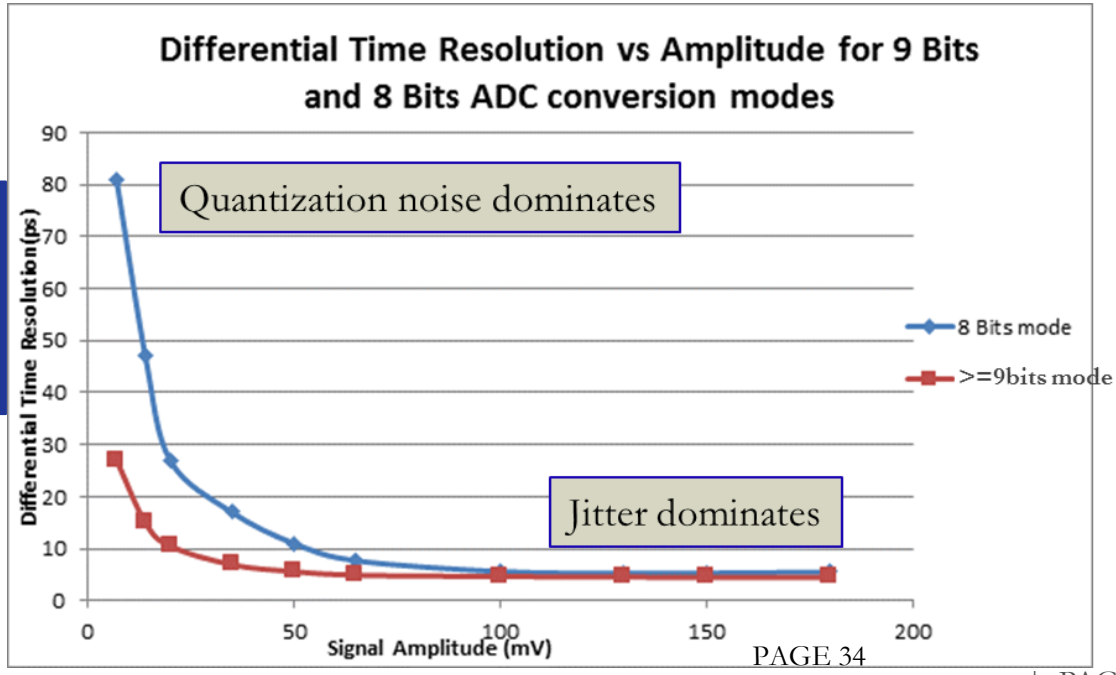
➔ decrease of channel instantaneous dead time

- The quantization noise affects the timing precision only for very small signals

⇒ as expected **no significative change** measured for 11, 10 and 9-bit modes

⇒ **for digital signals, 8 bits or less is adequate => reduced dead time (< 200 ns)**

No degradation on timing for pulses above 100mV for 8 bits



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