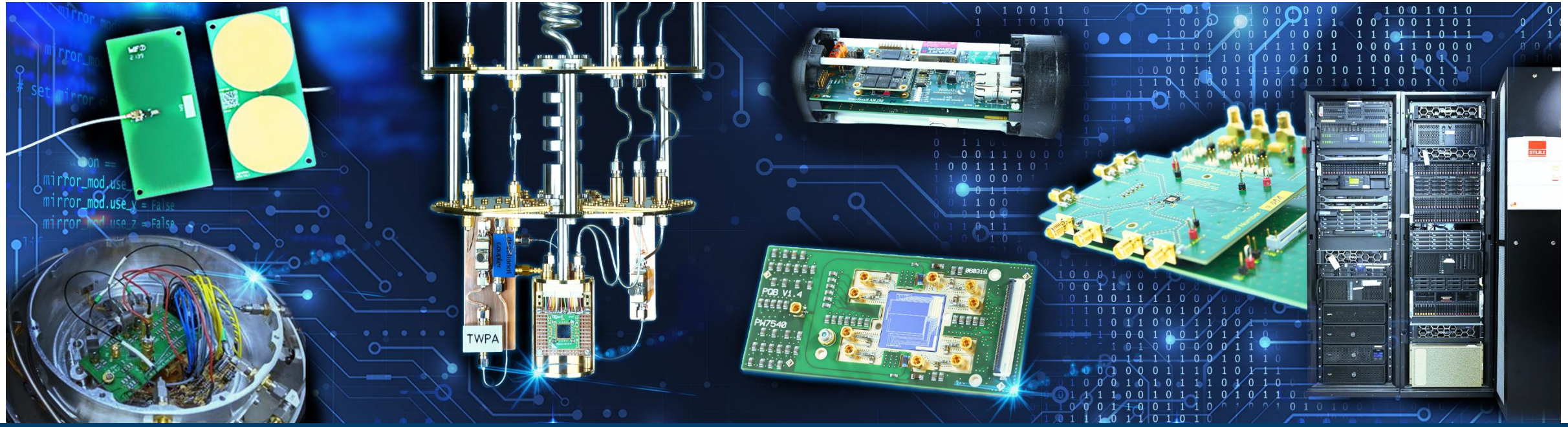


SUB 100 PS READOUT ELECTRONICS FOR PHOTOMULTIPLIER BASED MULTI-CHANNEL DETECTORS

30.05.2023 | DAVID ARUTINOV

THE ACTUAL WORK HAS BEEN PERFORMED BY LIUBOV JOKHOVETS, LUKAS KRYSTOFIAK, FLORIAN RÖSSING, CHRISTIAN GREWING

Member of the Helmholtz Association

JÜLICH Forschungszentrum | ZEA-2 Electronic Systems

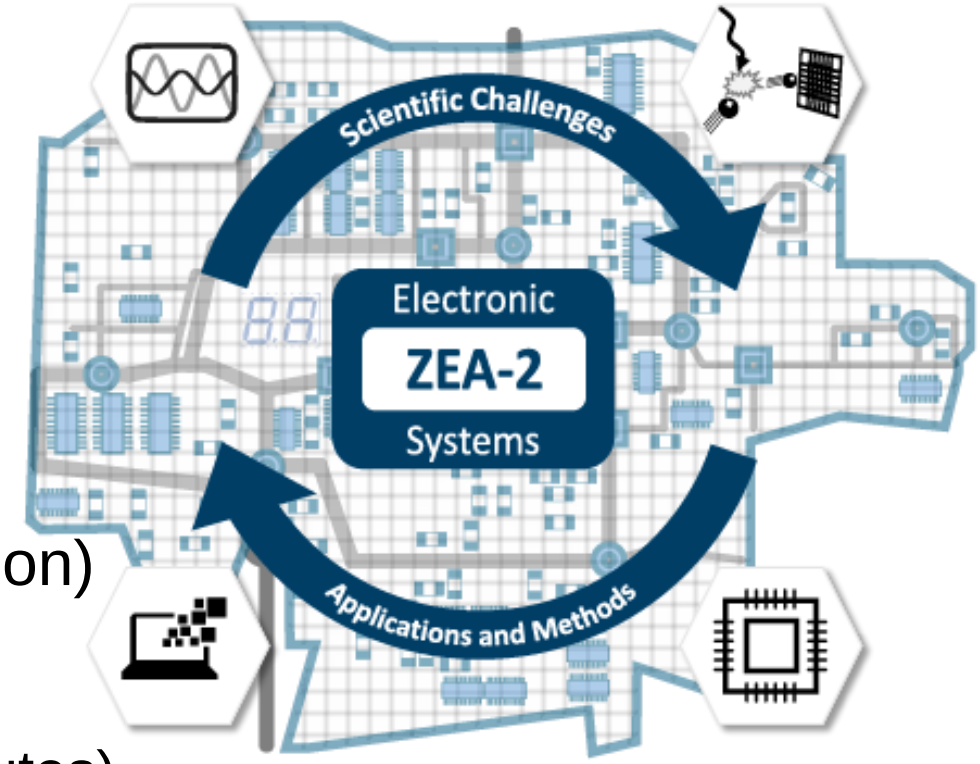
CONTENT

- WHO WE ARE
- WHAT WE DO
- OUR MOTIVATION
- OUR APPROACH
- WHAT HAS BEEN DONE
- NEXT STEPS
- CONCLUSION
- ANNOUNCEMENT

ZEA-2 – SYSTEM HOUSE FOR SCIENCE

FACTS & FIGURES

- **Employees: approx. 100**
  - approx. 65 scientists, engineers und technicians
  - approx. 15 doctoral researchers (PhD students)
  - approx. 10 students (Bachelor/Master) p.a.
  - 2 administrative staff members
  - approx. 12 apprentices (SW Eng., IT, administration)
- **Funding**
  - 85% base funding (PoF in cooperation with 12 institutes)
  - 15% third-party funding (desire to increase)



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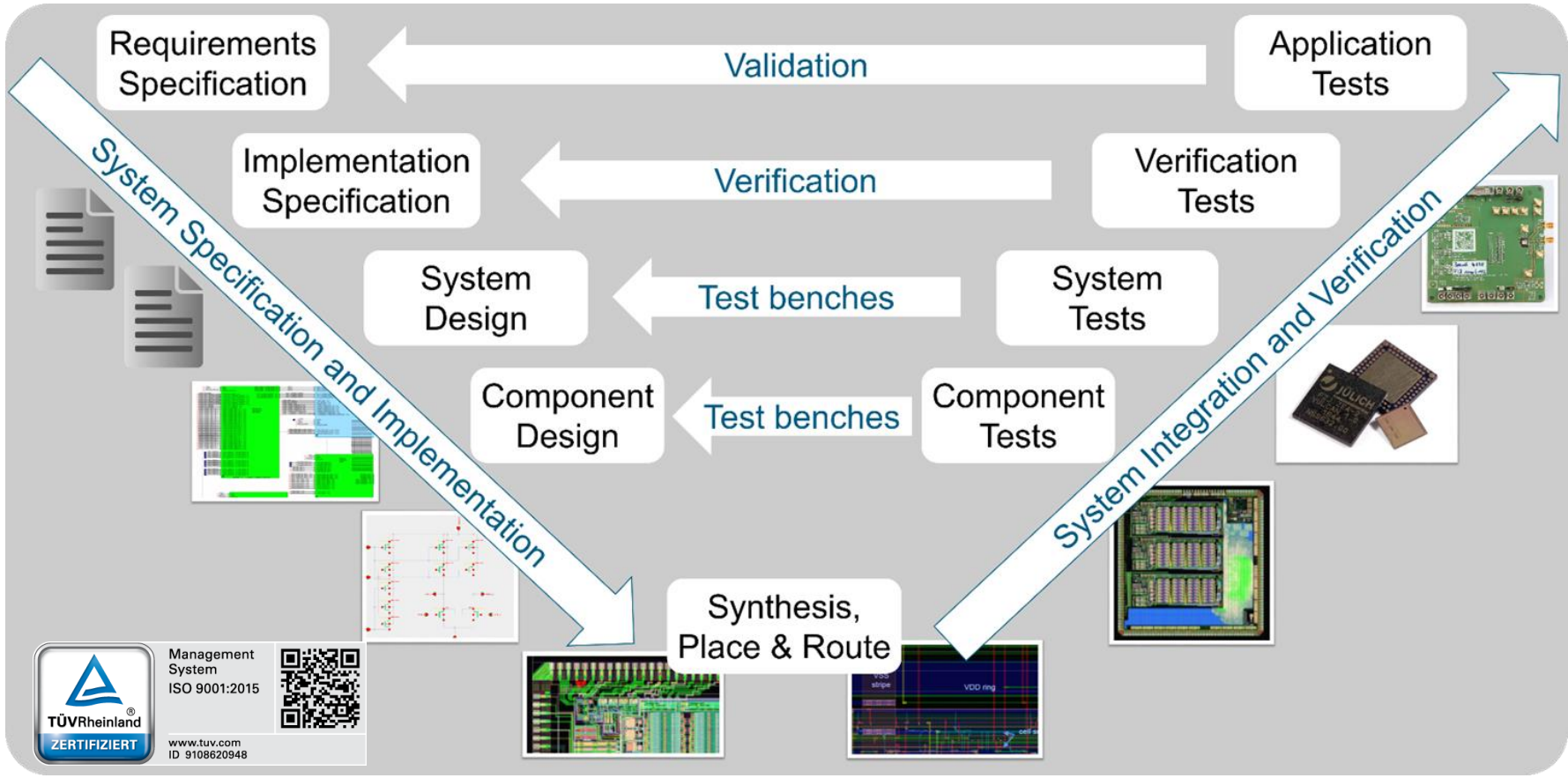
Geb.02.5
02.5
Zentralinstitut für Engineering, Elektronik und Analytik (ZEA)
Systeme der Elektronik (ZEA-2)
Eingang E1
19 56 JÜLICH

ZEA-2 – SYSTEM HOUSE FOR SCIENCE

FACTS & FIGURES

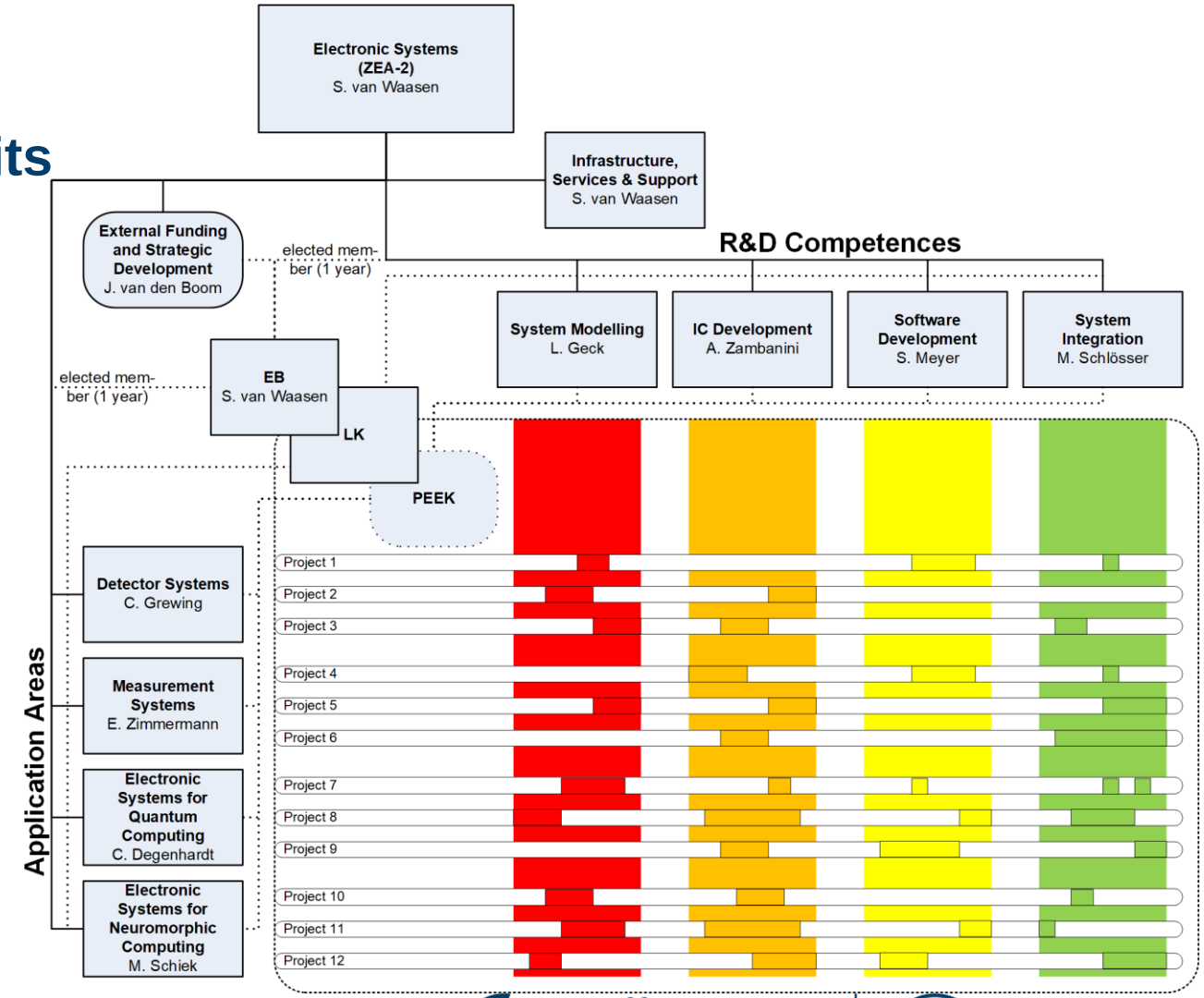
- **Project Management**
  - ISO 9001:2015
  - Top down approach
  - Review process
  - Verification



ZEA-2 – SYSTEM HOUSE FOR SCIENCE

FACTS & FIGURES

- **System Solutions w/ Integrated Circuits**
  - Detector Systems
  - Geo-Science
  - Quantum Computing
  - Neuromorphic Computing
- **R & D Teams**
  - System Modelling
  - IC Development
  - Software
  - Integration / Verification



ZEA-2 – SYSTEM HOUSE FOR SCIENCE

FACTS & FIGURES

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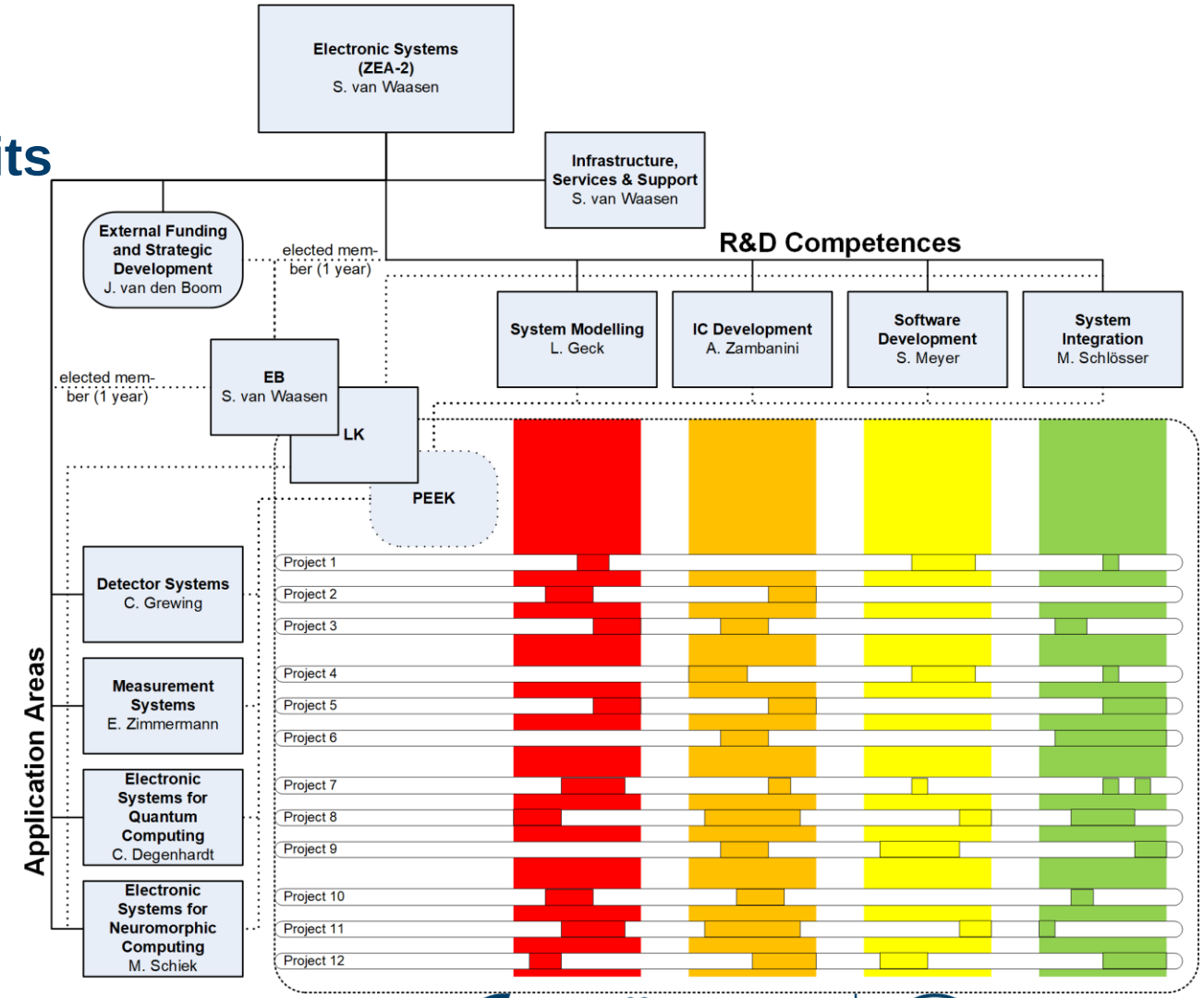
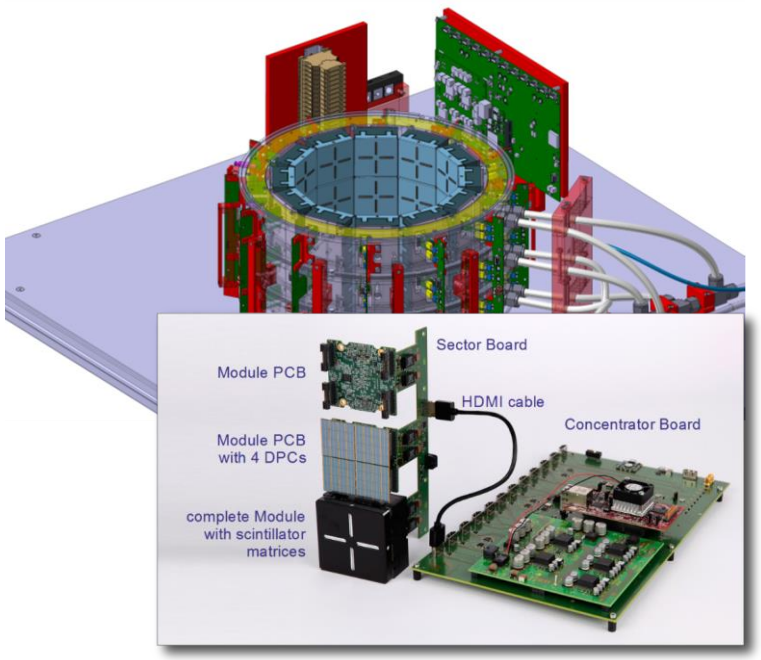


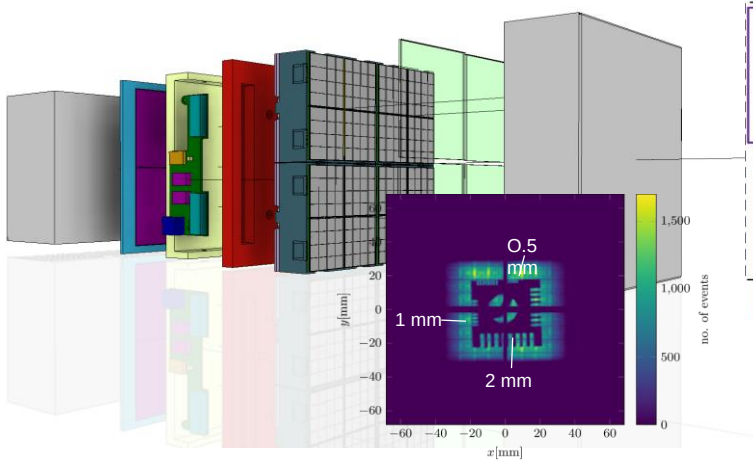
ZEA-2: SYSTEM HOUSE FOR RESEARCH IN JÜLICH

DETECTOR SYSTEMS: A FEW SELECTED PROJECTS



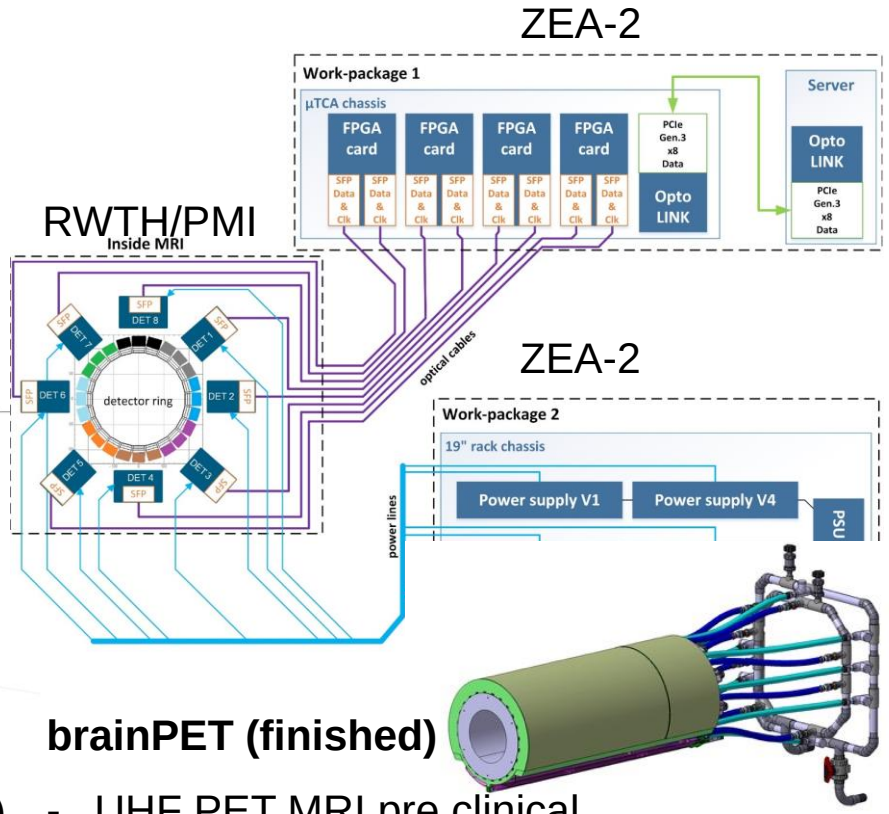
PhenoPET(finished)

- PET for transport in plants
- **Task: a complete system**



TREFF neutron detector (finished)

- Neutron beam monitoring
- **Task: a complete system**



brainPET (finished)

- UHF PET MRI pre clinical
- **Task: DAQ / PS**

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ZEA-2: SYSTEM HOUSE FOR RESEARCH IN JÜLICH

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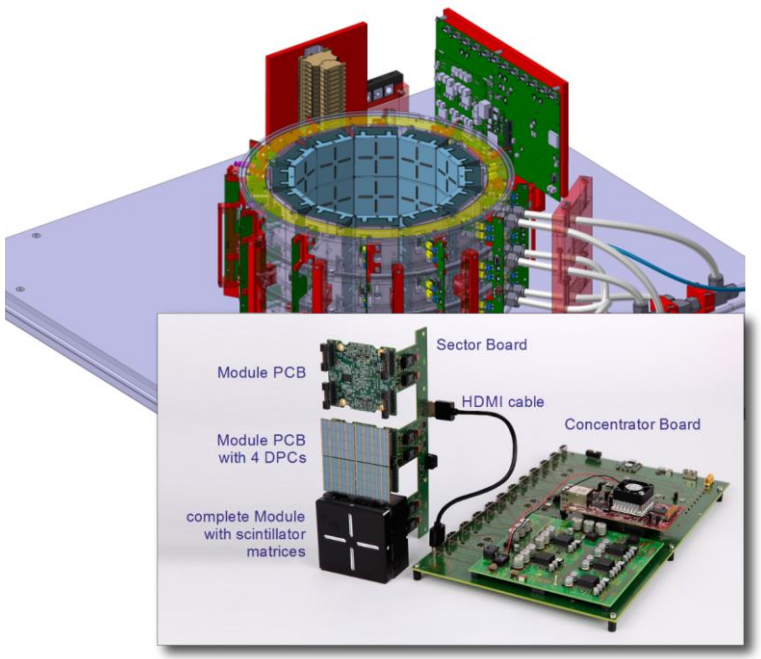

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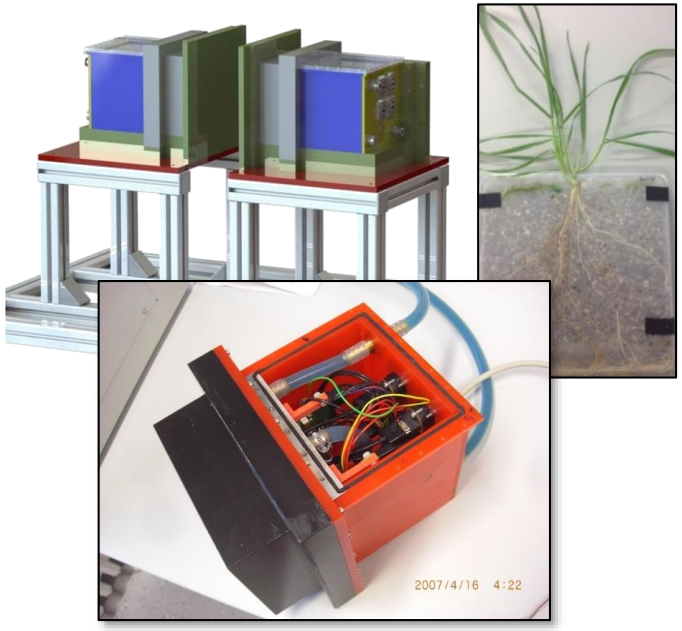
- **Task: a complete system**
- **2D-PhenoPET 2.0**



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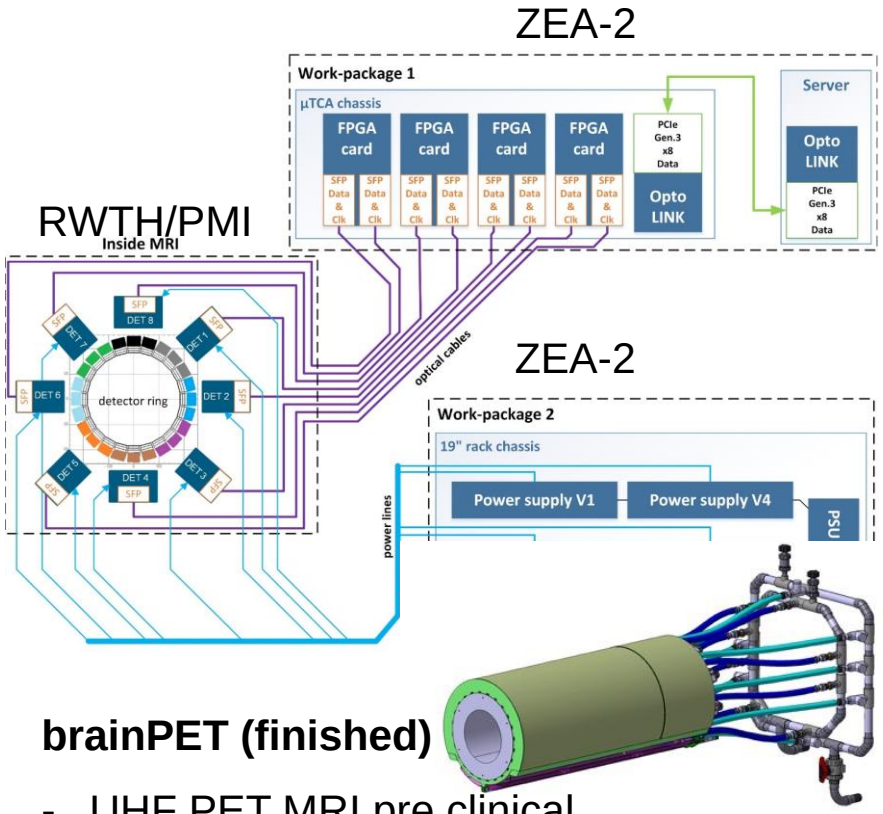
- Neutron beam monitoring
- **Task: a complete system**
- **2D-PET (ongoing)**



brainPET (finished)

- UHF PET MRI pre clinical
- **Task: DAQ / PS**
- **brainPET 2.0 (is being planned)**

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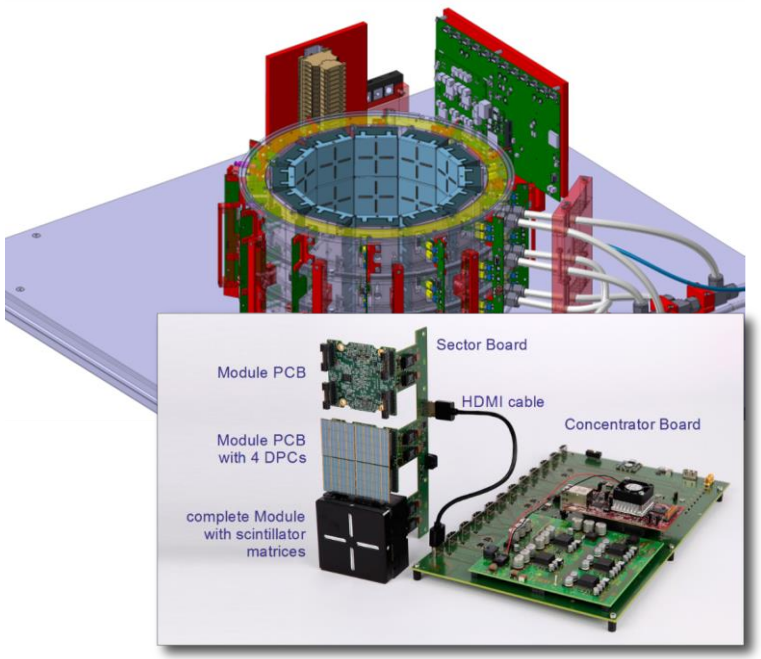

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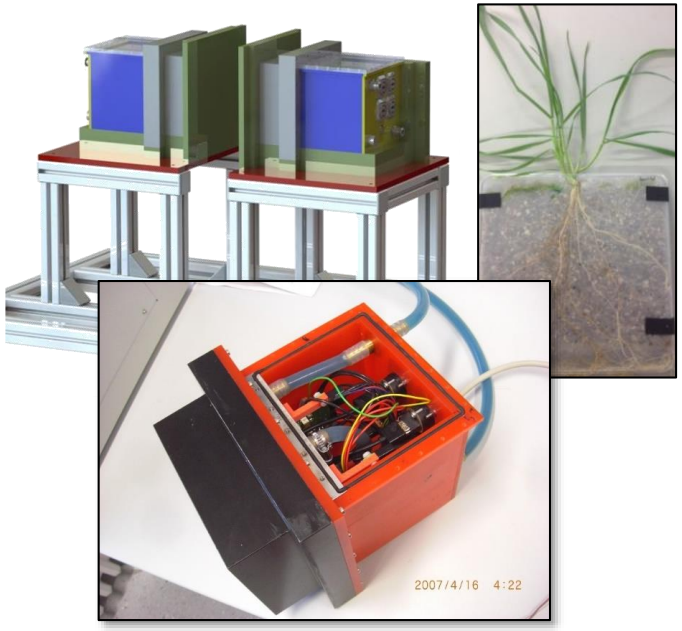

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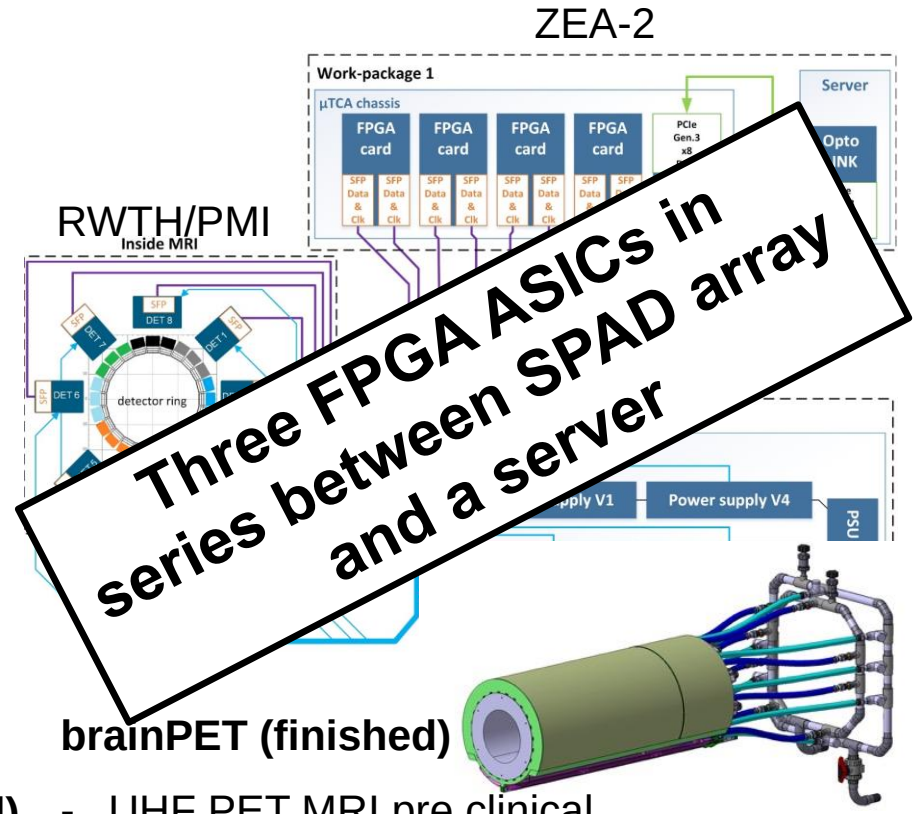

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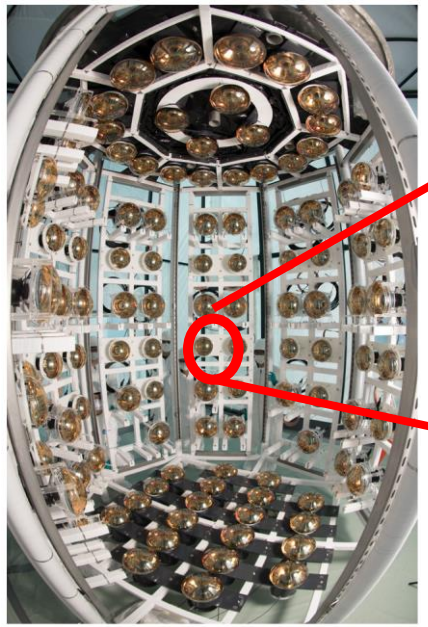
ZEA-2: SYSTEM HOUSE FOR RESEARCH IN JÜLICH

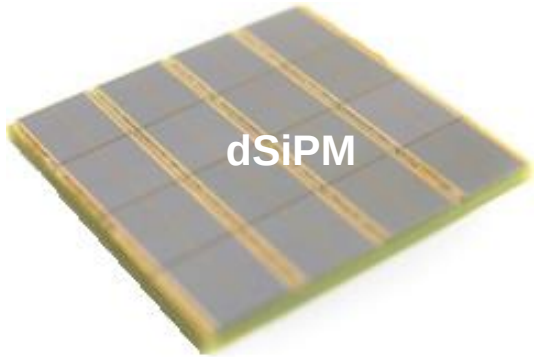
ANNIE EXPERIMENT: A LOW COST DETECTOR SOLUTION (PROPOSAL)

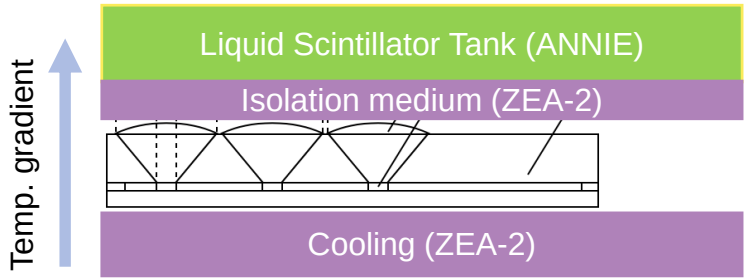


ANNIE WbLS tank surrounded by photodetectors

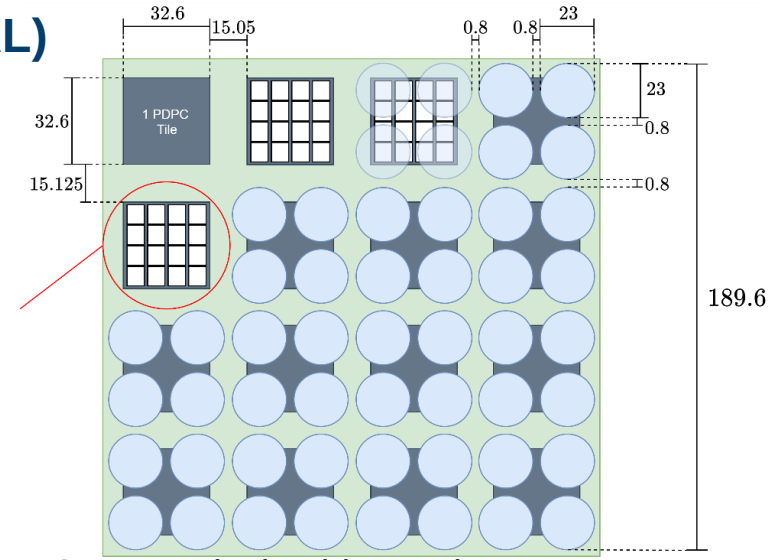
Large PMTs

silicon instead vacuum tube





Additional challenge: thermal separation of the Tank and detector



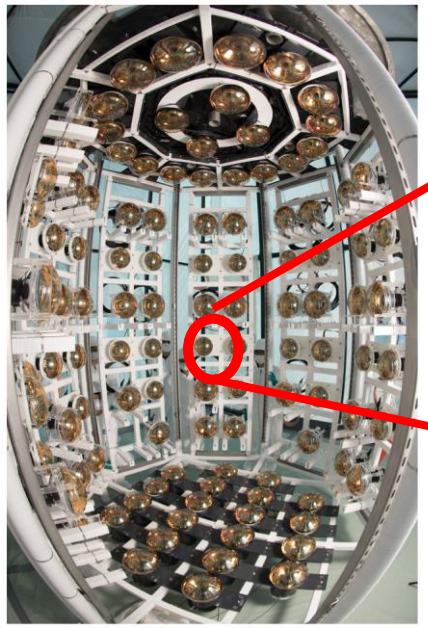
Smart optical guides and concentrators to reduce coverage area

Together w/ Uni Tuebingen and Uni Mainz

A generic proposal for liquid scintillators in preparation. Aim: propose low-cost solution for LS applications

ZEA-2: SYSTEM HOUSE FOR RESEARCH IN JÜLICH

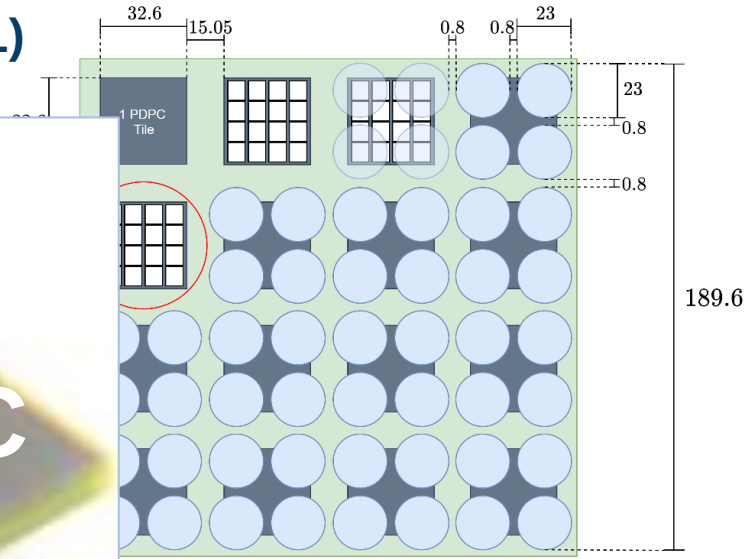
ANNIE EXPERIMENT: A LOW COST DETECTOR SOLUTION (PROPOSAL)



ANNIE WbLS tank surrounded by photodetectors

Large PM

Additional challenge: thermal separation of the Tank and detector



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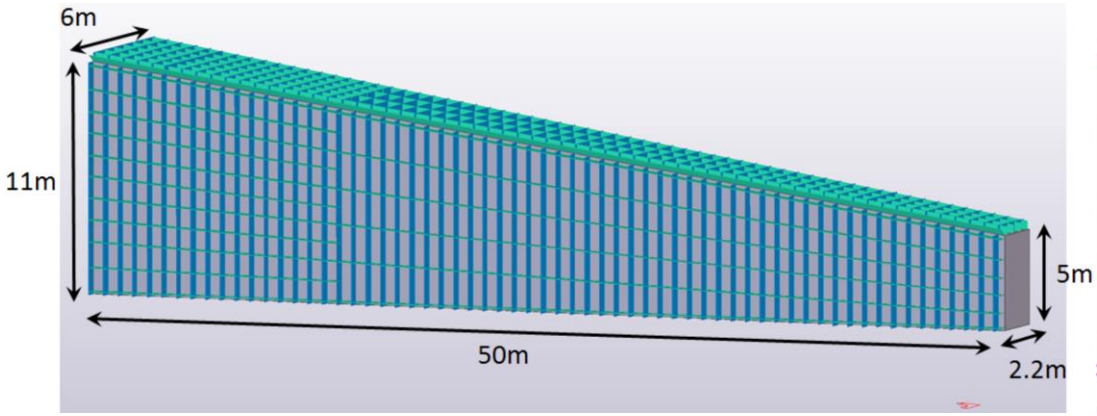
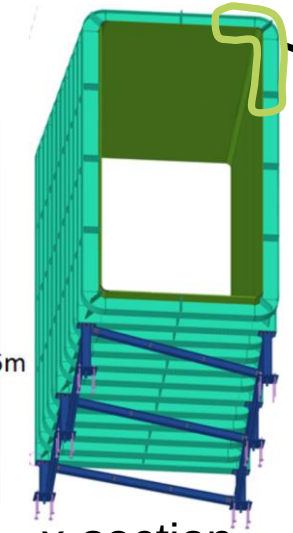
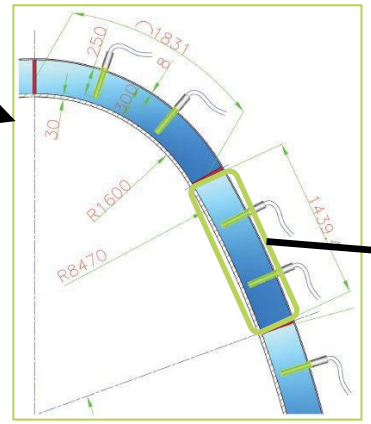
ZEA-2: SYSTEM HOUSE FOR RESEARCH IN JÜLICH

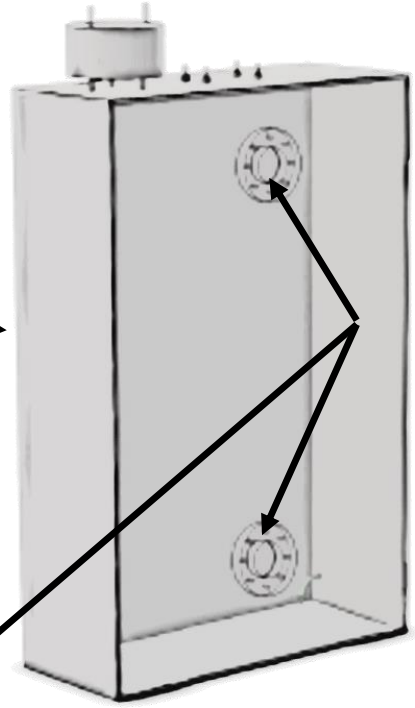
SHiP SBT EXPERIMENT: YET ANOTHER LS DETECTOR

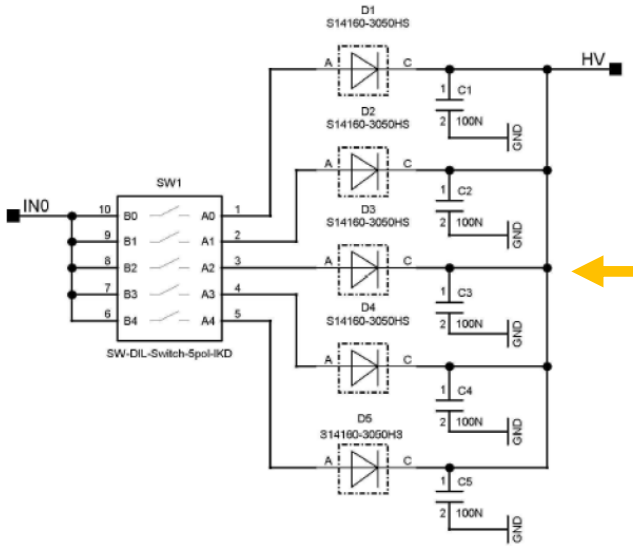


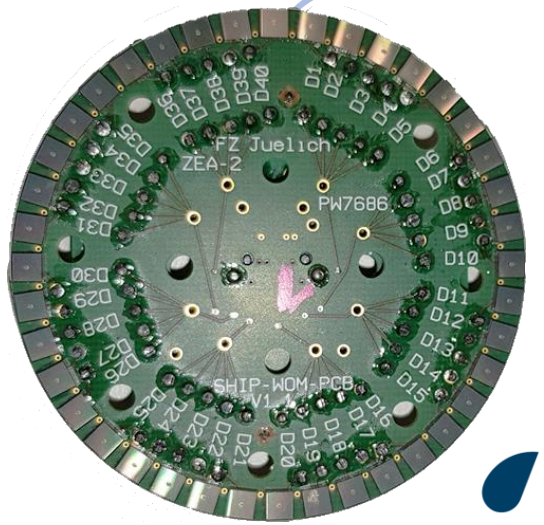


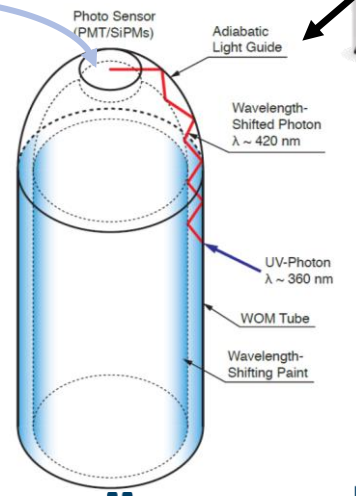
x-section











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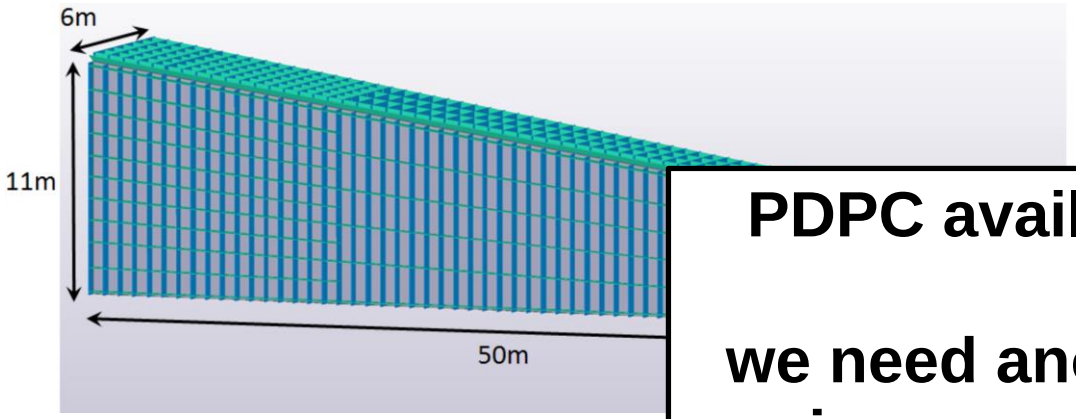
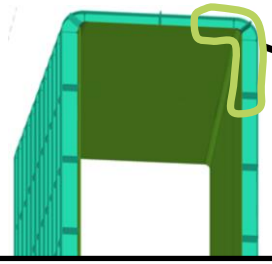
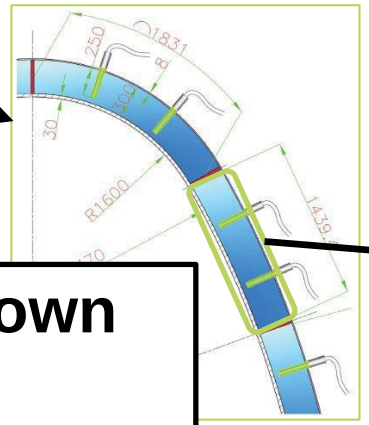
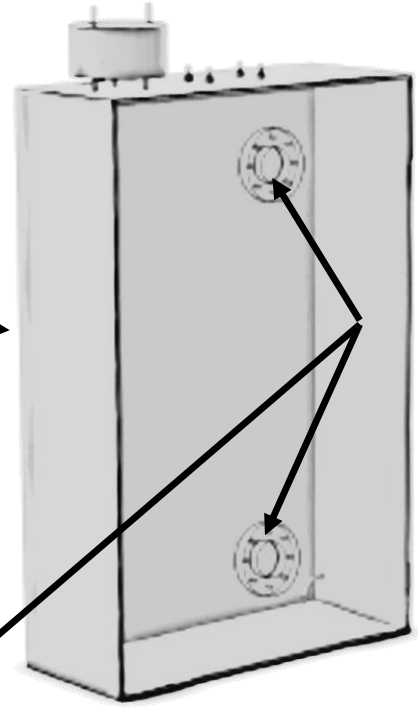


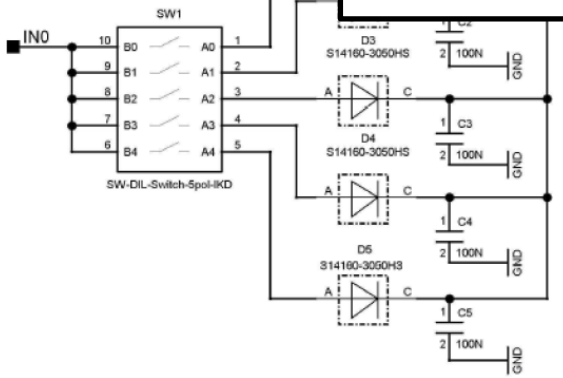


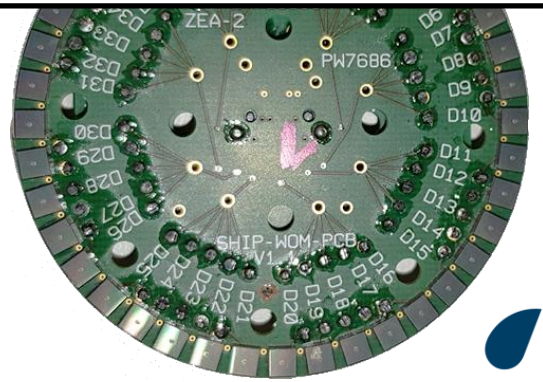


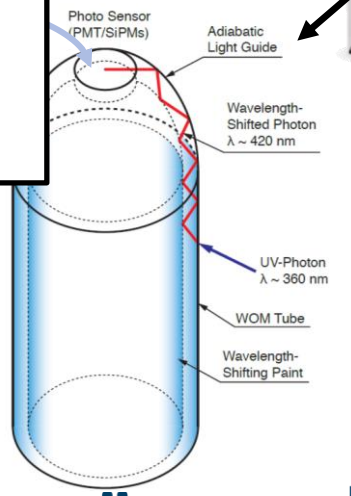


PDPC availability → unknown

we need another (digital) SPAD image sensor or a feature extraction ASIC for an aSiPM structures







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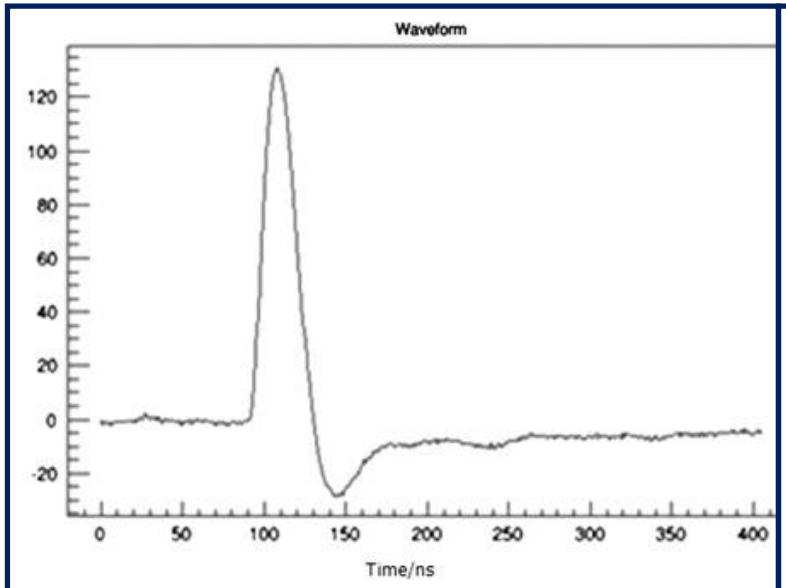
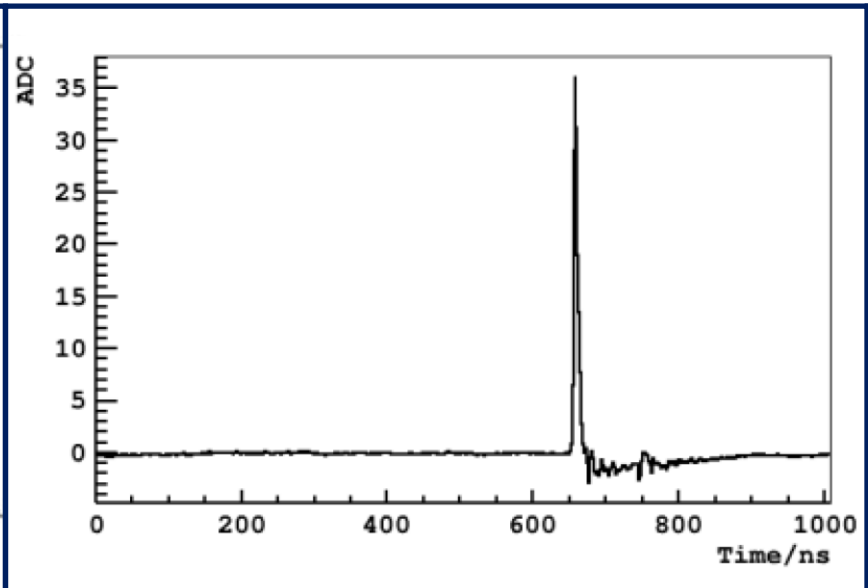
COMMONALITIES

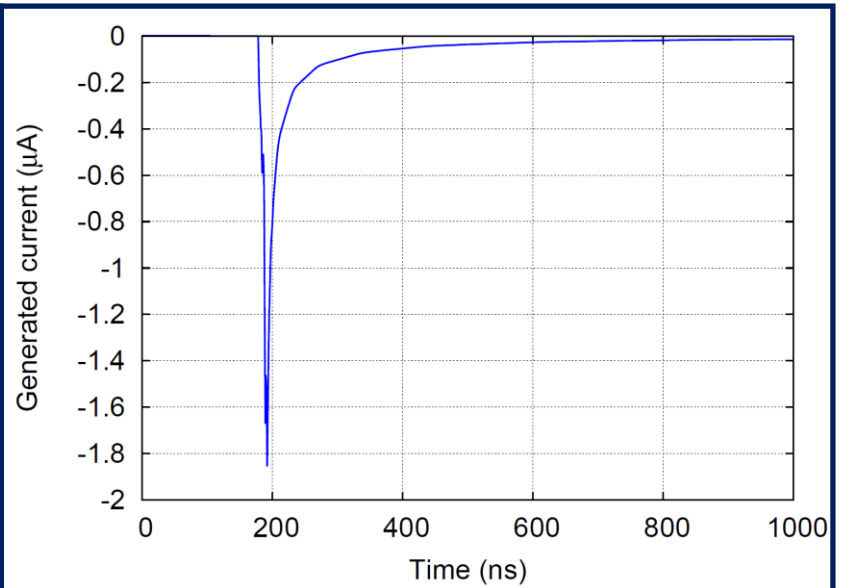
SiPM / STRAWS / PMT



SiPM Waveform
Yu et al, 2018



PMT Waveform
Zhang et al, 2019



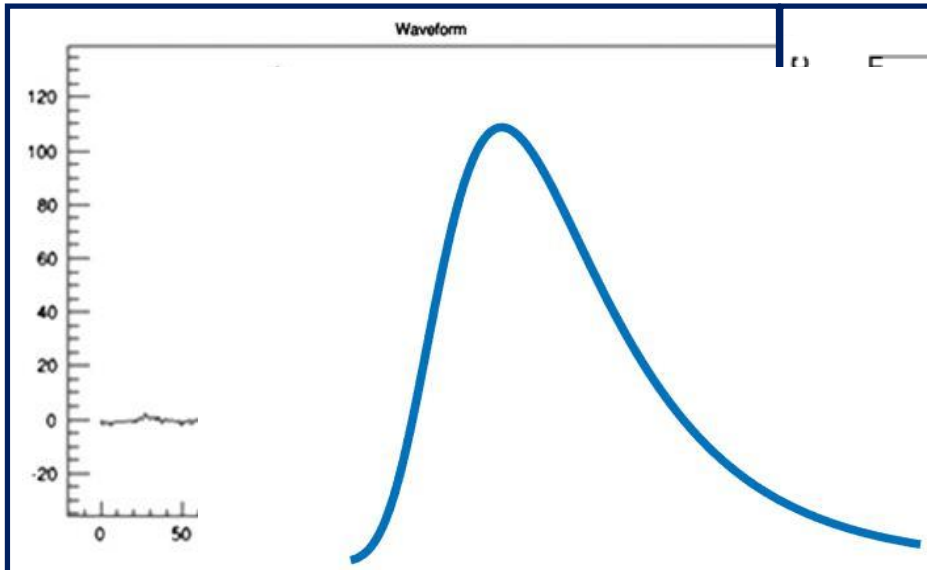
Strawtube Waveform
Przyborowski *et al* 2016

characteristic shape: fast rise with a slower fall

Timescale	1ns to 1us	Current	1uA to 100mA	Charge	10fC to 500pC

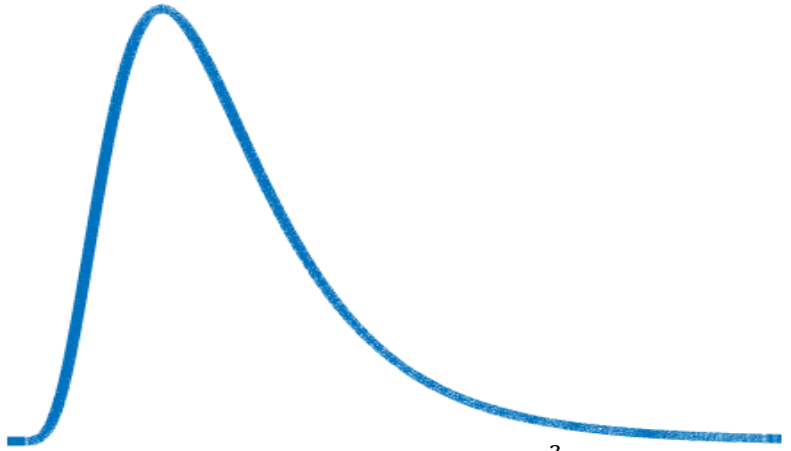
COMMONALITIES

SiPM / STRAWS / PMT



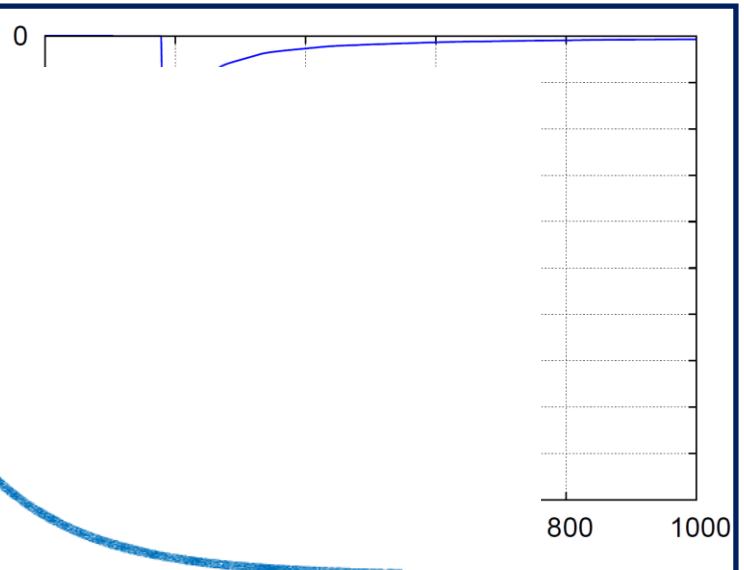
$$P(t; t_0, \tau, A, n) = A\left(\frac{t - t_0}{\tau}\right)^n e^{-\left(\frac{t-t_0}{\tau}\right)}$$

Jokhovets et al, 2019



$$P(t; \tau, \sigma, A) = e^{-\frac{1}{2}\left(\frac{\log\frac{t}{\tau}}{\sigma}\right)^2}$$

Jetter et al, 2012



.6

Timescale	1ns to 1us	Current	1uA to 100mA	Charge	10fC to 500pC

GENERIC RECEIVER ELECTRONICS

LITERATURE RESEARCH: READOUT ASICS

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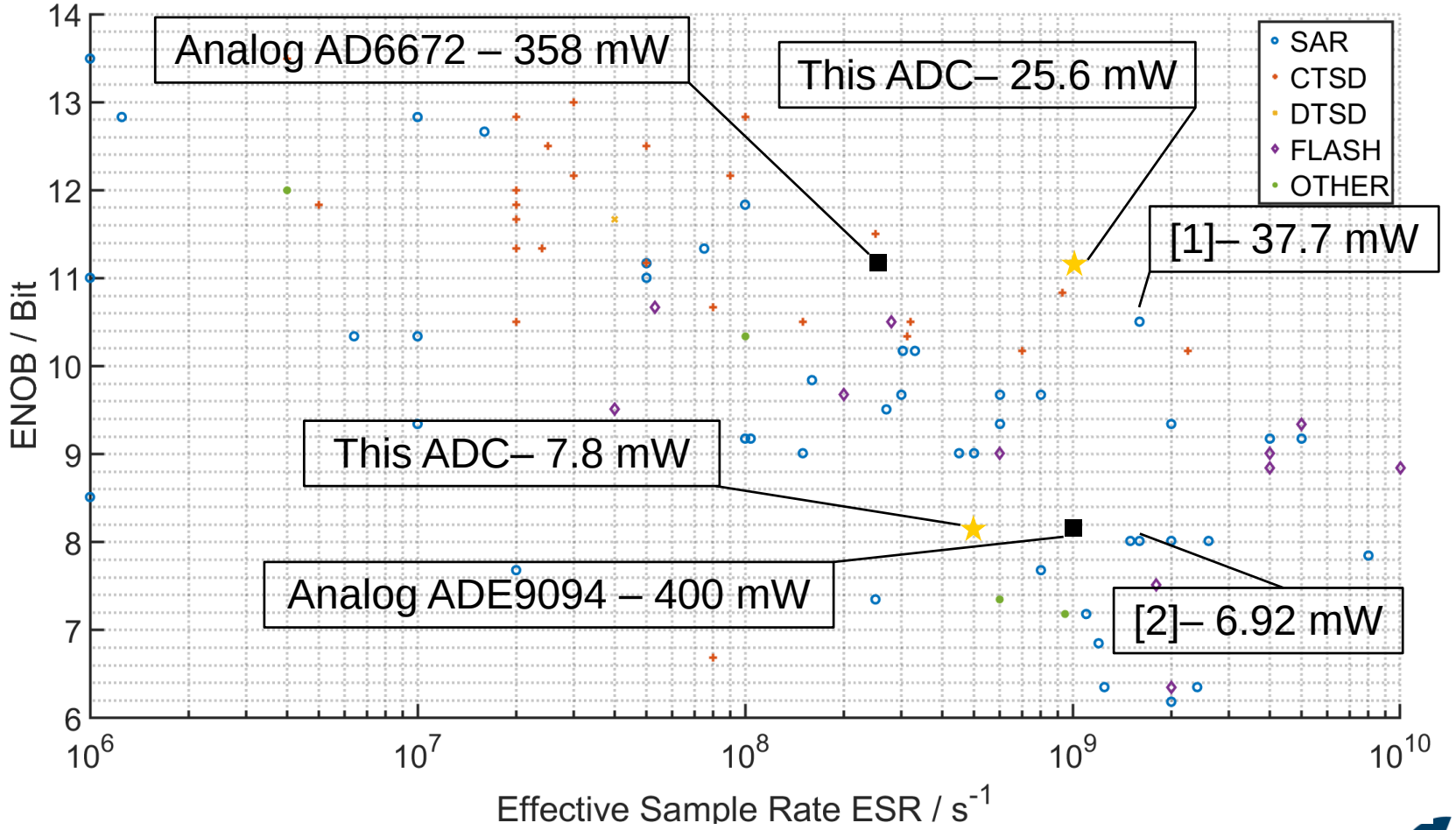
GENERIC RECEIVER ELECTRONICS

LITERATURE RESEARCH: ADCs

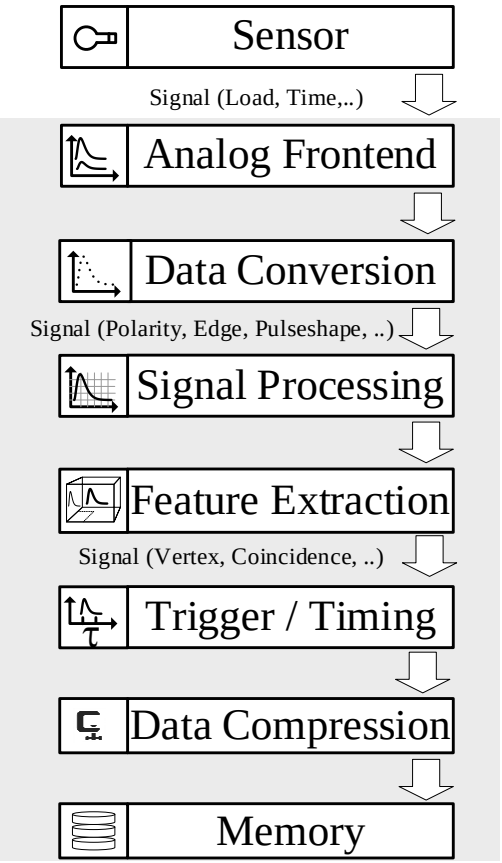


- ISSCC & VLSI 2016–2018 publications
- Off-the-shelf components as reference

→State-of-the-art high performance ADCs can compete in large-scale implementations

GEROLD

CONCEPT



- Power Reduction :
  - Close to Sensor
  - Data compression
  - System-on-Chip with Signal Pre-processing
  - Sensor-near Data HUB
- Optimized Signal Performance:
  - Analog Front-end
  - Flexible Dynamic Range ADC
- Low Footprint:
  - System-on-Chip with Clock Generation
  - Integrated Power Control
  - Integrated Bias Control
- Flexible Trigger Options

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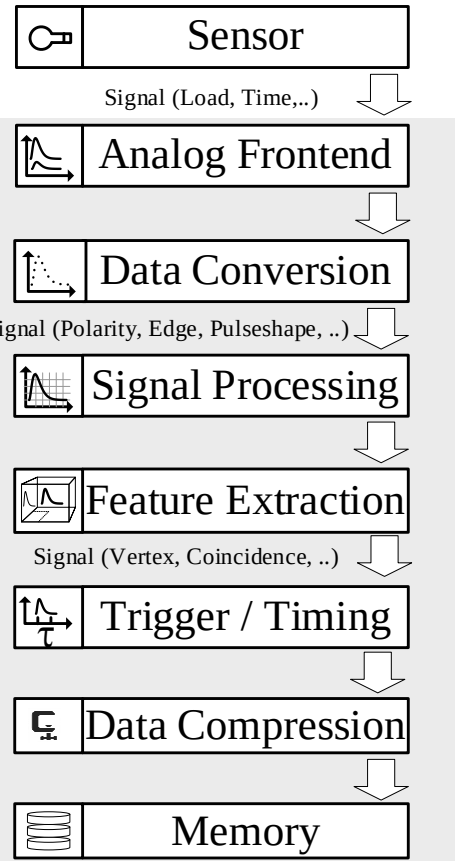
CONCEPT

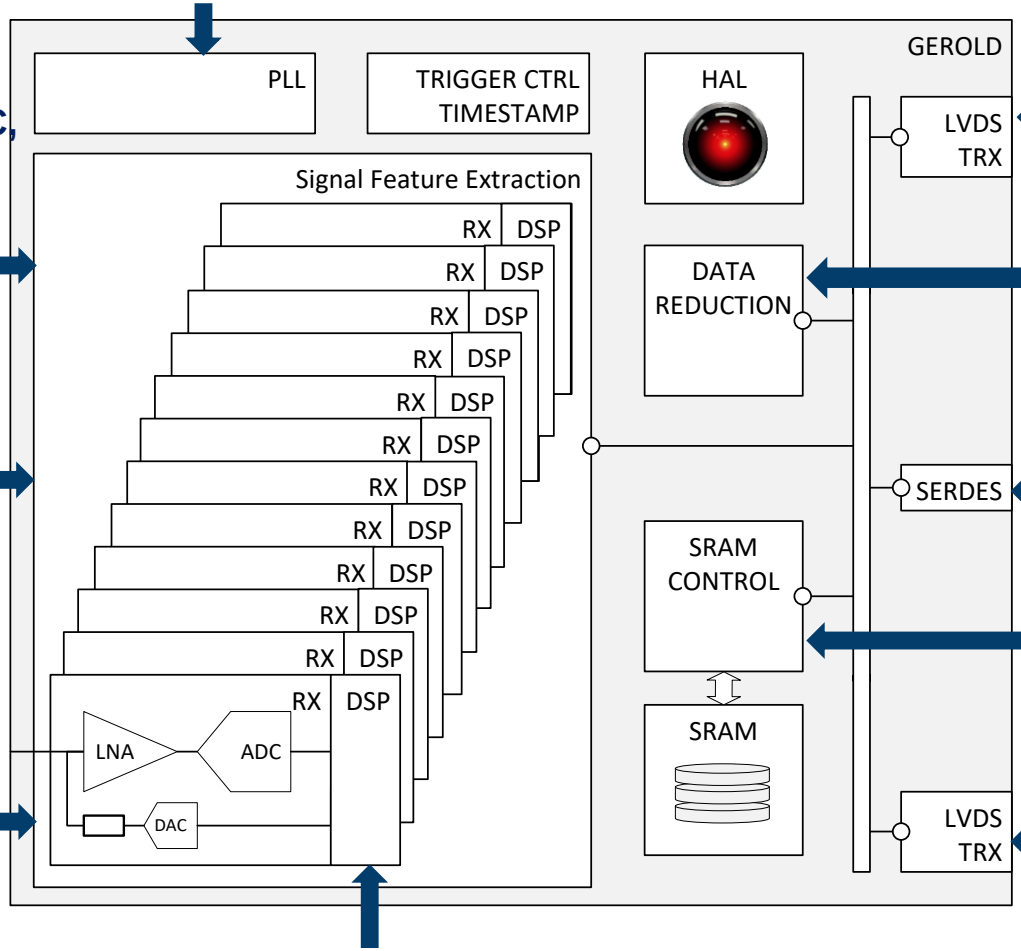


Internal Clock Generation

Up to 64 ADC in one ASIC, variable to combine for higher clock or ENOB

Programmable Input Impedance <10 – 100Ohm

Programable Bias
Built-in Self Test



LVDS Interface to link up with other ASIC

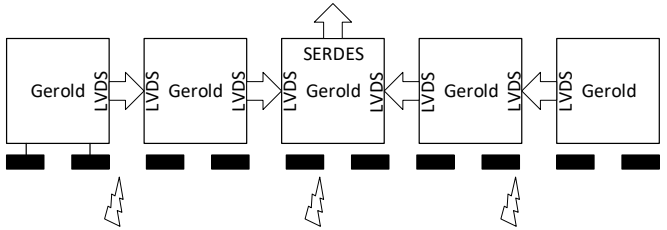
Data ordered by timestamp and zerosuppression

Highspeed Interface to optical converter for up to 100m Data upload

Built in SRAM Memory to lower Bandwidth requirement to average

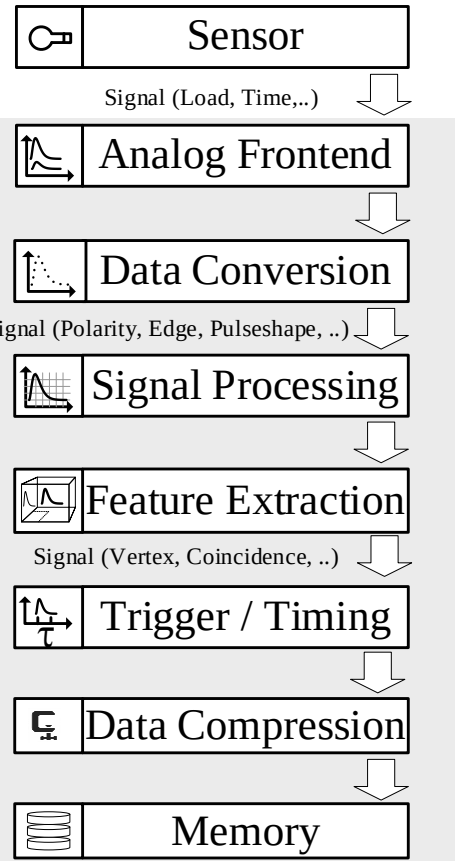
LVDS Interface to link up with other ASIC

Calculation of TOA, Feature Extraction: Wavelet, TOT, Number of Hits,…



GEROLD

CONCEPT



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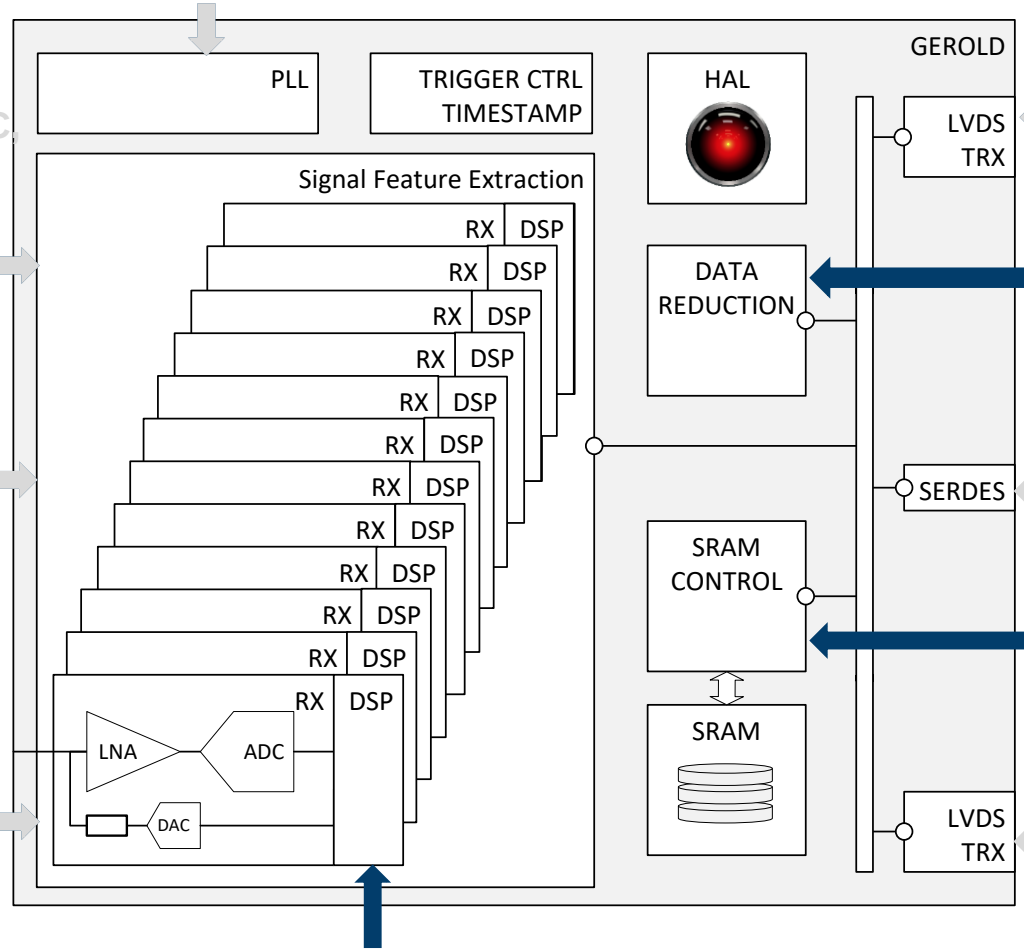
Programmable Input Impedance <10 – 100Ohm

Programable Bias
Built-in Self Test



LVDS Interface to link up with other ASIC

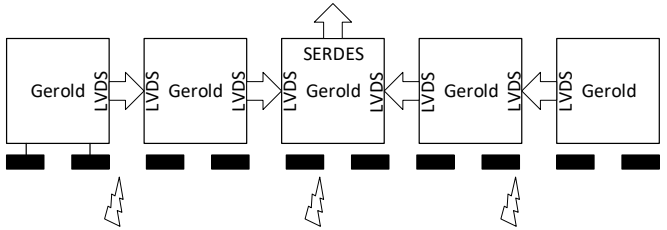
Data ordered by timestamp and zerosuppression

Highspeed Interface to optical converter for up to 100m Data upload

Built in SRAM Memory to lower Bandwidth requirement to average

LVDS Interface to link up with other ASIC

Calculation of TOA, Feature Extraction: Wavelet, TOT, Number of Hits,…



CMOS → 28/22nm

GEROLD

ANALOG FE

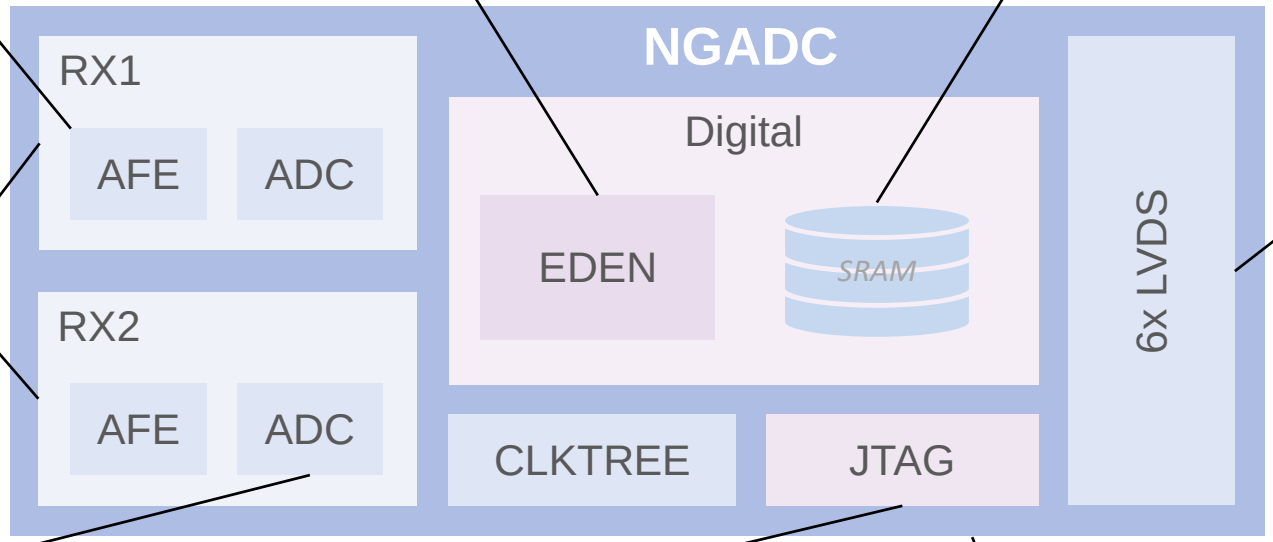
Configurable Front-End
Impedance 50 Ω, tunable
Bandwidth ≥ 350 MHz
Transimp. range 1-10 k Ω
Bypass option

Configurable RX
2 parallel channels *or*
Time interleaved (2x rate)

Pipelined SAR ADC
Two stages (4 bit & 8 bit)
Sample Rate ≤ 500 MS/s
Resolution 8-12 bit

Trigger Options
Level threshold
Integral threshold
External trigger

On-Chip Memory
16 kByte SRAM
Variable data format



LVDS Output
6 pairs, ≤ 1 GHz each
Throughput ≤ 12 Gbit/s
Configurable output
- 6x data
- 5x data + 1x clock
- 1x data + 1x clock
- 1x data

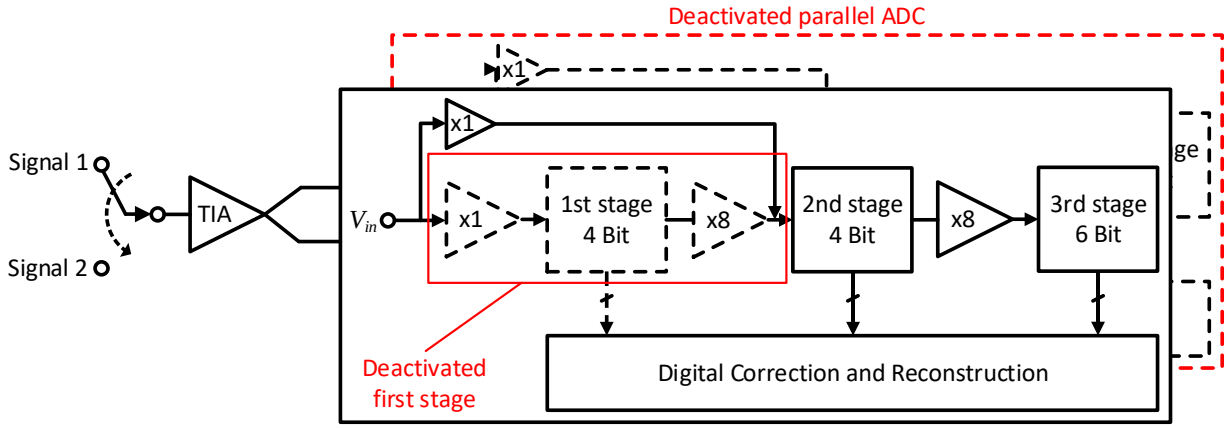
Programming Interface
JTAG standard, ≤ 100 MHz
Config registers 984 bits

Interrupt Interface
1 configurable input
1 configurable output

GEROLD

ADC

- Software-configurable
- Low power consumption
- Small area ~0.16 mm²



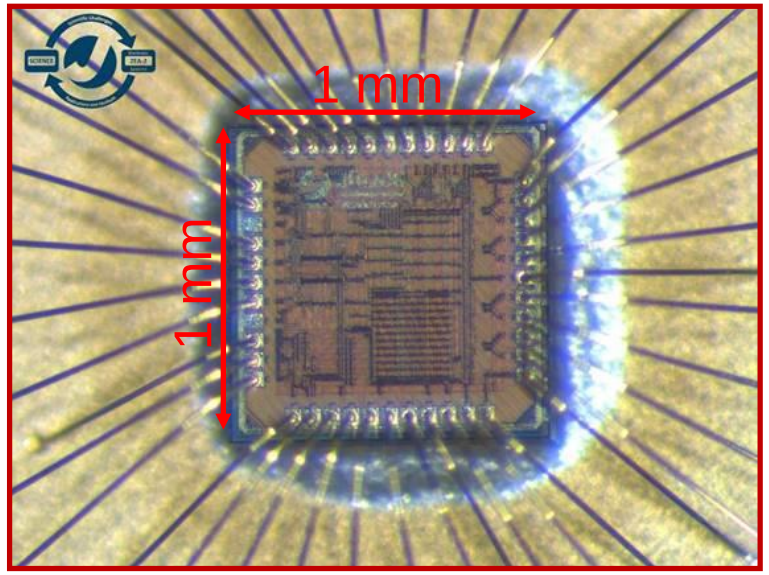
- Composed of three SAR ADC cores
- Configurable pipelining
  - High-precision mode: 12 Bit
  - Low-power mode: 9 Bit
- Configurable Parallelization
  - Double sample rate / amount of channels

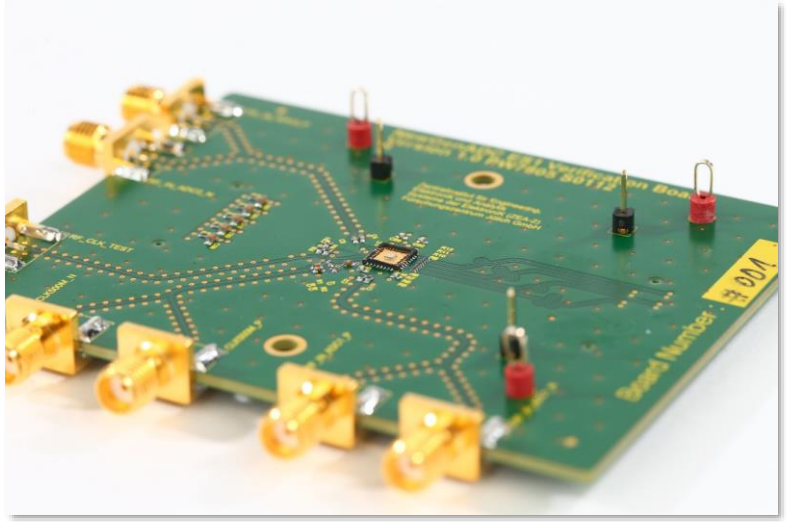
Resolution/ Bit	Time Interleaved	Sample Rate /MHz	Max. Channel	Power /mW
9	✗	≤ 500	2	4+3.8
9	✓	≤ 1000	1	8+7.6
12	✗	≤ 500	2	6+6.8
12	✓	≤ 1000	1	12+13.6

GEROLD

ADC

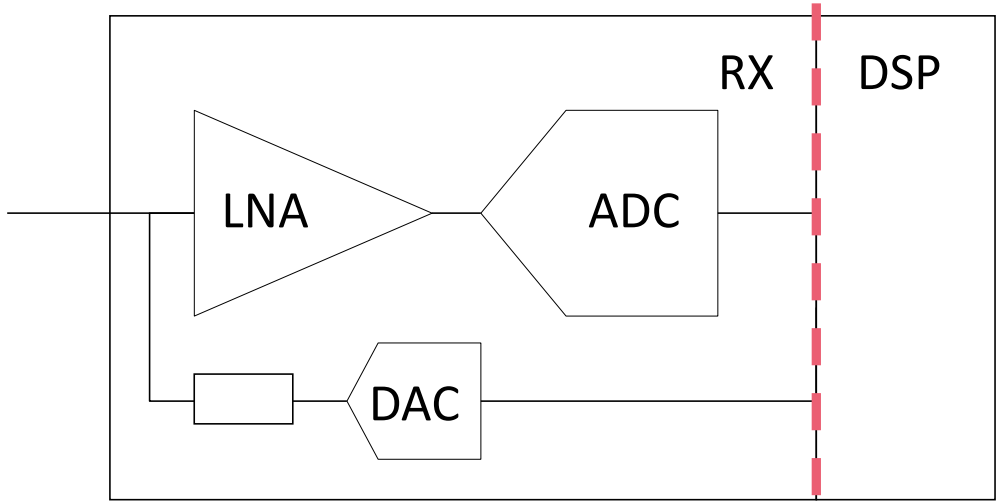
- Main feature:
  - Configurable SAR ADC (11 / 8 Bit, 400 / 700 MSPS)
    - Effective number of bits lower (~ 8bit / 7bit)
      - The discrepancy with the design values is yet to be understood
  - SRAM memory + digital trigger
  - QFN32 package with glass lid

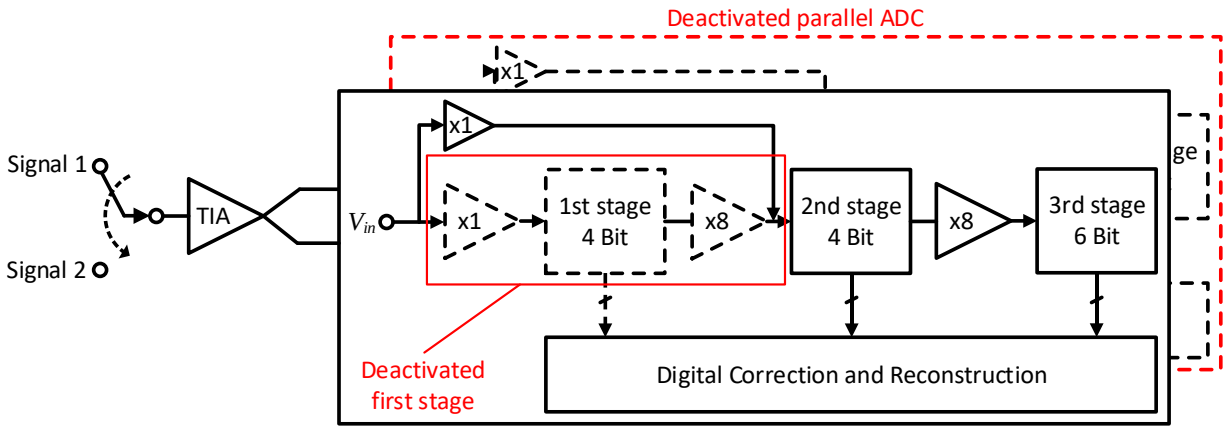


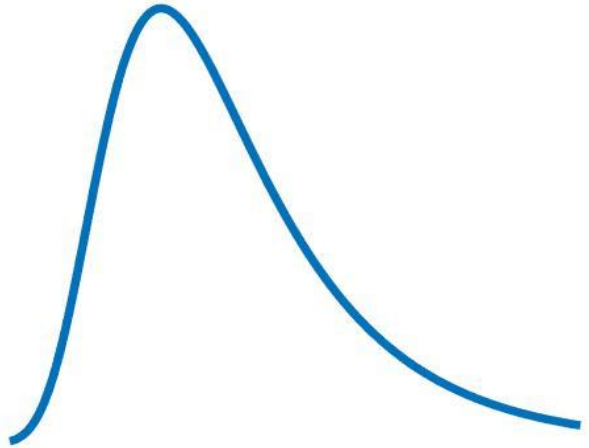


DIGITAL PART

A POSSIBLE DSP







$$P(t; t_0, \tau, A, n) = A\left(\frac{t - t_0}{\tau}\right)^n e^{-\left(\frac{t-t_0}{\tau}\right)}$$

Jokhovets et al, 2019

- Feature: sampling
- DSP: linear rise approximation

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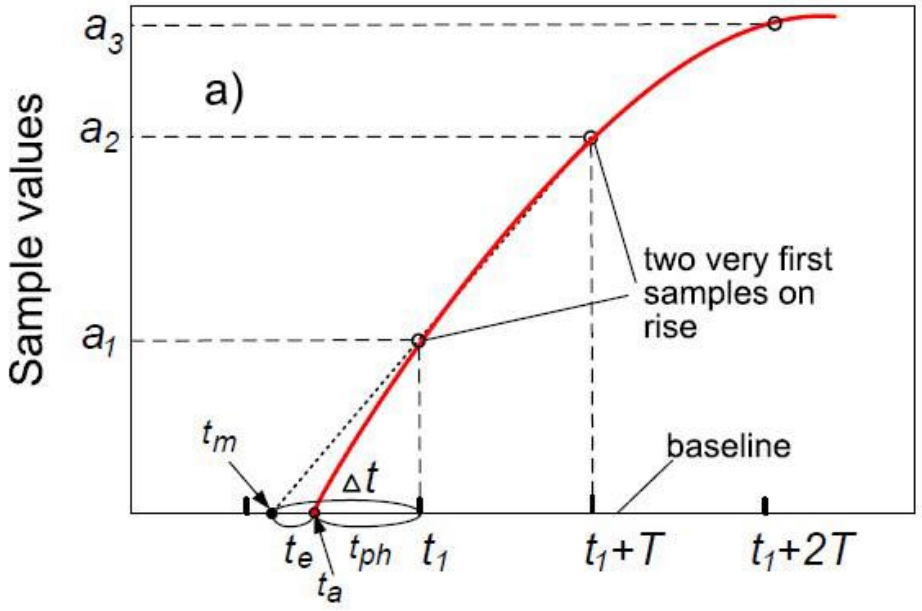
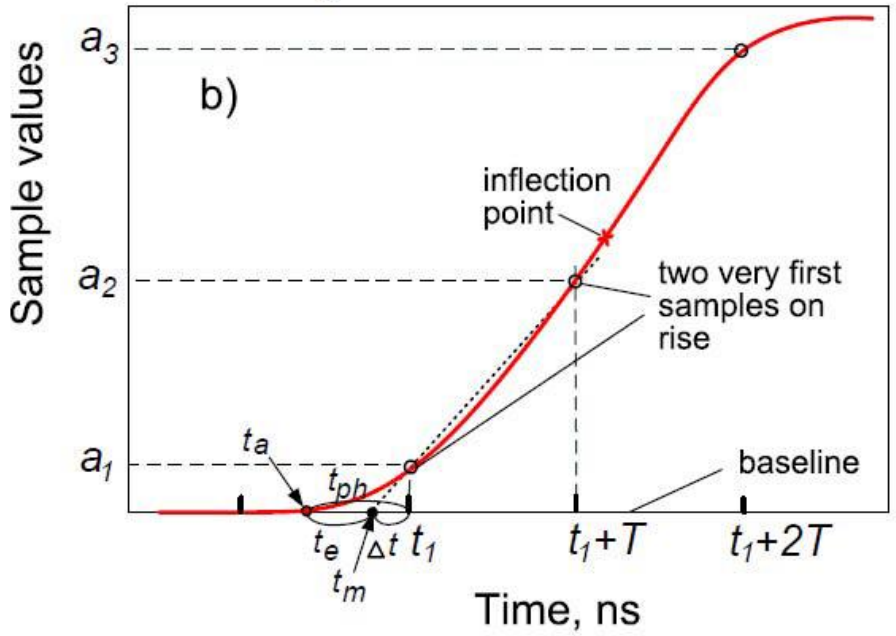
SUB-100 PS – OUR APPROACH

LINEAR RISE APPROXIMATION METHOD



CR-RC model of a pulse



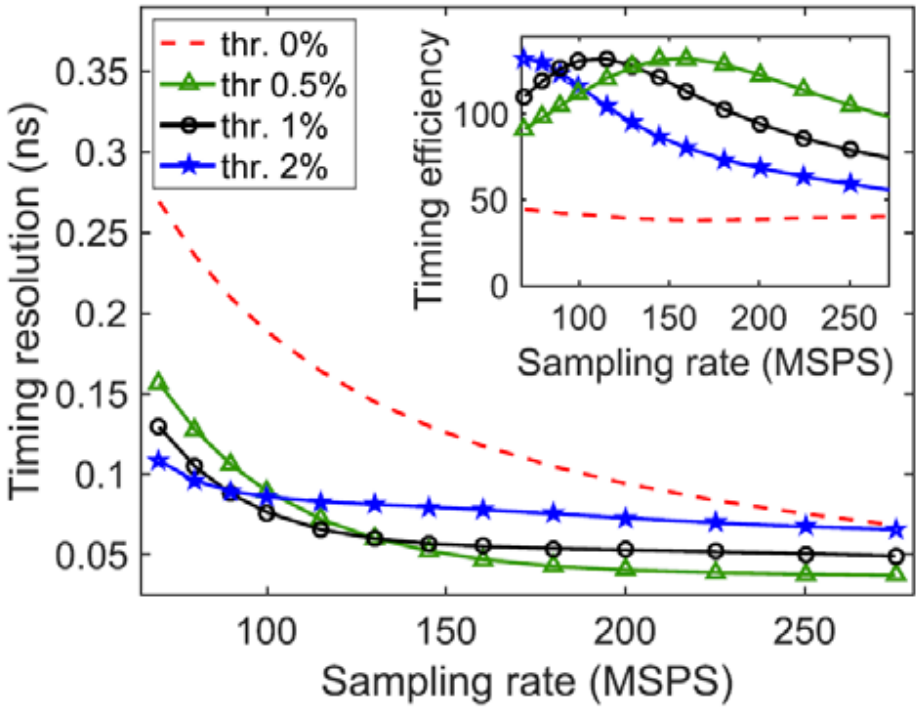
CR-RC^2 model of a pulse

The method is based on free running ADC and recording of a few first samples after the threshold. Calculated resolution depends on pulse shape

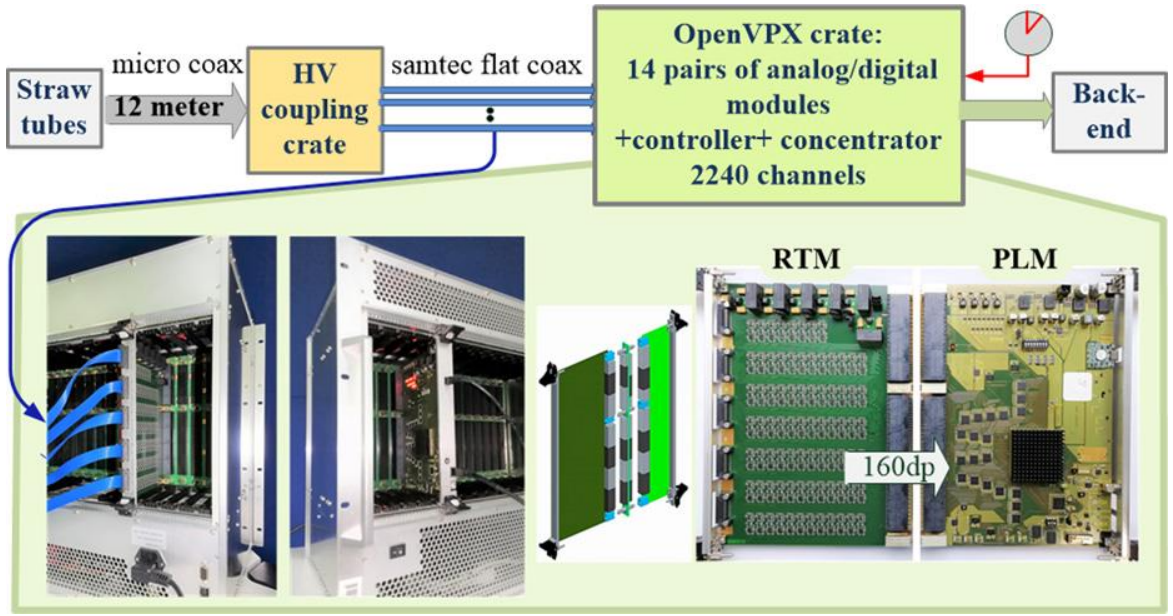
SUB-100 PS – OUR APPROACH

NON-LINEAR RISE APPROXIMATION (nLRA)

nLRA is tuned to nonlinear rise-time of pulse LE



for pulses with 15ns t_r

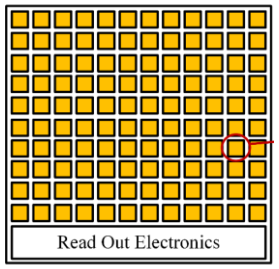


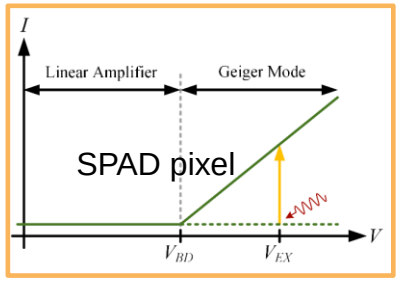
- Readout system for straw-tubes (PNDA). Now repurposed to work with SiPMs and to test nLRA for pulse arrival time
- ADC speed: 250MS/s – **two times slower then current GEROLD FE ADC**

- **Results promising:** test bench measurement ~ 105ps time for 250MS/s ADC
- Will need to add CR-RC$^{(n)}$ into analog FE and implement nLRA into FPGA for test purposes. And then into silicon

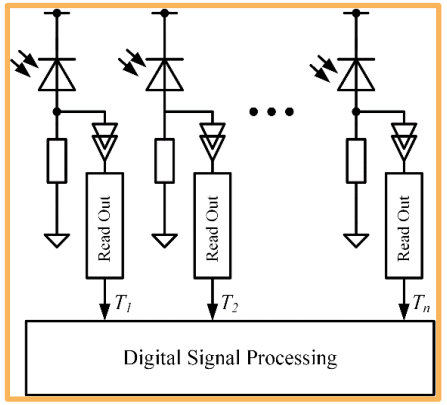
SPAD IMAGE SENSOR

PROJECT WE HAVE IN MIND

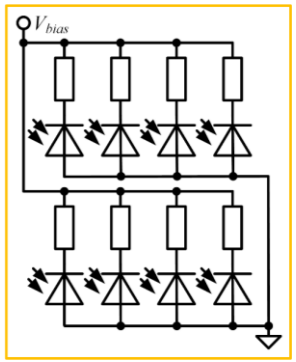


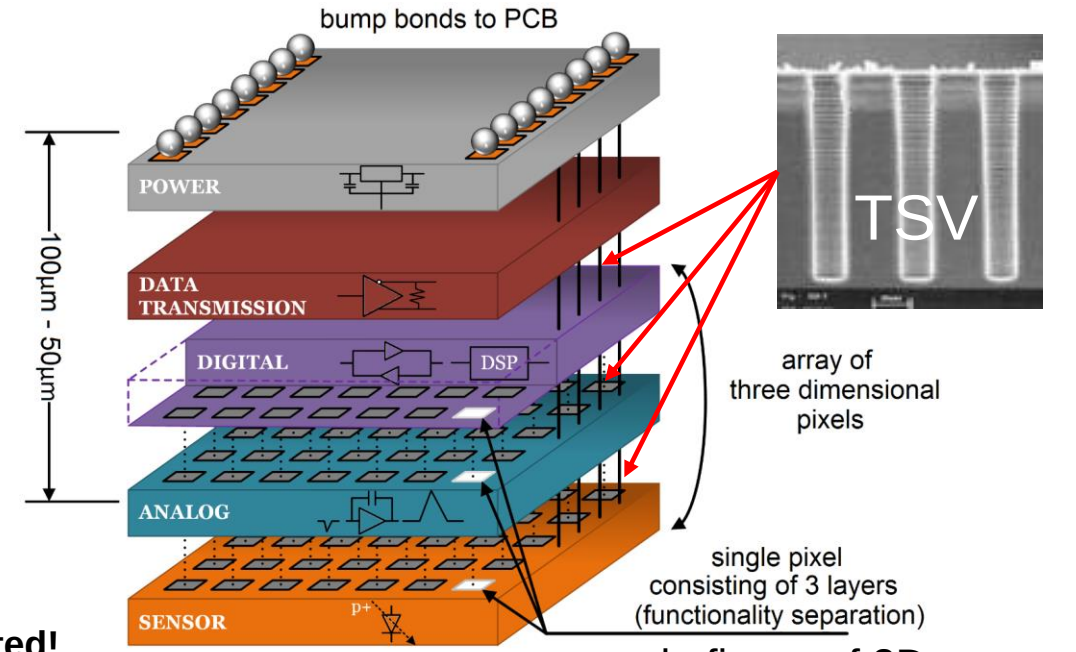


digital



analog





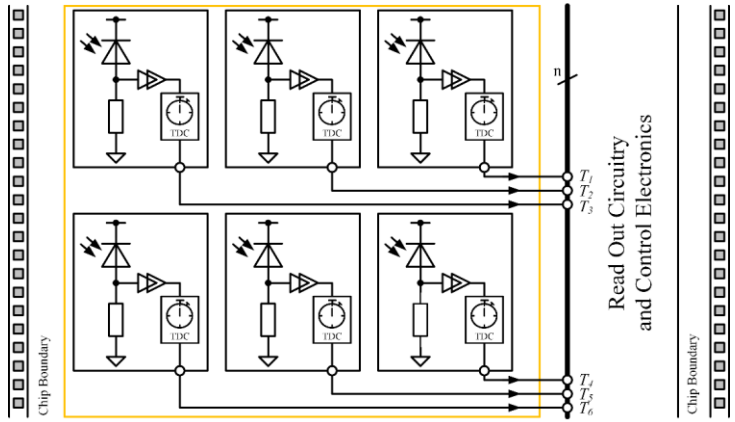
example figure of 3D sensor

Digital, not analog! Each pixel connected!

3D integration:

- more space for functionality
- Each layer – dedicated technology
- Mixing otherwise unmixed functionalities

Proposal of a scalable dSiPM SPAD array with SPAD level TDC is submitted



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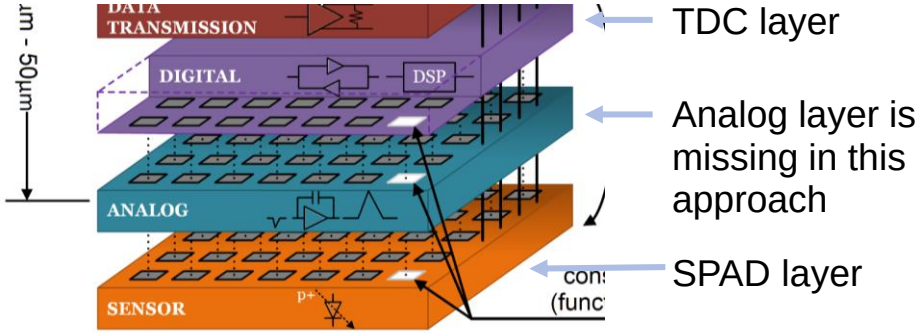
NEXT STEP II: SPAD IMAGE SENSOR

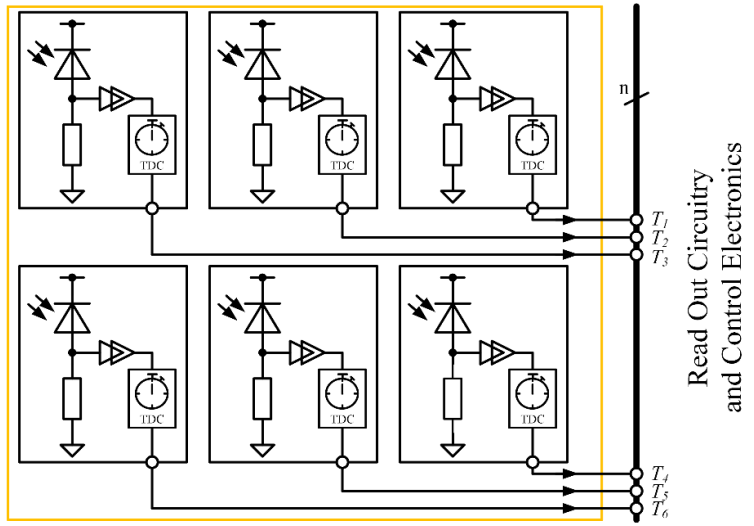
with SPAD level TDC using 3D Integration

Goal: implement TDC to be used with SPAD pixels

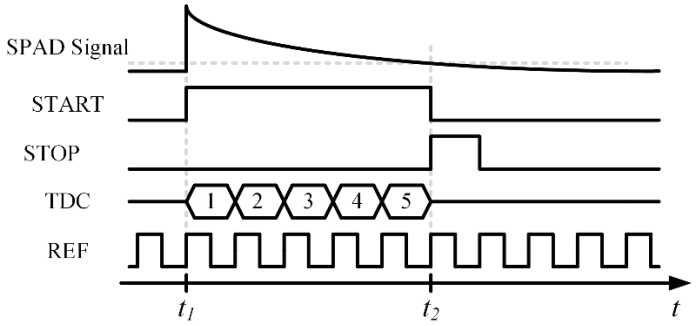
- TDC information encoded in time-domain: interval (Δt) between 2 voltage values ~ signal amplitude
- Charges generated in SPADs - similar → signal shapes similar
- CMOS shrinking + Vcc downscaling → design of analog circuits complicated + thermal noise floor goes up. Not very beneficial for high-res ADCs
- TDC information (time-over-threshold measurement) often used in HEP for particle detection
- Less power wrt. ADC



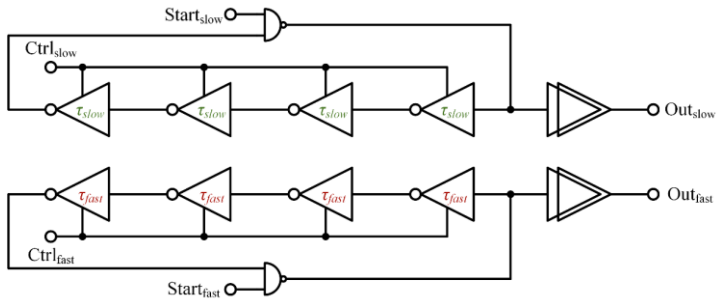
Proposed 3D concept for dSiPM



Each SPAD has local TDC



TDC principle



Vernier RO proposed as TDC

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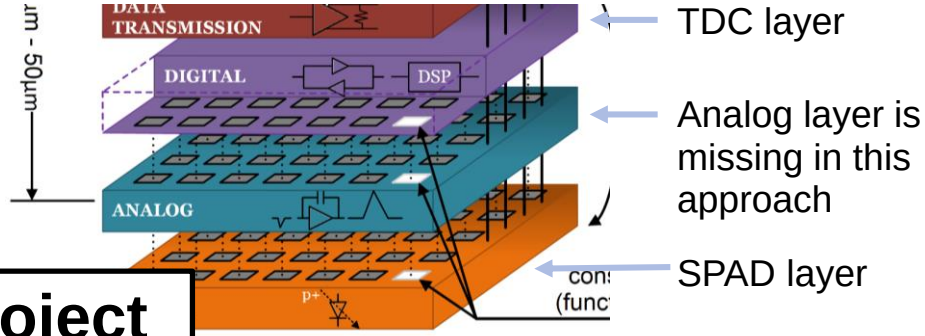
- CMOS shrinking + Vcc downscal
  complicated + thermal noise floo
  high-res ADCs
- TDC information (time-over-thres
  HEP for particle detection
- Less power wrt. ADC

Already submitted project proposal for TDC

Includes engineering runs

Together with RWTH and help from Fraunhofer



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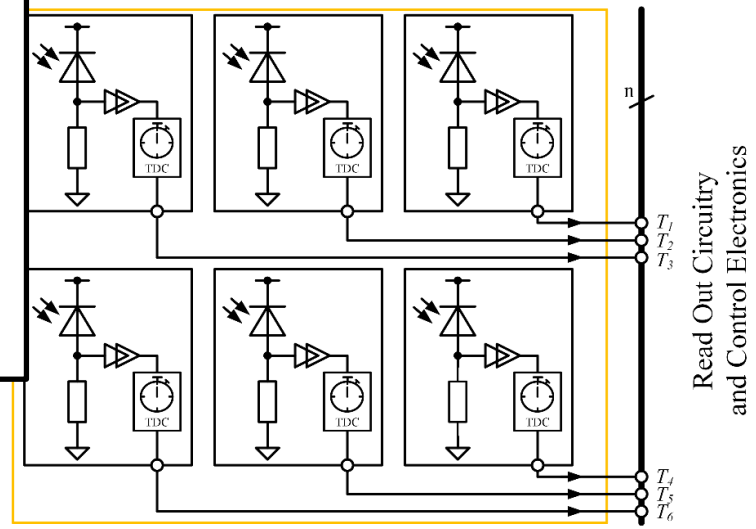

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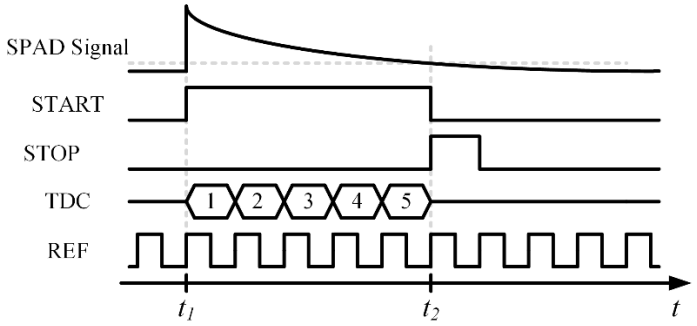

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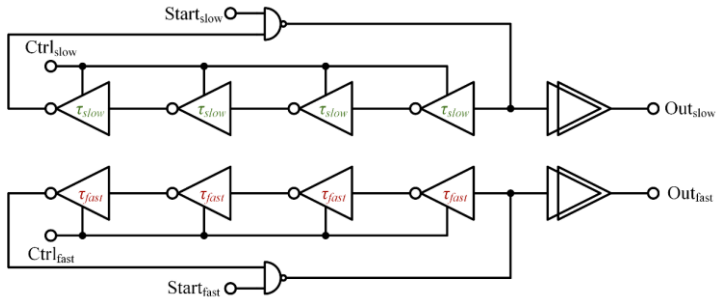

Vernier RO proposed as TDC

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MRI-PET ELECTRONIC WORKSHOP IN DUISBURG

When, Where: September 12-13 2023, Duisburg, Germany

Participant Groups:

- Electronic developers (**technology enablers**)
- major players in the field PET and PET/MRI R&D (**application**)
- Representatives from funding bodies and industry (**funding**)

Questions to answer:

- What is the vision for the next 3-5 years for your group?
- What are the parameters you would like to improve, new concepts you'd like to realize?
- What new technology, methodology is important to develop / improve to achieve your goals?
- What would you need to enable your ideas?
- Building networking, collaborations and writing common proposals
- Brainstorming regarding funding with funding body representatives

#PETtech23

PET Electronics & Technologies 2023

Workshop on
Electronics and Advances for Future High-Performance PET Systems

September 12th – 13th 2023
at Fraunhofer-inHaus-Zentrum in Duisburg, Germany

SAVE THE DATE

Contact:
Anna Herholz
Mail: PET-workshop@ims.fraunhofer.de
Phone: +49 203 3783 210

Fraunhofer IMS · CERN · Ghent University · Neuromed I.R.C.C.S. Istituto Neurologico Mediterraneo · Jülich Forschungszentrum

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UC Davis
LMU Munchen
U Krakov
U Valencia
U Heidelberg
KU Leuven

INFN Torino
LBL
LIP
CEA
EPFL

Broadcom
Tezzaron
WEEROC
Siemens MI
.....

SUMMARY

- We are currently working on a new distributed readout ASIC (GEROLD) for various applications based on SiPMs, Straw-Tubes, and PMTs
  - One of the main drivers - find an alternative to PDPC, use broader spectrum of aSiPMs
  - A significant portion of modules are implemented or in the design phase. Work on RAM is ongoing.
  - Anyone willing to join us will be very welcome
- An application for a small 3D SPAD “image sensor” prototype is submitted and we are waiting for an approval from financial body.
  - And we mean to continue working on 3D-integration for SPAD sensors
  - Anyone willing to share this burden will be met with open arms

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  - Anyone willing to share this burden will be met with open arms

And please, do not hesitate to grab the PET workshop flyers!

Duisburg is not Elba, but the organization committee will do its best to outshine high unemployment rate and old glory of now abandoned coal mines of the city.

THANK YOU!