A real time sub-picosecond phase correction system

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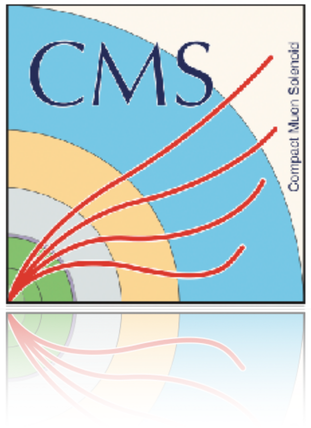
29/05/2023



FAST 2023

The need for Precision Timing

- The use of precision timing to measure time-of-flight or to distinguish events from the same bunch crossing in collider detectors has become a common feature of many modern experiments.
- Many new experiments are pushing the boundaries of precision timing measurements to improve background suppression and precision measurements

HL-LHC time v. Position of 140 pile up bunch crossing.

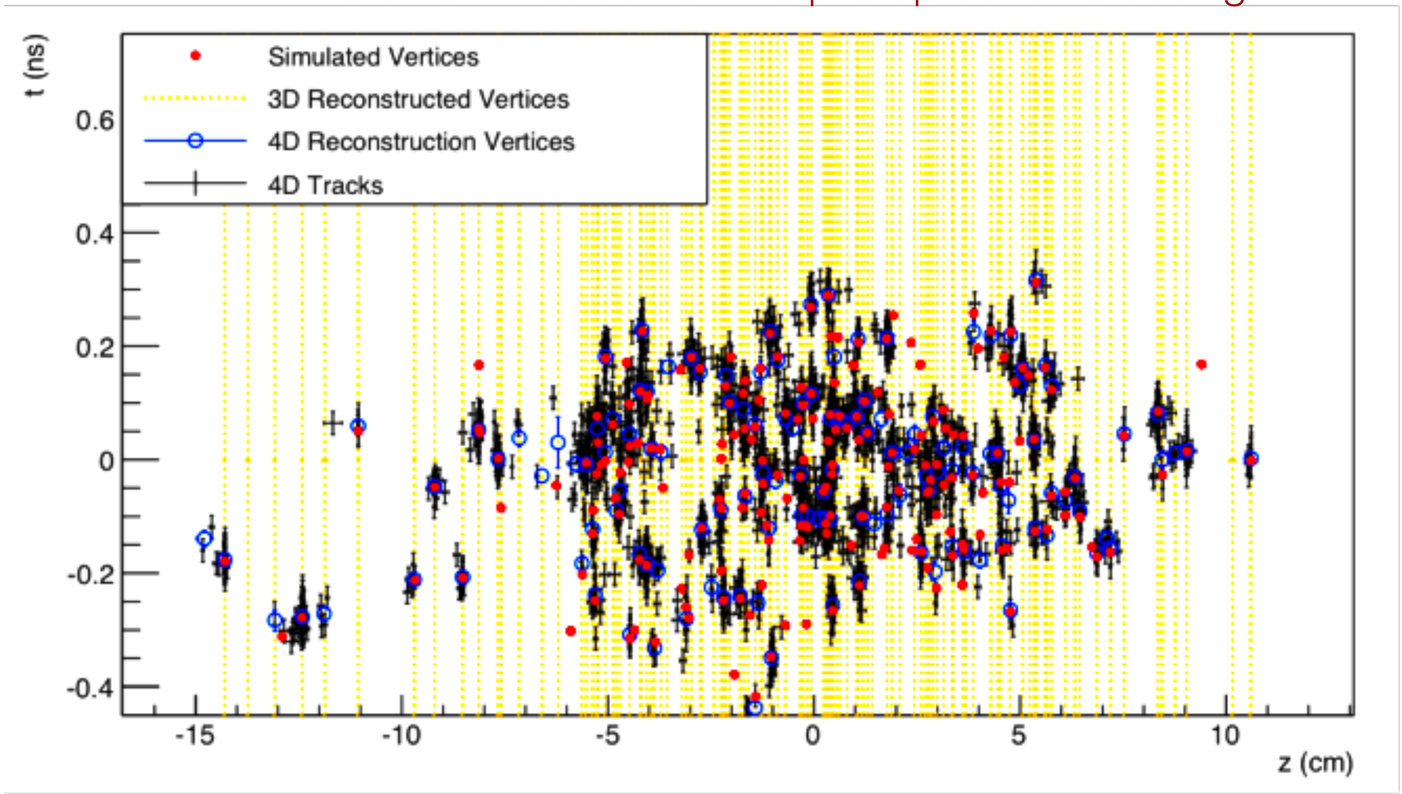


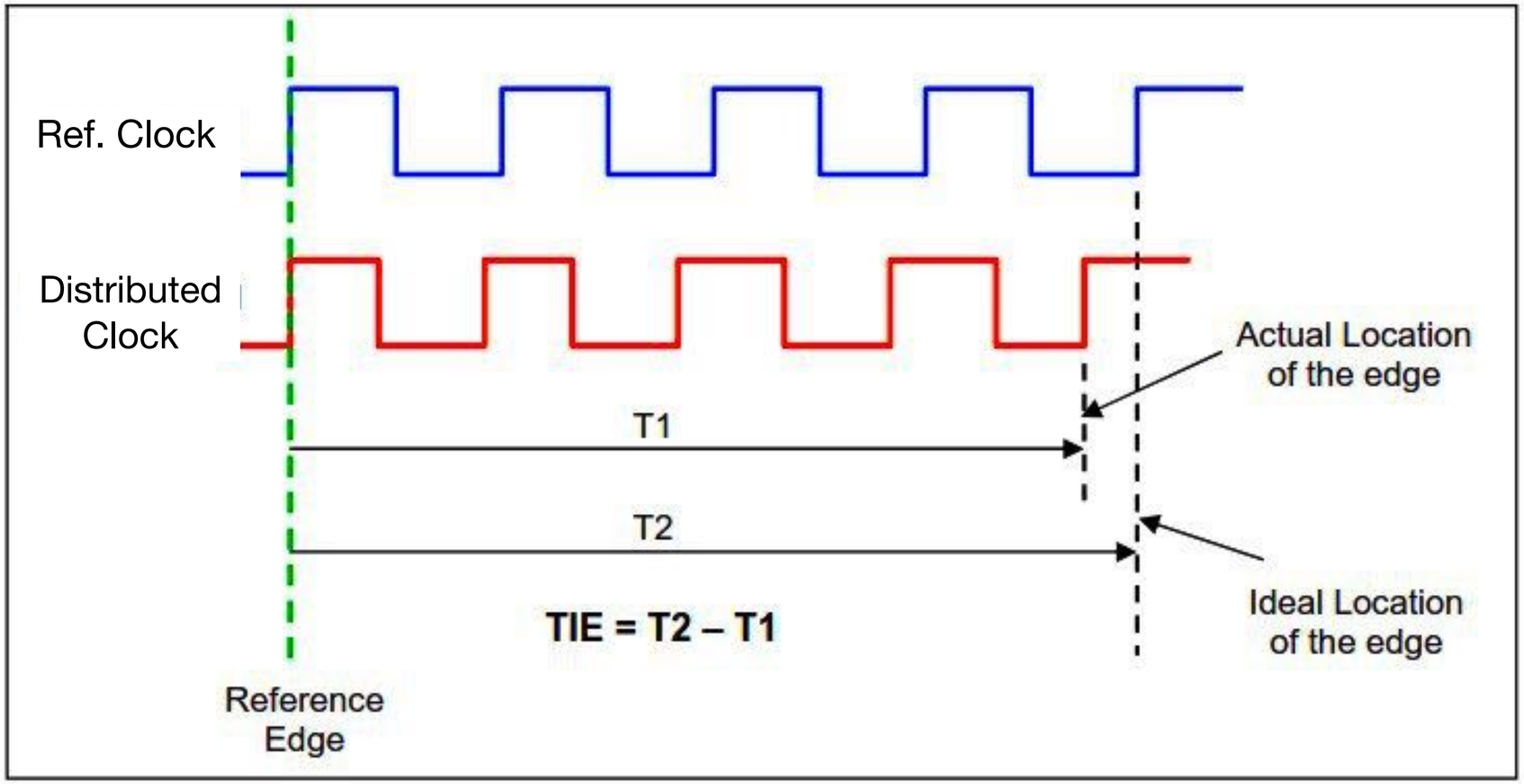
Figure shows the simulation of CMS detector where vertices that are overlapped spatially can be resolved in the time domain

https://doi.org/10.22323/1.398.0813

Time Interval Error (TIE)

Quantifying Time Jitter in Clocks

- The Time Interval Error is the time difference between the edge of the reference clock and the edge of the distributed clock
- TIE is measured for multiple edges and the standard deviation is quoted as a measure of jitter/wander.
- High speed variation in TIE is called Jitter
- Low speed variations in TIE is called Wander



Precision Timing Needs Better Clocks

- The time resolution of the detector system has contributions from

$$\sigma_t \approx \sigma_t^{clock} \oplus \sigma_t^{ele} \oplus \sigma_t^{detector} \ldots$$

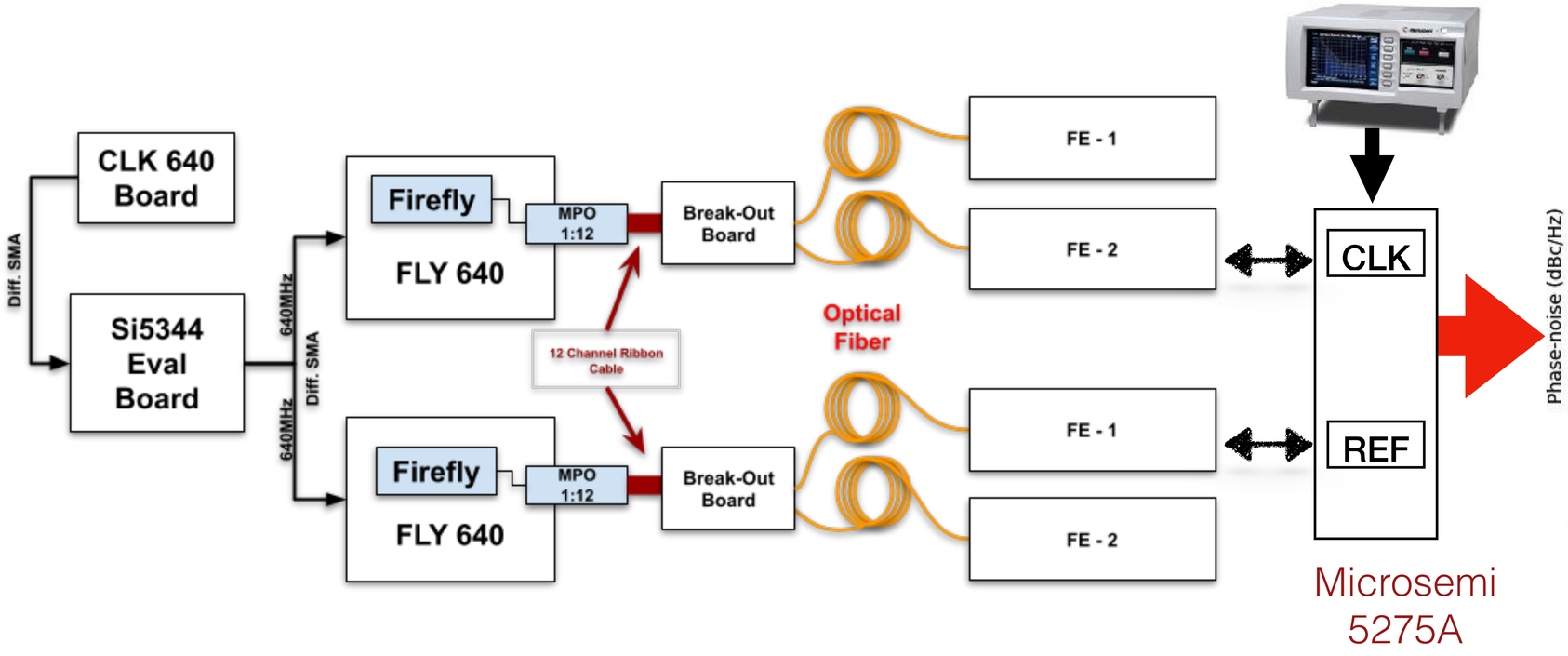
- In order to measure the time of interaction in your detector precisely, you need to have a reference clock with jitter that adds marginally to the measurement that you are making

Jitter (High Speed Variations) can be mitigated using jitter attenuators and dedicated channels for distribution

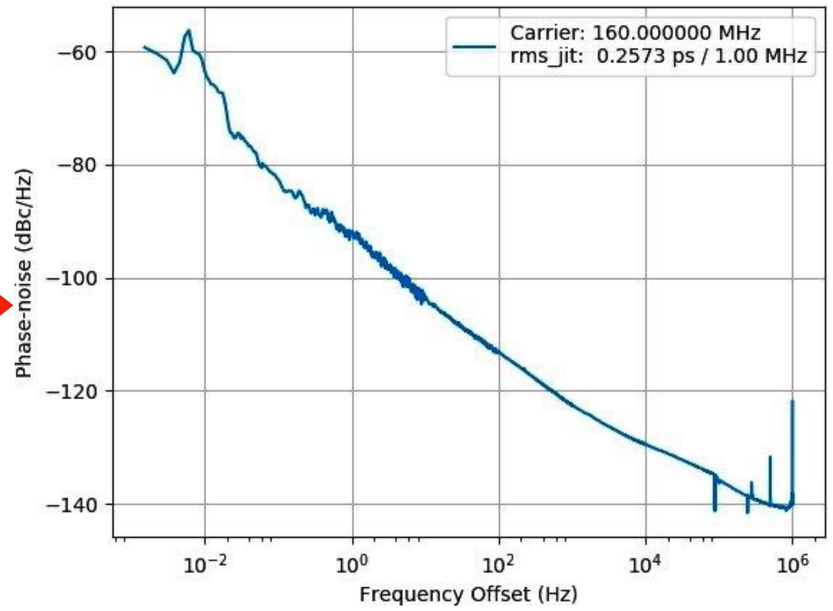
Lets look at such a scalable prototype without jitter attenuator

‘Pure’ Clock Distribution System

Distributing clocks using dedicated channels



Phase Noise Plot 0.1Hz - 1MHz
[160MHz Carrier Frequency]



- A dedicated clock fan-out system was built for this purpose using off-the-shelf components keeping scalability in mind
  - RF Quality Fanout from ON Semiconductor (NB7VQ1005MMNG)
  - Each FLY 640 board scalable up to 216 output channels employing 18 fireflies

$$\sigma_{phase} = \frac{1}{2\pi f_0}\sqrt{2\int_{f_L}^{f_H} L(f)\,df}$$

$$\sigma_{phase} = 0.26ps$$

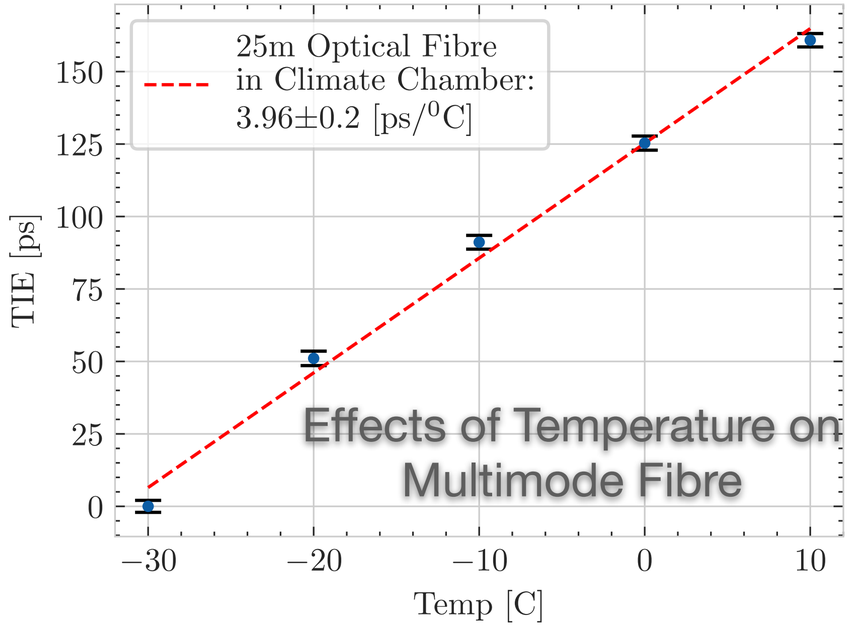
But what about wander?

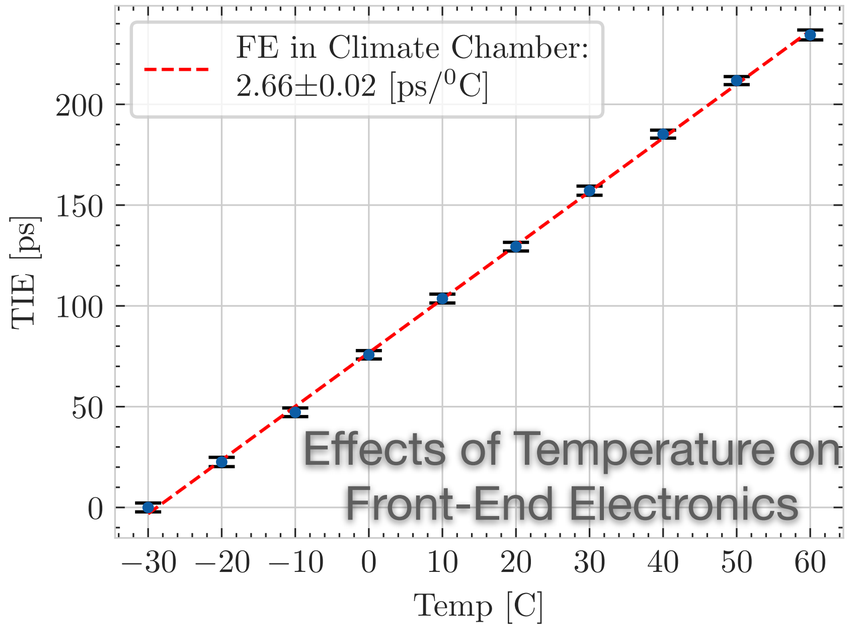
Note: Light travels ~300 microns in a picosecond in free space

Effects of Environment on the Clock

- Environmental effects such as temperature can introduce low frequency wander in the distributed clock
- Propagation time of 100m long multi-mode fibre changes by ~16ps/^{0}C
- Dedicated channels or jitter attenuator won't mitigate these effects

For a high precision clock, we need to monitor these shifts and correct for it.





Measurements made at the HPTD lab in CERN

Questions:

1. How do we measure wander?
2. How do we correct for it?

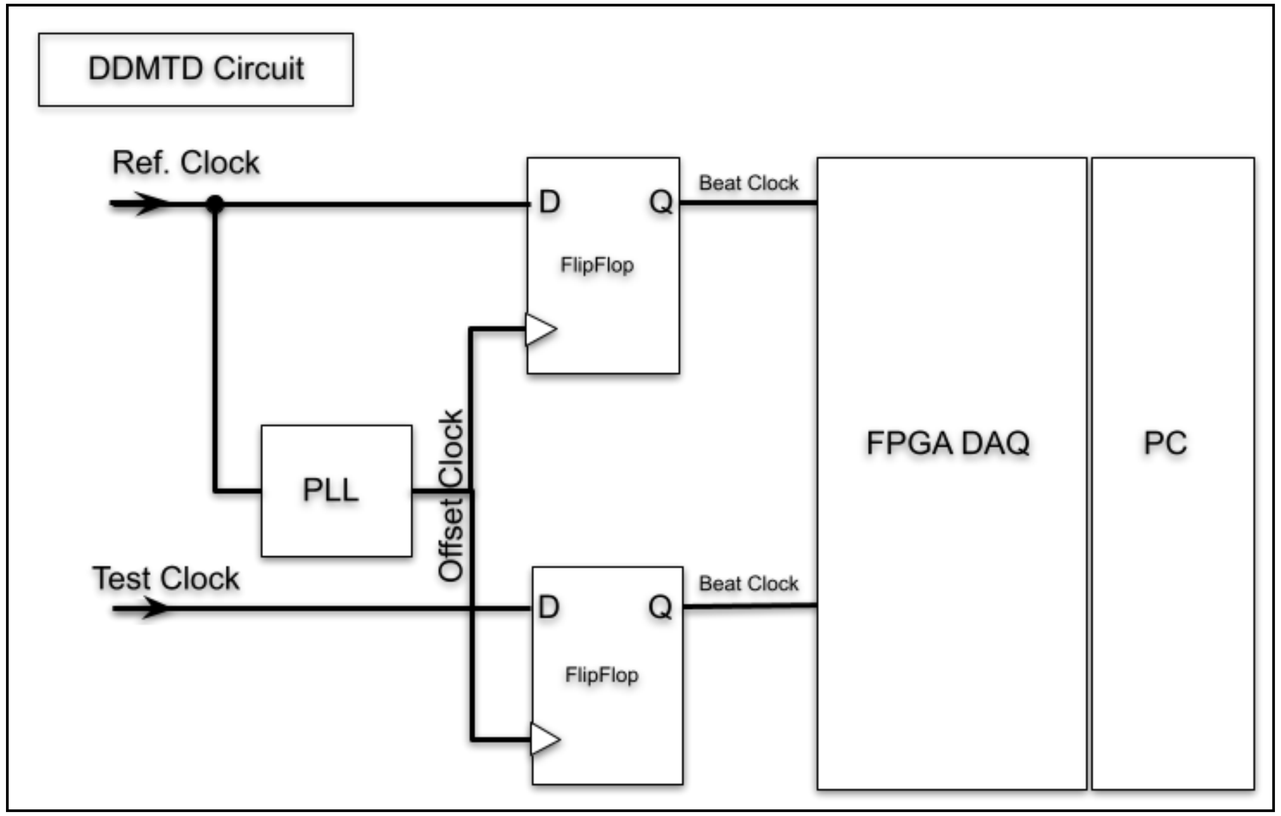
Measuring Time

Digital Dual Mixer Time Difference (DDMTD) circuit *

- Reference Clock and Test Clock are heterodyned with the help of a PLL and Flip Flops
- The PLL generates Offset Clock with the frequency relation:

$$f_{offset} = f_{ref} \cdot \frac{N}{N+1}$$

- N is the integer that determines the number of input clock cycles required for a full phase cycle of the heterodyned signal
- The time difference between the beat clocks is used to calculate TIE between the Ref.Clock and the Test Clock



Schematic of DDMTD Circuit

*First proposed by P. Moriera in 2010

This means sub-picosecond precision

Plugging in some numbers

$$f_{beat} = \frac{1}{N} \cdot f_{offset} = \frac{1}{N+1} \cdot f_{ref}$$

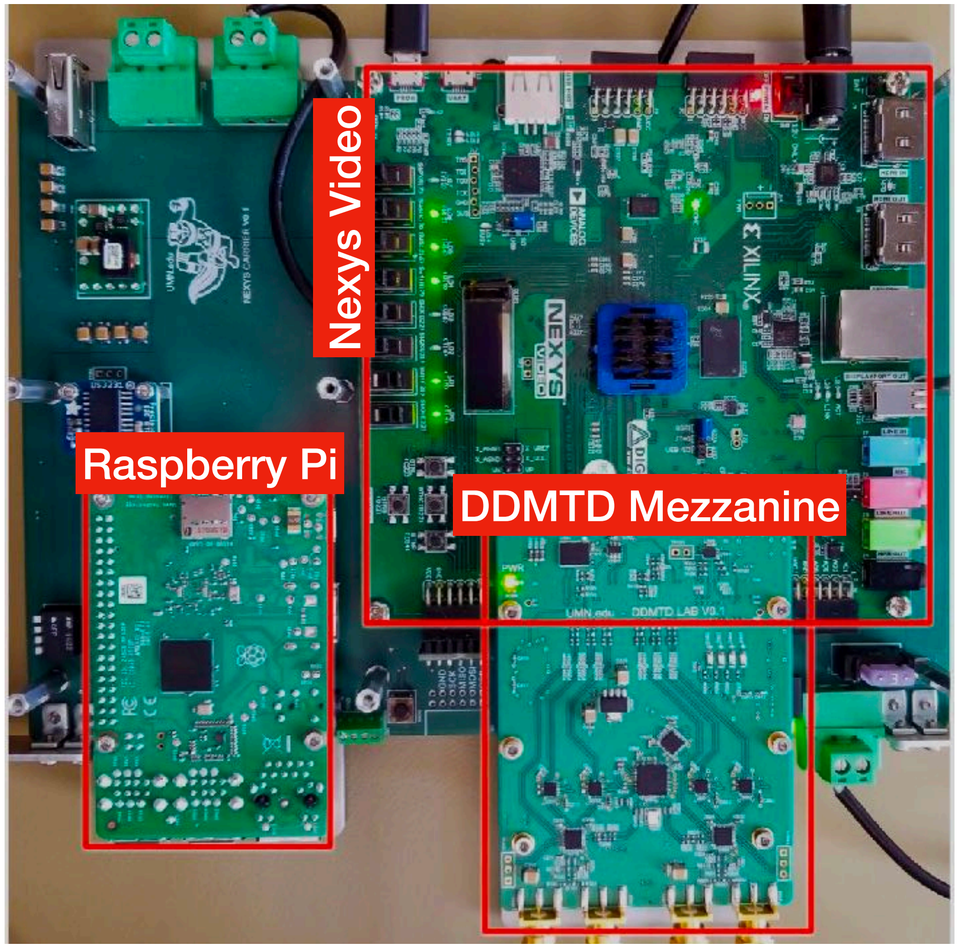
$$\Delta t_{min} = \frac{\Delta t_{beat}}{N+1}$$

With $N = 100k,\ \ f_{ref} = 160MHz,$

$$f_{beat} = 1.599984 \text{ kHz}$$

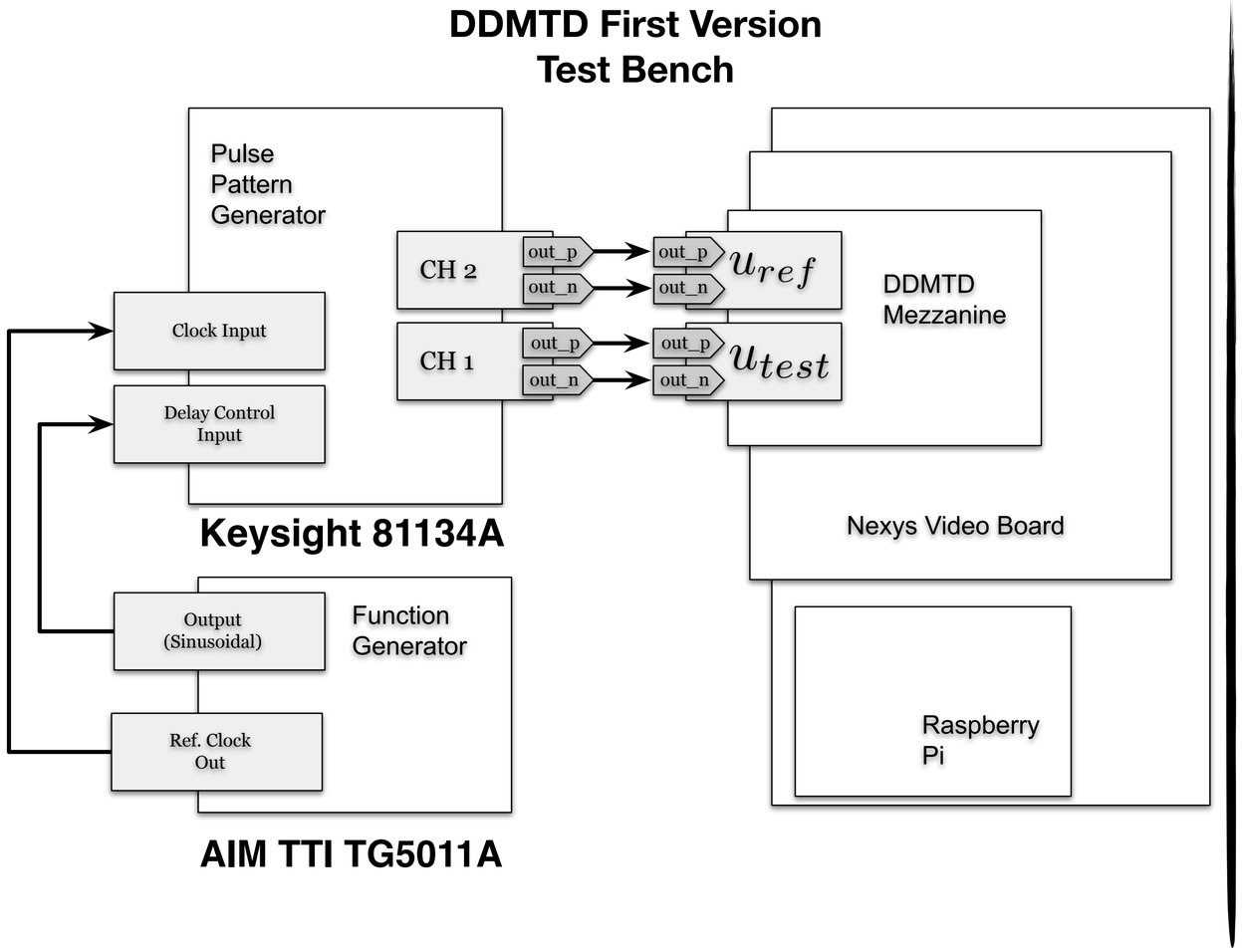
$$\boxed{\Delta t_{min} = 62.5fs}$$

Note that as we sample at f_{beat}, we lose sensitivity to higher frequency jitter.

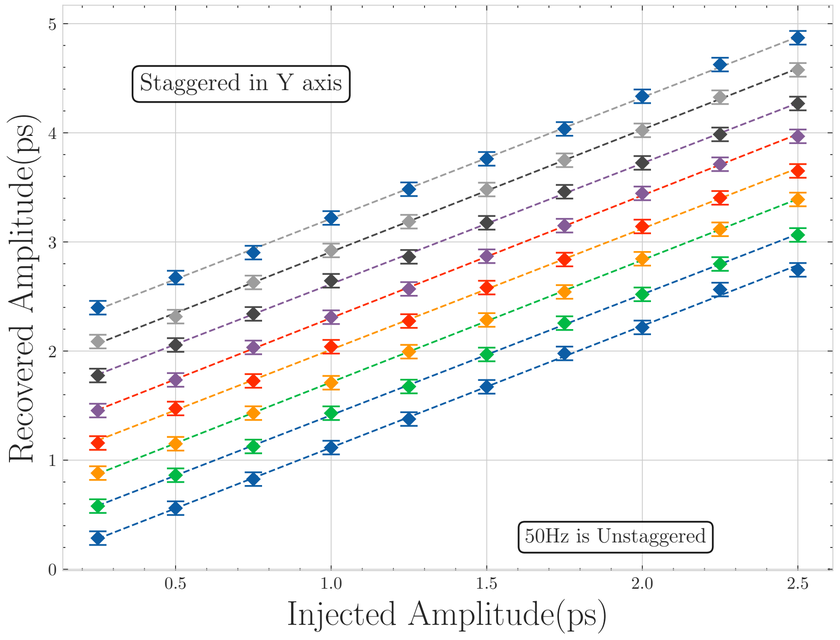


First Version of Single Channel DDMTD Board

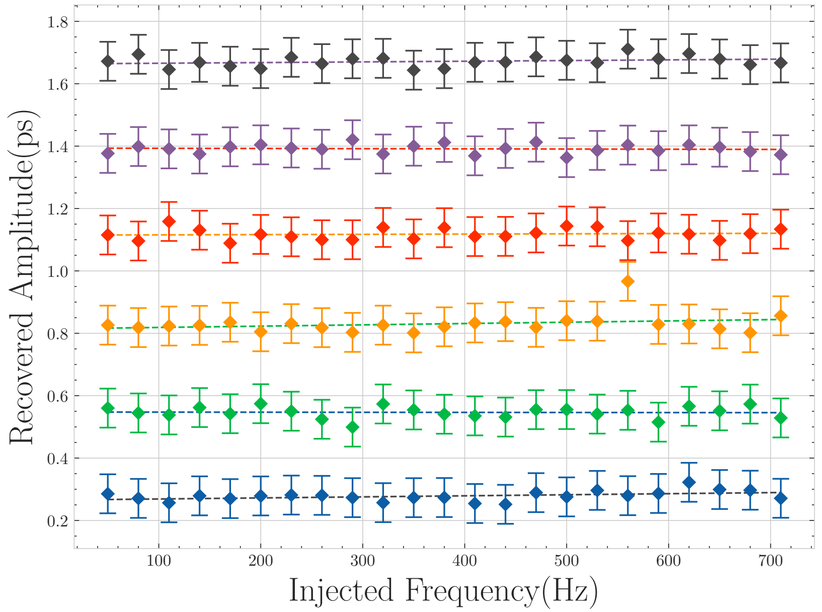
DDMTD Performance



	Fit Slope
50Hz	1.115 +/- 0.012
140Hz	1.107 +/- 0.005
230Hz	1.120 +/- 0.004
320Hz	1.109 +/- 0.009
410Hz	1.123 +/- 0.006
500Hz	1.106 +/- 0.007
590Hz	1.121 +/- 0.007
680Hz	1.111 +/- 0.008



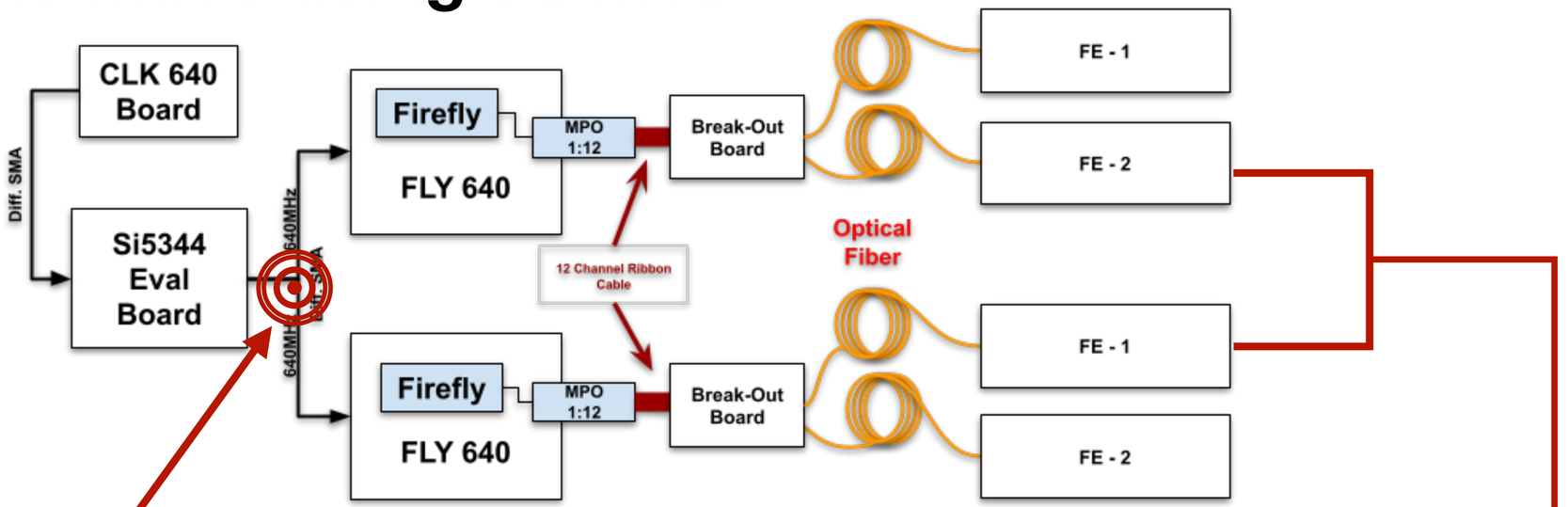
	μ_{rec_ampl} (ps)
0.250ps	0.278 +/- 0.003
0.500ps	0.547 +/- 0.004
0.750ps	0.831 +/- 0.007
1.000ps	1.118 +/- 0.004
1.250ps	1.391 +/- 0.003
1.500ps	1.672 +/- 0.003



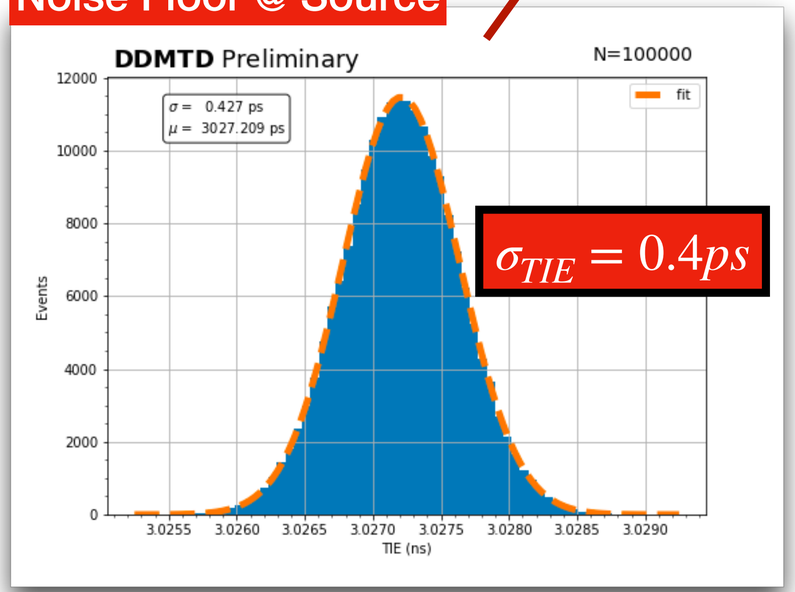
More Information Published Here: 10.1088/1748-0221/18/01/T01003

Revisiting Pure Clock Distribution

Measurements made using DDMTD



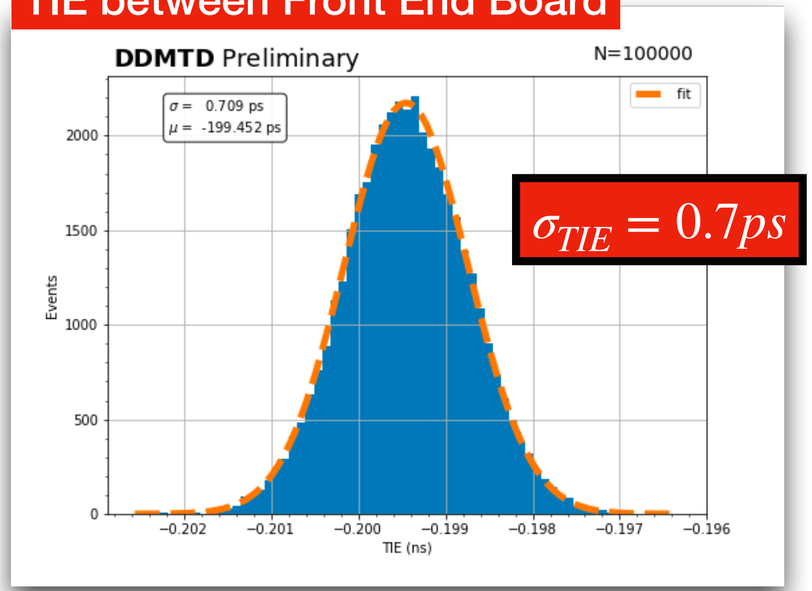
Noise Floor @ Source



$\sigma_{TIE} = 0.4ps$

$$f_{ref} = 160MHz$$
$$N = 100k$$
$$f_{beat} = 1.599984 \text{ kHz}$$
$$\Delta t_{min} = 62.5fs$$

TIE between Front End Board

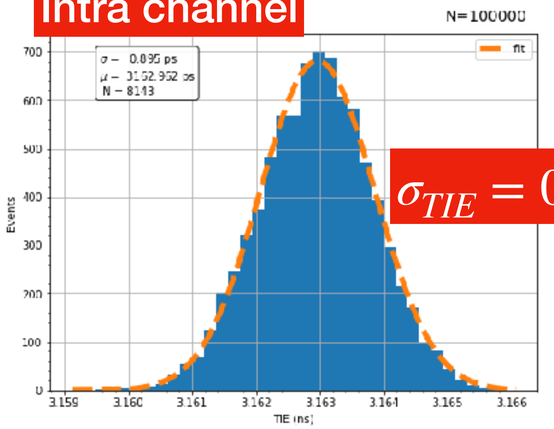


$\sigma_{TIE} = 0.7ps$

24 Channel DDMTD System

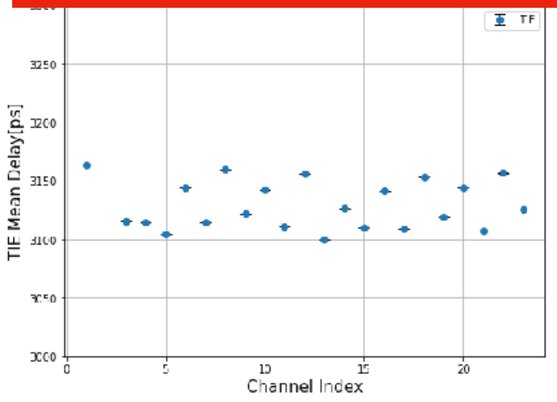
This board fans out clock generated by the OCXO to 24 channels and measures the drift of the returning clock w.r.t the reference clock

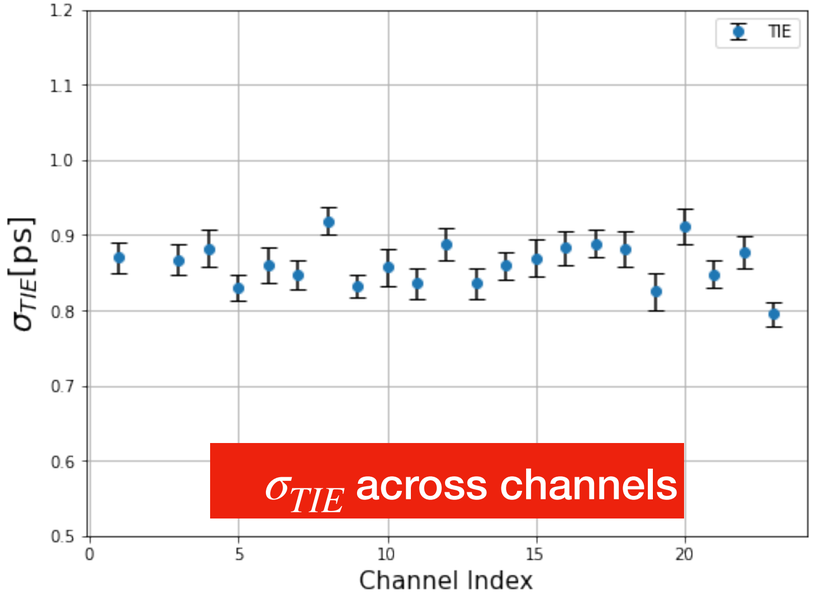
Intra channel



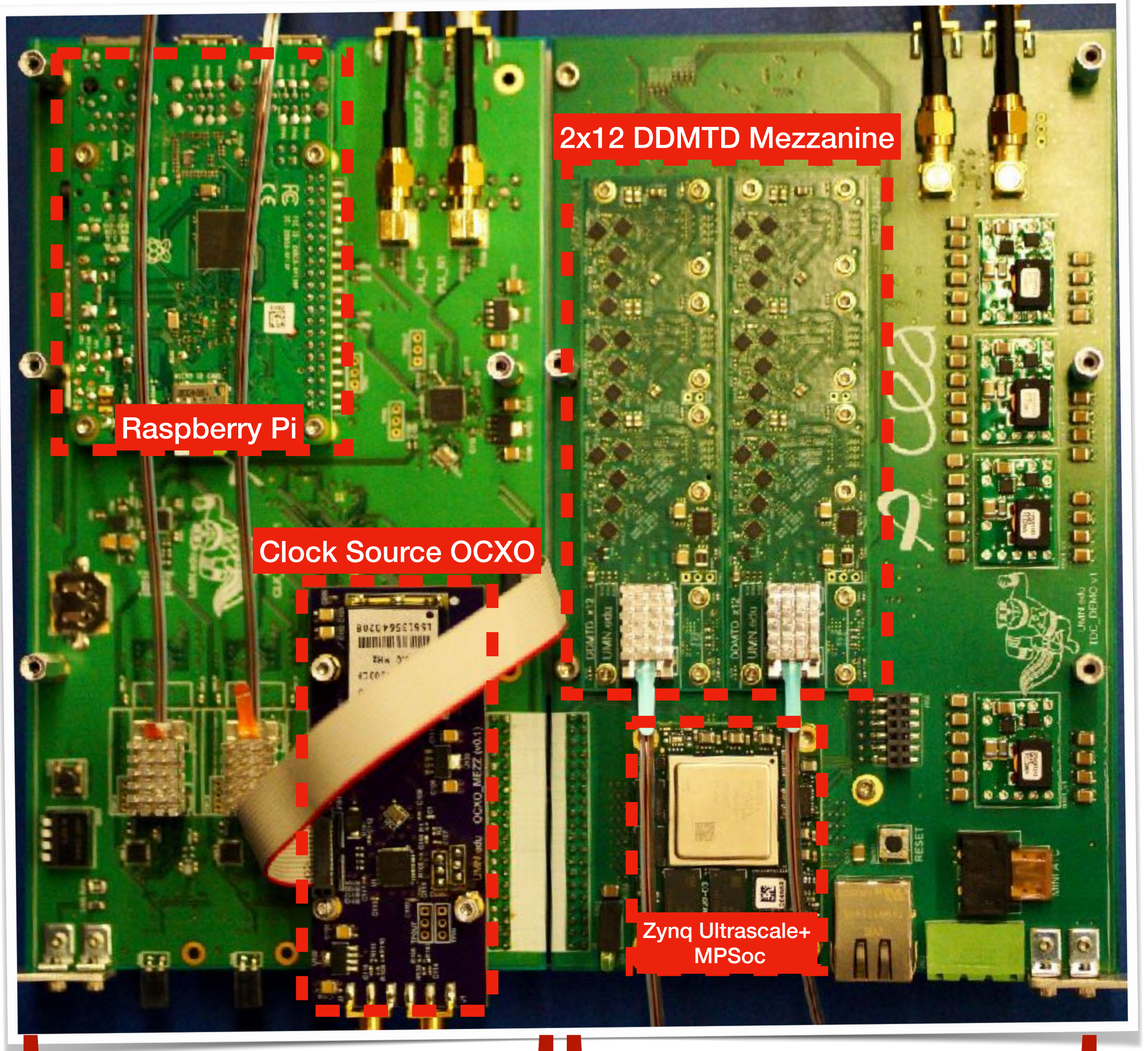
$\sigma_{TIE} = 0.9ps$

Mean of TIE across channels





σ_{TIE} across channels



Clock Generated And Distributed

Returning channels measured using DDMTD

Questions:

1. ~~How do we measure wander?~~
2. How do we correct for it?

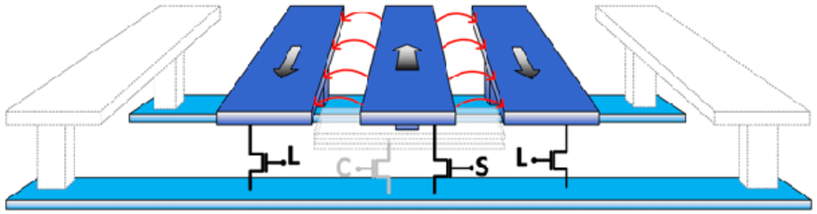
Correcting for Drifts in Clock

How Digitally Controlled Phase Shifter (DCPS) Works

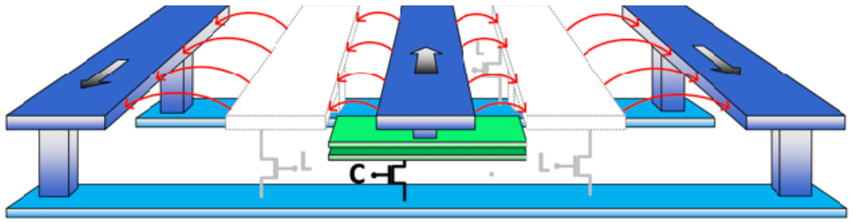
3D structure of a unit cell

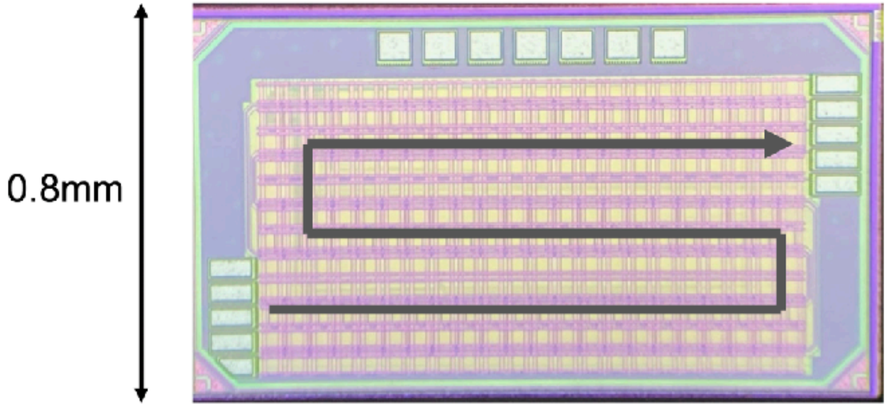
- Coplanar waveguide with ground return lines
- Transmission line delay is tuned by controlling the propagation velocity

Low Delay State



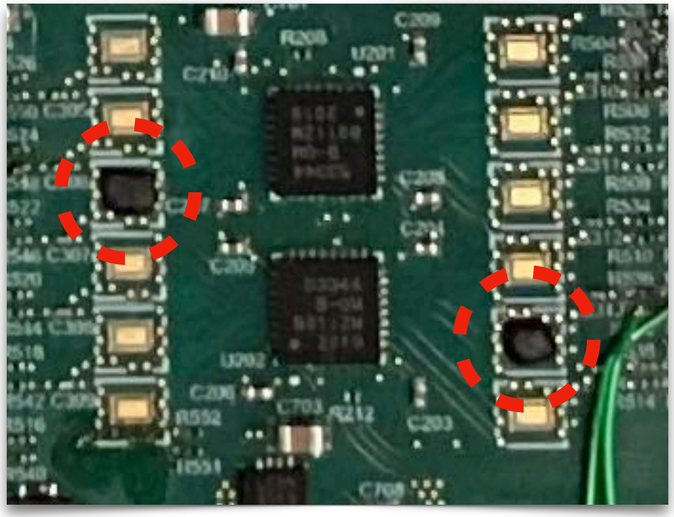
High Delay State





- Chip fabricated with TSMC 65nm CMOS process
- Consists of 66 delay units arranged in 3 rows

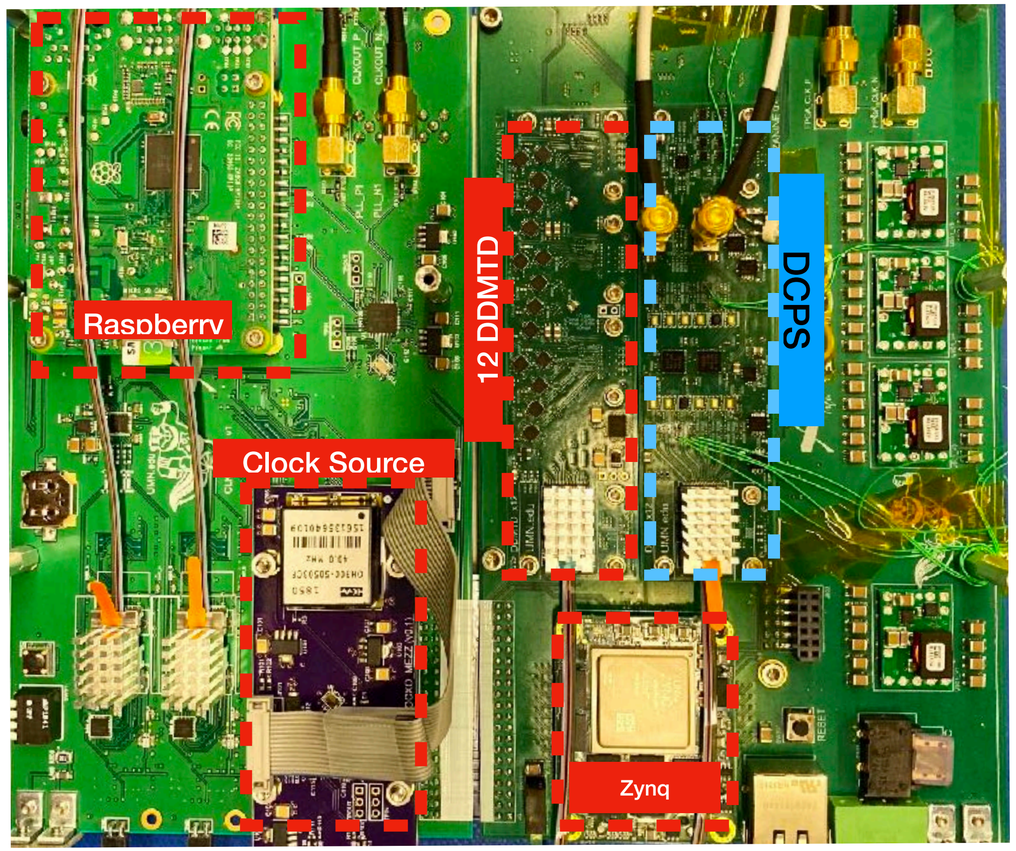
- Chip are wire-bonded to the mezzanine board
- 2 out of 12 channels are populated in this particular board

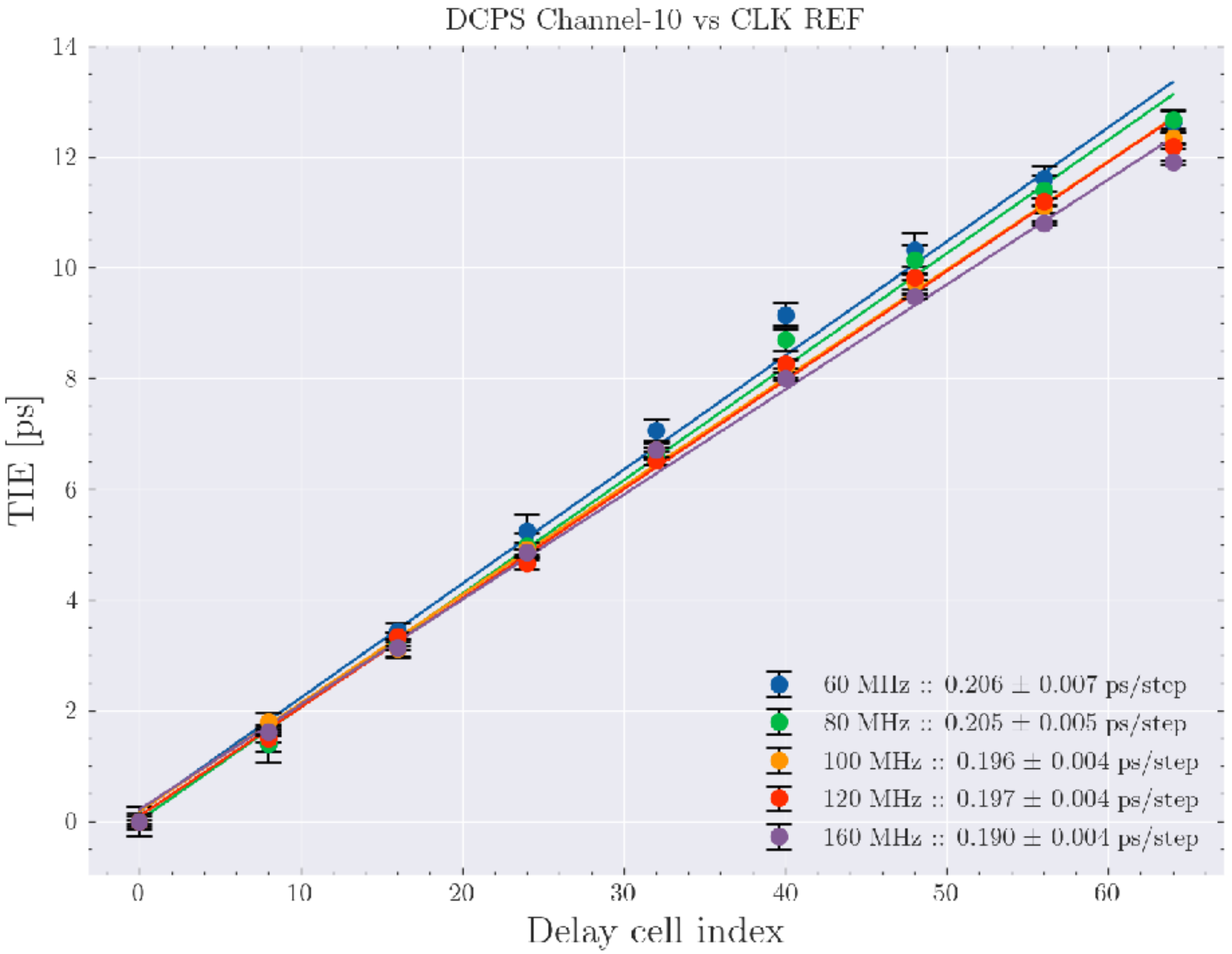


Multi Channel DCPS Test Bench

Delay measurements were made by activating the delay steps of the ASIC cumulatively (in steps of 8 units)

We measured the TIE b/w the distributed clock and the reference clock using DDMTD



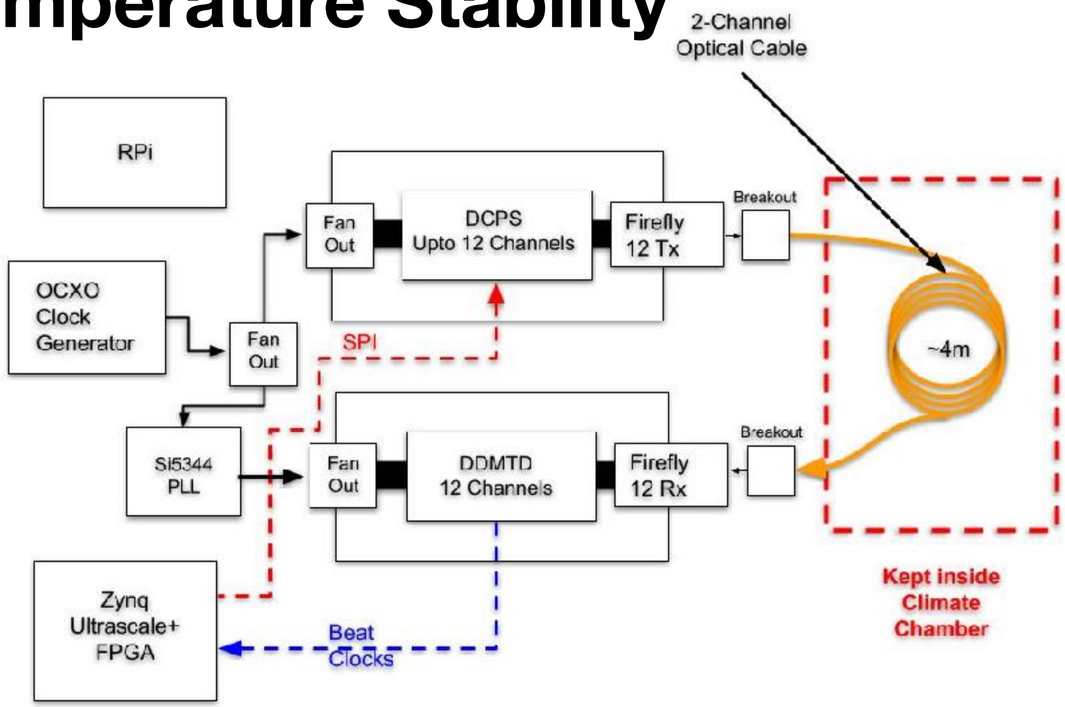


The DDMTD measures a DCPS induced phase shift of

$200fs/step$ with range of $\approx 12ps$

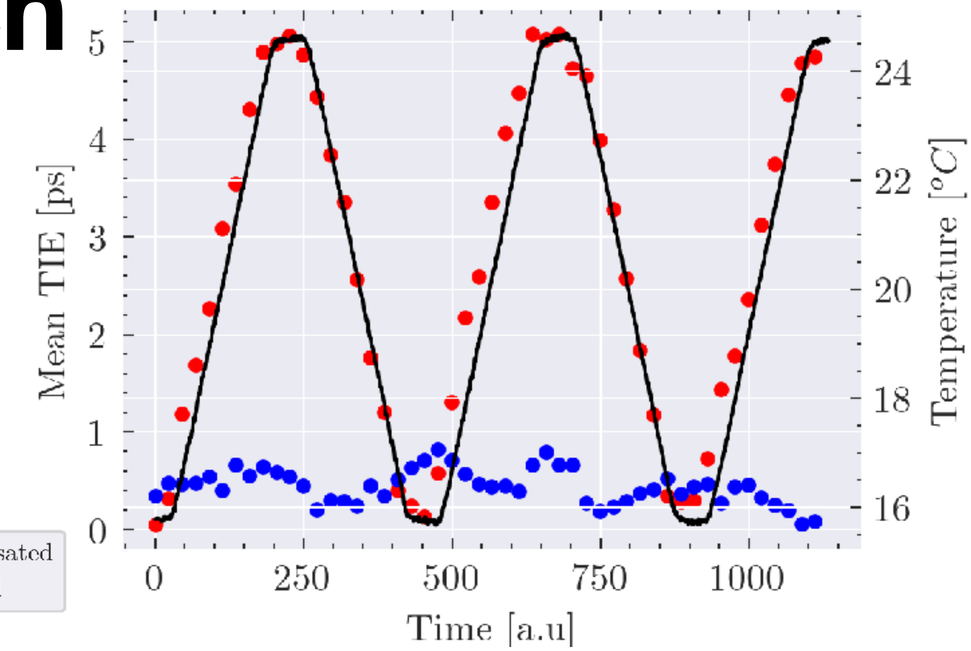
Multi Channel DCPS Test Bench

Temperature Stability

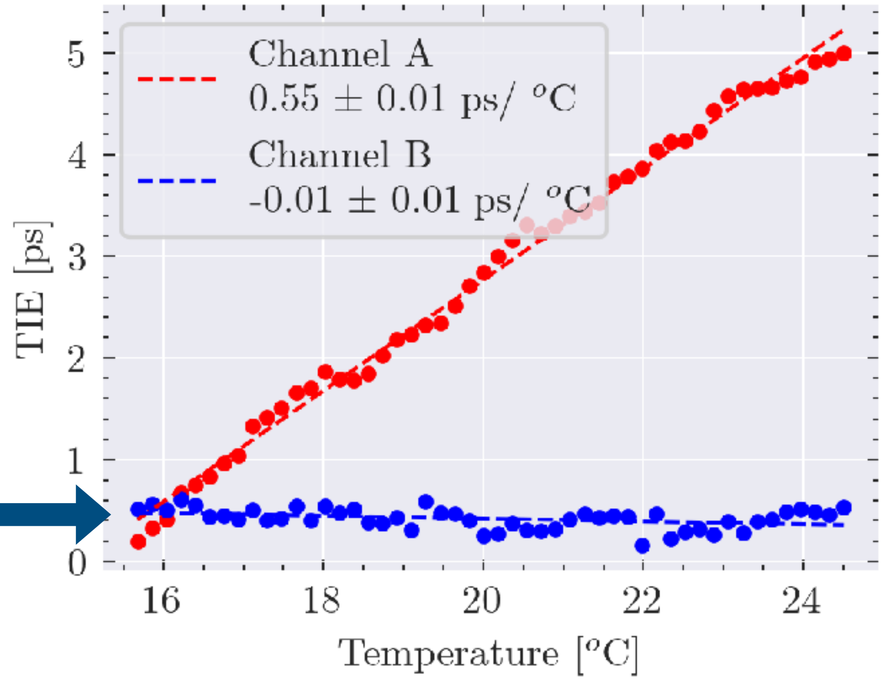


- Routed 2 Channels through Climate Chamber
  - Channel A
    - **Not Stabilized by DCPS**
  - Channel B
    - **Stabilized by DCPS**
- ~ 4m of cable kept inside the climate chamber
- Temperature was varied between 16°C → 24°C
- Phase variation was measured using DDMTD
- Corrections were applied to channel B
  - Channel A left untouched

CLK → 160MHz (DDMTD N=100k)



Compensated channel stabilizes clock to sub-picosecond precision

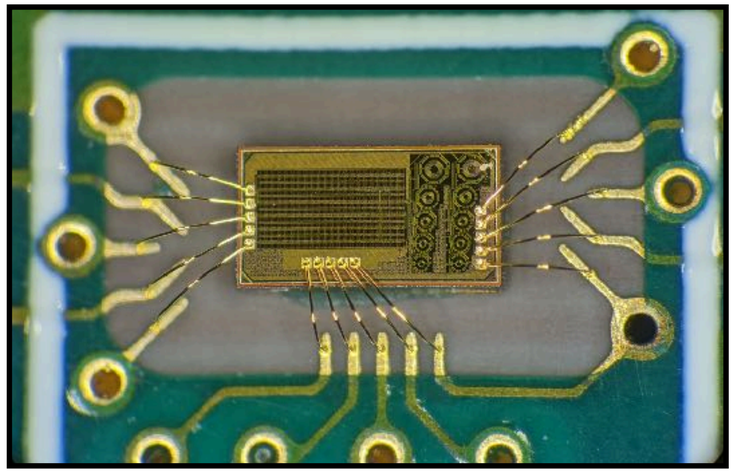


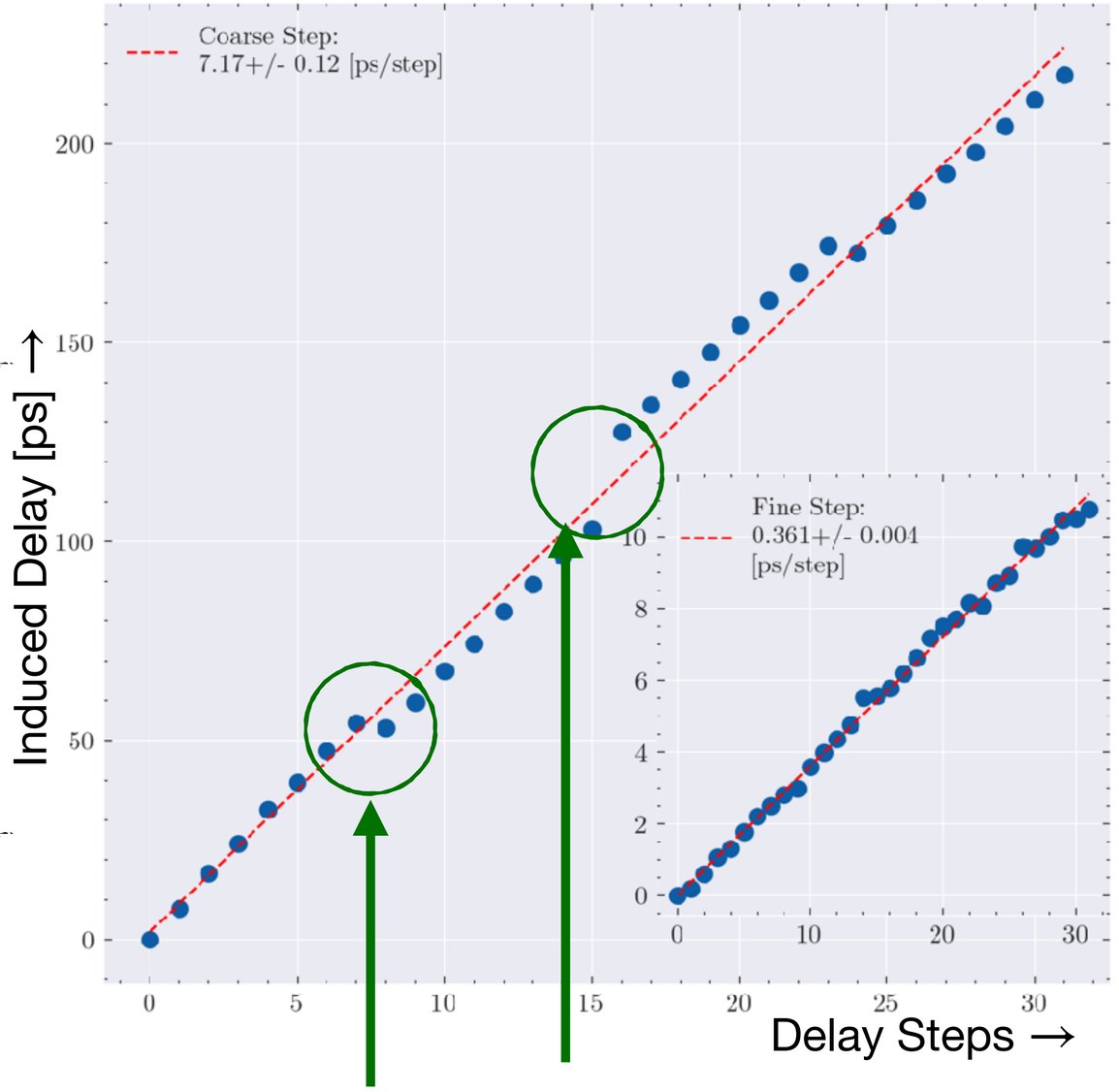
DCPS ASIC Version 2

A second version of the DCPS ASIC was designed with dynamic range in mind

- Dynamic range of ~250ps
  - 5 coarse delay steps → 8ps, 16ps, 32ps, 64ps, 128ps
- With ~400fs granularity
  - 32 fine delay steps

ASIC Under Microscope →





Discontinuity due to 64,128 coarse delay
Rectified in next revision

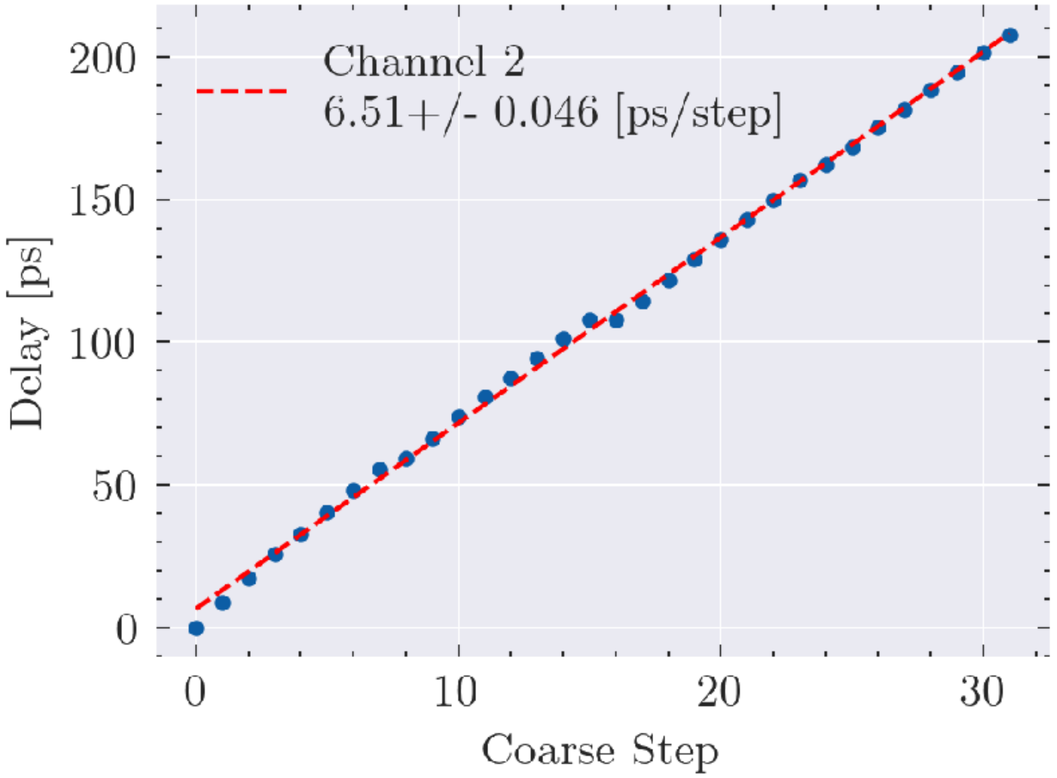
DCPS ASIC Version 3

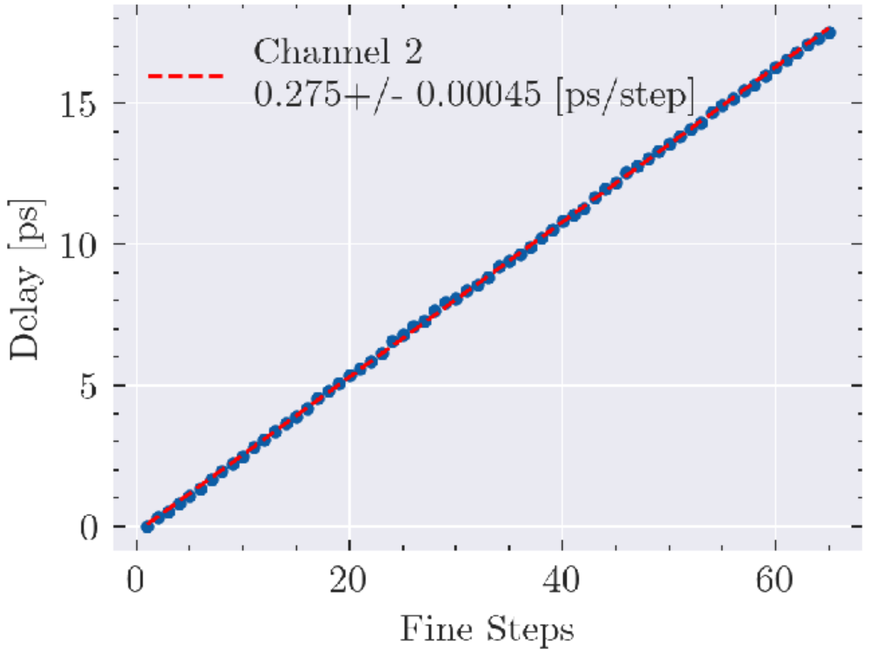
A third version of the DCPS ASIC was designed with radiation tolerance in mind

- Dynamic range of ~250ps
  - 5 coarse delay steps → 8ps, 16ps, 32ps, 64ps, 128ps
  - 2 Tuning Bits
- With ~300fs granularity
  - 66 fine delay steps

DCPS v3 has been designed with radiation tolerant I2C controller

Further tests are being conducted (including radiation hardness)





Summary

Pure Clock Distribution System & DDMTD

- Demonstrated a scalable clock distribution system that is capable of distributing clocks with sub-picosecond precision
- DDMTD circuit is a low cost circuit capable of tracking low frequency wanders of the clock

24 Channel DDMTD Board

- Developed system capable of tracking the long term wander of 24 channels of clock simultaneously.
  - Scalable architecture, developed with offline corrections in mind
- Each channel provides sub-picosecond precision
- Stability of the DDMTD measurements are consistent across channels

Digitally Controlled Phase Shifter ASIC

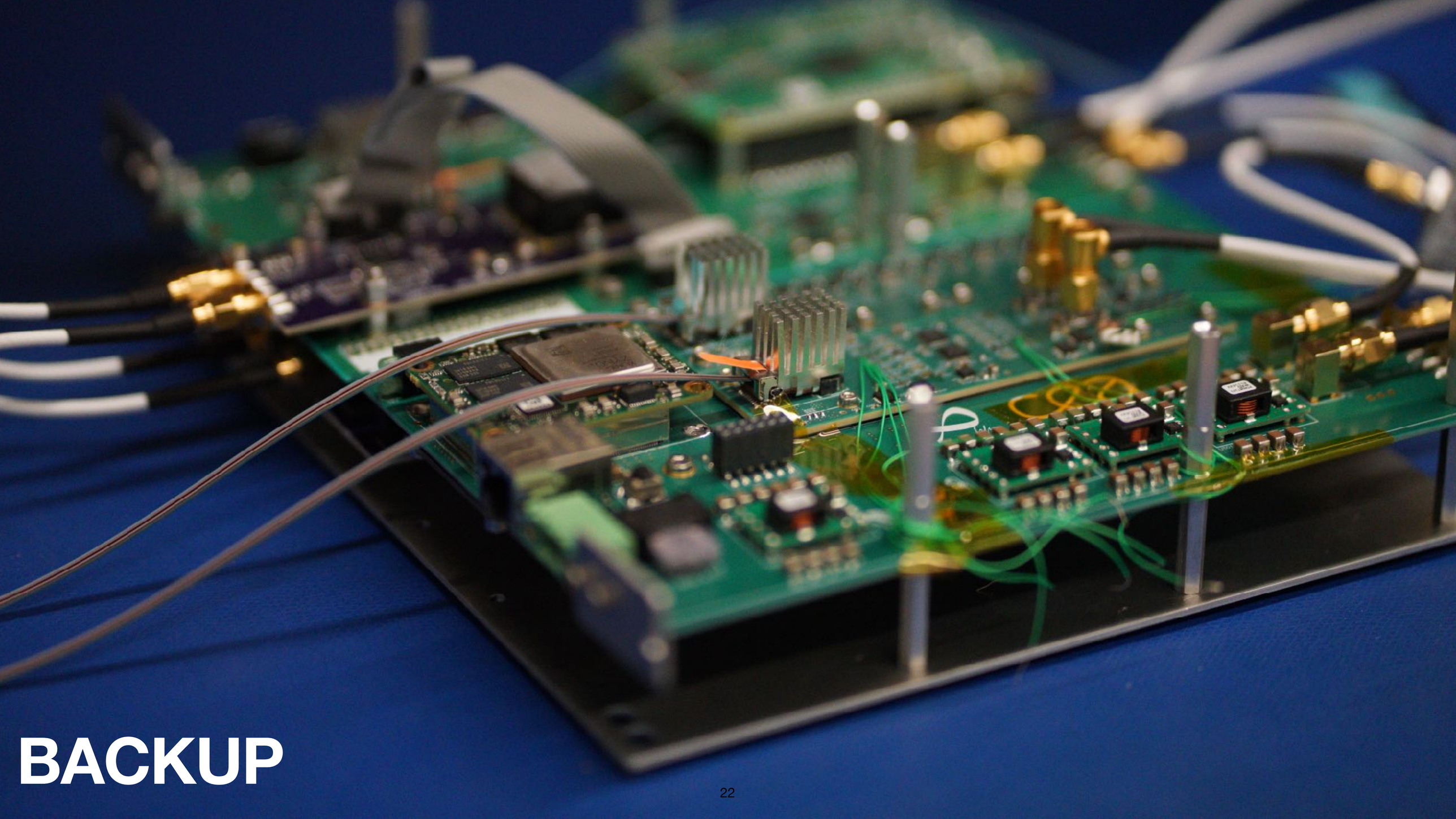
- Demonstrated system capable of tracking long term wander of the clock and correcting for it in real time with **sub-picosecond precision**
- The DCPS distributing the clock doesn’t introduce a significant amount of phase noise
- High Dynamic Range >200ps with ~300fs steps
- Designed to be dispersion free up-to ~500MHz
- Radiation tolerant (DCPS v3)

Acknowledgements

- This project is funded by US-DOE Office of Science (High Energy Physics) under Award Number DE-SC0020185

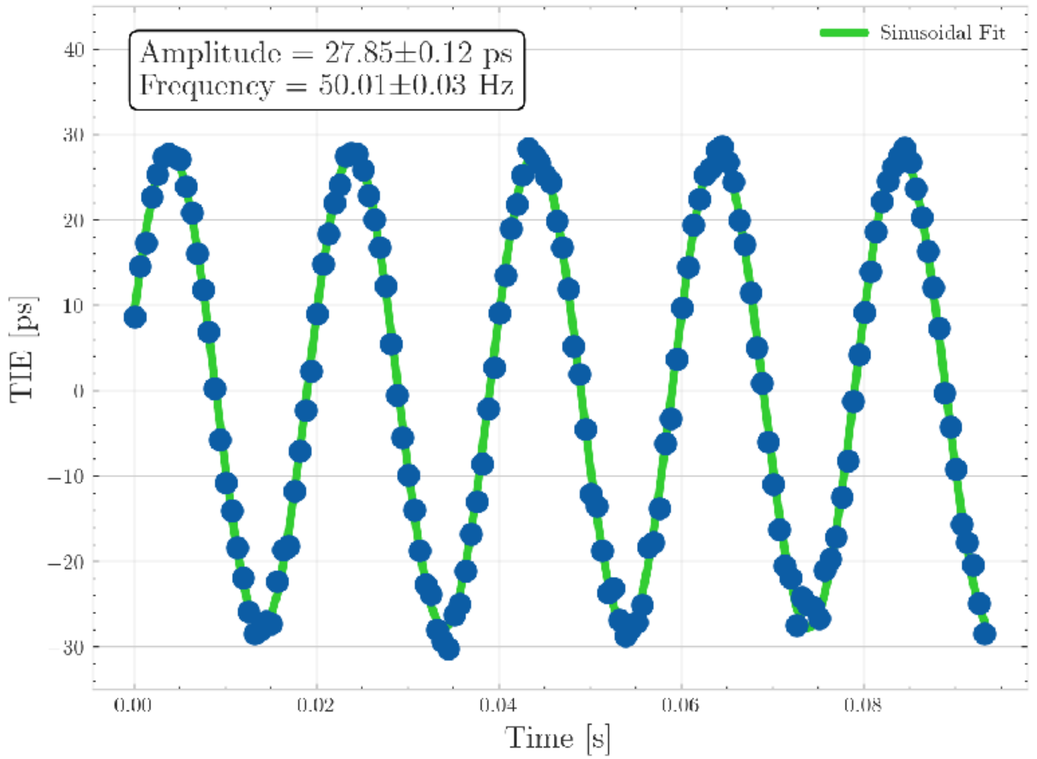
- We thank HPTD lab at CERN for all their support during commissioning and testing of the DDMTD Board

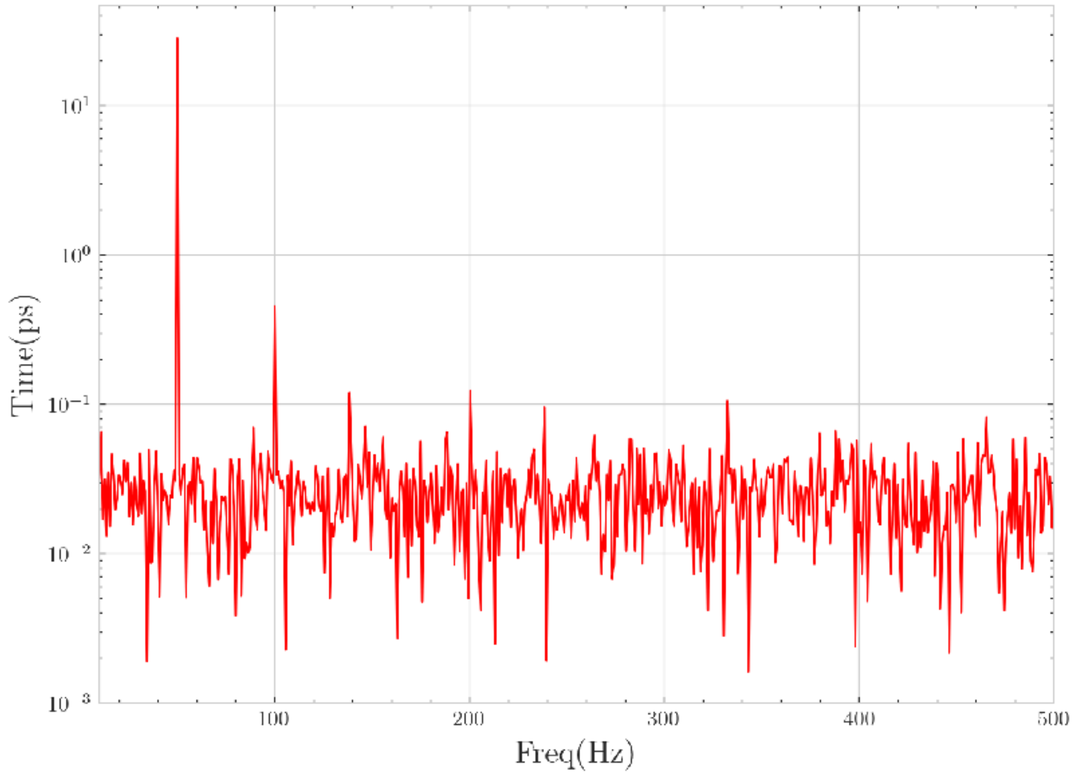
- Special thanks to Fermilab for helping us with the radiation tolerant DCPS v3



BACKUP

DDMTD Performance





DDMTD Linearity