Contribution ID: **58** Type: **not specified**

A real time sub-picosecond clock phase correction system with a dynamic range of 256ps

Monday 29 May 2023 12:05 (25 minutes)

The use of precision timing to measure time-of-flight or to distinguish events from the same bunch crossing in collider detectors has become a common feature of many modern experiments. Currently achieving a precision of 30 picoseconds is seen as an attainable goal. To move to a precision close to one picosecond will require further advances in our time measurement technology. One central component of any time measurement is a precisely aligned reference clock distributed to all of the detector elements. When the required precision of the measurement is of the order of picoseconds, environmental changes need to be tracked and corrected to maintain the precision of the reference clock.

In this talk we will present the design and testing of a system capable of measuring the drift in the clock phase (wander) and correcting for it in real time with sub-picosecond precision. For this we have developed an ASIC, using the TSMC 65nm process, that is capable of adjusting the phase delay of a digital clock signal with sub-picosecond precision and a dynamic range of 256ps. This ASIC together with digital dual mixer time difference (DDMTD) circuit can be used for measuring wander and correcting for it with sub-picosecond precision. Using this system, we will demonstrate the feasibility of distributing reference clocks, detecting and correcting for changes in the phase delay to a precision of ˜300fs. We will also present a version of this ASIC that is designed to be radiation tolerant.

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