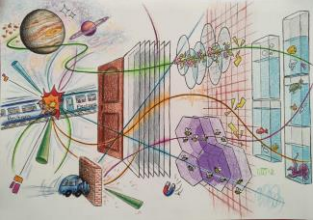
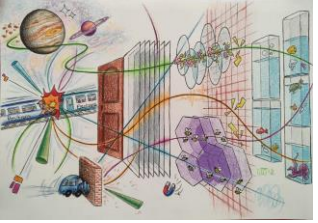




# Interconnect and device fabrication technologies

G. Calderini (LPNHE Paris), D. Dannheim (CERN), F. Huegging (Bonn)



# Todays' session

DRD3

## Three short talks

- Introduction and analysis of interests
- In-house interconnection technologies
- Interconnection technologies via specialized vendors
- Discussion

## Keycode:

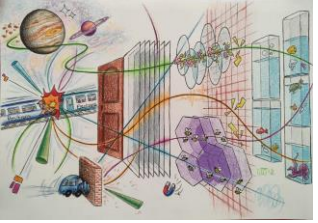
Milestones / Deliverables

S = short term (3 years)

M = medium term (6 years)

L = long term (>> 6 years)

| | | |
|---|---|---|
| 11:00 | **Introduction and analysis**<br>*222/R-001, CERN* | *Giovanni Calderini*<br>11:30 - 11:40 |
| | **In-house interconnection technologies**<br>*222/R-001, CERN* | *Dominik Dannheim*<br>11:40 - 11:50 |
| | **Interconnection technologies via specialised vendors**<br>*222/R-001, CERN* | *Fabian Huegging et al.*<br>11:50 - 12:00 |
| 12:00 | **Discussion**<br>*222/R-001, CERN* | *All*<br>12:00 - 12:30 |



# Interconnection task

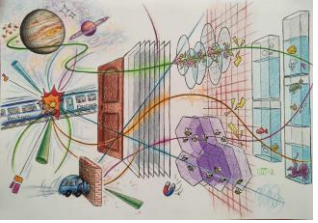
DRD3

## Interconnections are a strong point of future detector and electronics development

They have a critical role in the development of detectors and electronics

Sensor-FE, Tier to tier, multiple stacks

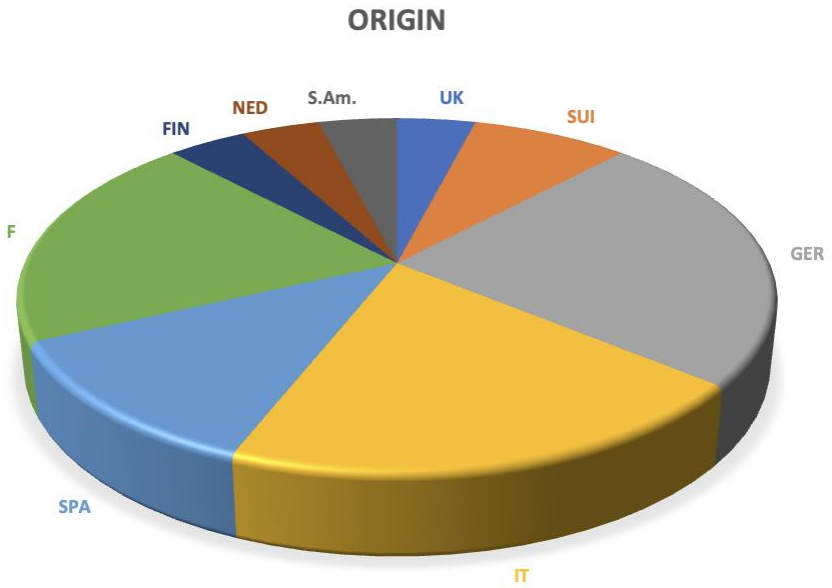
Interconnections for modules, interconnection for characterization

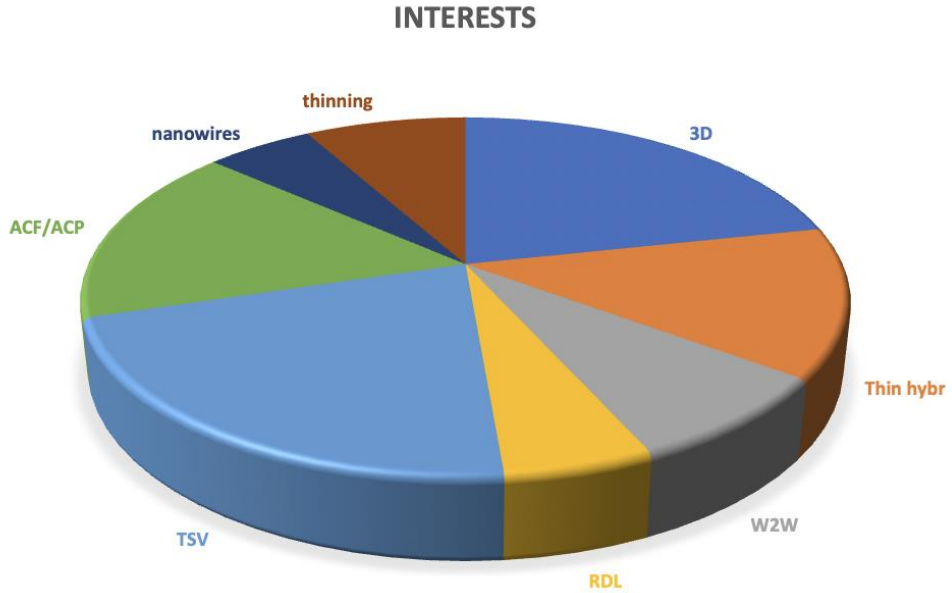


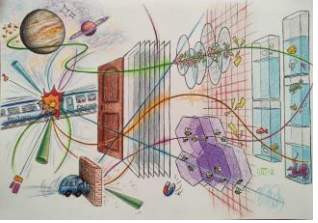
# Interest in the community

DRD3

- In questionnaire: 35 groups / 85 questionnaires already interested and planning to have resources
- Among them 25 gave some specific information
- 15-20 FTE already declared





# Strong interplay with DRD7

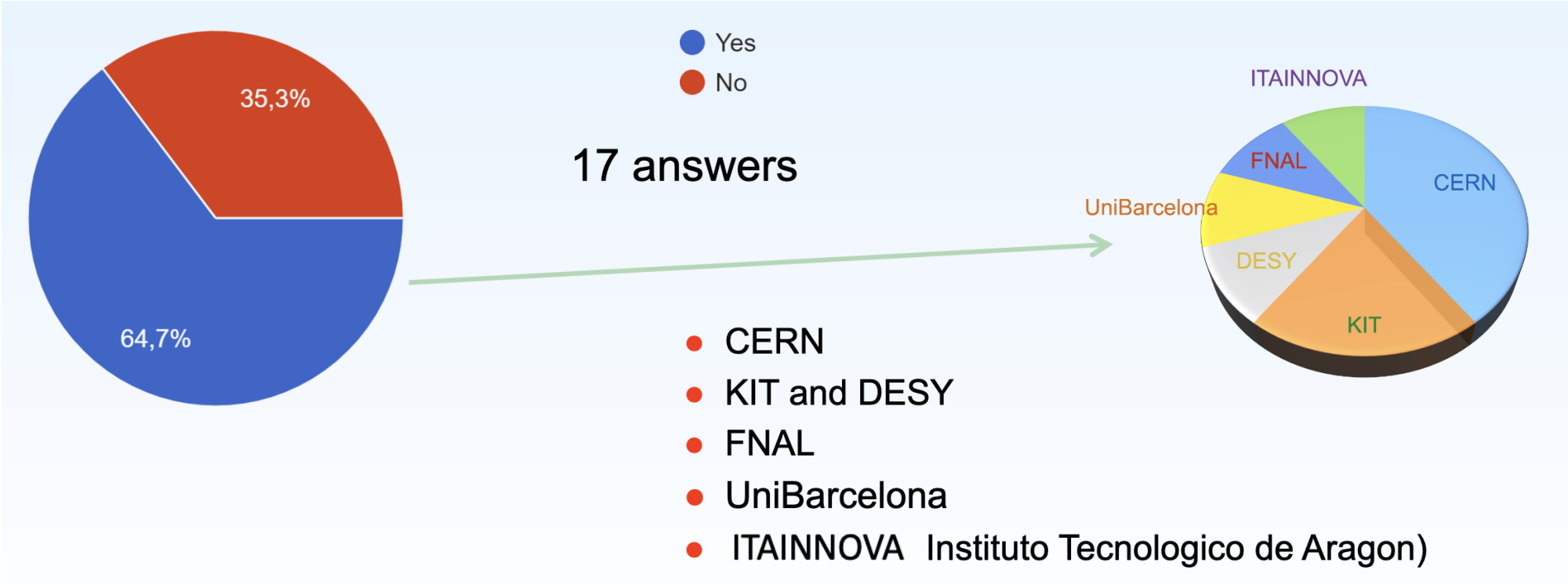


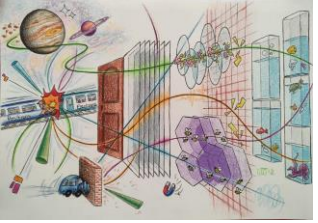
TSV, RDL -> 6 institutes

3D, direct wafer bonding -> 3 institutes

ACF/ACP -> 2 institutes

Statistics from interconnection interests inside the “Emerging technologies, DRD7.5”

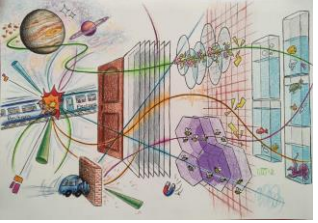




# Interconnection technologies



Different stages and technology levels



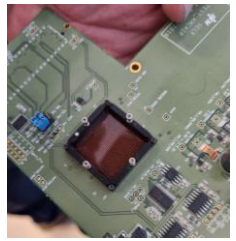
# I – Maskless connections

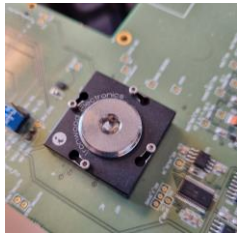
DRD3

## Testing and fast connections: not only to have a cheap way to test objects but also for fast prototyping

Application possible even for temporary connection

(Temporary connections already widely used in testing / characterization)





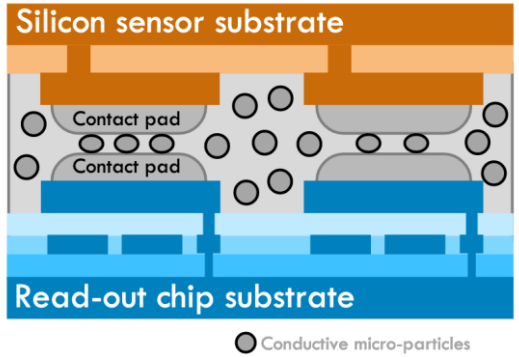
ATLAS AM chips test setup

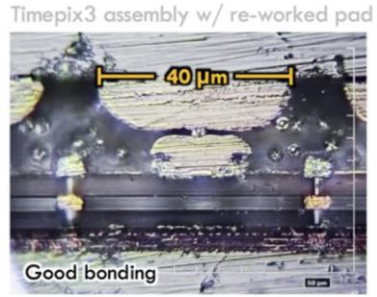
## Permanent maskless connections (for example ACF/ACP)

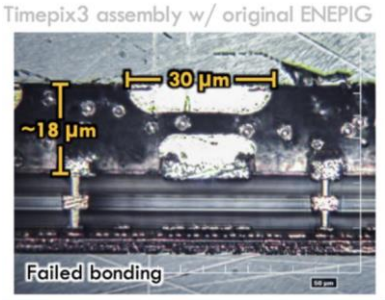
Maskless, in house technology

Allows for cheap interconnection
Quick turnaround time

Wafer and device level connection



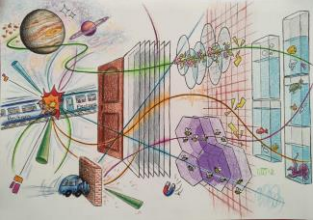




Milestones:

M3.7.1.1: consolidate yield (>>99%) (S)

M3.7.1.2: proof of small pitch (below 30um) (S)

D3.7.1.1: reliability of connections / rad hardness demonstration (M)



# II - More advanced bumping / bonding interconnections

DRD3

## Different technological level

This needs today RTO or industry

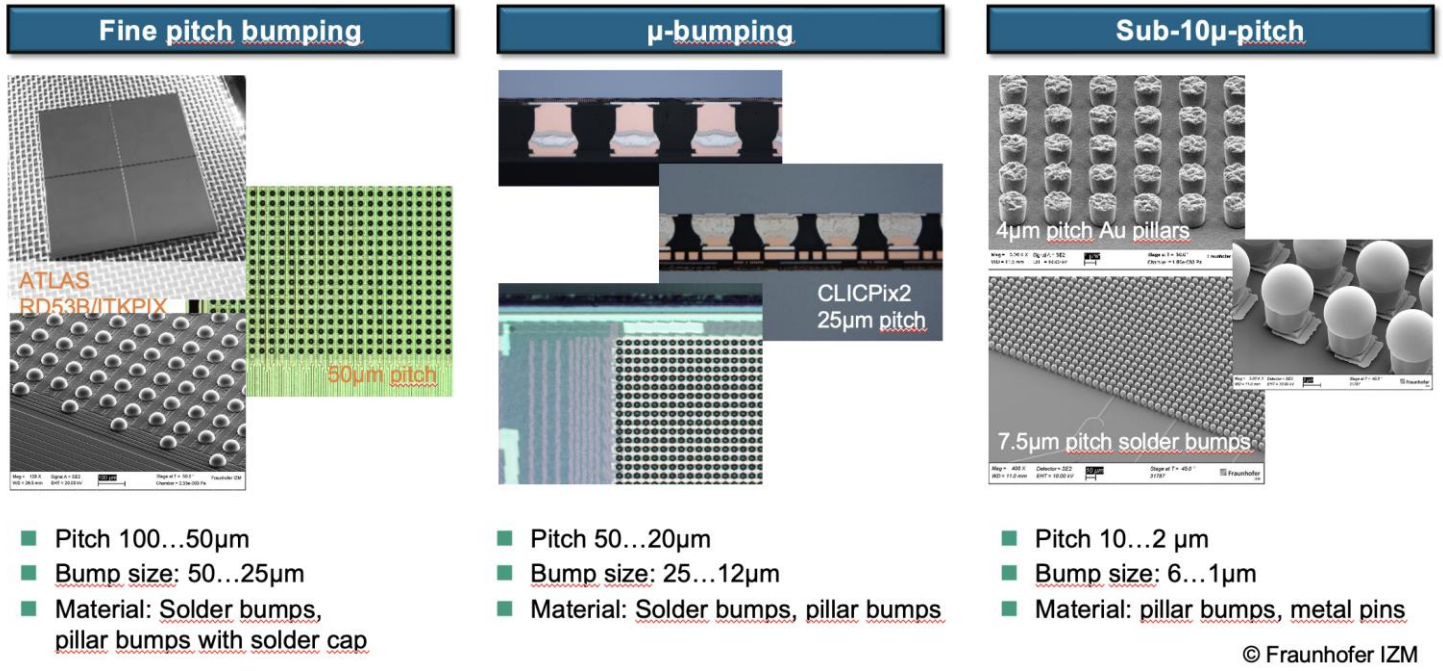
## Vendors busy with upgrade productions

Move part of process to laboratories

## Different features from different technologies can address specific complex issues

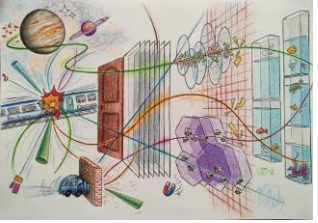
- small pitch
- process-temperature constraint
- electrical properties (current, C)
- connection flow
  (wafer-wafer, device-wafer)

Examples of interconnection technologies provided by IZM




Milestones:

M3.7.2.1: develop maskless post-processing (S)
M3.7.2.2: make basic processes accessible to selected laboratories (M)
M3.7.2.3: develop device-wafer approach (necessary for prototypes) (M)



# III - 3D and vertical integration

DRD3

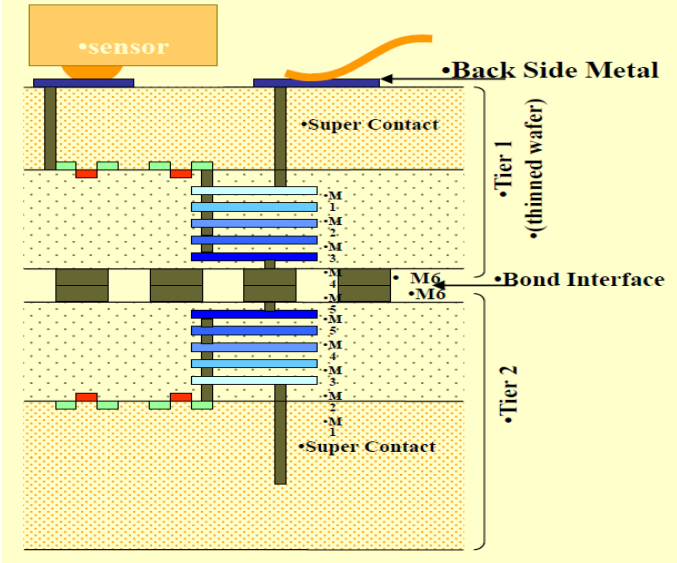
Via industry
it will profit of commercial drive

Stack to match digital/analog
many reasons to do so

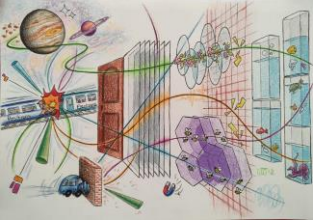
Could allow complex communication between different connected devices

Allow to contact/power/read a lower layer through an upper one

Multi-tier, mixed-technology




Milestones:
M3.7.3.1: demonstrate the w2w process for FE-sensor connection (S)
M3.7.3.2: use TSV to access lower tiers through sensors (S)
M3.7.3.3: connection made possible for post-processed devices (M-L)



# Wrap-up



## See next talks for more details on the different technologies

### Interconnections are essential point of all hybrid sensor-FE technologies

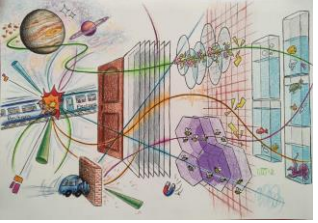
Different levels:

- Cheap temporary (for test) or permanent connections
- Fast connections for prototyping: short turn-around
- More advanced - partially in-house - process to address specific constraints (small pitch, temperature)
- Complex interconnection process via RTOs/industries

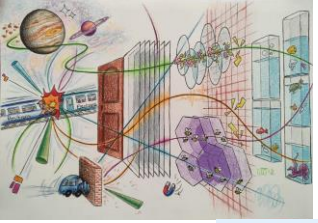
### For monolithic technologies, interconnections are necessary for multi-tier extensions

Strong link with electronics (DRD7)

It is critical now to get organized: community feedback is needed



# DRD3



# Strong interplay with DRD7



## 3D integration & high density interc. (5)

ECFA European Committee for Future Accelerators | DRDT 7.5 Emerging Technologies

Please describe the topics you (and/or your group) would like to participate in?

- Integration of single photon sensor and readout chip (*UniBarcelona*)
- Characterisation of 3D stacks, with focus on irradiation studies (*CERN*)
- Power consumption, heat, combine analogue, digital and photonic functions (*CERN*,

Test and characterization

Developments of TSV, TGV, RDL and 3D ICs

- Edgeless IC design (*FNAL, KIT*)
- High-density integration sensor, electronic & photonic ICs (*KIT, DESY*)
- 3D integration of silicon photonics and Electronic IC using TGV and TSV (*CERN, KIT*)
- Development of detector modules concepts for 3D stacked MAPS with redistribution layers (*CERN*)
- Design and prototyping of chip/sensor/interconnect assemblies focusing on low mass, powering, heat dissipation, signal integrity, and electromagnetic compatibility (EMC) (*ITTAINOVA*)
- 3D Tools for LVS and DRC; partitioning of functions across layer stack (*FNAL*)

ECFA DRDT 7.5 Kick-off 13