In-house interconnect technologies

G. Calderini[1)], F. Dachs[2)], D. Dannheim[2)], R. De Oliveira[2)], P. Riedler[2)], J. Schmidt[2,3)], P. Svihra[2)], M. Van Rijnbach[2,4)], M. Vicente[5)], A. Volker[2,3)], J. Weick[2,6)]

1) LPNHE Paris
2) CERN
3) KIT Karlsruhe
4) Oslo Univ.
5) Geneva Univ.
6) TU Darmstadt

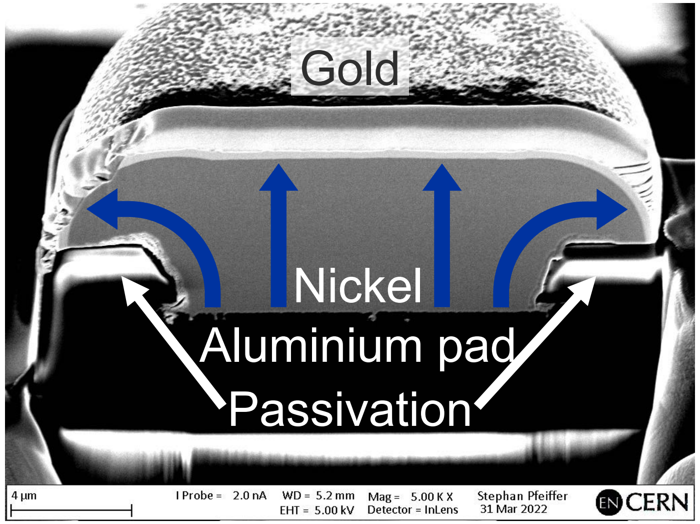
Motivation

- **Advanced plating and interconnection technologies are required for hybridisation and module integration of hybrid and monolithic pixel detectors**
- **Industrial processes are often costly, limited to wafer-level processing**
- **Alternative in-house processes offer several advantages:**
  - Mask-less single-die processing → important during R&D phase with MPW productions
  - Low cost, fast turnaround times
  - Tuning to specific applications for improved performance (pitch / density, sensor materials, mechanical properties, material budget)

→ **R&D on in-house plating and interconnect technologies is performed in the CERN EP R&D programme and the AIDAinnova collaboration, with links to several detector R&D projects**

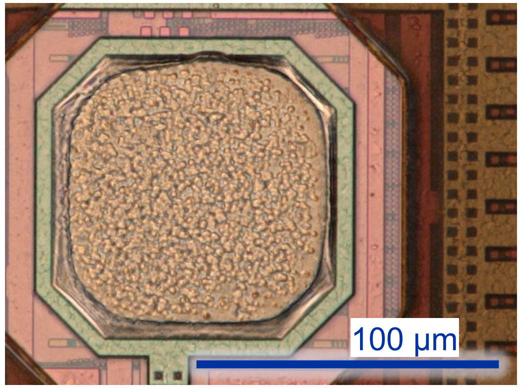
In-house plating

Cross-section of plated Timepix3 pad

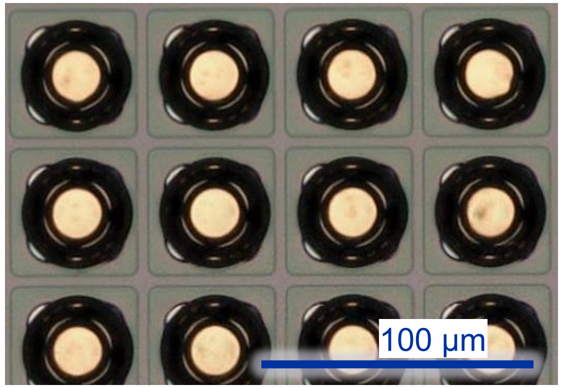


- **Maskless in-house single-die post-processing Electroless Nickel Immersion Gold (ENIG) process**
  - Developed in CERN micropattern lab
  - Process can be tuned for different applications
- **Pad metallisation basis for most interconnect technologies**

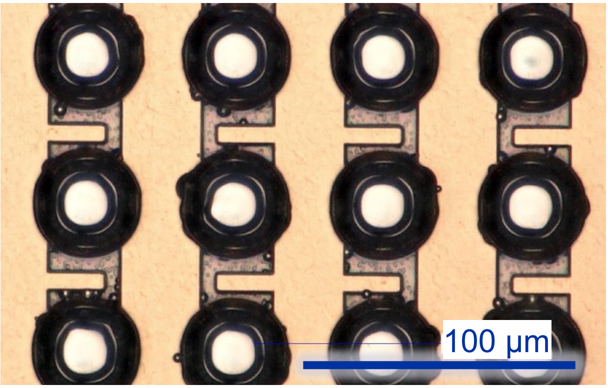
ALTIROC2 (ATLAS)



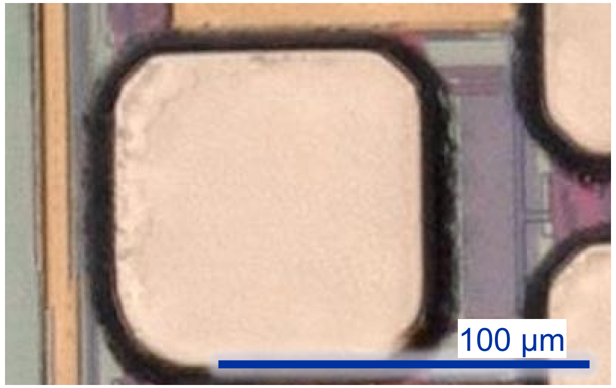
SPHIRD sensor (ESRF)



Timepix3 ASIC



MALTA (ATLAS)



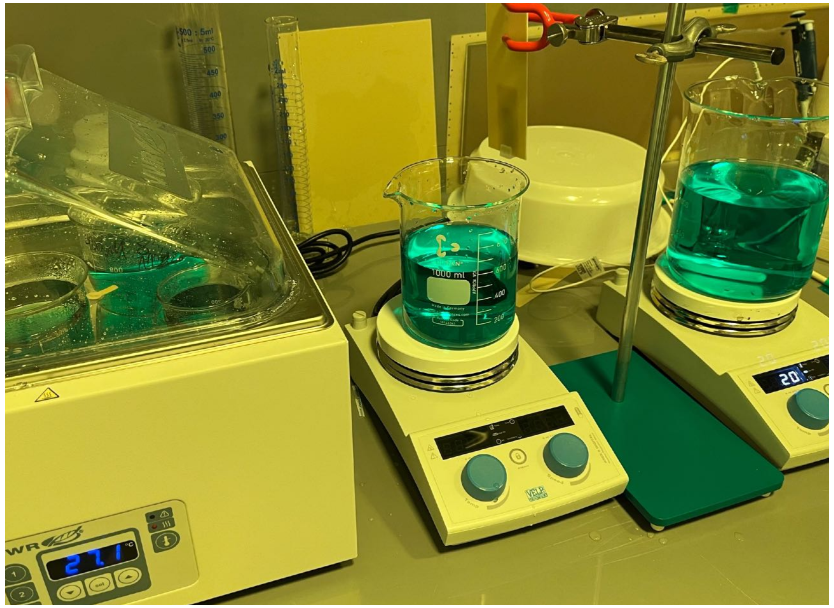
Solder-bump bonding | Hybridisation and integration with anisotropic conductive films and pastes (ACF, ACP)

Ongoing developments and future plans for plating

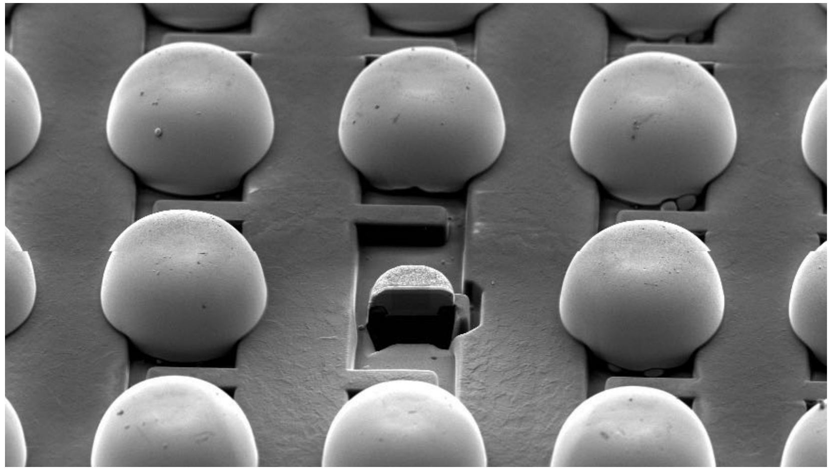
- **Improving plating topology (height, uniformity)**
- **Adapting for lower pitch down to 25 µm**
- **Masking with Photoresist (e.g. for active edge sensors)**
- **Scalability of the process (wafer sized sensors)**
- **Tests with new devices**

Plating process can be adapted to specific needs and transferred to labs in participating institutes
→ opportunities for collaboration within DRD3

ENIG plating setup at CERN



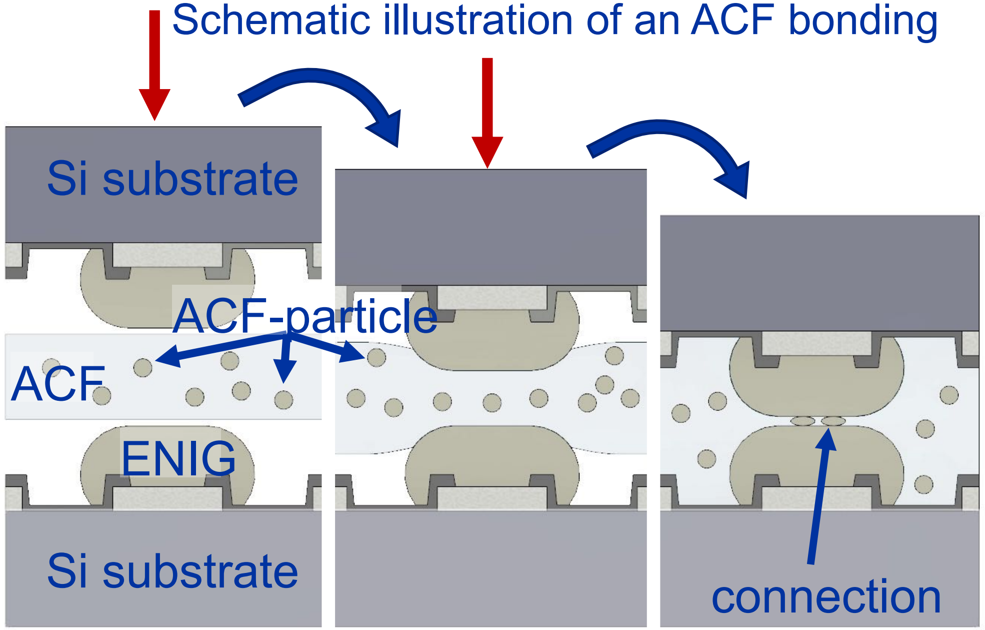
Skipped plating on Timepix3



Interconnection with Adhesives

- **Anisotropic Conductive or non-conductive Film / Paste (ACF / ACP / NCF / NCP)**
  - Epoxy film / paste with or without conductive particles

Schematic illustration of an ACF bonding



- **Thermocompression bonding process**
  - Flip-chip bonding machine for precise alignment + parameter control
  - Anisotropic/vertical electrical connection is achieved via compressed conductive particles or direct pad-to-pad connection
  - Permanent mechanical bonding via cured epoxy film / paste
- **Specific pad topology is achieved with ENIG plating**

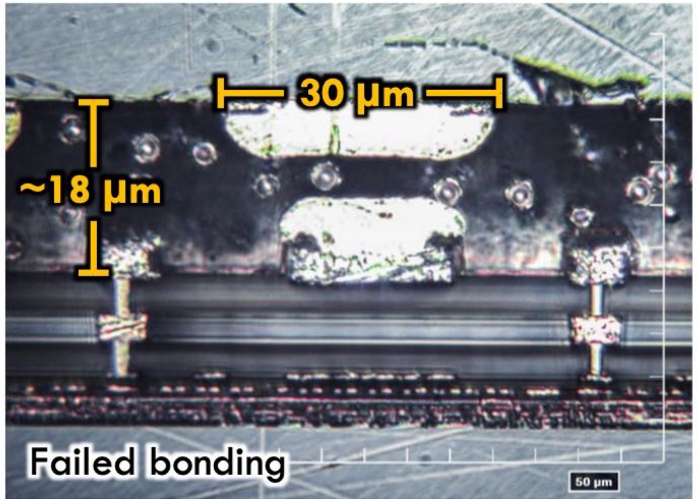
Flip-chip bonder

SET ACCµRA100

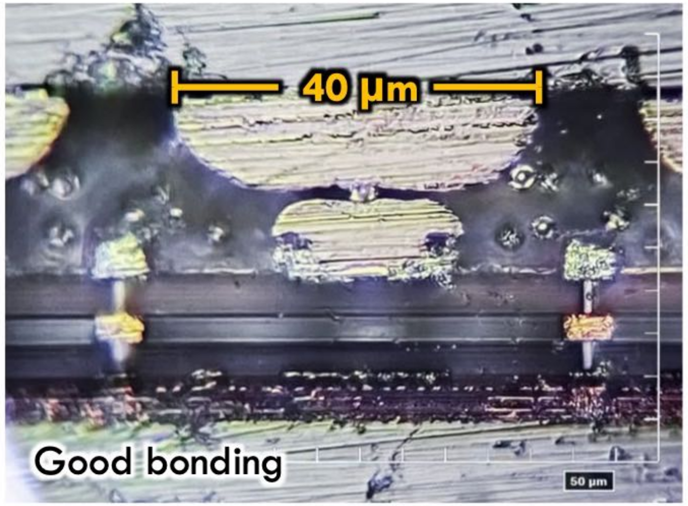
Hybridisation results with ACF/ACP

- **Proof-of-concept Timepix3 ACF/ACP assemblies**
  - Quality of ENIG plating is crucial
  - Bonding-parameter optimisation is crucial
  - Good interconnect yield for ACF demonstrated in test beam

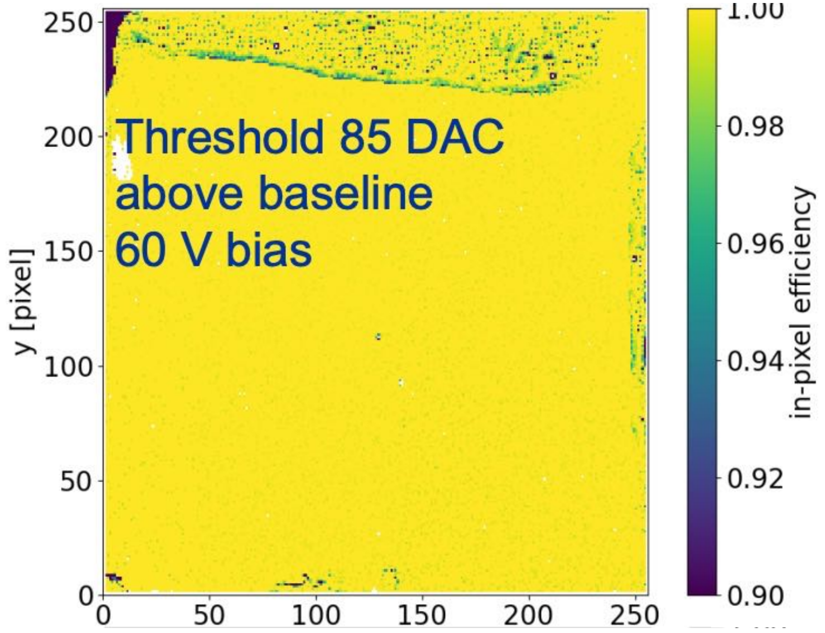
Timepix3 assembly w/ original ENEPIG



Timepix3 assembly w/ re-worked pad



Test-beam efficiency Timepix3 ACF assembly



Ongoing developments and future plans for hybridisation

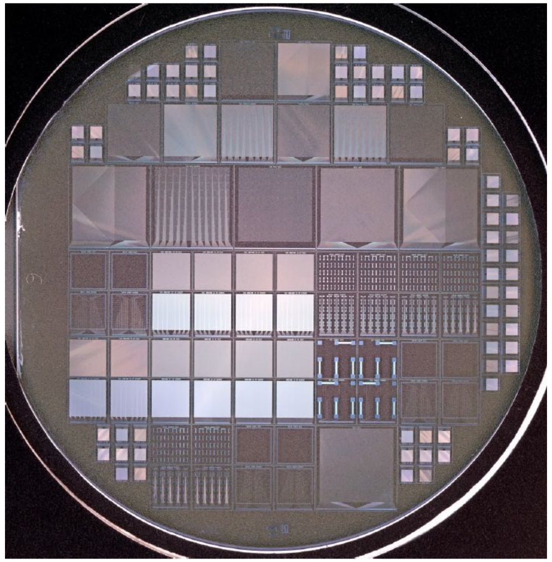
Optimisation of bonding parameters

- Use of custom-developed daisy-chains
- Test of different adhesives and micro particles

Reliability tests

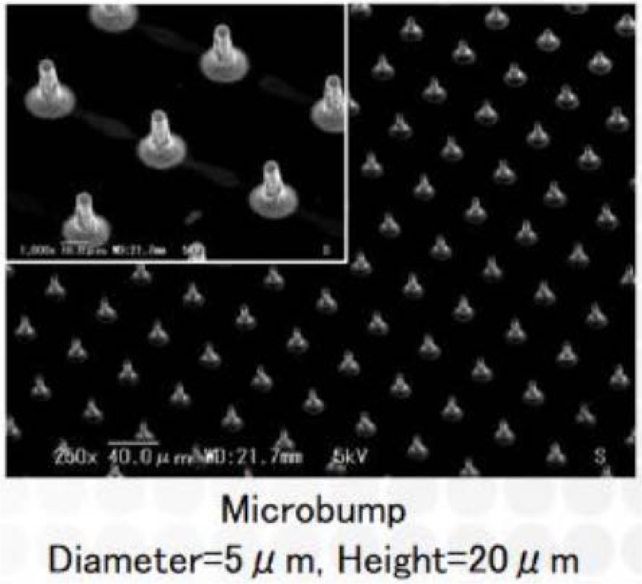
- Radiation hardness, electrical properties, mechanical strength, …
- Further evaluation in test-beam and lab

Daisy-chain structures, FBK



FONDAZIONE BRUNO KESSLER LPNHE PARIS AIDA innova

Micro-structured ink-jet printing



Ongoing / planned trials for multiple projects

- Timepix3, CLICpix2, SPHIRD, XIDER, PicoPix, TimeSpot, HGTD…

Exploration of alternative interconnect technologies

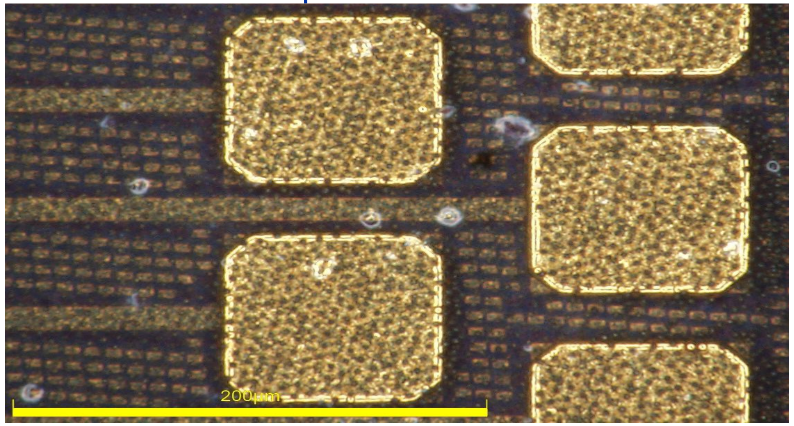
- Micro-structured ink-jet printing, AC-coupled devices, …

Opportunities for collaboration in DRD3: new use cases, production + testing of samples, process optimisation, …

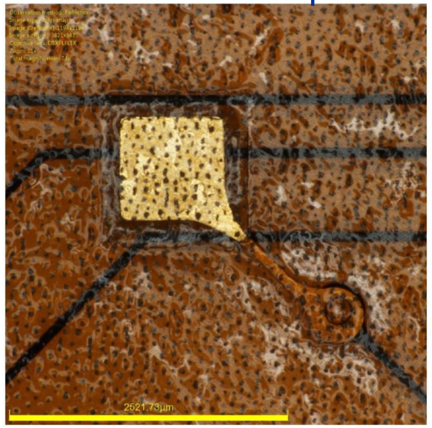
Module interconnection technologies

Conductive and non-conductive adhesives are also under study for large-pitch / low-density interconnects in modules:

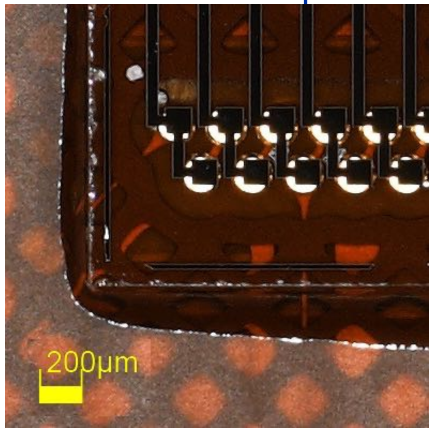
ACF on MALTA pads



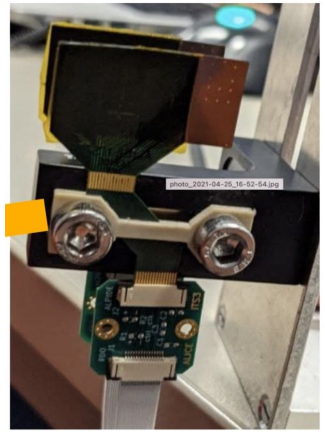
ACF on LUXE pad



NCP for 100µPET



ALPIDE ACF module in DESY TB



- **Cost effective**
- **In house** processing
- **No mask** needed

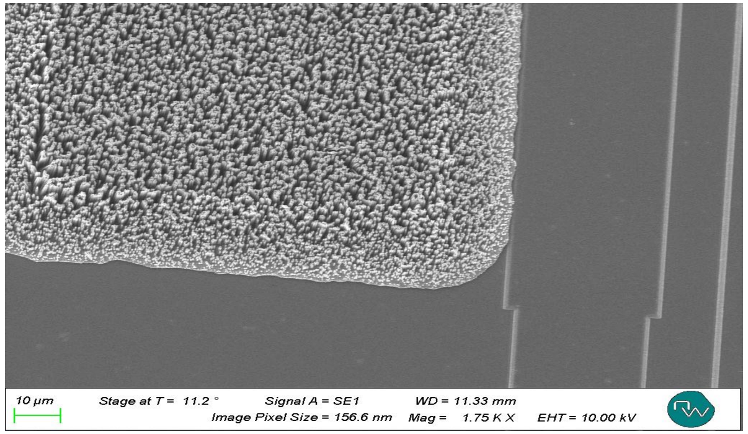
- **Scalable** on chip-chip or flex-chip
- **Glue support** for mechanical stability
- **Fast** interconnection
- Suitable for **large number of pads**

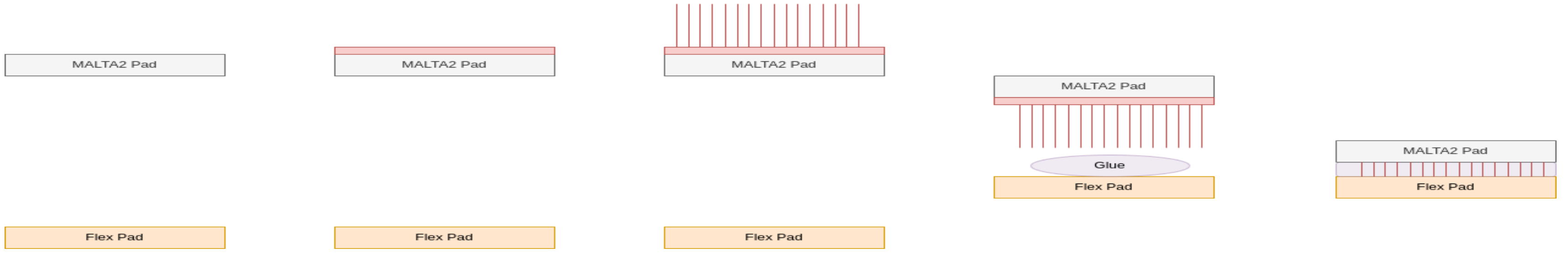
Proof-of-concept tests with **ALPIDE, MALTA, LUXE, 100µPET**

Ongoing developments and future plans for module integration

Nano wires for chip-to-flex interconnection

Nano wires on MALTA pad





Photolithography opening of pad

Apply seed layer

Apply nano - structure on chip pad

Glue addition possible in flip chip process

Connection through pressure and heat

- **Low** contact **resistance**
- **Low parasitic**
- **Chip** and **wafer** level
- Ongoing tests: MALTA on flex PCB

- **Scalable** on chip-chip or flex-chip
- **Glue support** for mechanical stability
- **Fast** interconnection
- Suitable for **large number of pads**
- Not (yet) fully **in-house**

Future plans:

- Integrate optical links
- Flex-to-flex interconnection

Open to new collaborators / use-cases within DRD3

Collaborations

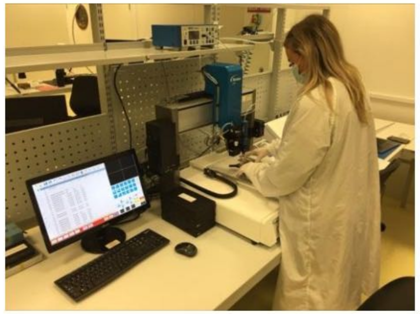
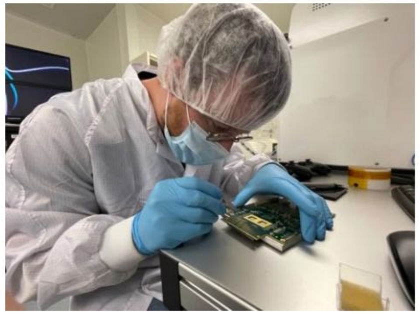
- Several groups and projects contribute to the developments
- Support from **EP R&D** and **AIDAinnova**
- Still in exploratory phase
  → **new groups and ideas welcome**

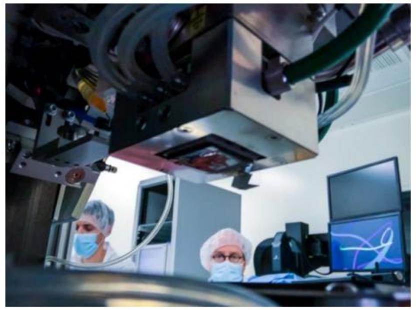
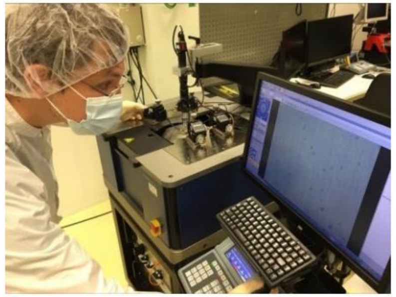
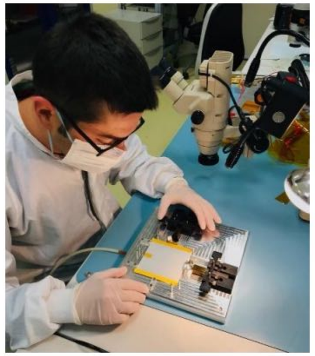
- Benefits of being part of **DRD3**:
  - **Visibility** / **approval status**
  - Enables additional **funding**
  - **Links** to other DRD activities (e.g. access to shared sensor productions, links to hybrid and monolithic detector developments)

Current contributors to in-house interconnect studies:

Participant	Current scope of activities / collaboration
CERN	Plating, hybridisation, module building, testing (EP R&D)
Geneva Univ.	Flip-chip component placer, hybridisation, module building, testing (EP R&D)
LPNHE, Paris	Testing of hybrid assemblies (AIDAinnova)
ESRF, Grenoble	Hybridisation of small-area devices
FBK, Trento	Design and production of chain devices (AIDAinnova)
Conpart, Norway	Procurement of conductive particles and films for ACF/ACP (AIDAinnova)
IFAE, Barcelona	Optimisation of ENIG plating for large-pitch sparse interconnects (AIDAinnova)
USTC, Hefei	Optimisation of ENIG plating for large-pitch sparse interconnects
IZM, Berlin	Highly-integrated structure studies (i.e. RDL and encapsulation)
KIT, Karlsruhe	Micro-structured ink-jet printing for hybridisation

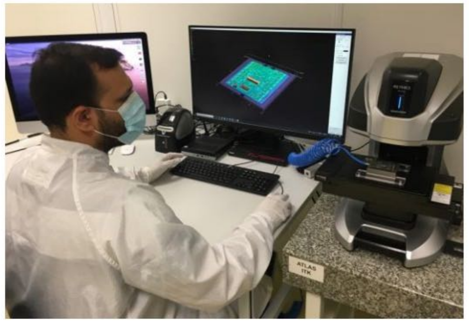
Backup







Anisotropic Conductive Adhesive (ACA) Bonding

ACA connection done at Geneva University using semi-automatic flip-chip bonder

- Precise temperature, pressure and alignment control
- Heating up to 400 ℃ and force applied by bonding arm up to 100 kgf
- Available for bonding with **a**nisotropic **c**onductive and **n**on-conductive **f**ilm/**p**aste – **ACF/ACP** or **NCF/NCP**

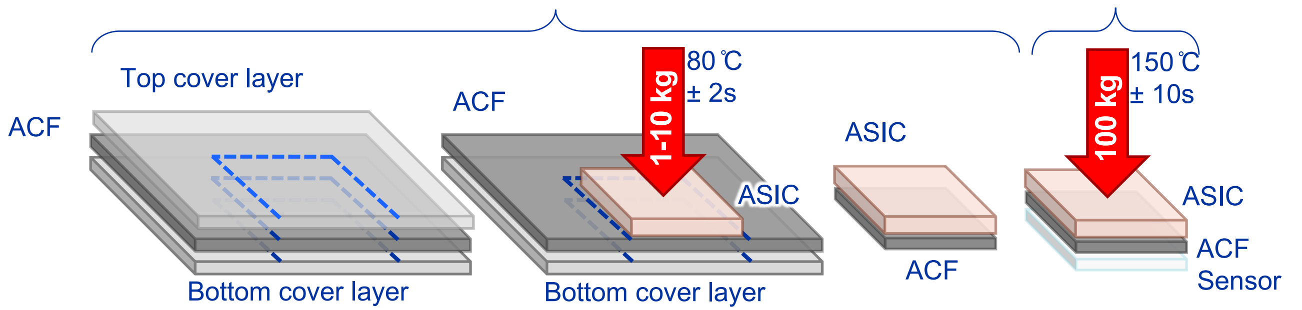
UNIVERSITÉ DE GENÈVE
FACULTÉ DES SCIENCES

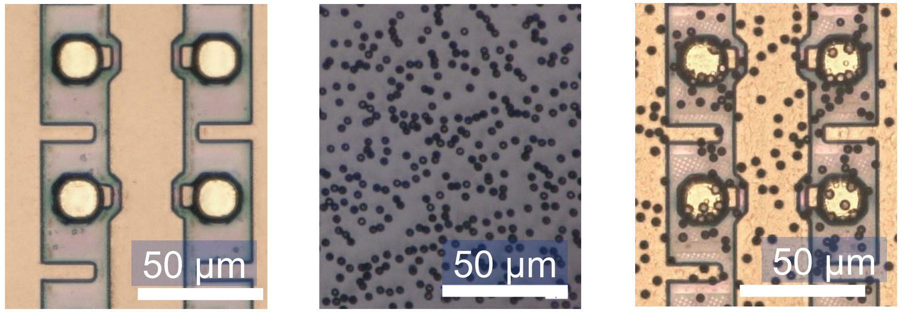
Flip-chip bonder

SET ACCμRA100

ACF bonding has two steps – lamination and bonding

- Pressure applied to displace and compress particles
- Epoxy cures at 150 ºC for a few seconds only



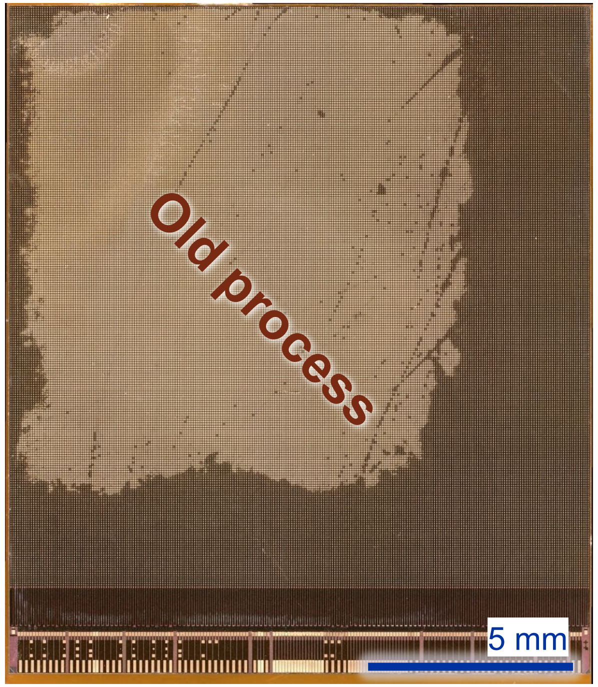


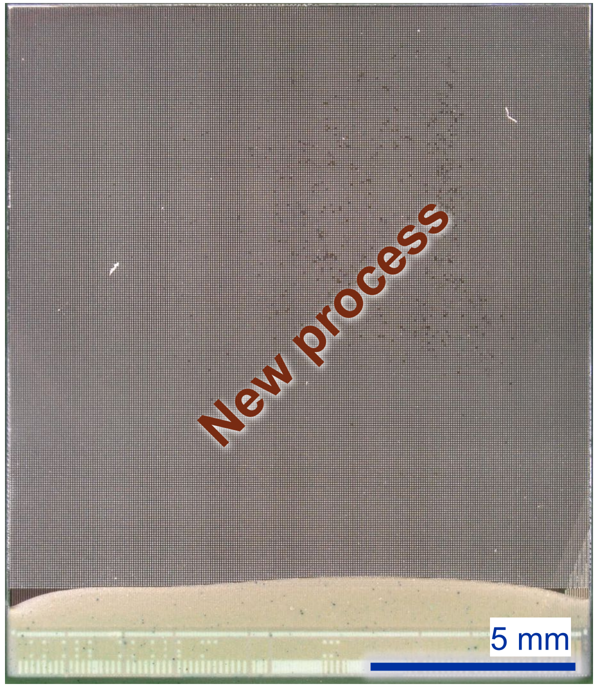
by Mateus Vicente

Improvements
Electroless Nickel

- **Small pad size, pitch and single-dies are challenging to plate**
  - Different plating behaviour near the edge
  - Faster diffusion to small pads
  - Sensitive to parameters and contaminants
- **Significant improvements**
  - Uniformity (edge pullback, skipping…)
  - Reproducibility
- **Wide variety of chips plated**

Differently plated Timepix3 chips





Examples of some plated chips

	Pad size	Pitch	ENIG height
Timepix3	12-14 µm	55 µm	3-8 µm
SPHIRD Si sensor	19 µm	50 µm	5-6 µm
MALTA	88 µm	120 µm	3-10µm
ALTIROC2	92 µm	-	5 µm

Daisy-chain devices

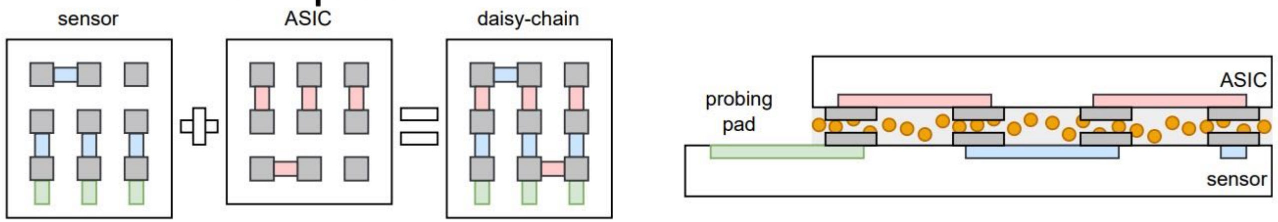
Daisy-chain 6” quartz wafer with 625 µm thickness designed and produced at FBK

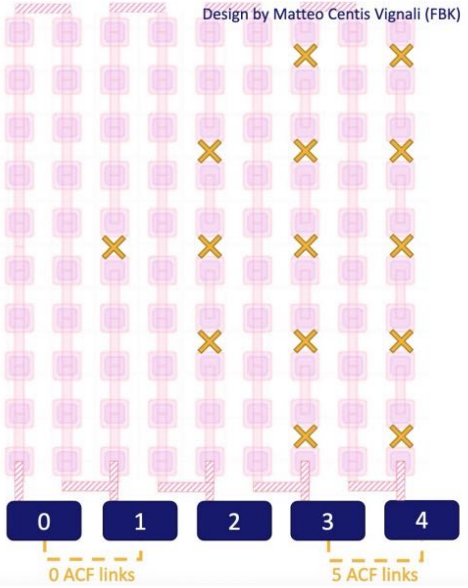
Study of ACA interconnection properties

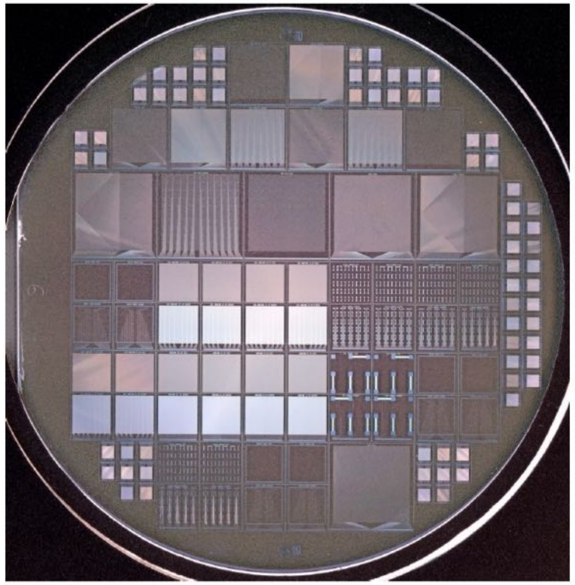
- Low-pitch and large-pitch reliability
- Resistance measurements
- Mechanical analysis

Surface properties similar to typical ASICs and sensors

- Al metal pads 2.5 µm thick
- 950 nm thick passivation







	pitch	size in mm	connections	per wafer	type	diceable
160x160 20um	20 um	3.2 x 3.2	25600	36	grid	no
CLICpix2	25 um	3.2 x 3.2	16384	34	grid	no
400x400 25um	25 um	20 x 20	640000	5	grid	yes
Timepix3	55 um	14 x 14	65536	4	grid	no
Timepix3 islands	55 um	14 x 14	65536	4	grid	no
RD53	50 um	20 x 20	160000	4	grid	no
RD53 islands	50 um	20 x 20	160000	2	grid	no
70x70 140um	140 um	20 x 20	2112	3	peripheral	yes
10x10 1000um	1000 um	20 x 20	400	3	grid	yes
3x3 4500um	4500 um	20 x 20	36	1	grid	yes

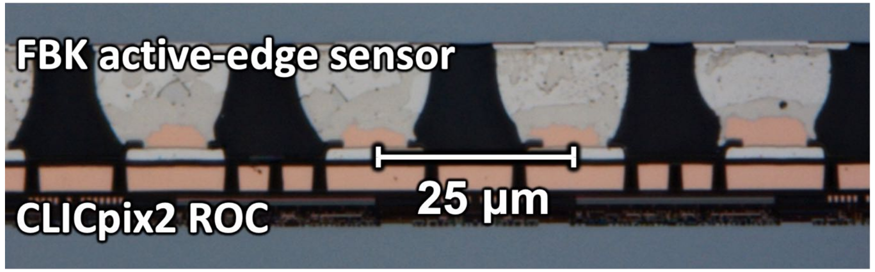
Single-die small pitch bump-bonding

Fraunhofer IZM

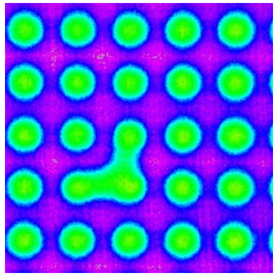
R&D with Fraunhofer IZM for development of single die bonding process down to 25 µm pixel pitch

- Based on support wafer processing
- Verified for multiple assemblies (50 µm, 100 µm, 130 µm sensor thickness) in lab and beam-test
- **Interconnection yield above 99.7% for all devices** arxiv:2210.02132 (JINST accepted)

Cross-section of bonded assembly



X ray image of bumps



provided by Nikon XT V 160
by Abishek Sharma