

# Interconnect technologies via specialized vendors

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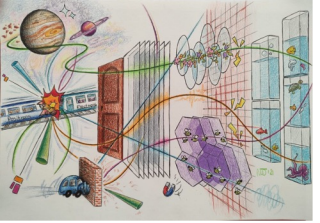
2) LPNHE Paris

3) CERN

4) Fraunhofer IZM Berlin

5) University of Bonn





Interconnect technologies in DRD3 are closely connected to DRD7:

- DRDT 3.4 - Develop full 3D-interconnection technologies for solid state devices in particle physics
- DRDT 7.5 - Evaluate and adapt to emerging electronics and data processing technologies, in particular:
- 3D integration and high density interconnects

For DRD 7 this means something which comes as part of novel chip technologies from wafer fabs like:

- CHIPLETS or CoWoS (Chip on Wafer on Substrate)
- 3D integration technologies are embedded in the chip technology which become available via Europractice for instance:

[https://indico.cern.ch/event/1214423/contributions/5184101/attachments/2612045/4513183/230315\\_ECFA\\_workshop.pdf](https://indico.cern.ch/event/1214423/contributions/5184101/attachments/2612045/4513183/230315_ECFA_workshop.pdf)

In our case we have more in mind interconnection as post processing step by packaging industry/institutes, e.g.:

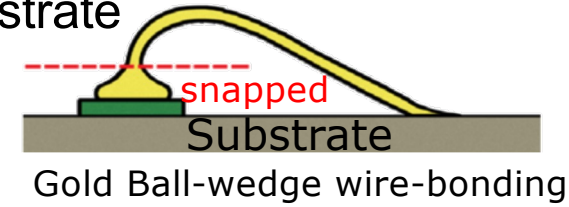
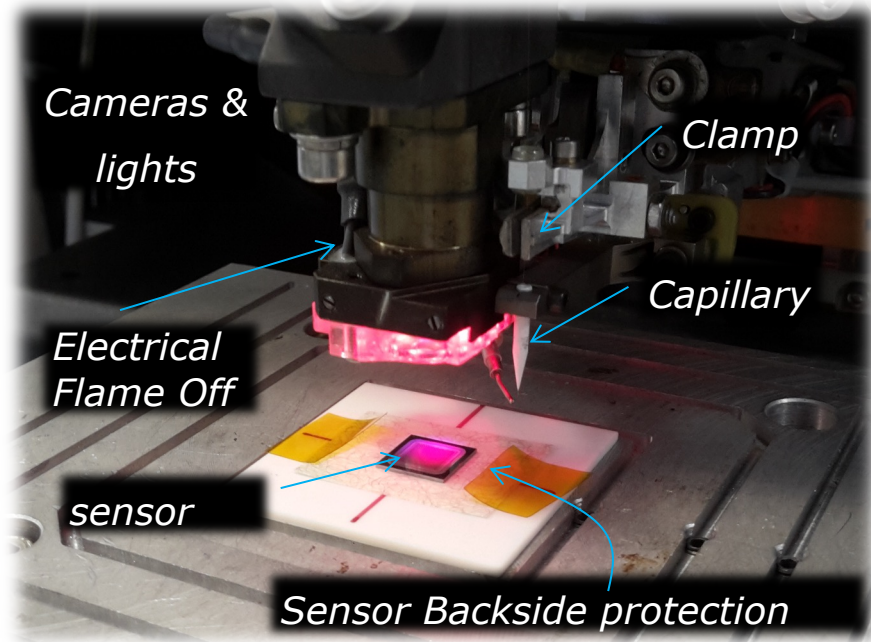
- Hybrid pixel detectors, i.e. separate development of sensor and electronic part which is finally interconnected at dedicated third vendor
- This is presented here with input from semi-industrial partners: Fraunhofer IZM Berlin, IPE KIT Karlsruhe



# Stud Ball Bumping (SBB) process

- Gold stud bumping is an evolution of the ~ 60 years-old wire bonding process.

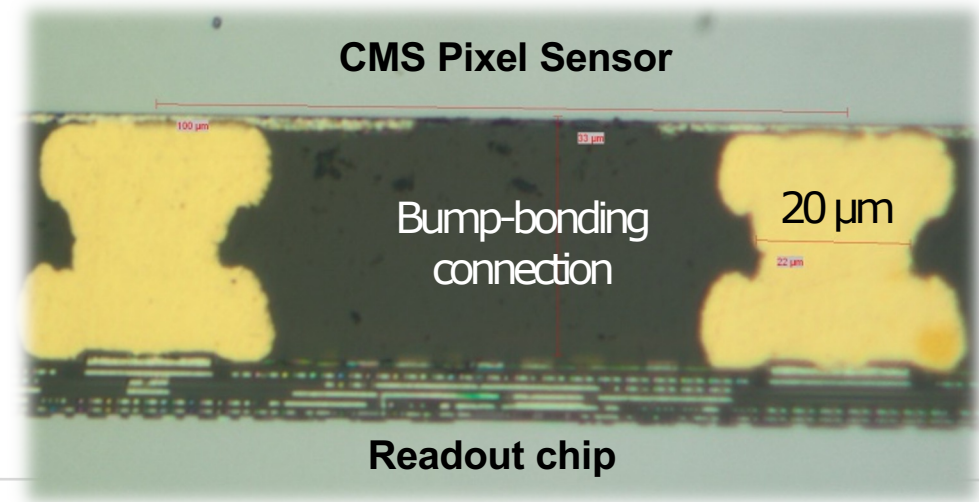
Gold stud ball: the wire is snapped off after the ball is initially connected to the substrate



- ✓ **Low-cost process:** direct deposition on Al pad (No UBM, lithography process)
- ✓ **Fast deposition:** 20 bumps/s
- ✓ **Short setup time:** ideal for single die bump-bonding (i.e. prototype and R&D)

## Achieved Bump & pitch size

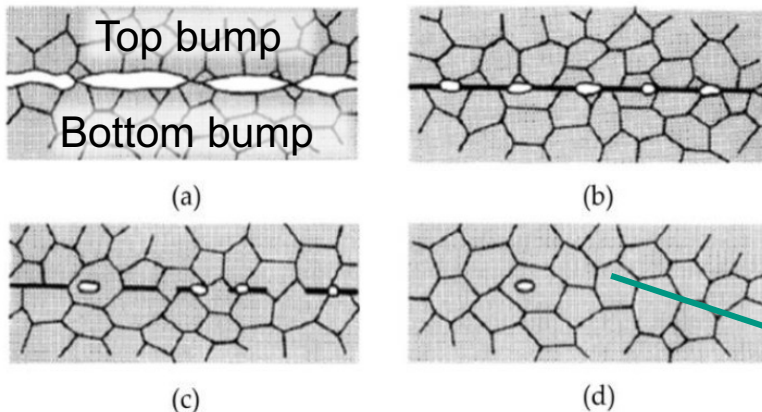
| Au wire diameter (μm) | Bump diameter (μm) | Minimum pitch (μm) |
|-----------------------|--------------------|--------------------|
| 25                    | 60                 | 100                |
| 15                    | 30                 | 50                 |
| 12.5                  | 23                 | 30                 |



# Bonding process

## Bonding process is based on metal-to-metal diffusion process

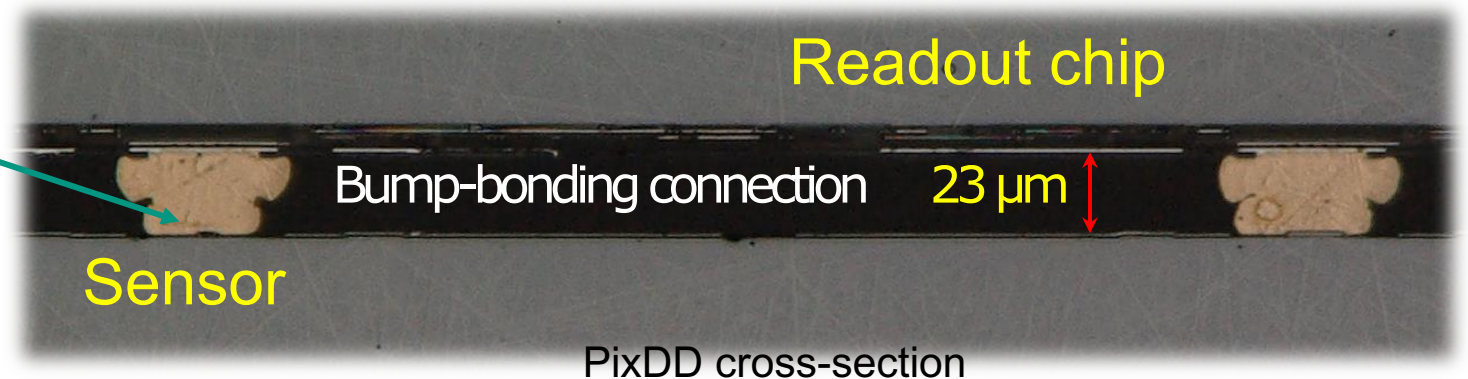
- Metal diffusion bonding, also known as Thermo compression bonding (TCB), is a direct solid-state diffusion bonding process and is based on atomic contact. In this bonding technique, two metals are brought into contact by applying heat and force simultaneously after which the atoms diffuse to form the bond interface

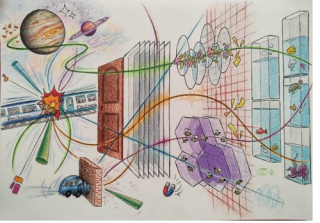


- The **diffusion rate** depends on the chosen **temperature** and applied **pressure** where grain boundary diffusion in both sides

- ✓ **No  $\mu$ -voids** (inside the bumps)
- ✓ **No intermetallic layers** (AuxAly)

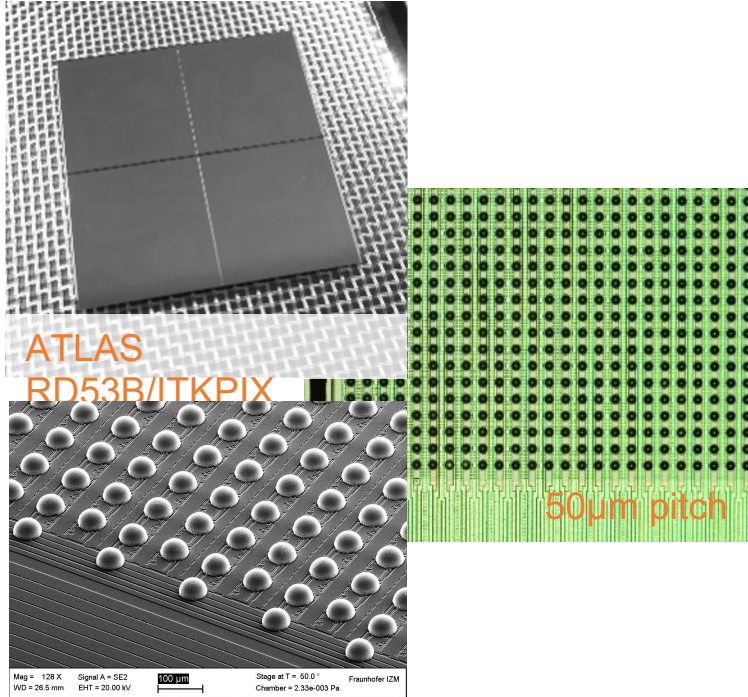
- ✓ High mechanical strength > **6 gr/bump**, which is x 3 higher than the standard industrial process





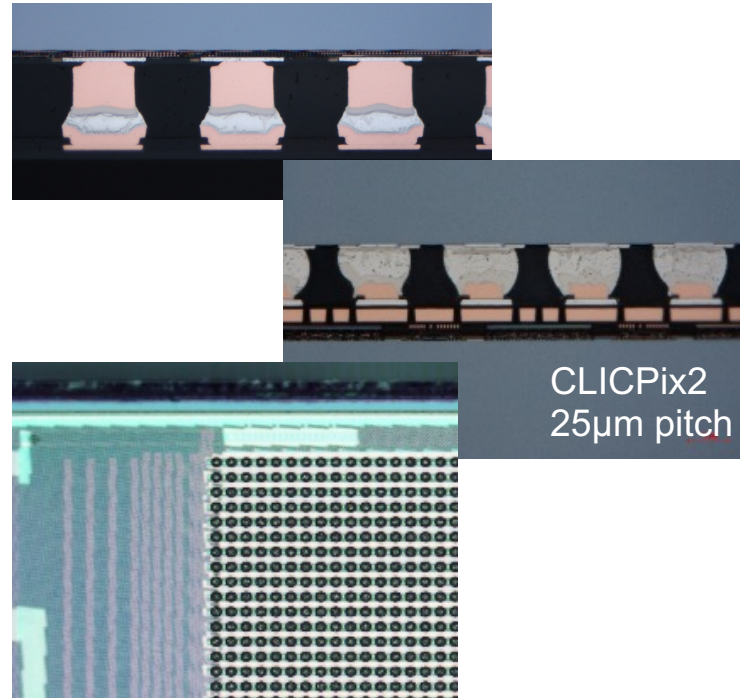
# Interconnects – Assembly Pitch DRD3

## Fine pitch bumping



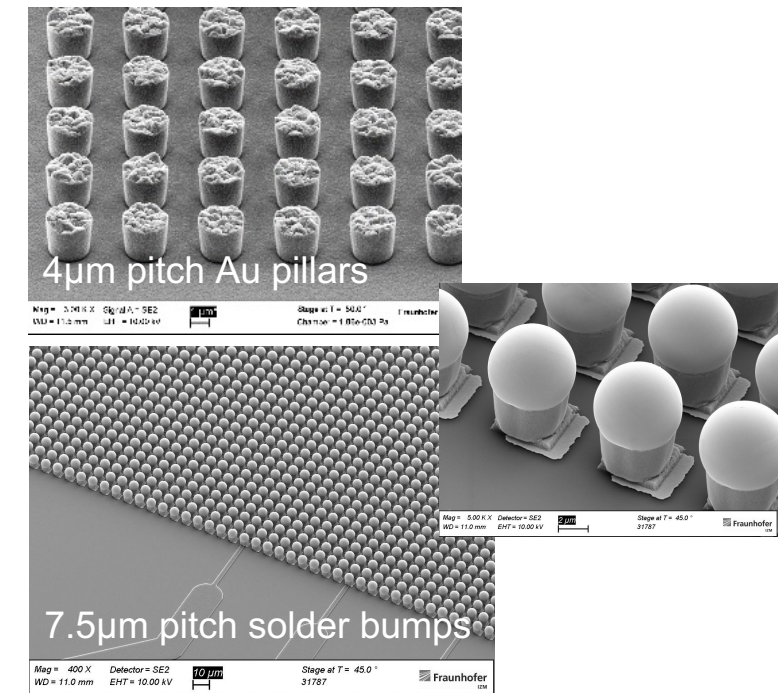
- Pitch 100...50µm
- Bump size: 50...25µm
- Material: Solder bumps, pillar bumps with solder cap

## µ-bumping



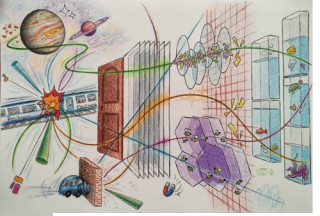
- Pitch 50...20µm
- Bump size: 25...12µm
- Material: Solder bumps, pillar bumps

## Sub-10µ-pitch



- Pitch 10...2 µm
- Bump size: 6...1µm
- Material: pillar bumps, metal pins

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# Wafer2Wafer – Die2Wafer Bonding DRD3

## Metal-Oxide-Hybrid-Bonding

### Motivation for DBI®

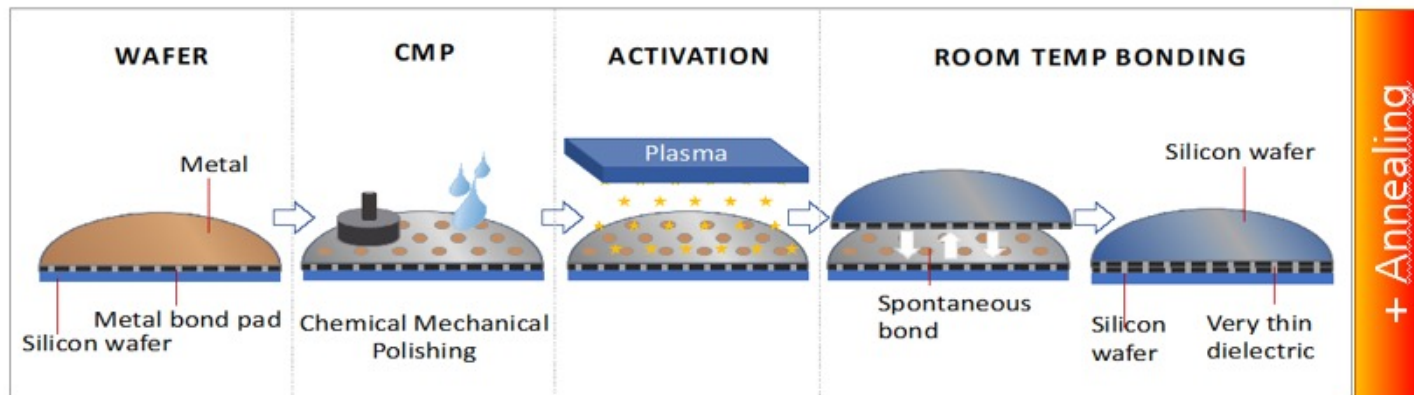
- W2W , D2W, D2D
- Highest interconnect density:  
I/O pitch down to 1  $\mu\text{m}$
- High alignment accuracy
- No bumps, no intermetallics
- No gap – no underfilling
- 3D chip stacking: memory chips,  
CMOS image sensors (CIS)

### Process

- SiO<sub>2</sub> passivation + Cu pads
- Surface planarization (CMP)
- Surface activation  
(plasma, chemicals)
- Room temperature bond
- Annealing 200 – 350°C

### Challenges

- Particle free surface required
- Cu-Oxide surface roughness < 1nm
- Cu dishing  $\leq$  5nm
- Delicate die and wafer handling to  
avoid contamination and particles
- Processes licenced by XPERI/ADEIA:
  - DBI-Ultra: D2W HB, DBI: W2W HB
  - Zi-Bond: W2W DB

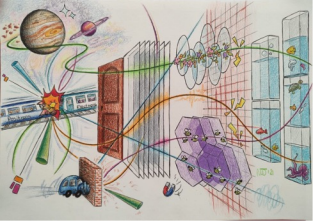


Drawing by F.Huegging, University of Bonn



**IEEE 72nd ECTC 2022:**  
papers from  
AMD, Samsung, Sony,  
Xperi, Applied Materials,  
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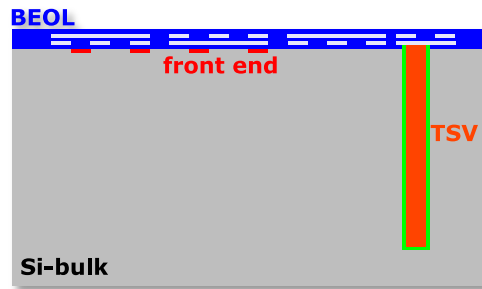


# 3D Integration

# DRD3

## Wafer FAB

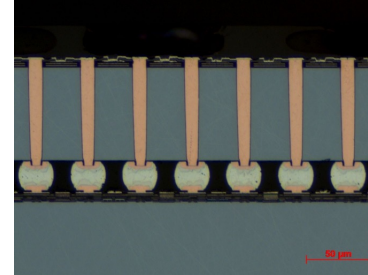
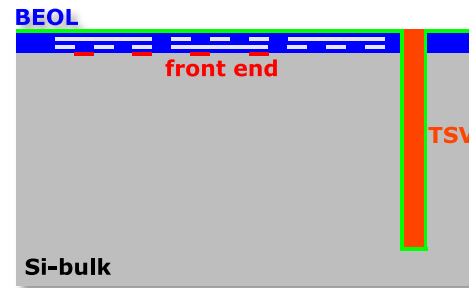
### Via middle



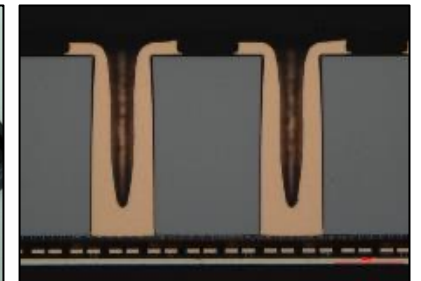
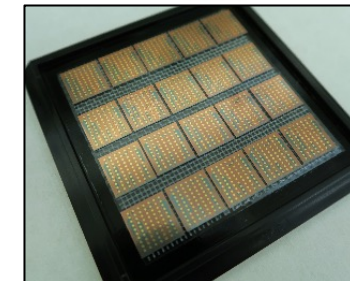
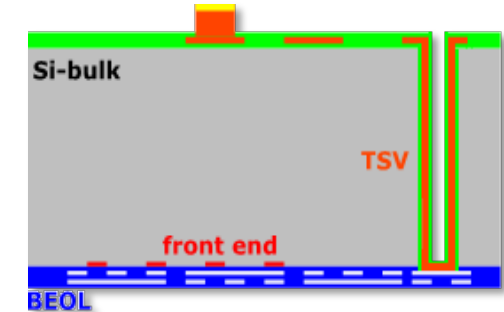
- Fab source that offers TSV service
- Fab that offers 3D TSV R&D on 200/300mm wafer size
- 200/300mm TSV backside processes at packaging institute/industry

## Packaging Institute/Industry

### Front Side - Via last

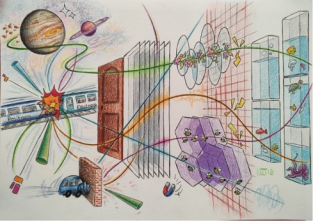


### Back Side - Via last



- TSV optimized CMOS BEOL design
- Adequate amount of setup wafer material
- continuous wafer flow to establish a reliable process
- Institute/industry that offers 3D TSV R&D on 200/300mm wafer size

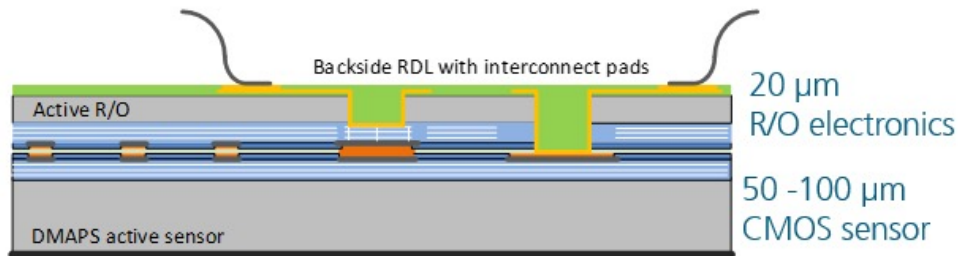
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# Wafer2Wafer – Die2Wafer Bonding DRD3

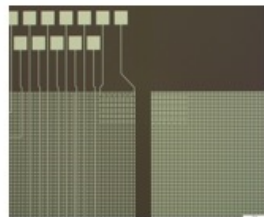
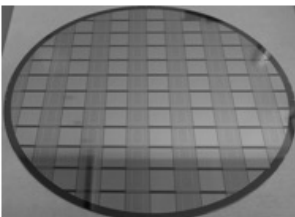
## Advanced Bonding Technologies

### AIDAinnova: Ultra Thin Hybrid Pixel Detectors

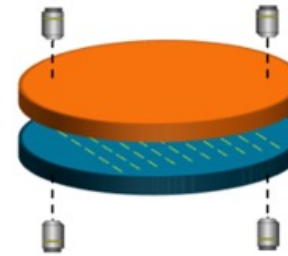


#### Features:

- R/O backside redistribution layer (RDL) with contact pads
- Thinned R/O wafer (i.e. TIMEPIX3) with backside via last interconnection
- Combined polymer – metal - bonding
- Thin DMAPS sensor with contact pads and backside processing

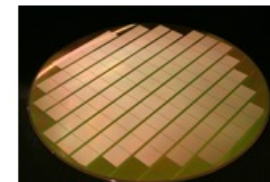


Process setup  
wafer from IZM



#### Tasks:

- Fabrication of technology development and characterization wafer by Fraunhofer IZM
- W2W bonding process development by Fraunhofer IZM
- TIMEPIX3 wafer provided by CERN MEDIPX collaboration
- TIMEPIX3 adapted sensor design by University of Bonn
- 200mm sensor wafer fabricated by Lfoundry



TIMEPIX wafer  
from CERN



Task 6.4: Wafer to wafer  
bonding technique

Slides: F. Huegging (Bonn), I. Gregor (DESY&Bonn), T. Fritzsche (IZM)

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