
# DRD7.1
# High Data Rate ASICs

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# Introduction

## High Data Rate ASICs

- Currently: ASICs between 2.56 - 20.48 Gbps/chip (e.g.: RD53, VeloPix, lpGBT, etc)
- Ambitions for future detectors: >250 Gbps/chip

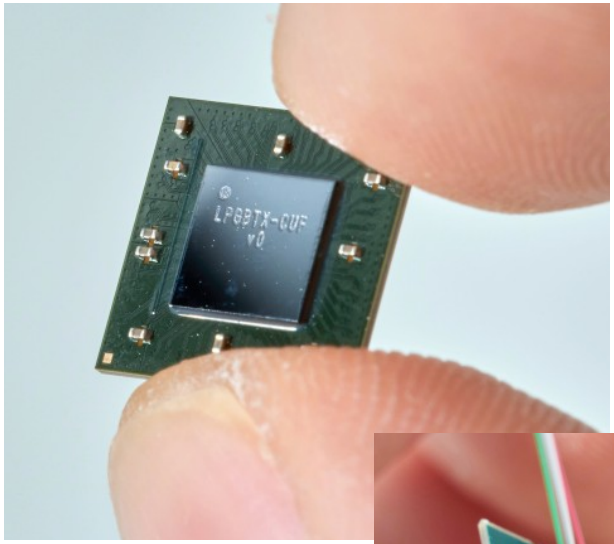
## Today, two types of links deployed in large experiments

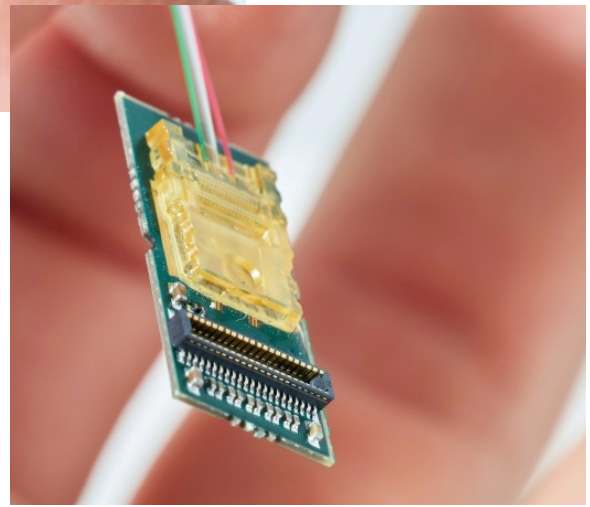
- Electrical links (up to 1.28 Gbps)
- Optical links – VCSEL/PD-based (2.56 – 10.24 Gbps)

# State of the Art

## Example: Versatile Link +

- Fastest per-link speed being deployed at large scale in LHC experiments
  - 2.56 Gb/s downlink
  - 10 Gb/s uplink
- Multi-ASIC solution
  - GBTIA – 5 Gb/s TIA receiver (130 nm)
  - LDQ10 – 4-channel 10 Gb/s VCSEL driver (65 nm)
  - lpGBT – transceiver ASIC (65 nm)



# General Trends

**Alternative approaches to high speed links are being studied in the community**

- Prominent: Si-Photonics, RF links & free space optics – see Fabrizio's presentation

**Higher data density requires high-bandwidth links to move closer to front-ends**

- Need to handling high speed  links inside FE ASICs
- Associated challenges: integration & co-packaging (hybrid detectors) + power delivery

**New CMOS technology nodes**

- Design complexity, effort & verification increase

**All-digital architectures for high speed link components being adopted**

- Example: Digital clock generation circuits vs analog architectures → new approaches for rad-hardening

# High Speed ASICs – Building Blocks

**Main focus in ASIC developments: circuit radiation tolerance (SEE & TID)**

**Key circuit blocks enabling high speed ASICs**

- Modulation, Coding, FEC
- Serializers / Deserializers
- Clock Generation and Distribution (PLL, CDR)
- Receivers & Transmitters (Baseband: TIAs, ADCs, TDCs, DACs – RF: LNAs, PAs, Mixers, ...)
- Auxilliary Circuits (e.g. SiPh - Thermal Control)

# High Speed ASICs – Modulation, Coding, FEC

### Very high speed wireline NRZ links (25 Gb/s+)

- Established and proven techniques (interleaving, scrambling, R-S FEC) remain relevant - also in terms of resource needs, latency, etc.
- Knowledge & implementations available in the community

### Advanced wireline links (PAM-4 and beyond)

- Typically no longer designed for error-free reception over physical link
- More aggressive FEC schemes employed to obtain error-free end-to-end transmission
    - Much larger encoder/decoders required, possibly increased latency
- **Little experience in the community at this point, some trade-offs remains to be studied**

### RF & Free Space Optical Links

- Applicable modulation schemes and coding are widely studied for commercial applications

# High Speed ASICs – Clock Generation

**Per-link data rate directly drives clock quality requirements**

- Issues such as power supply sensitivity will start becoming design drivers
- Low-jitter clock generation research (established during VL+ developments ) needs to be continued
- Needs to be considered also at the detector & module design stages

**Some synergies with requirements of timing detectors (DRDT7.3)**

- High quality clocks required for high speed & high resolution front-end ADCs/TDCs
- > 10 Gb/s: high speed links begin driving the requirements

**Very important consideration also for multi-GHz RF links**

# High Speed ASICs – Serializers & Deserializers

**Widely studied & implemented commercially at the data rates we target**

- Digital circuits → radiation effects & hardening well-understood
- Often strongly coupled to clock generation circuit
- Challenges lie mostly in the actual implementation and verification process
    - Skirting the boundary between ‘full-custom’ & ‘digital’ workflows

# High Speed ASICs – Receivers & Drivers

**Receiver & Driver circuits in CMOS technologies**

- Need for high speed & high voltages (biasing, large output swing)
- Conflicting with performance & TID tolerance  of thick-oxide devices in low-voltage CMOS nodes

**Conventionally, different technologies might be preferred for such blocks (e.g. BiCMOS, SiGe)**

- Largest issue for use in community: Technology radiation qualification
- Could be approached as a common R&D effort - likely to have large synergies for RF links

**Si-Photonics ring modulators require active temperature control**

- Requires full ADC/DAC & control loop design – such “auxiliary” functions can become large projects on their own
- Similar challenge: polarisation control

# High Speed ASICs – Integration

**Interconnect parasitics become significant design consideration at high speeds**

- **Wirebond:** inductance in particular must be minimized and well modelled
- **Flip-chip integration:** could be incompatible with the hybrid detector designs that drive the data density requirements
- **Advanced interconnects:** e.g. TSVs being studied – little community experience for HS links

**Activities on interconnect modelling & driver circuit design will have large impact**

- Similar activities foreseen in DRD7.5 (Emerging Technologies)

# High Speed ASICs – Powering Needs

**Need for voltages larger than typical I/O voltages (e.g. 1.8 V)**

- Required for e.g. photonics modulators, VCSELs, PD biasing, RF circuits

**Power density**

- TX output circuits may dissipate >>100 mW per lane in small area
- Multi-lane system requires providing **and distributing** this current to all drivers on-chip → IR drop, EM considerations

Will need to investigate suitable powering schemes (on-chip vs off-chip regulation, power distribution network current capabilities)

# Calls for Action

## Identified avenues for activities & collaboration

- Studies of FEC trade-offs for advanced (PAM-4+) wireline links
- Low-jitter clock generation & distribution studies on ASIC- and detector-scale
- Systems-focused interconnect studies (simulations & prototyping): flip-chip, wirebond, TSVs
    - Large impact on high speed driver designs
- High-voltage output drivers for implementation of rad-hard SiPh links
    - Associated powering challenges
- Integrated temperature control circuits for SiPh links
- Radiation qualification of new technologies for RF/driver/receiver circuits (e.g. SiGe)

# Collaboration – Opportunities

**Multiple groups in the European community working on high speed ASICs components**

- Wireline (incl. Silicon Photonics):  CERN, INFN, Nikhef, KIT, IN2P3, Universities: KU Leuven, AGH, Bonn, Pisa, ...
- Wireless:  e.g. CEA, IPHC, Unversities: Uppsala University, Wuppertal, Heidelberg, Bergen, ...

**Some overlap in activities observed – likely a good catalyst for collaboration**

- Need to engage in talks, encourage specialization & align on common goals

# Collaboration – Challenges

**CMOS down to 28 nm is widely employed commercially**

- Circuits, architectures, technology challenges, etc. have been extensively studied in the literature
- Our key focus can be on radiation tolerance: **How much of this is research, how much is engineering?**

**Complexity increases rapidly at this node (relative to our community size)**

- Engineering resource needs for first-time-right mixed-signal ASICs become immense!
- Analog & digital functional & SEE verification, STA (+timing characterization), power integrity (EM/IR), IP release engineering, …

**Both factors together lead to a shifted balance between “research” and “development”**

- Must reflect in the allocated resources: experience, expectations of publications, novelty of developments, PhD theses

# Collaboration – Challenges

**ECFA Roadmap calls for "Large-scale and realistic technology demonstrators"**

- Such developments require significantly more resources than small-scale prototypes

**Achieving this vision for high speed ASICs will require focus & collaboration**

- Challenges for this exist on technical (tools, specifications, …), legal (NDAs, design sharing) and coordination (schedules, grants, resources) levels → see also DRD7.7 presentations

# Call for Discussion

**Closing remark: Proposals for applications of DRD7.1 R&D**

- In LHCb, ALICE: already on the horizon, time scale is short (2030)
- Success will require rapid consolidation into working demonstrators
    - This needs to inform the choices (technology, risk, maturity, ...) we make!

**Will SiPh become the future of high speed links in HEP?**

- Strong signals of interest from experiments
- Multiple well-advanced ASIC developments in the pipeline, strong emphasis from EP R&D program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