Prospects on the Power and readout efficiency

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Identified future challenges

Power distribution will be a key element in the success of future experiments, due to large increase of current needed by the ASICs and the thin amount of cabling that can be installed.

In the ECFA Detector R&D Roadmap document, these domains of interest have been identified:

- DCDC powering (high conversion ratios for reducing the current in the cables)
- Serial powering
- Disruptive or unconventional powering schemes (like power over fibre or wireless power). DC optical power supply modules will become an essential building block for silicon photonics

In all scenarios

- Need of intelligent power management and multiple supply voltages in the ASICs (linear regulators on chip)
- Need of going in deep submicron technology to meet Grad level of radiation tolerance for front end ASICs
- Need to be tolerant to high magnetic fields

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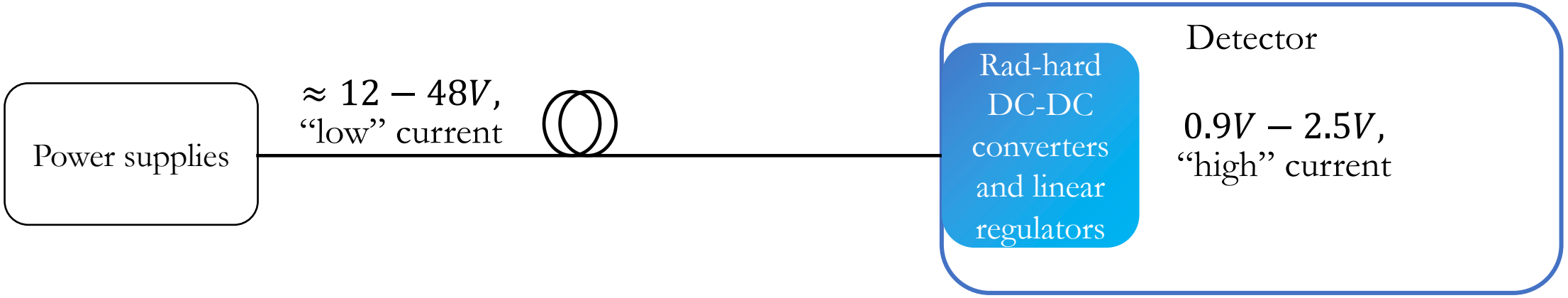
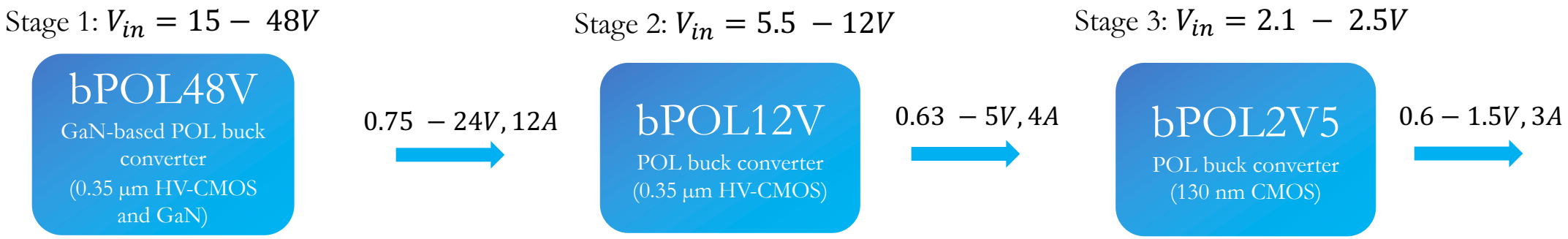
Challenges for the future: radiation

		2030-2035 (LS4)	FCC hh
Vertex detector	Radiation tolerance TID (Grad)	1	30
	Radiation tolerance NIEL (x e16 neq/cm2)	6	100
Tracker	Radiation tolerance TID (Grad)	0.25	1
	Radiation tolerance NIEL (x e16 neq/cm2)	0.3	1
calorimeter	Radiation tolerance TID (Grad)		50
	Radiation tolerance NIEL (x e16 neq/cm2)		100

Power management and distribution



Power management ASICs
State of the art



Information and datasheets available at: https://espace.cern.ch/project-DCDC-new
Contact: **dcdc.asic.support@cern.ch**

Power management ASICs
State of the art

Stage 1

bPOL48V
GaN-based POL buck converter
(0.35 µm HV-CMOS and GaN)

Stage 2

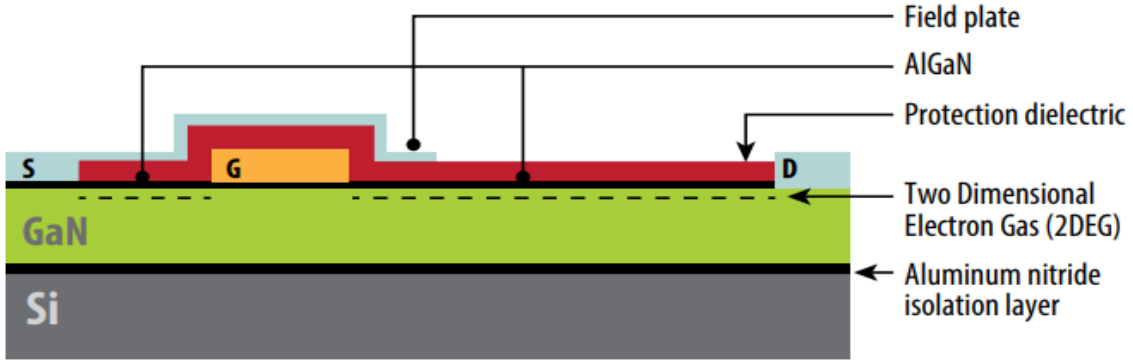
bPOL12V
POL buck converter
(0.35 µm HV-CMOS)

Stage 3

bPOL2V5
POL buck converter
(130 nm CMOS)

		bPOL48V	bPOL12V	bPOL2V5
Specs	Vin	15-48V	5.5-12V	2.1-2.5V
	Vout	0.75-24V (Vout/Vin must be > 1/20, min switch on time 40 ns)	0.63V-5V	0.6-1.5V
	Iout max	12A	4A	3A
Radiation tolerance	TID max	228 Mrad	150Mrad	100Mrad
	SEE max	88 MeV/(mg/cm²)	45 MeV/(mg/cm²)	40 MeV/(mg/cm²)
	DD max	4e14 n/cm2 2.23e14 p/cm2(30MeV)	7e15n/cm2 1.2e15p/cm2 (27MeV) 2.34e15p/cm2(230MeV)	2e16n/cm2 6.6e15p/cm2 (25GeV)

Stage1: Why GaN?

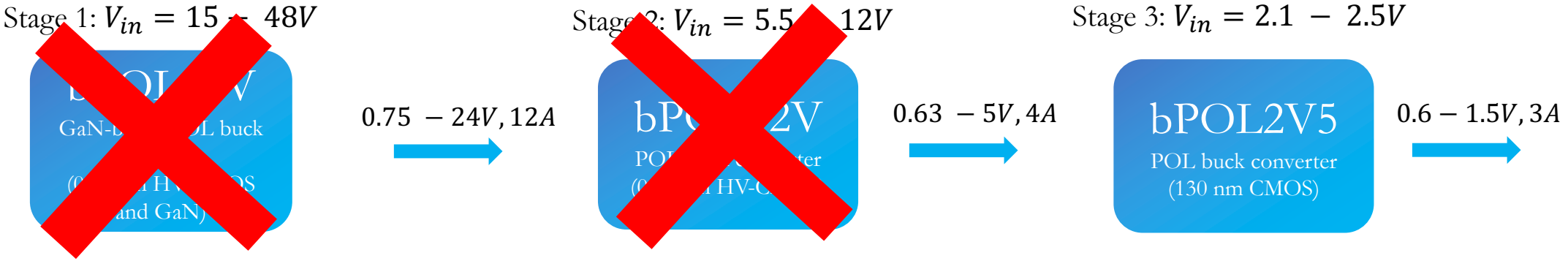


GaN power FETs offer superior performance compared to Silicon devices:

- Smaller size and increased breakdown voltage for the same on-resistance
- Faster switching (which leads to reduced losses and smaller passive components)
- Increased radiation hardness (no SiO2, responsible for most TID effects in Si MOSFETs, in contact with the channel).

Long term availability

(production fab closed for both technologies)



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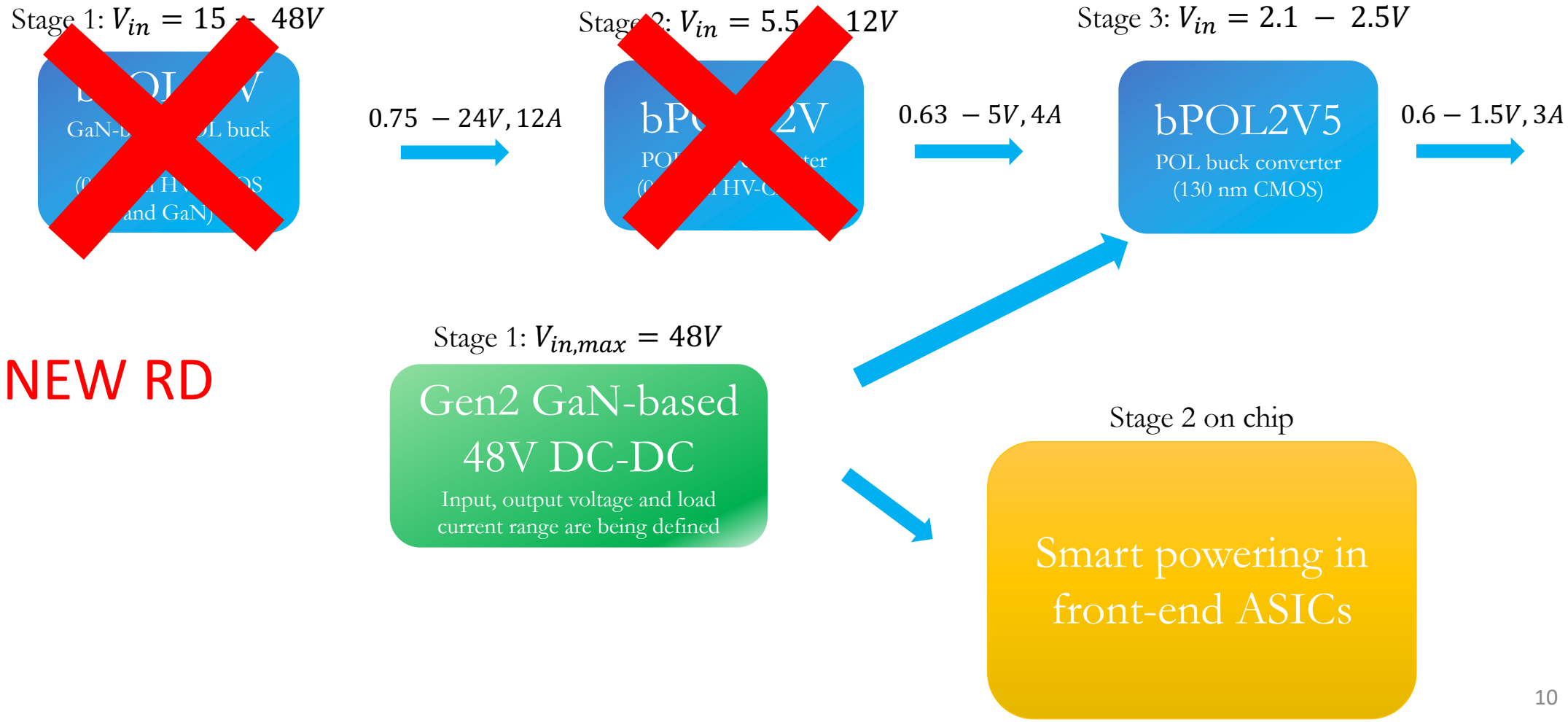
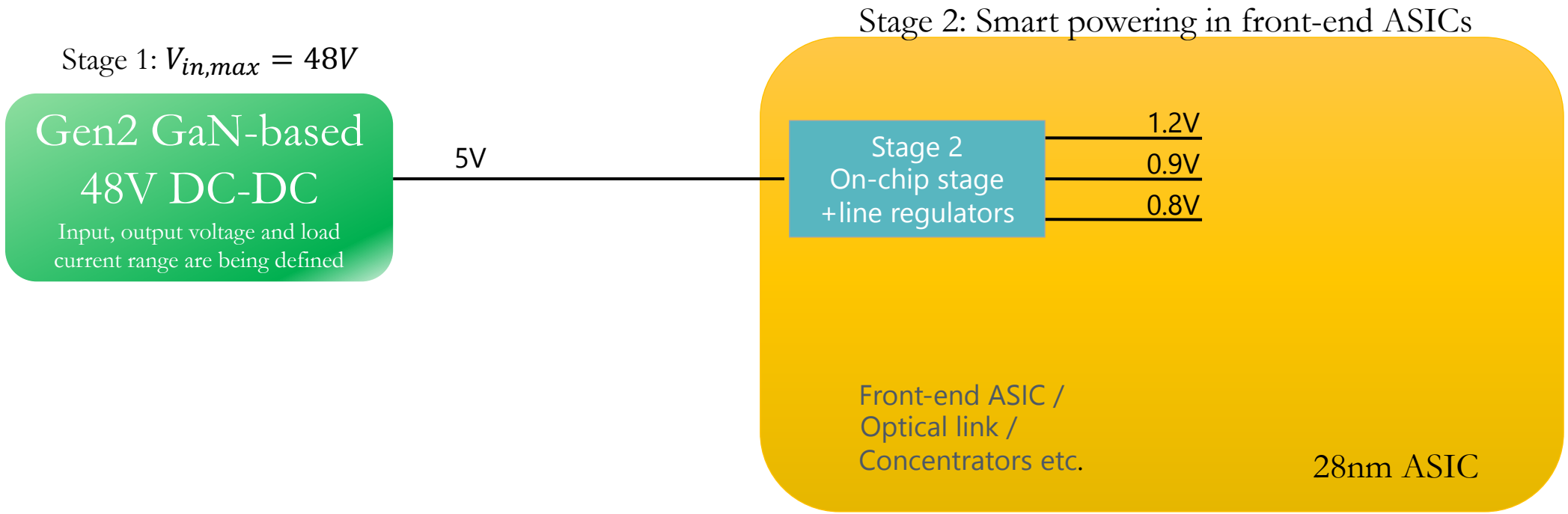


New power distribution scheme



Stage 1 based on HV CMOS technology and GaN power stage

Stage 2 is a fully integrated solution with all components inside the 28nm ASIC

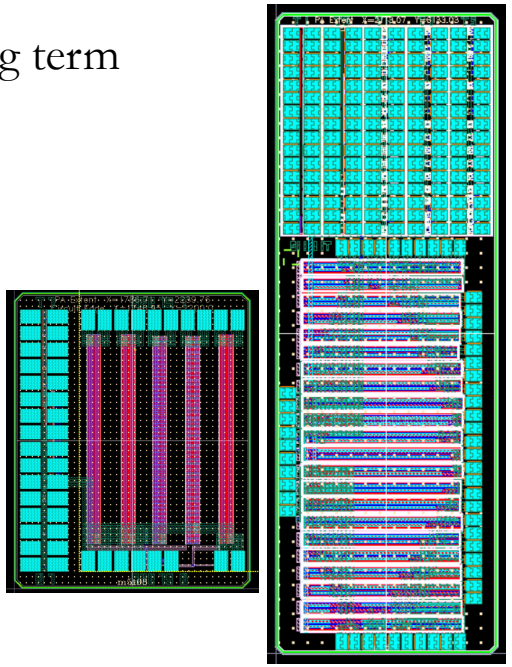
Stage1: Ensuring the long-term availability of high voltage technologies

We need to find suitable technologies (both High Voltage CMOS and GaN) which are available in long term

HV CMOS technology must be found:

- The radiation characterization of the OnSemi I4T is being finalized. (Test chips designed in 2020).
- As an alternative solution, the ST 0.16 BCD SOI will be tested.
- Future HV technologies must be tested

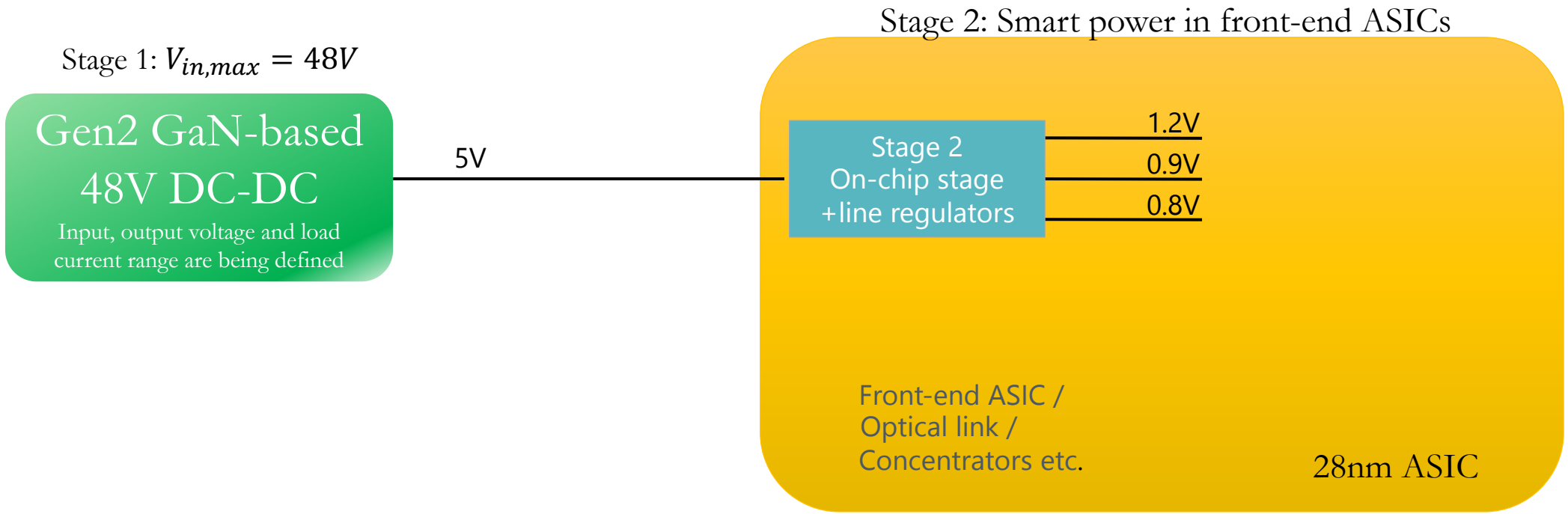
OnSemi I4T test chips



GaN

- Survey of commercial components (EPC, Infineon, ST, GaN System)
- Test of accessible GaN process for radiation (IMEC GaN technology)

Stage2: fully integrated DCDC in front-end technology



Stage 1 based on HV CMOS technology and GaN power stage

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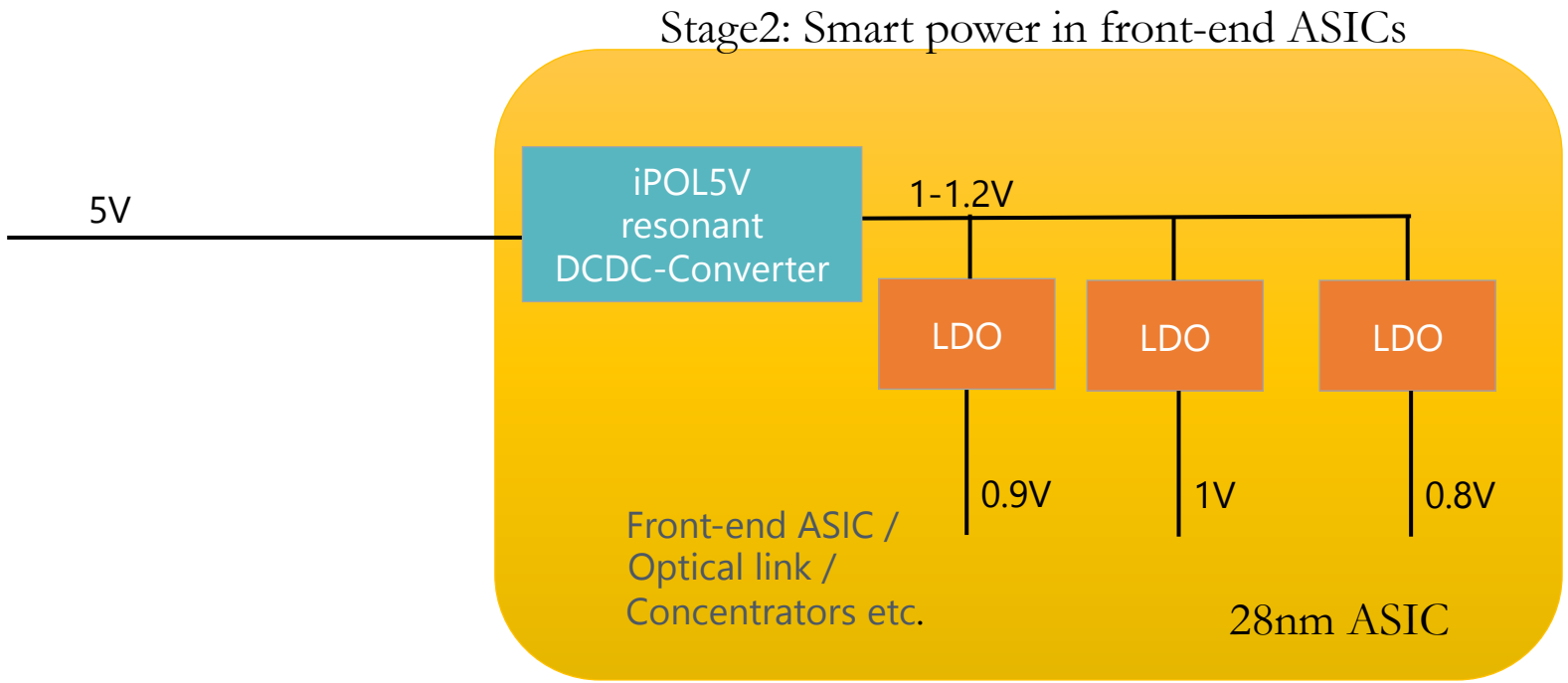
Stage2: fully integrated DCDC in front-end technology



Smart distribution on chip is necessary to limit the power requirements.

A fully integrated DCDC will provide a ~1V on chip from 5V power bus.

Different part of the circuit can be supplied with different voltages with full integrated LDO

This innovative power distribution scheme do not require additional external components.

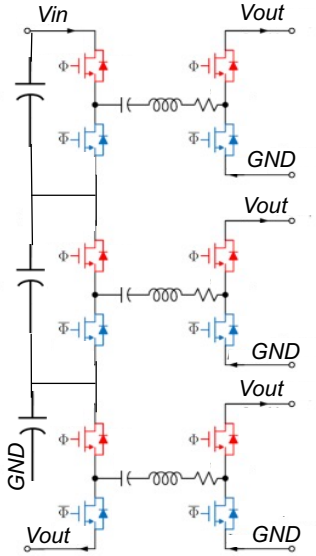
Stage2 iPOL5V: 5V-input resonant DC-DC converter

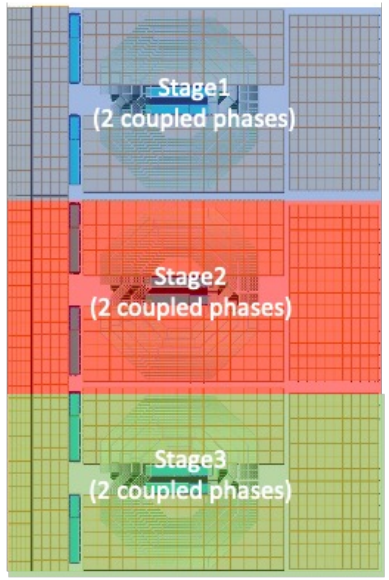
iPOL5V is a **fully integrated** resonant DC-DC converter developed in a 28 nm CMOS technology that can be integrated as a Macro Block in more complex ASICs (e.g. PicoPix).
R&D has started in Q4, 2021.

The target V_{out} is $0.9 - 1V$, with a tentative maximum current of $500\ mA$.

Added value:

- ultimate solution for low mass: no external components
- unprecedented radiation hardness for DC-DC converters: target TID tolerance is 1 Grad
- large reduction of input current (factor ≈ 4)
- a fully integrated solution relaxes the PCB design



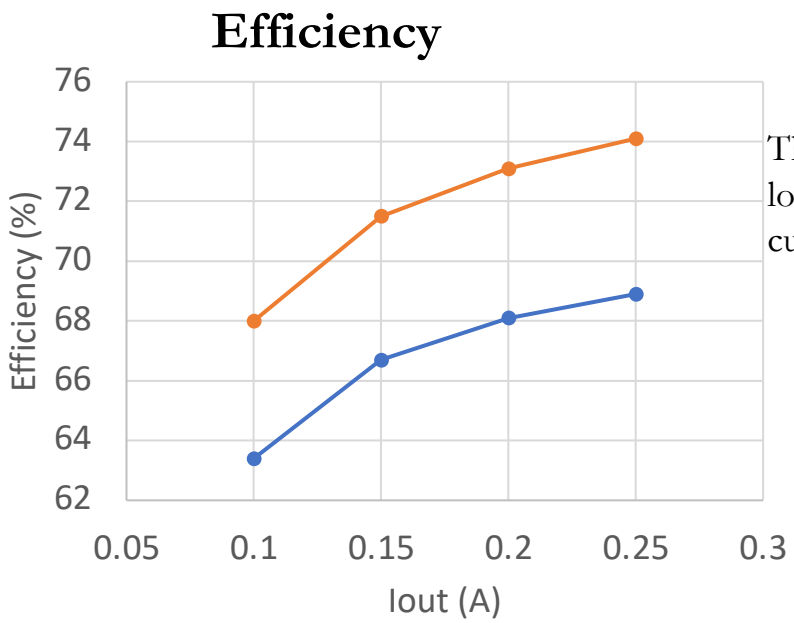


Design started, submission of the first prototype in Q2 2023.
A full PicoPix could be powered by parallelizing several iPOL5V cells.

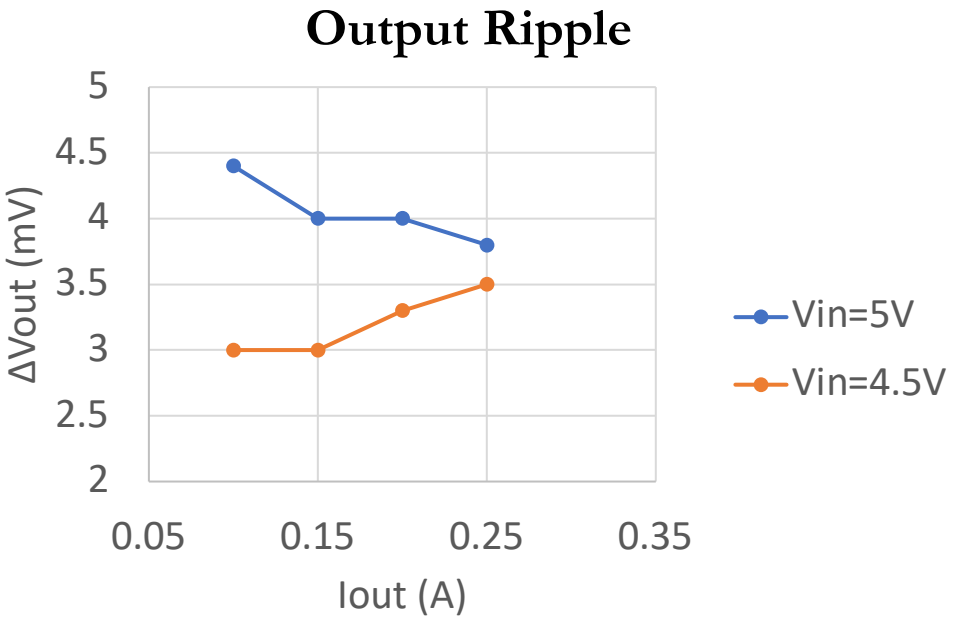
Design done in collaboration with Udine

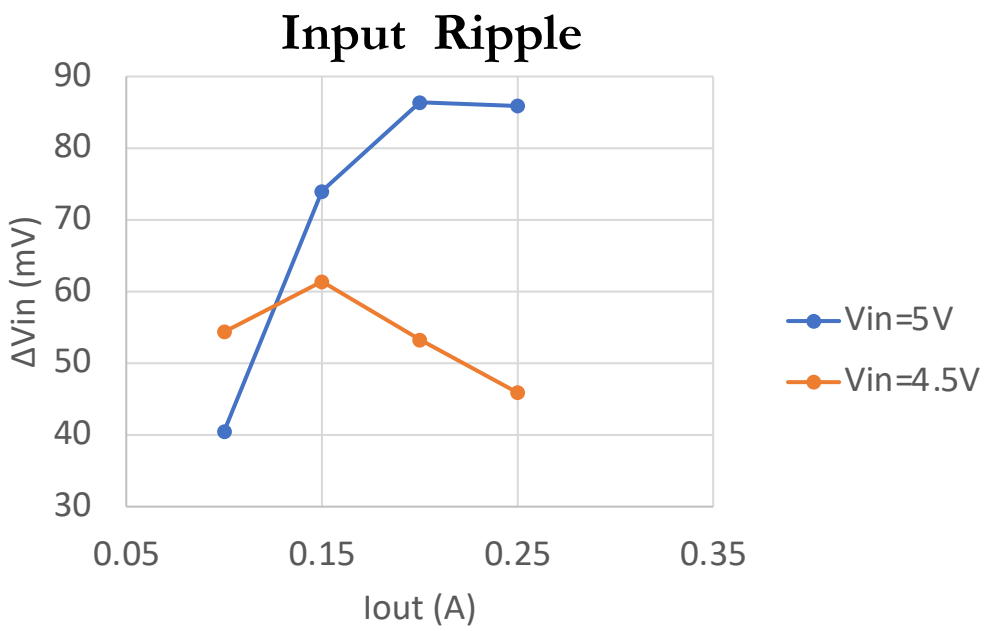
Stage2 iPOL5V Simulation results

The simulated block has been conceived to provide up to 250 mA, a larger load current can be provided by using larger FETs or additional phases.



The input current is lower than the output current by a factor ≈ 4



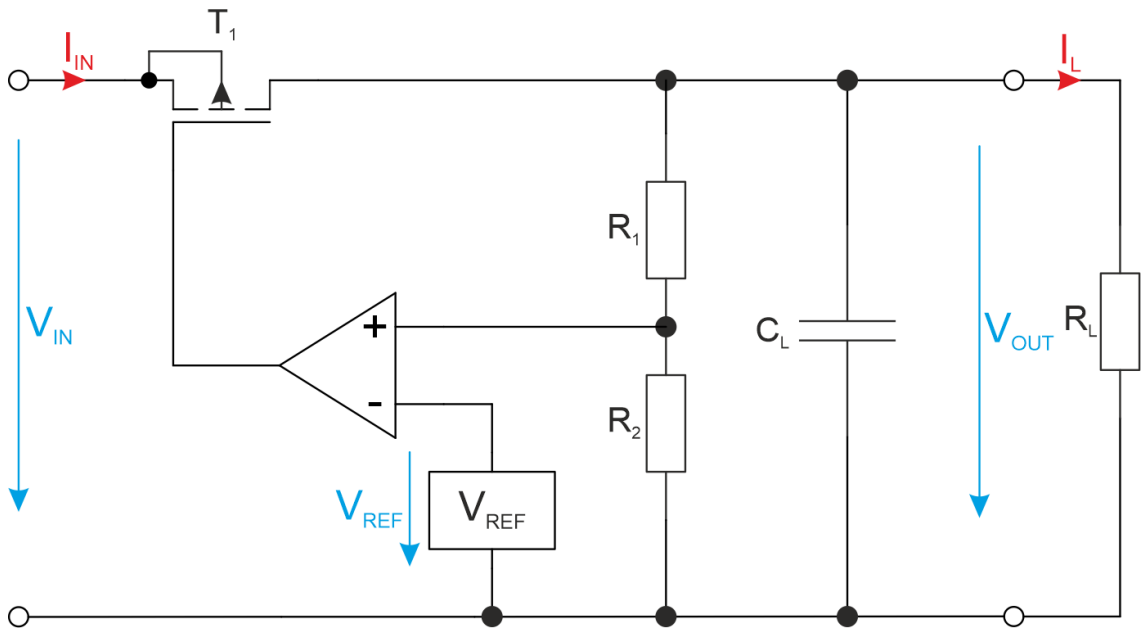


Stage2: LDO low drop-out linear regulator

A fully integrated linear regulator is under design in TU Graz with these specifications

- Input Voltage V_{IN} = 0.9V – 1.2V
- Output Current I_L =150mA
- PSRR >10dB @ 1Hz < f_{ripple} < 1GHz)
- Minimum Drop Voltage $V_{drop,min}$ = 50mV
- Max. TID 1 Grad
- Mainly using core transistors

First prototype during 2023



Conclusions

Power distribution will face several challenges

- High current demand at low voltage, low mass cabling
- very high radiation levels
- magnetic field
- front-end ASIC on-chip smart power distribution

In the ECFA Detector R&D Roadmap document, three domains of interest have been identified:

- DCDC powering (high conversion ratios for reducing the current in the cables).
- Serial powering.
- Disruptive or unconventional powering schemes (power over fibre or wireless power).

For DCDC powering we have identified avenues for activities & collaboration:

- find suitable technologies for HV CMOS and GaN for first stage DCDC converters and design high conversion ratio converters
- design IP blocks in deep submicron technologies for smart power handling on front-end chip

The amount of work is large, collaboration with University of Udine and TU Graz is already on-going

Community is more than welcome to join this development or explore the others domains