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Availability and Access to Advanced (Silicon) Technologies for the HEP community via the EUROPRACTICE services

Paul Malisse, imec

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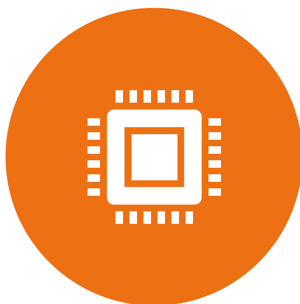
THE 3 PILLARS OF THE EUROPRACTICE SERVICE

- EUROPRACTICE is a true one-stop shop that lowers the barrier to access all services that you need to design and fabricate electronic circuits and smart integrated systems:



FABRICATION SERVICES

DESIGN TOOLS

TRAINING & WEBINARS

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TODAY

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TODAY's Foundry Offerings

ASICs

Smart Power

MEMS

Photonics

Microfluidics

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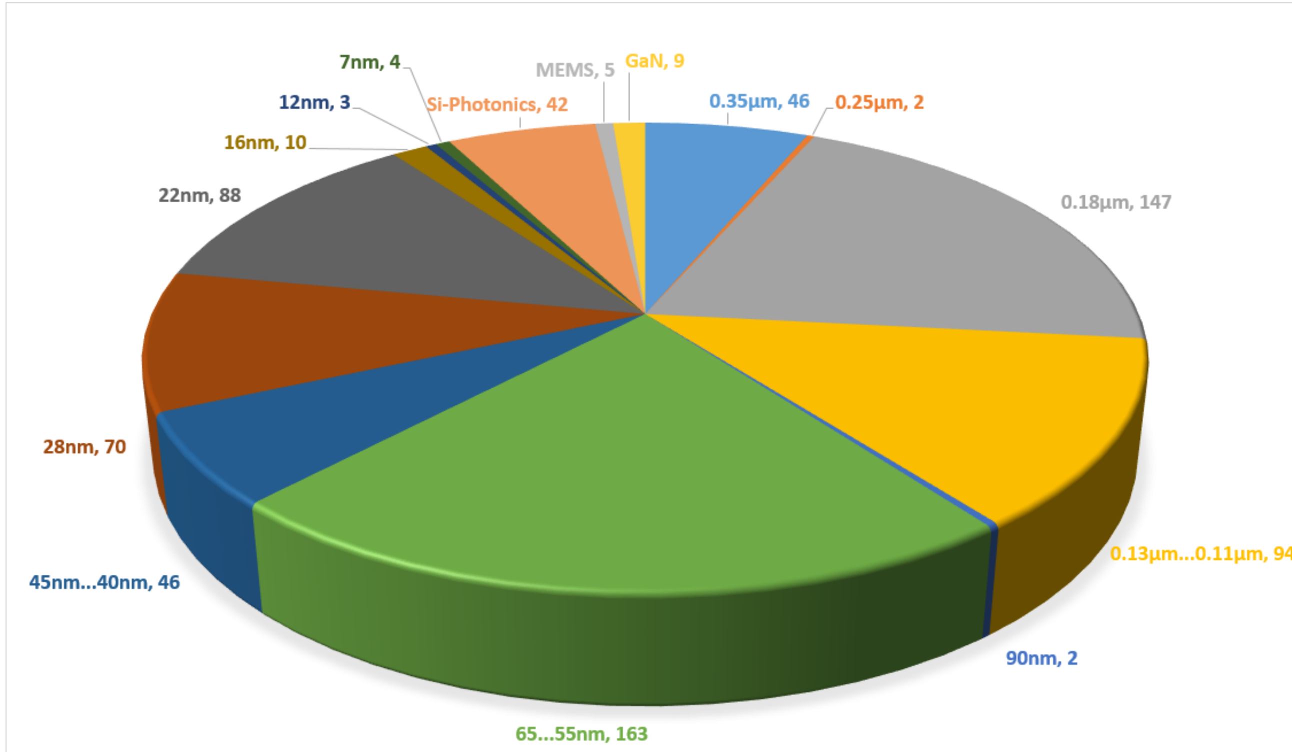
TODAY's ASIC technology usage - anno 2022



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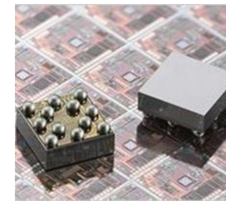
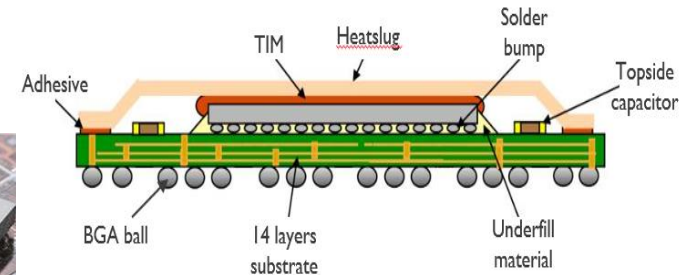
TODAY's assembly techniques

- Standard packages are available and used frequently
- Complex circuits and technologies require more advanced assembly techniques.
  - Wire bond Ball Grid Array's
  - Wafer Level Chip Scale Package (WLCSP)
  - Flip Chip Ball Grid Array's with complicated substrate design





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THE FUTURE

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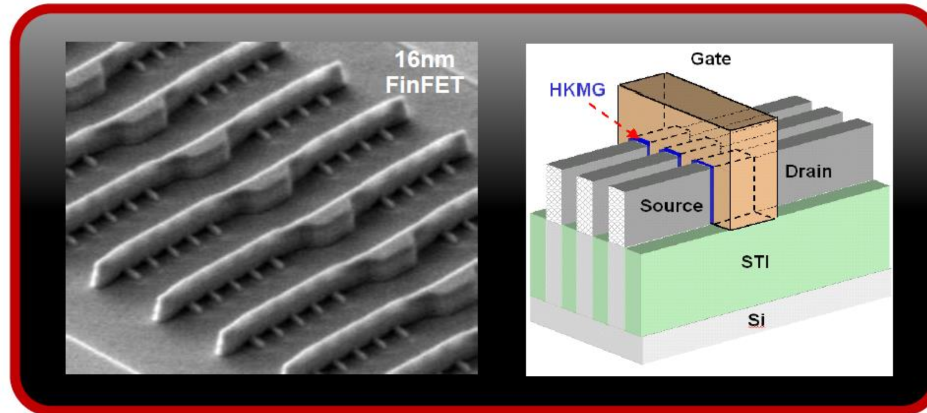
TSMC FinFET Technology

tsmc

Security C – TSMC Secret

- Better electrical control over channel and more effective leakage suppression
- Driving current enhancement
- Better analog performance from higher intrinsic gain



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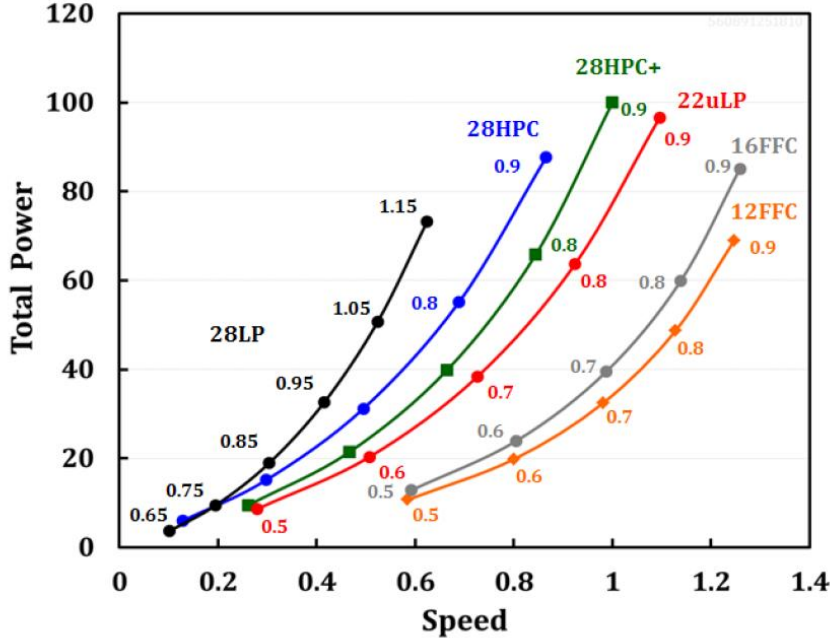
TOMORROW's technology offerings



tsmc

Security C – TSMC Secret

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THE ECONOMICS

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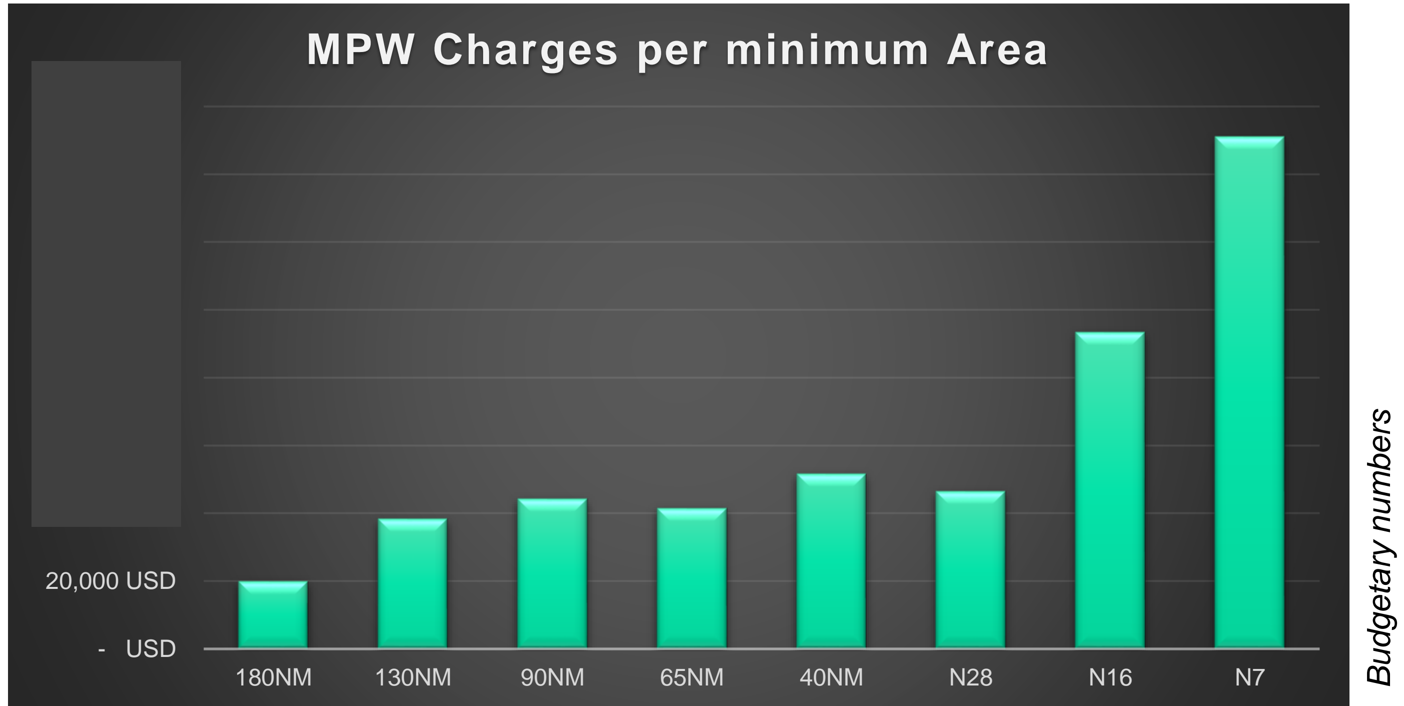
The FUTURE



Budgetary numbers

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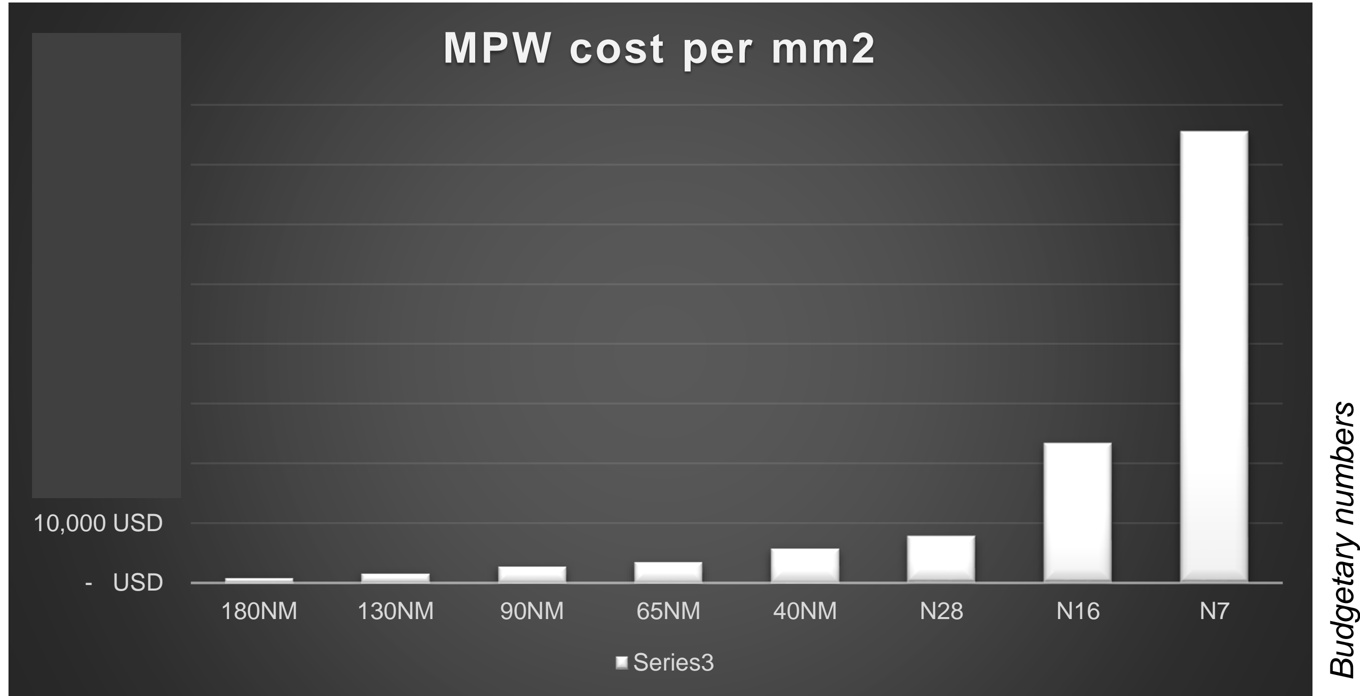
The FUTURE



Budgetary numbers

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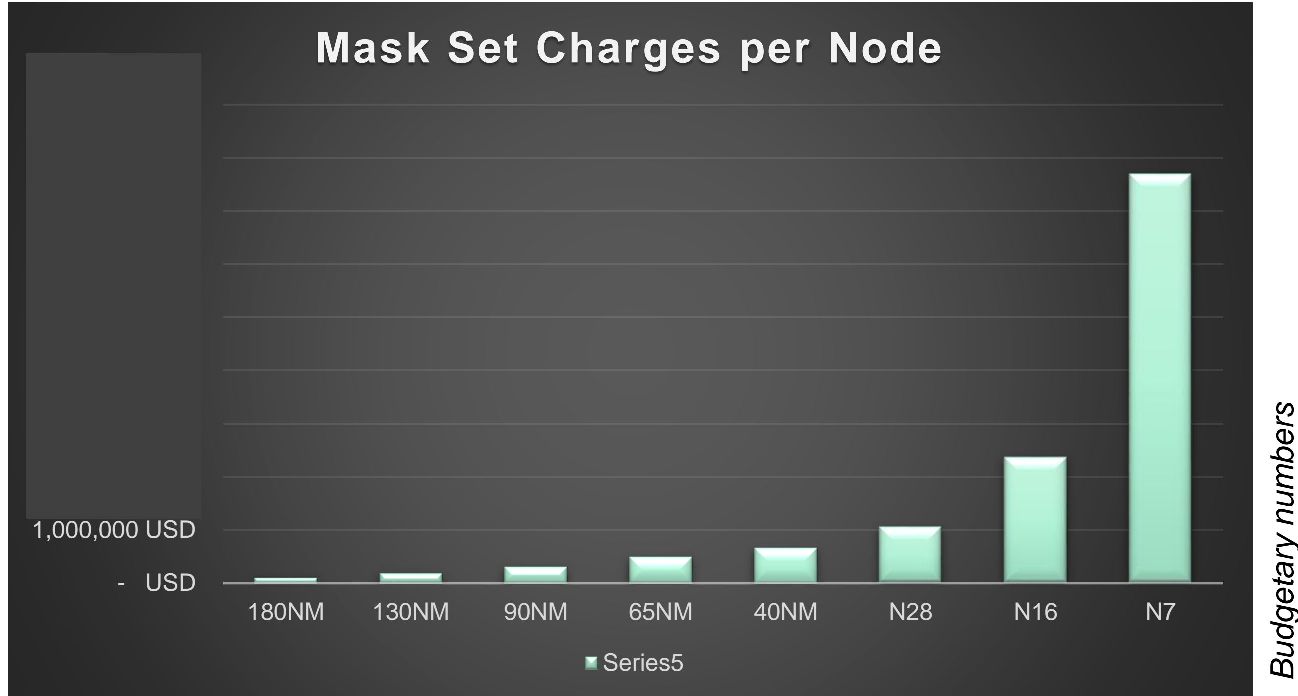
The FUTURE



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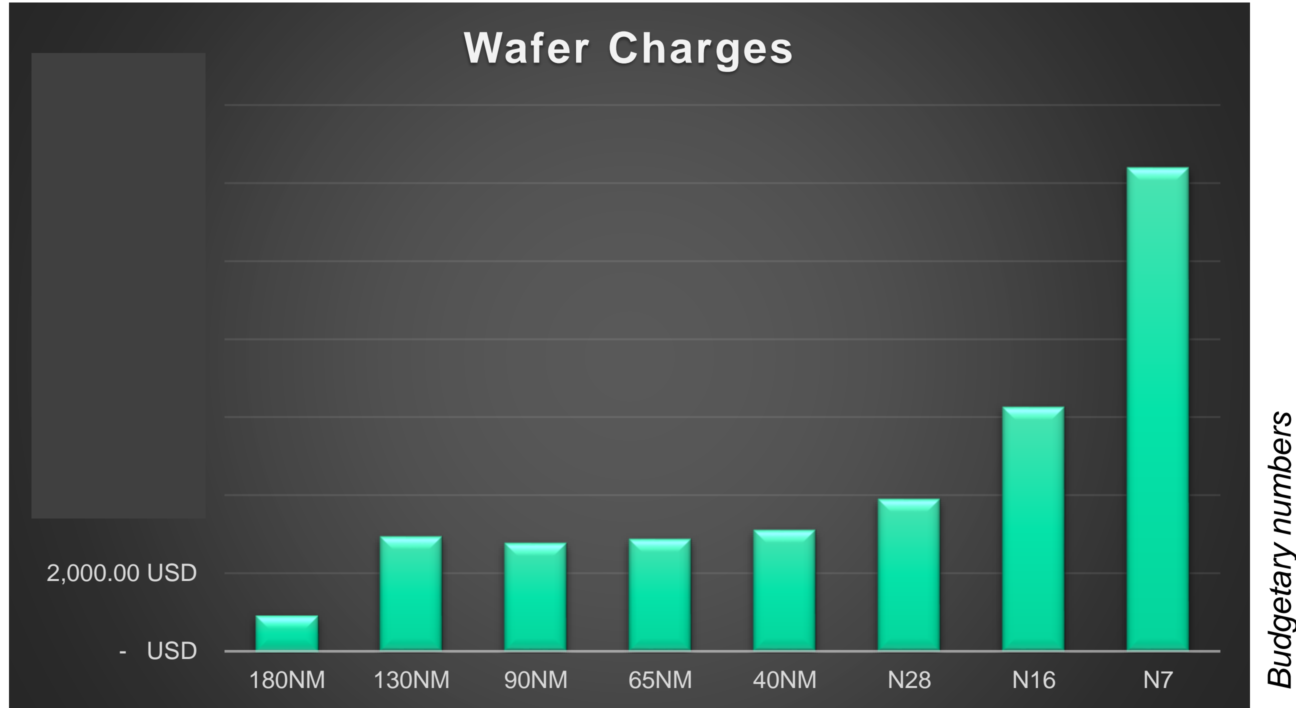

Budgetary numbers

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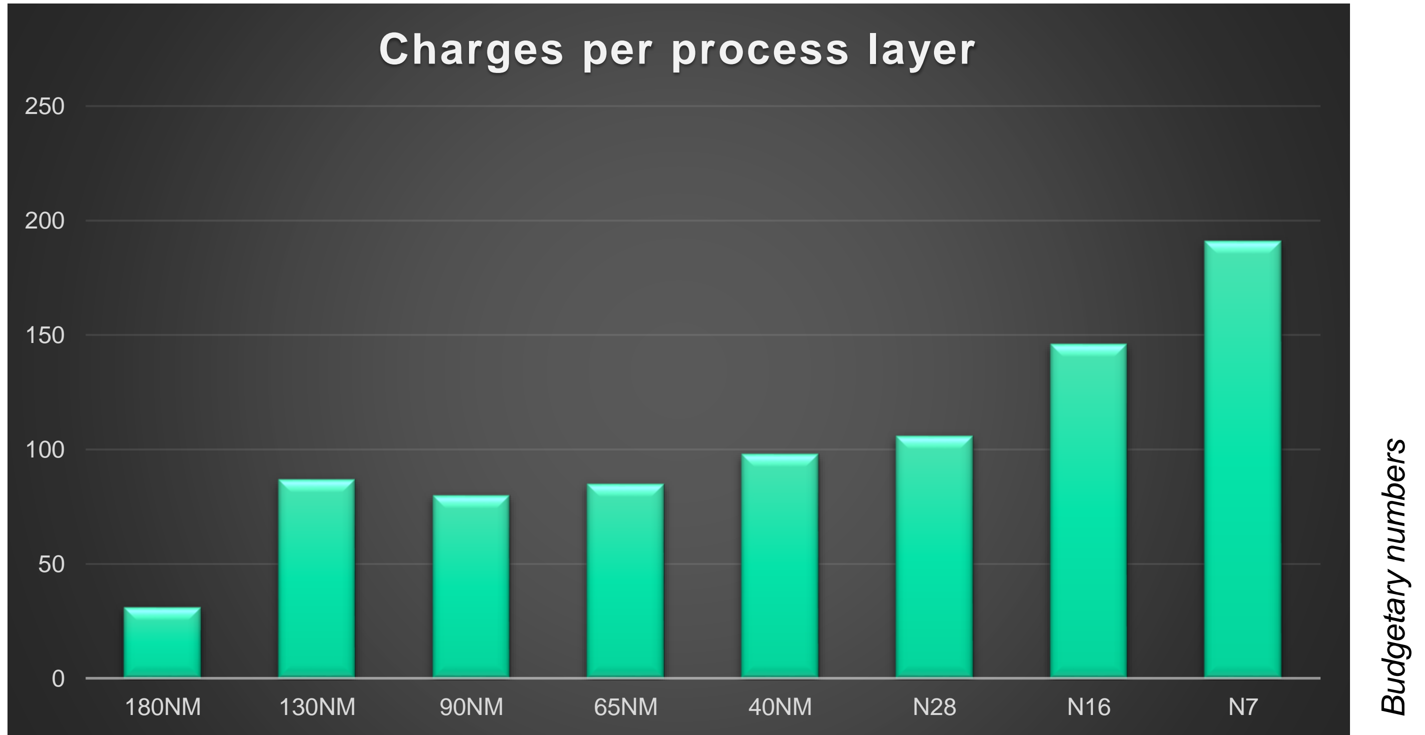

Budgetary numbers

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THE NEXT LEVEL

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MORE than SILICON: New Assembly Techniques

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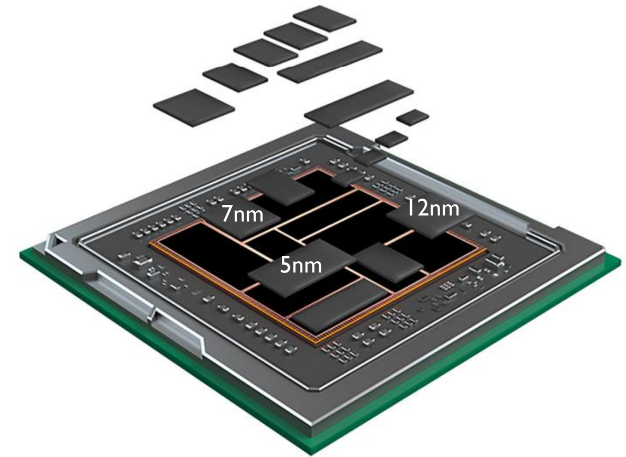
MORE than SILICON: CHIPLETS

- ❑ Different ASIC, Different TEAM
- ❑ Different Semiconductor and foundries combinable
- ❑ Cost optimization
  - ❑ Higher Yield (KGD)
  - ❑ HW Reuse
  - ❑ Dedicated technology for dedicated functions
- ❑ System Flexibility
  - ❑ customized and upgraded easily
- ❑ Reliable - Test coverage
- ❑ Shorter Time to Market - Modularity
- ❑ Performance scaling



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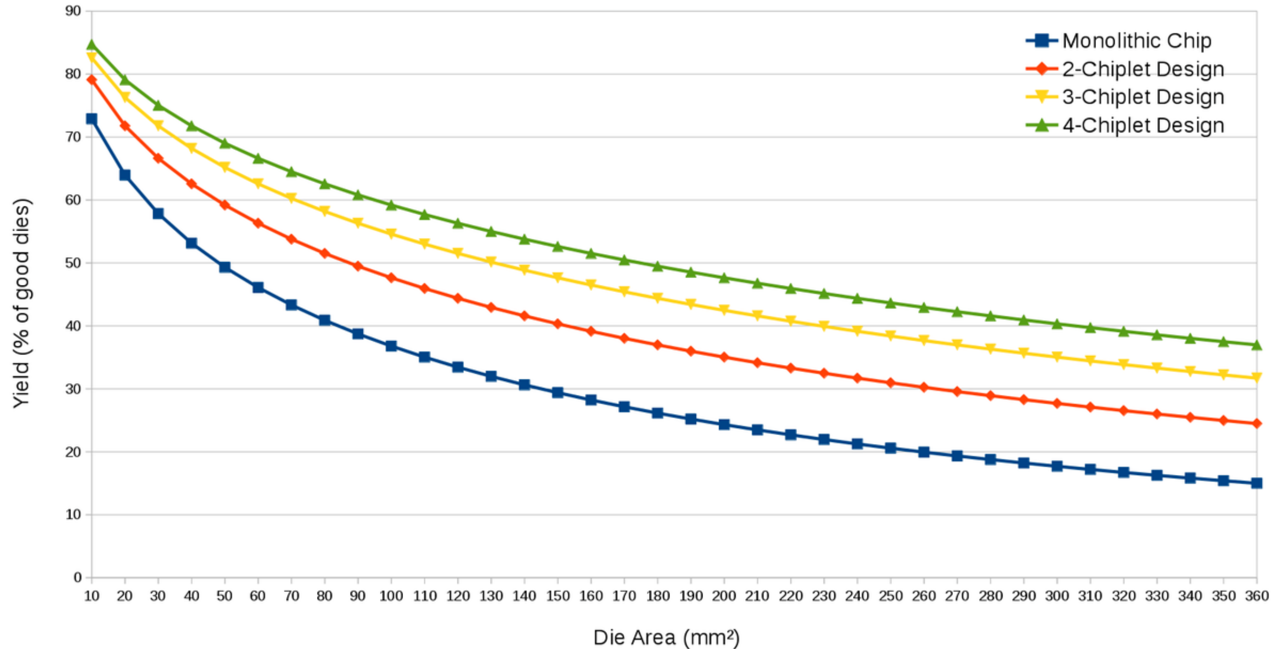
MORE than SILICON: CHIPLETS



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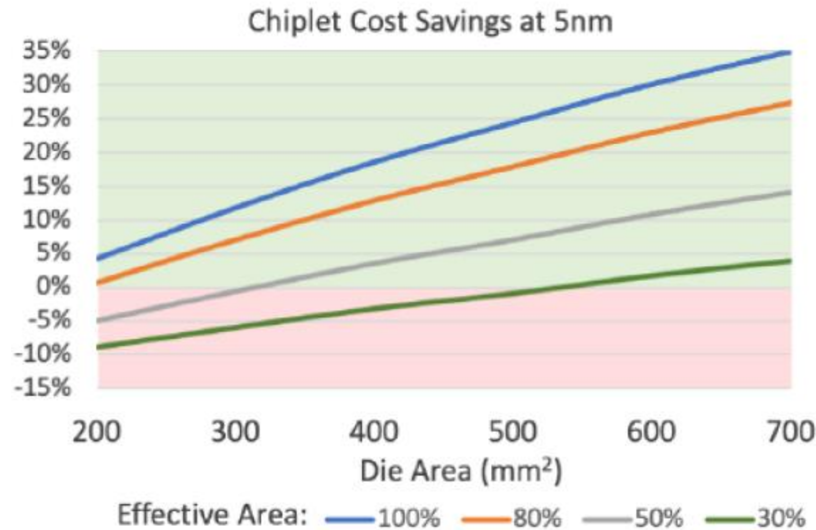
MORE than SILICON: CHIPLETS

The Linley Group
Powered by TechInsights



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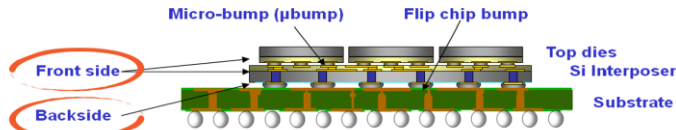
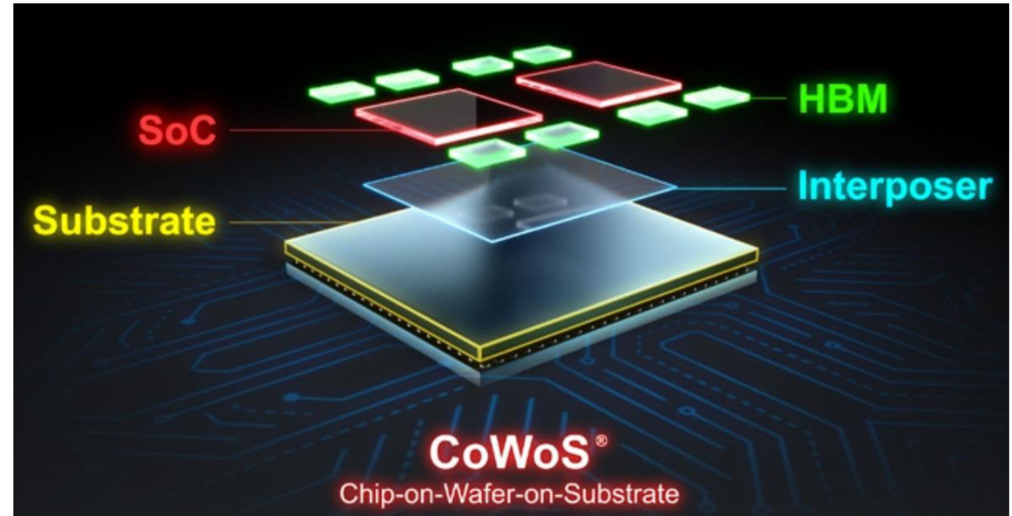
CoWoS (Chip on Wafer on Substrate), *also known as* ***TIS*** *– Through Interposer Stack*

- A 2.5D advanced packaging technology offered by TSMC
- Incorporates multiple dice side-by-side bonded using micro-bumps on a silicon interposer
- Uses TSVs on silicon interposer to connect to package substrate using C4 bumps



Front Side Interconnect – interconnect between top dies (e.g. HBM dies) to the silicon interposer using micro-bumps.

Backside Interconnect – interconnect between the silicon interposer (with TSV) to the flipchip bump and to the package substrate



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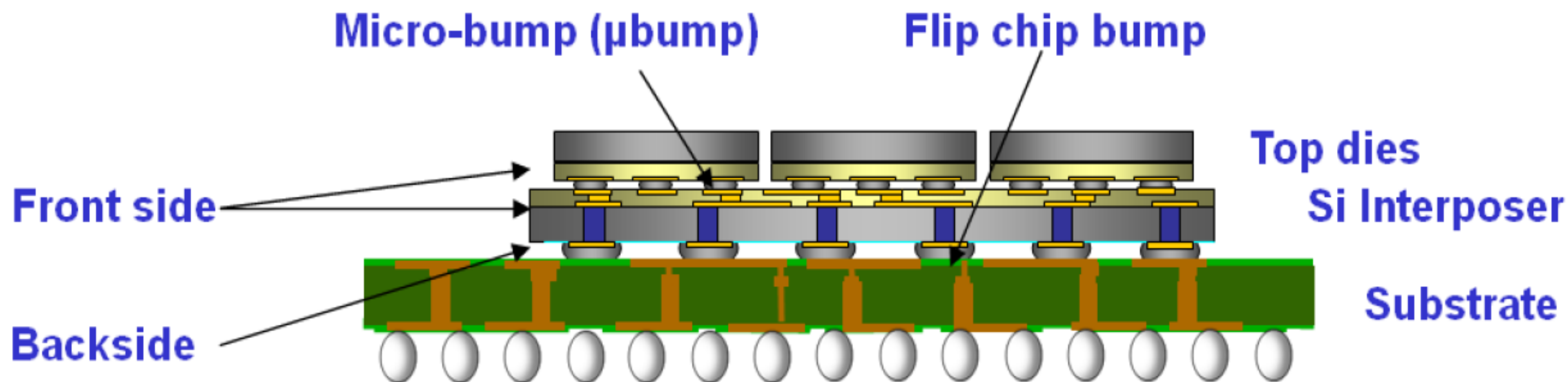
- **CoWoS** (Chip on Wafer on Substrate), *also known as* ***TIS*** *– Through Interposer Stack*



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PHOTONICS

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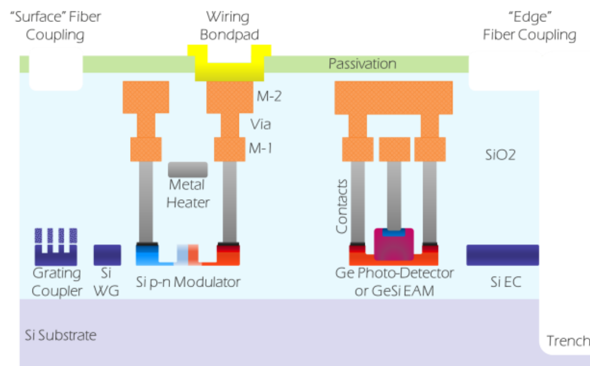
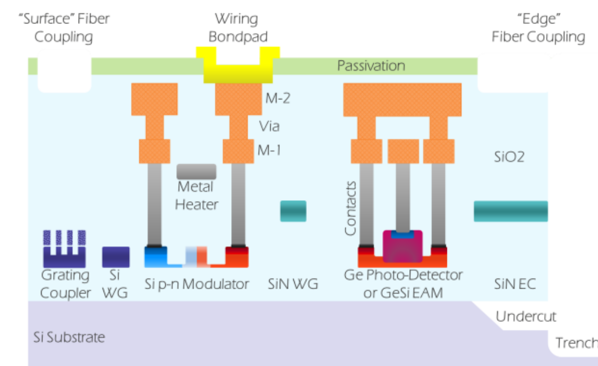
Imec 200mm Silicon Photonics Platform Evolution

iSiPP50G (2014)



iSiPP200 (2020)



- CMOS full compatible flow (130nm)
- Fully integrated photonics platform
  - 1310nm/1550nm wavelength
- Low loss passive waveguide devices
- Low loss fiber coupling structure
- 56Gb/s+ (Ge) Si modulators
- 56Gb/s+ Ge (Si) photodetectors

iSiPP50G features augmented with:

- Undercut → Improved thermal efficiency and mode confinement
- PECVD SiN WG and edge coupler or SiON edge coupler

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Imec 200mm Silicon Photonics Platform Evolution

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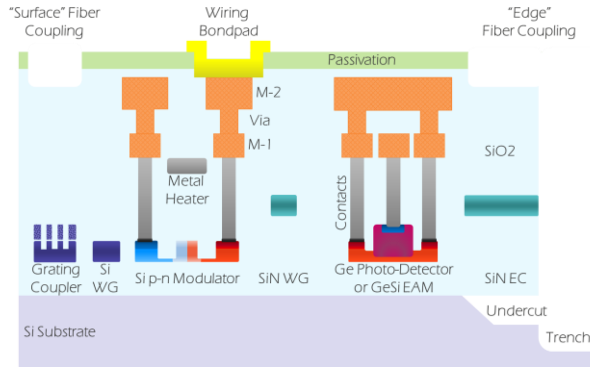
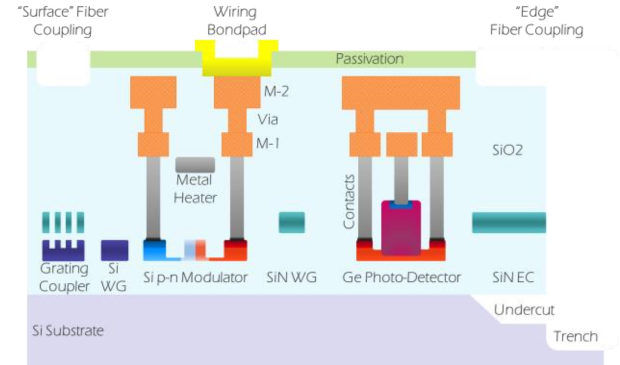
iSiPP200 (2020)



iSiPP50G features augmented with:

- Undercut → Improved thermal efficiency and mode confinement
- PECVD SiN WG and edge coupler <u>or</u> SiON edge coupler

iSiPP200N (2023)



iSiPP200 features augmented with:

- LPCVD SiN low loss WG
- LPCVD SiN CWDM
- **LPCVD edge coupler**

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CONCLUSIONS – The REALITY

- **MORE ADVANCED TECHNOLOGIES ARE IN REACH**

- **ASSEMBLY PROCESSES BECOMING functional part of the component**
  - **Performance, Economics, Form Factor, Security of IP**

- **NRE's will become even more dominant for smaller projects**

- **CO-DESIGN and VERIFICATION becoming more important**
  - **New Tool flows**
  - **New Skillsets**

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QUESTIONS

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