

# Availability and access to modern EDA tools and IP block sharing in HEP community via the EUROPRACTICE services

DRDT7.7 Tools and Technologies 15<sup>th</sup> March 2023



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# Europractice

- Europractice is currently funded until 2025
- Europractice is more well regarded today than at any point in the last ten years
- I hope for an “easy” renewal
  
- Europractice can never be the total solution



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# RISC-V

- **We are currently fairly well placed**
  - ▶ **Some debug tools**
  - ▶ **Using RISC-V as an IP integration example in courses**
  
- **Processors mean programs, which run slowly in simulation**
  - ▶ **Emulators? E.g. Protium, Palladium, HAPS**
  - ▶ **FPGA prototyping**



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# System Integration 2.5D/3D etc

- This is all going to be very difficult
- Different approaches from vendors
  - ▶ Cadence versus Synopsys
- Design tools not there yet (as a full flow)
- Places a greater load on verification



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# Photonic ICs

- **Design tool flows are maturing**
  - ▶ Still feels like old IC flows
  - ▶ Synopsys currently leading
- **There are currently lots of PIC processes**
  - ▶ Not many scale to volume
  - ▶ Rationalisation is already taking place
  - ▶ PDKs are variable
- **It is an area in a state of flux**
  - ▶ In three years it will be something
    - Maybe not what we want



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# IP Exchange

- CERN already has the right to exchange some TSMC layout between collaborating institutes
- We (Europractice) expect to introduce a much easier way to get EDA vendor approval for design sharing
  - ▶ Hope to make it as easy as just requesting access to a particular piece of IP
  - ▶ CERN is the ideal test case
- Legal requirements are well understood
  - ▶ Mechanics of implementation are a challenge
- This is perhaps the most important task of this phase of Europractice
- Chiplets
  - ▶ Chiplet bank



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# Cloud

- **Cloud use is presently forbidden by EUA**
- **We have a Cadence cloud offer (not widely publicised)**
  - ▶ **All bundles\***
  - ▶ **Central license server**
  - ▶ **Cloud formation templates**
  - ▶ **Machine images**
  - ▶ **An easy launcher based on SOCA**
- **We have hopes that other vendors will offer similar soon**
- **PDKs represent a challenge**



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# Scaling

- Each IC will have more transistors, systems will have multiple IC's
- As node sizes decrease, number of design rules also rise
- DRC and verification are getting more demanding
- The solution is parallel algorithms
  - ▶ More cores
  - ▶ More licenses
- Possible solutions
  - ▶ 1. The market will adapt
  - ▶ 2. Booster packs of some licenses
  - ▶ 3. Spot licenses
- Also, emulators?



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# The rest

- Open source tools
- Open source pdks
- Device modelling and cryogenic CMOS
  - ▶ QuantumATK ->TCAD ->SPICE actually works
- Export restrictions
  - ▶ So far tools can be restored on request
  - ▶ So far no deemed export issues
- Does the way we use design tools need to change?
  - ▶ The Vitis FPGA flow
  - ▶ “ML”



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