Implementing DRD7:

An R&D Collaboration on Electronics and On-detector Processing

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4D for trackers challenges: an overview

Adriano Lai,

INFN Cagliari

4D for tracking: main concepts and requirements

1. In our sense, 4D-tracking concerns inner tracking (vertex detection) and consists in adding the temporal coordinate in single hit detection by means of a "precise time measurement" (**typically $\sigma_t < 50$ ps per hit required**)

2. 4D tracking comes along with **high intensity** (high density of events in space and time). This implies a number of **strictly associated requirements**:
    - Small pixel pitch ($\sigma_s \approx 10$ μm)
    - High fluence and dose ($\Phi > 10^{16}$ n_{eq}/cm^2, TID > 1 Grad)
    - High data bandwidth, due to increase in the amount of information at the pixel level and event rates (≈ N x 100 Gbps/ASIC)

3. **Remark:** in general, the **increase in functionality** and complexity should be implemented **without a corresponding increase** in space and power budget (!)

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   ← Silicon Photonics

3. **Remark:** in general, the **increase in functionality** and complexity should be implemented **without a corresponding increase** in size and power budget (!)

Main (preliminary) requirements in next-generation (4D)trackers

Requirement	LHCbU2 Run5 (Scenario A)	LHCbU2 Run5 (Scenario B)	NA62++ (HIKE)	CMSPPS/ run4(5)	CMS run5 forward	FCC–hh (VERY preliminary)
Pixel pitch [μm]	55	42	≤300	50-100	≈100	10
Hit time resolution RMS [ps] (electronics stage)	30	30	30	30	30	< 20
NIEL lifetime for sensors [n/cm^2]	6 x 10^{16}	8 x 10^{15}	n x 10^{16}	10^{16}	n x 10^{15}	10^{18}
TID lifetime for electronics [Grad]	2.4	0.3	2	1	0.05	x10 ?
Power budget [W/cm^2]	1.5	1.5	≈ 4.5	1-2	1	TBD
Power per pixel [μW]	25	14	300	25-50	100	TBD
Hit rate [GHz/cm^2]	12 (max)	2.5	10	6	6	30
Data BW [Gbps/ASIC]	250	94	10-20	100	10	x10 ?
Material budget (per station)	<0.8% X_0	<0.8% X_0	<0.5% X_0	< 1	1	x 0.3
Trigger scheme/peculiarities	triggerless	triggerless	Tbd (triggerless?)	Tbd (triggered?)	triggered, serial pwr	TBD

Further upcoming interests on 4D tracking (with similar specs): high intensity/ rare effects (e.g. PIONEER proposal @PSI, π rare decays), neutrino tagging techniques in LBL experiments, Muon colliders (background rejection).

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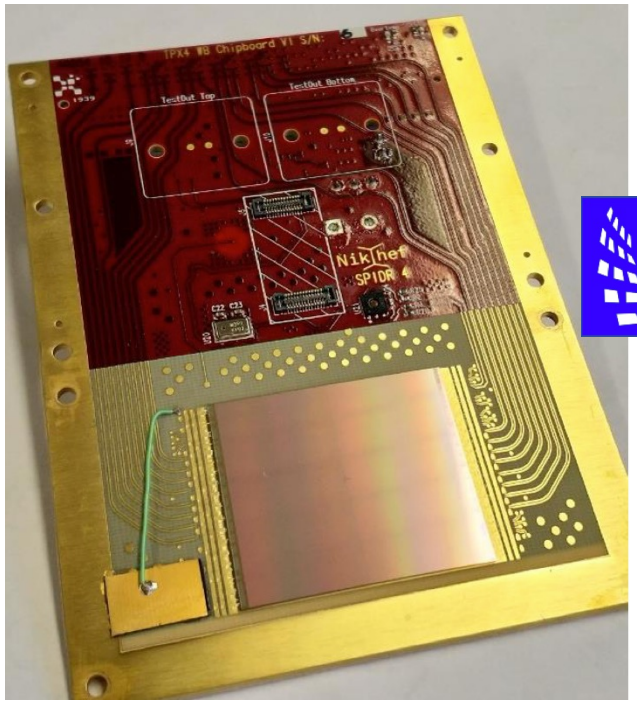
Present experiences in 4D-tracking (ASICs)

kind of starting points, towards the full specs of the previous table



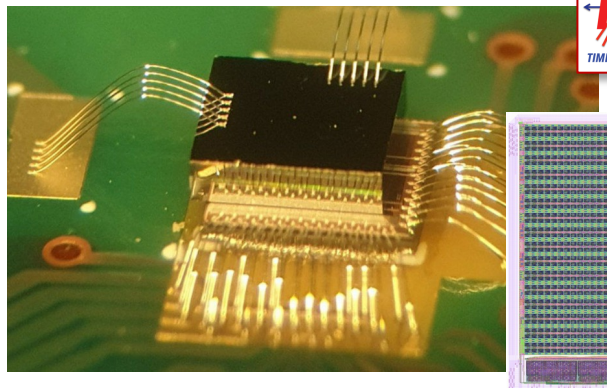
medipix collaboration

Timepix4 ("mature" device)

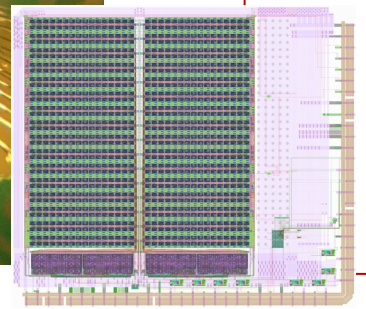
- CMOS 65nm – 10 metal
- 512x448 pixels 55 µm pitch
- 10.8 kHz/pixel
- TDC bin size: 195 ps
- Analog FE (AFE) σ_t:
  - ≈ 60 ps (10ke pulse – no sensor)
  - ≈ 80 ps (10ke pulse – sensor)
- SEU protection: no

PicoPix (R&D, demo)

- under definition
- **CMOS 28-nm** 64x64
- Pitch ≈ 45 µm
- σ_t ≈ 20-30 ps
- Similar architecture and clock distribution strategy as Timepix4
- TSV use



TimeSPOT — TIME and SPace real-time Operating Tracker



Timespot1 (R&D ASIC)

- CMOS 28nm – 8 metal
- 32x32 pixels 55 µm pitch
- 200 kHz/pixel (limited by data BW)
- TDC bin size: 50 ps
- AFE avg. σ_t:
  - 20-80 ps (10ke pulse – no sensor)
  - 30-100 ps (10ke pulse – sensor)
- Power:
  - 10 µW (AFE)
  - 40 µW (TDC) @ 350 kHz (LHCbU2 input rate)
- SEU protection: no

IGNITE1 (R&D, demo)

- under definition
- **CMOS 28-nm** 64x64
- pitch TBD
- σ_t ≈ 20 ps
- New architecture and new clock distribution strategy
- TSV use

Main issues encountered

And technical challenges in 28nm

Learning from first experiences in CMOS-28 nm design for timing (TimeSPOT ASIC):

A. Implementing a **pixel** circuit having the required specifications **is tough but reacheable:**
   1. F/E consumption kept around 10 µW/pixel (@12ke and 100 fF)
   2. TDC consumption scales with rate (Vernier architecture). Consumption < 40 µW @350 kHz, with margin of reduction.

→ Dedicated developments on **cooling techniques** can be very beneficial at the system level!

B. Most issues are at **global level** and concern global lines:
   1. Clock stability and jitter, requires very accurate **clock distribution** (see the Timepix4 DLL technique) and local filtering (use of diffused PLL)
   2. Important **IR drop** and reduced voltage headroom in this technology can heavily compromise a good performance at the pixel level: power distribution is very critical

The use of 3D interconnection (TSV) becomes not preferred/useful, but mandatory for high performance 4D-tracking. The access to this technique is diffused at the industrial level bur still young and limited in our community (see FEI4 and Timepix4). Access is still complicated and expensive…

(more than) Expressions of interests

*A starting, **largely incomplete** list*

At different level of interest, involvement and activity, many institutes have joined/ are willing to join the 4D-tracking challenge on the electronics side:

1. **INFN** Sezioni Bari, Bologna, Cagliari, Milano, Milano Bicocca, Padova, Pisa, Pavia, Torino
   → **IGNITE initiative on high rate tracking**
2. **CERN, NIKHEF, IGFAE Santiago**
   → **PicoPix developments for LHCb**
3. **PSI, Fermilab** → **Interest in CMS Endcap MTD extension (η>3) development**
4. **Bristol** → **developments on precision timing ditribution techniques in DUNE**
5. **SLAC** → **TDC design in CMOS 28-nm**
6. **…**

Please make a step forward if not listed and willing to be…

Is cooordination/collaboration possible? and how?

Some final comments…

1. **4D techniques are crucial** in the inner trackers of the next generation of upgrades

2. Many issues in 4D-tracking are system related on a fundamental basis
   - **3D-High-Density-Interconnnect** for coping with data density and accurate distribution of global lines
   - Developments on **cooling techniques** to allow higher power budget while minimizing material budget
   - **Silicon Photonics**
   - …

3. Is the separation in development themes DRDT*n* (always) an effective approach? How do they communicate at the decisional level?