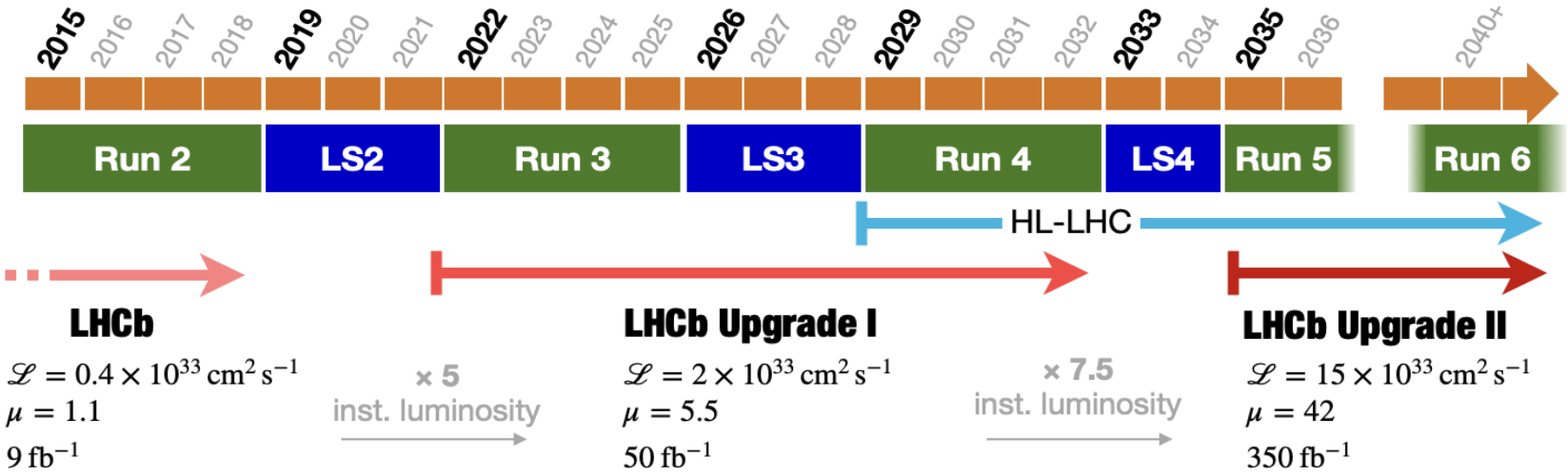
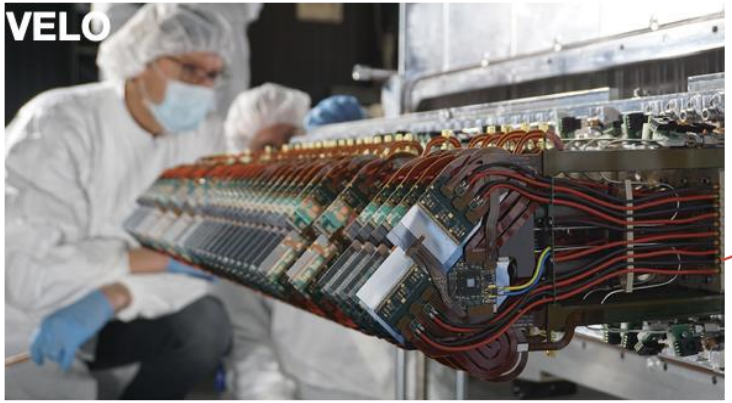
4D tracking challenges for the LHCb VELO Upgrade

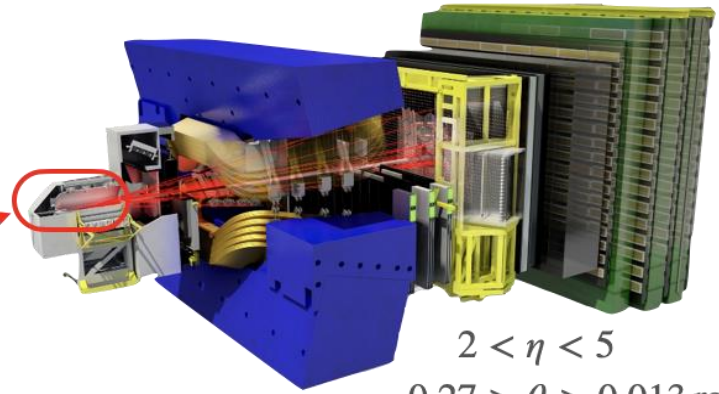
DRD7 implementation workshop
14 & 15 March 2023

Martin van Beuzekom
Nikhef

LHCb timeline



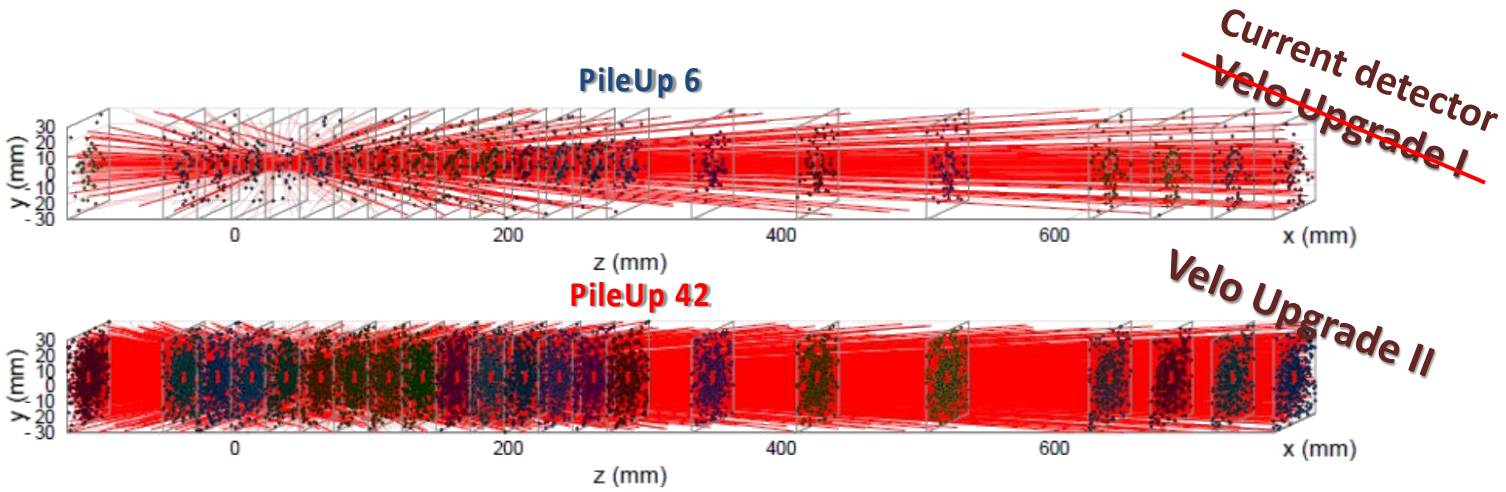




$2 < \eta < 5$

$0.27 > \theta > 0.013\,\mathrm{rad}$

Higher luminosity: PileUp challenge

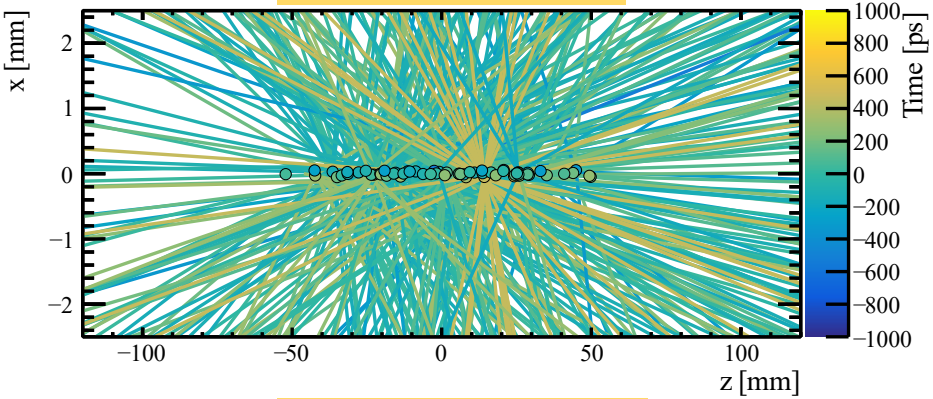


- Lower triggering efficiency (online reconstruction, software trigger)
- Higher combinatorial background and ghost rate
- Much more computing power for reconstruction

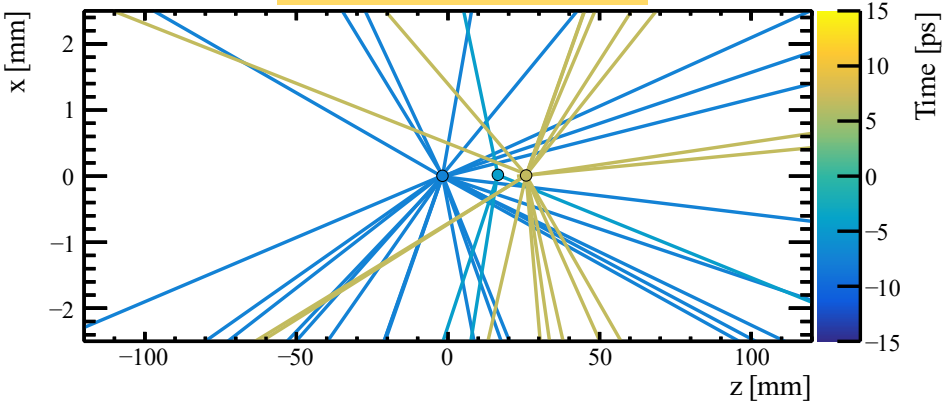
Requirement for upgrade II: keep same performance

Solution: add timing -> 4D tracking

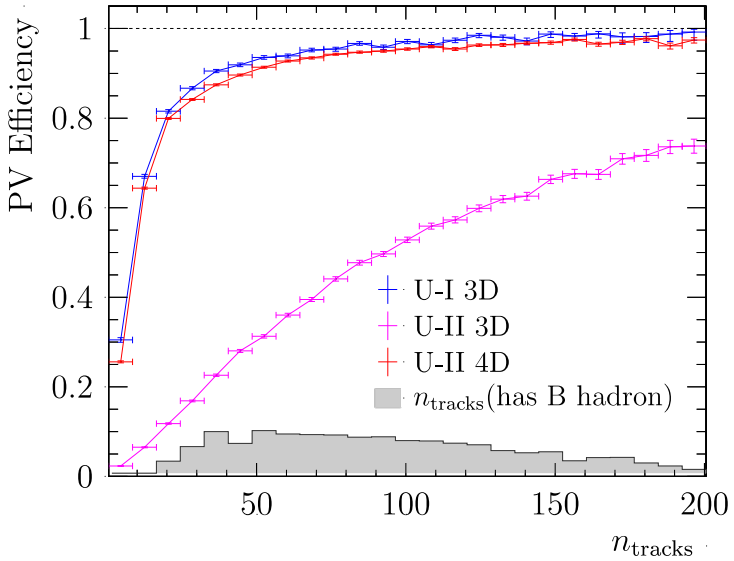
2 ns time window



30 ps time window

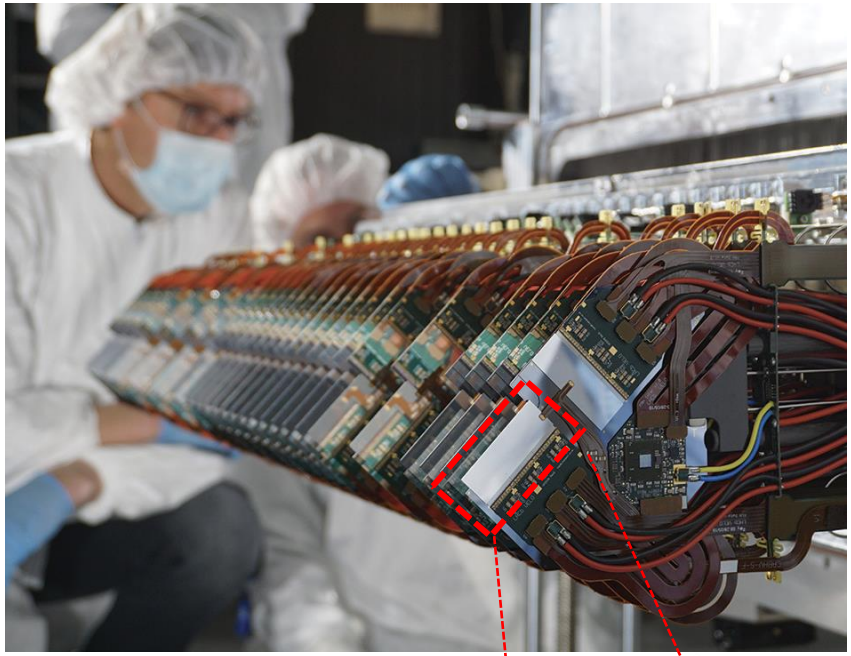


Courtesy: R. Geertsema

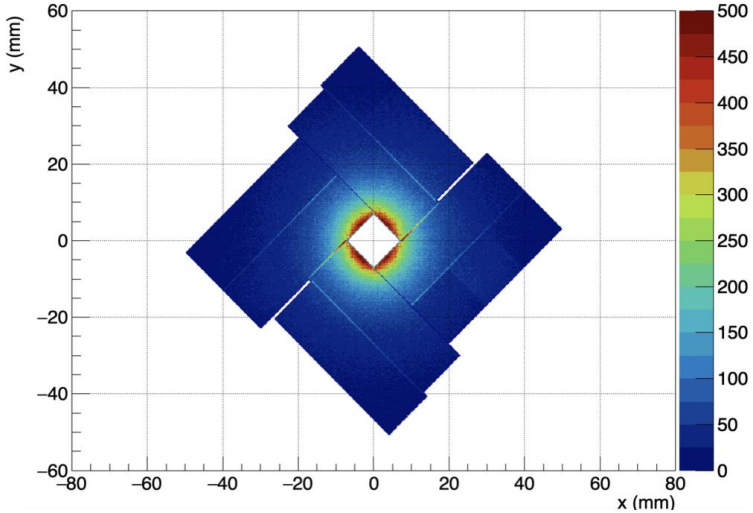


- Timing regains detector performance
- Need 20 ps track time resolution
- Hence 50 ps hit-time resolution
- 4D tracking is beneficial for track reconstruction

Starting point: current VELO



Sensor + 3 ASICs

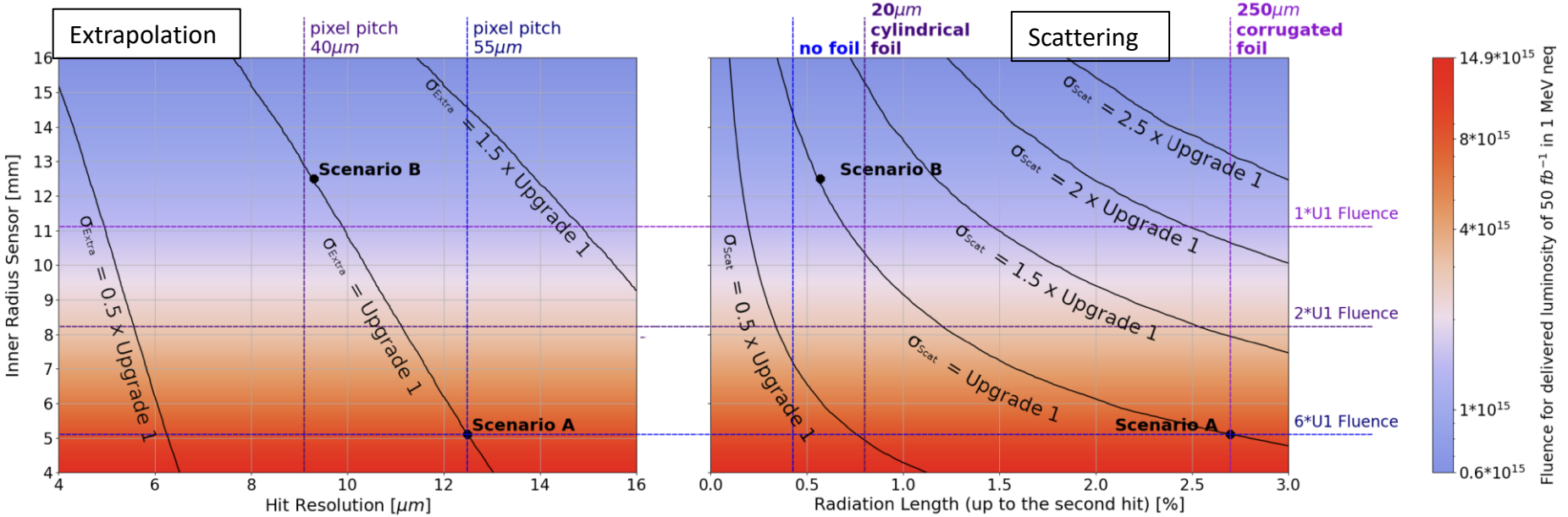


- Planar silicon pixels, 55 μm pitch
- Binary readout with VeloPix
  - 256 x 256 pixels, 2 cm^2 per ASIC
  - Data driven
- Planes perpendicular to beam
  - 5.1 mm distance
- Highly non-uniform track density
  - Factor 40-100 across sensor

Distance to the beam is a key parameter

$$\sigma_{IP} = \sigma_{extra} \oplus \frac{\sigma_{scat}}{p_T}$$

Define two ‘extreme’ scenarios to guide R&D



Scenario A (location of current detector):

- 5.1 mm from beam
- 55 μm pixels
- TID 2.5 Grad, 5×10^{16} 1 MeV n_{eq} cm^{-1}
- >250 Gbps data rate (2 cm^2)

Scenario B:

- 12.5 mm from beam
- 42 μm pixels
- 5x smaller material budget
- > 94 Gpbs data rate (2 cm^2)

Find the optimal configuration

physicists

engineers

- Smaller pixels
- Faster timing
- Thinner sensors (less signal)
- Less material
- Lower power

- Larger pixels (more area per pixel)
- Large signals
- Low pixel capacitance
- Generous power budget

Time resolution

Requirement:

- track time resolution 20 ps -> hit time resolution 50 ps
  - n.b. with resolution the RMS value is meant, not bin size

$$\sigma^2_{hit} = \sigma^2_{sensor} + \sigma^2_{ASIC} + \sigma^2_{clock\text{-}system}$$ 50 ps

$$\sigma^2_{front\text{-}end} + \sigma^2_{TDC} + \sigma^2_{on\text{-}chip\text{-}clock}$$ 30 ps

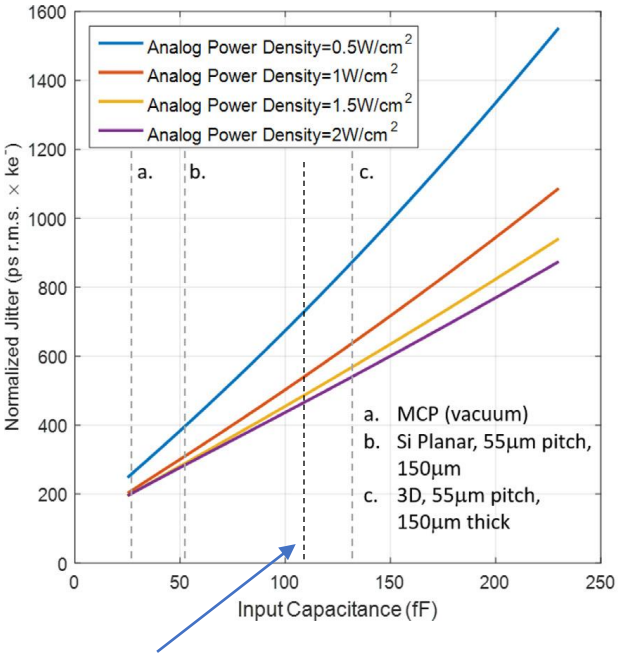
~25 ps ~10 ps (40 ps bins) ~10 ps[(a)]

(a) N. Egidos et al., **DOI:** 10.1109/TNS.2021.3057581

How to get good time resolution

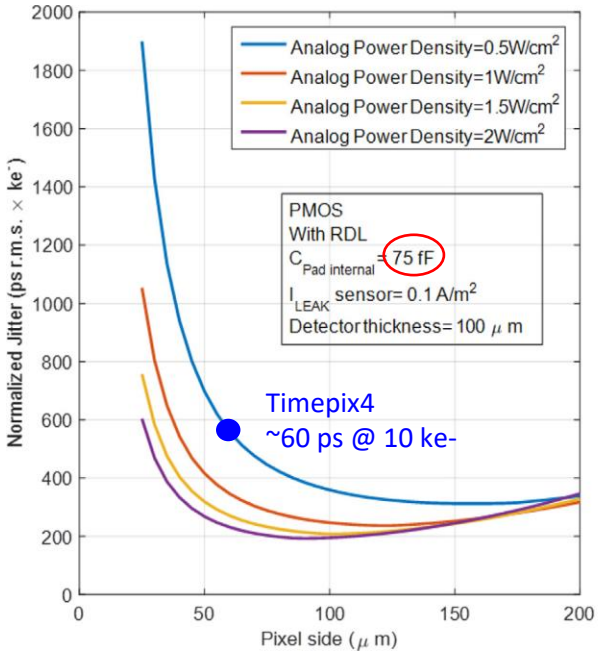
Maximise dV/dt at amplifier output to minimize jitter

$$\frac{dv_{out}(t)}{dt} = \frac{Q_{in} g_m}{C_O(C_{IN} + C_{FB})} \frac{\frac{Q_{in}}{C_{FB}} - V_{th}}{\frac{Q_{in}}{C_{FB}}}$$



3D trench 110 fF

DOI 10.1088/1748-0221/15/09/P09029

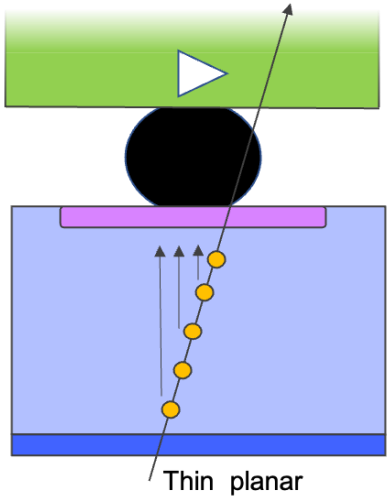


Best time resolution with:

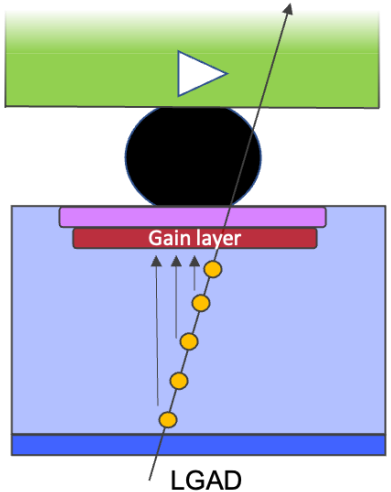
- Large signal Q_{in} (large current)
- Low capacitance C (all caps)
- Large power P (large g_m)

R. Ballabriga et al.
https://doi.org/10.1016/j.nima.2022.167489

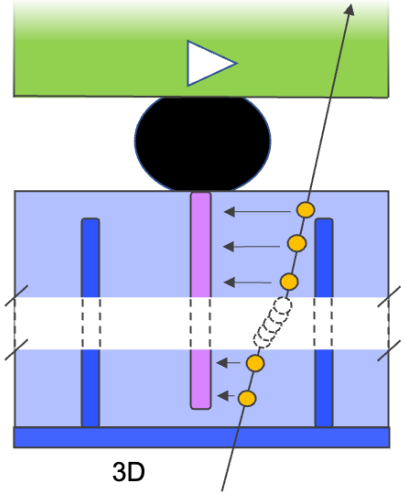
Sensors = DRD3 (current state, improvements ongoing)



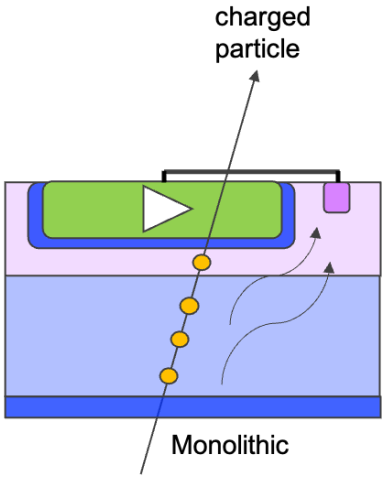
- Small signal, if thin
- Medium capacitance
- Reasonably rad. hard
- Low material



- Large signal (gain)
- Good time resolution
- Medium capacitance
- Modest rad. hard
- Non-uniform rad. profile



- Large signal
- Good time resolution
- Rad. Hard
- High capacitance
- More material



- Small signal
- Very low capacitance
- Low material
- Modest rad. hard
- Modest time resolution

Table of specifications for VeloPix2

Requirement	scenario S_A	scenario S_B
Pixel pitch [µm]	≤55	≤42
Matrix size	256×256	335×335
Time resolution RMS [ps]	≤ 30	≤ 30
Loss of hits [%]	≤ 1	≤ 1
TID lifetime [MGy]	> 24	> 3
ToT resolution/range [bits]	6	8
Max latency, BXID range [bits]	9	9
Power budget [W/cm^2]	1.5	1.5
Power per pixel [µW]	23	14
Threshold level [e$^-$]	≤ 500	≤ 500
Pixel rate hottest pixel [kHz]	> 350	> 40
Max discharge time [ns]	< 29	< 250
Bandwidth per ASIC of 2 cm^2 [Gb/s]	> 250	> 94

Priority

Challenging!

doable

More detailed information: LHCb-PUB 2022-001 (https://inspirehep.net/literature/2020914)

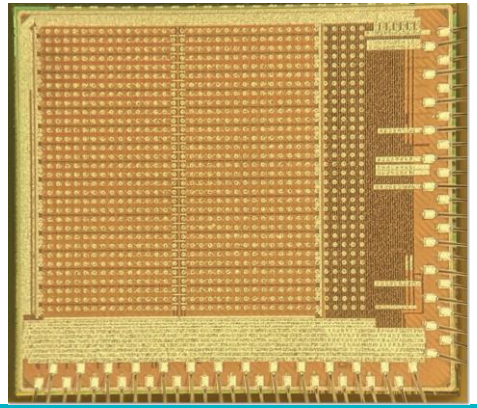
Towards VeloPix2: ongoing ASIC developments

A. Lai
X. Llopart

- Two parallel developments in R&D ('exploration') phase
  - Target same specs, both using 28 nm CMOS
  - Gain experience with technology

TimeSPOT -> IGNITE (12 INFN sites)

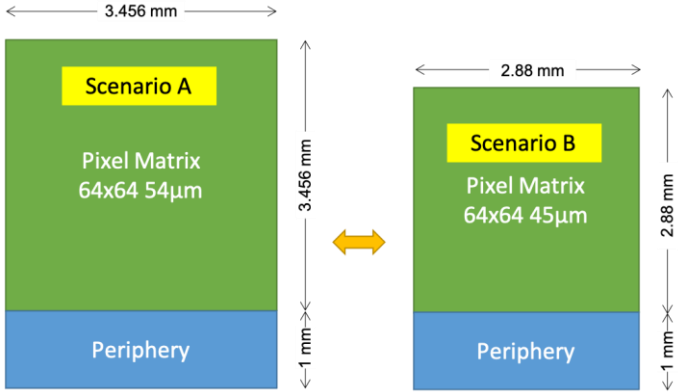
- Timespot0 (single cells)
- Timespot1 (full func., 32x32 pixels, 55 μm)
- Exists and tested: 'real life' experience
- Further developed within IGNITE project



Timespot1

PicoPix (CERN, Nikhef, IGFAE)

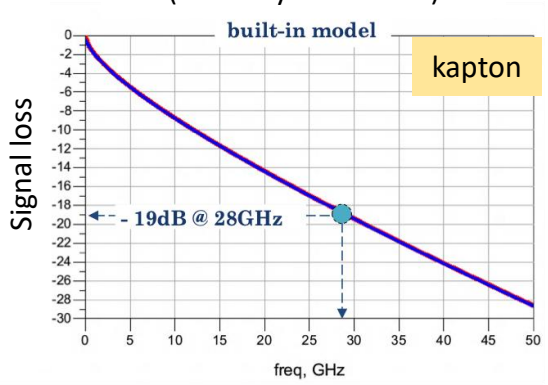
- Experience from Timepix4/VeloPix
- Fully func. 64x64 pixel demonstrator
- 2 pixel sizes: 55 and 45 μm
- Expected submission mid 2024

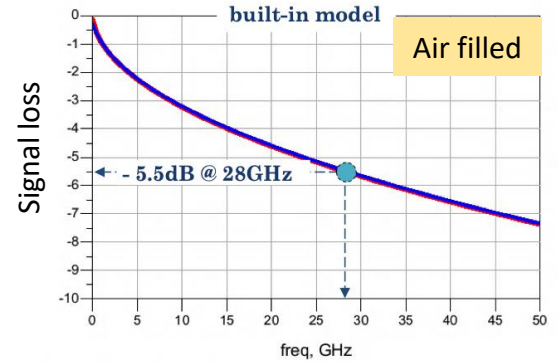


Data transmission challenge (not only LHCb/VELO)

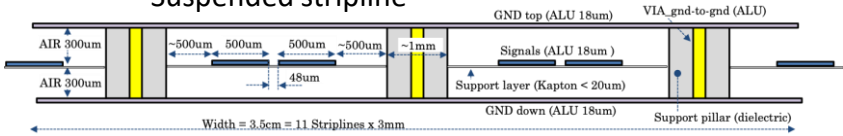
- 25+ Gbps low power links are essential
  - Data BW > 100 Gbps/chip
  - Clock cleaning / stability
- Data transmission path is as important as driver
- Either 50-70 cm over copper (kapton, vacuum)
- Or do we dare to put electro/optical in vacuum?
  - ~150 Mrad / ~3x10^{15} n_{eq} at 20 mm (next to ASIC)
  - TID < 10 Mrad at 10 cm
- Multi-level signalling (e.g. PAM4)
  - Complexity might not outweigh the benefits for short cables

Attenuation in 1 m stripline
(courtesy V. Gromov)





Suspended stripline

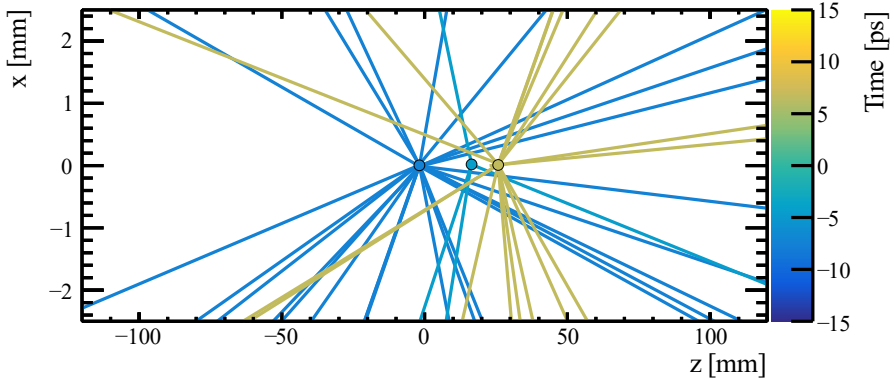


Other challenges that require development

- Voltage (IR) drop
  - System level (cabling): rad. hard regulators near ASIC?
  - ASIC level: TSVs to supply power at multiple points along column?
- Data ordering, sorting, pre-processing in FPGA
  - Sorting in time and in ’phi (azimuthal angle)’ is beneficial for track reconstruction
  - Total VELO bandwidth ~ 30 Tbit/s
- Time calibration of small pixels
  - Need time calibration per pixel, interplay with (conversion) gain variation
  - Need on-chip and in-system functionality to determine calibration parameters
- Not only electronics challenges:
  - Cooling with least amount of material
  - Mechanics, large moveable detector in vacuum
  - Shielding from beam, and guiding of beam mirror currents
  - Not to mention the reconstruction software …

Summary

- The LHCb VELO Upgrade-II will be a fully 4D tracking detector
- Has to cope with L = 1.5 x 10^{34} cm^2s^{-1} at 5 – 12 mm from beam
- Hit time resolution of 50 ps
- Defined two scenarios for R&D
  - A: near beam, 2.4 Grad, >250 Gbps per ASIC
  - B: away from beam, 80% reduction of material, and 42 μm pixels
- Coming 2-3 years are crucial to develop necessary technologies

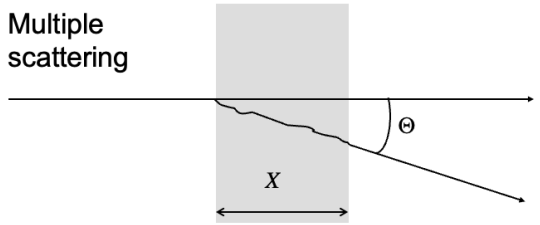


Back up material

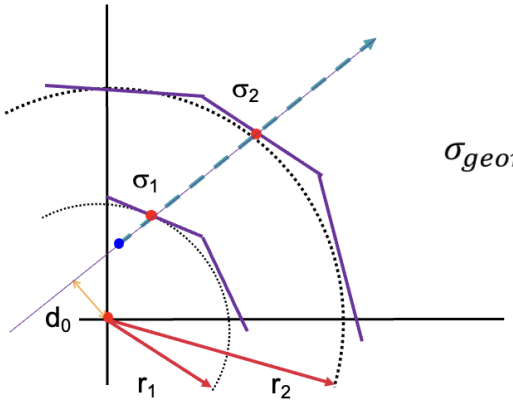
Impact parameter resolution

3 main ingredients:

- intrinsic hit resolution σ_1, σ_2
- Distance to 1st measured point and lever arm
- Multiple scattering in detector material and RF-foil
  - worse at low P_T



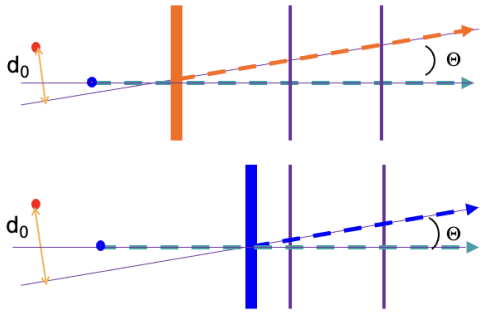
$$\sigma_{MS} = \frac{r}{p} 13.6\,MeV \sqrt{\frac{x}{X_0}} \left[1 + 0.038 \log\left(\frac{x}{X_0}\right)\right]$$



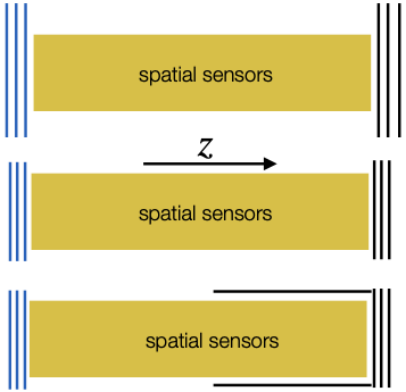
$$\sigma_{geom} = \sqrt{\frac{r_2^2\sigma_1^2 + r_1^2\sigma_2^2}{(r_2 - r_1)^2}}$$

$$\sigma_{d_0}^2 \approx \sigma_{geom}^2 + \left[\frac{r}{p_T} f\left(\frac{x}{X_0}\right)\right]^2$$

location of material is important



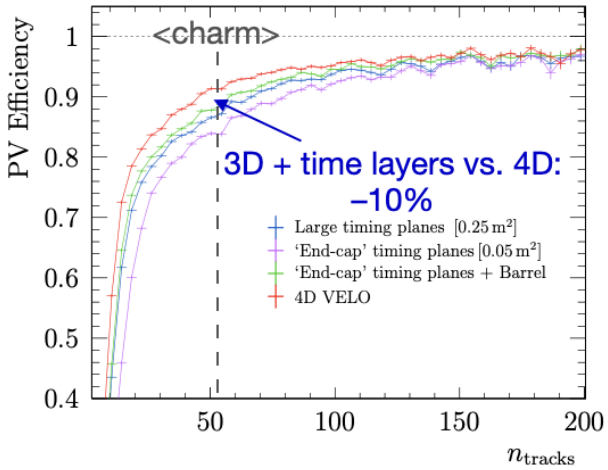
Why not just timing layers?

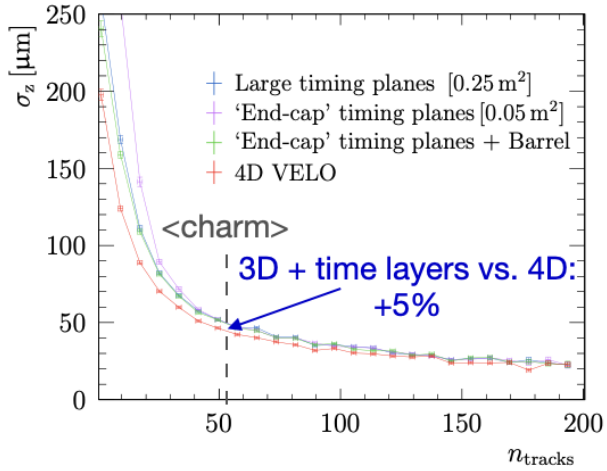


3D VELO + timing layers

- at least 3 layers for efficiency and and combinatorics removal
- larger pitch (100 μm)
- 25 ps per layer
- lower radiation tolerance acceptable
- very large area required compared to VELO ($$$)

	VELO *(à la U1)*	Large endcaps	Endcaps	Endcaps + barrel
Covered range	2 < η < 5	2 < η < 5	2.8 < η < 5	2 < η < 5
Area [m²]	**0.15**	**1**	**0.3**	**1.35**





4D VELO

- 50 ps single-hit resolution
- better performance (efficiency, ghost rate)
- lower cost
  - single sensor technology and ASIC
  - easier event reconstruction

T. Pajero
Pixel 2022