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4D for Calo Challenges: an overview

High performance sampling (TDCs, ADCs)

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Why 4D Calorimetry ?

- In high-pile up environment, use granularity in 4 dimensions (position and time) to be able to distinguish energy deposits from different particles:
  - 3D : limited by detector characteristics (granularity, Moliere radius, …) and the number of channels
  - Time : performances related also to detector (detector response, sensor characteristics – PMT, …), plus effect of the readout electronics
- In addition, energy measurement from charge, which can enter in the clustering algorithm and help further -> 5D techniques
- Not only Calorimetry - several detectors need Time & Amplitude measurements
- Beyond LHC (Higgs factories): no problem with pile-up but need of precise timing for improved 5D particle flow algorithms: distinguish between showers from different jets adding time information
- This short survey is based on (some) developments for LHC experiments, assuming that trends and challenges are common.
- We apologise for not mentioning many other developments…

Calorimetry vs Vertexing/Inner tracking

- Readout ASICs for calorimetry (or PID detectors in general) have some common specs/requirements/challenges with the most inner tracking detectors:
  - Complexity leading to System on Chip (SoC) architecture
  - Request for ultra-low power of readout ASIC (not as low as pixels) – fewer channels but more functionality per channel
  - High speed data links – fewer channels but more bits per channel
- But have a few different specs/requirements/challenges:
  - Amplitude measurement is needed, from a few up to ~15 bits
  - Higher sampling frequency (less granularity, pileup). In fact, do we need somewhere several hundred MSps or more?
  - Channel density is lower – do we really need to use immediately the smallest size technologies?

Fast sampling - State of the Art
Multi-channel ASICs already completed (only <= 130nm considered)

Chip	Experiment /Detector	CMOS nm	No. chan.	ADC Fsamp. / N-bit / power	TDC
SAMPA	ALICE/TPC	130	32	10MHz / 10-bit / 1.5mW	-
PACIFIC	LHCb/SciFi	130	64	40MHz / 2-bit	-
SALT	LHCb/UT	130	128	40MHz / 6-bit / 0.5mW	-

SoC type ASICs including: analog FE, DSP, high speed links, etc…

The first complex multi-channel ASICs with sampling rates up to 40 MSps – LHC collision frequency 40MHz – are already operational or are being installed in LHC experiments. This has become possible thanks to the technology scaling and architecture development, in particular squeezing the ADC power to a level below the power of the analog front-end.

Calorimetry - State of the Art
ASICs under development

Chip	Experiment /Detector	CMOS nm	No. Chan.	ADC Fsample / N-bit / power	TDC
HGCROC	CMS/HGCAL ALICE/FoCal	130	72	40MHz / 10-bit / 0.7mW	Yes, 25ps bin
COLUTA	ATLAS/LArCalo	65	8	40MHz / 15-bit / 140mW	No, 200ps - ns (OFC)
LiTe-DTU	CMS/ECAL	65	2	160MHz / 12-bit / 10mW	No, Clk

Several other projects (e.g. Dominique's talk next) are in less advanced stage ...

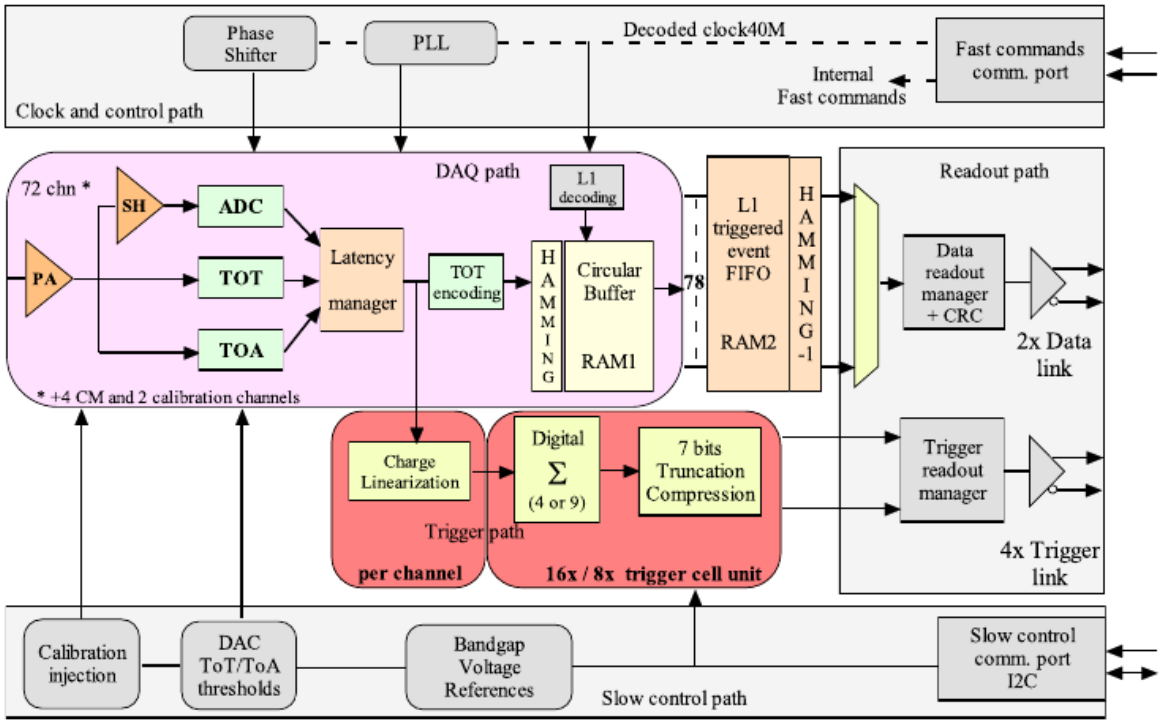
Where are we going (what sampling scheme) ?

- Fast ADC&TDC in each channel
- Fast high-precision ADC and time measurement from pulse shape
- Very fast ADC and time inferred from samples

Other considerations:

- SoC ASIC (HGCROC) vs FE&ADC ASICs (COLUTA, LiTe-DTU)
- Usage of commercial blocks (ADC in LiTe-DTU)
- CMOS 65nm, 130nm preferred

HGCROC for CMS Phase-2 Upgrade
Example of SoC readout ASIC



- CMOS 130nm
- 72 channels
- Sampling 40 MHz
- Time measurement
  - 10-bit TDC 25ps bin
- Amplitude measurement
  - 10-bit SAR ADC (linear range)
  - ToT 12-bit TDC 50ps bin (saturation)
- High speed links 1.28Gbps
- Power <15mW/channel
  - FE ~5.5mW
  - 10-bit 40MSps ADC ~0.7mW
  - 12-bit ToT TDC ~0.5mW@10%
  - 10-bit ToA TDC ~0.5mW@10%

Figure 1. HGCROC3 block diagram with 72 regular channels divided in two paths: data acquisition with memorisation (DAQ) and trigger path.

Project started ~2016, ASIC production 2023-2025, Data taking ~2029

Complex project starting now will have its application in >10 years...

Timing Detectors - State of the Art ASICs under development

Chip	Experiment /Detector	CMOS nm	No. Chan.	TDC / Total power per channel
TOFHIR	CMS/BTL	130	32	TAC+ADC10-bit40MHz, 20ps bin (~30ps) / ~17mW TOT amplitude measurement
ETROC	CMS/ETL	65	16x16	TOA+TOT, ~20ps bin (<50ps) / ~3mW
FastRICH	LHCb/RICH	65	16	CFD, 25ps bin (30-40ps) / ~6mW
ALTIROC	ATLAS/HGTD	130	15x15	TOA+TOT, 20ps bin (~35ps) / ~5mW TDC ~0.5mW@10% occupancy

NOT to be compared! – numbers very approximate, different operation scenarios – only to show order of magnitude

- Different techniques - CFD, TOA+TOT, TAC+ADC - are used for precise time measurement
- Time precision is strongly affected by sensor contribution
- CMOS 65nm or 130nm preferred

Technology considerations

- Accessible to the community, RadHard, TSMC-CERN-Institutes agreement simplifing common projects
  - CMOS: 130nm, 65nm, 28nm, other ?
- Fulfilling detector requirements
  - For Calorimetry&PID all 130/65/28 nm can be considered
- Development time of complex SoC ASIC takes 5-10 years → long term availability&support is crucial
  - CMOS (130nm?) , 65nm, 28nm

For LHCb Upgrade II different groups working for ECAL, SciFi, RICH, TORCH, MagnetStation, decided to use CMOS 65nm...

Key challenges

- Ultra-low power TDCs&ADCs crucial for high performance sampling
- TDC - requested specs: <10ps resolution and <1mW power
- Sampling&ADCs – various desired schemes&specs possible
  - Trade-off between resolution & sampling frequency & power
  - ADC with 50-100 MSps rate, 12-bit resolution, ~1mW consumption, can be done in CMOS 65nm (see top JSSC papers)
  - Sampling rate can be traded for resolution
- What is / will be possible to do ?
  - Top papers on TDCs, ADCs, designed in similar technologies, published in journals such as JSSC, are the best guide to follow
  - Large power savings possible with multi-channel ASIC activating ADCs, TDCs only when needed

There is NO readout ASIC without low-power low-noise analog front-end!

Thank you for attention