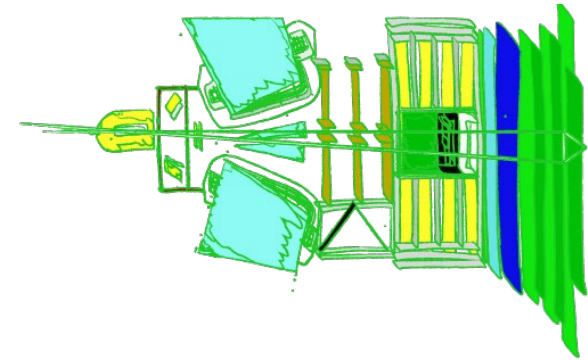


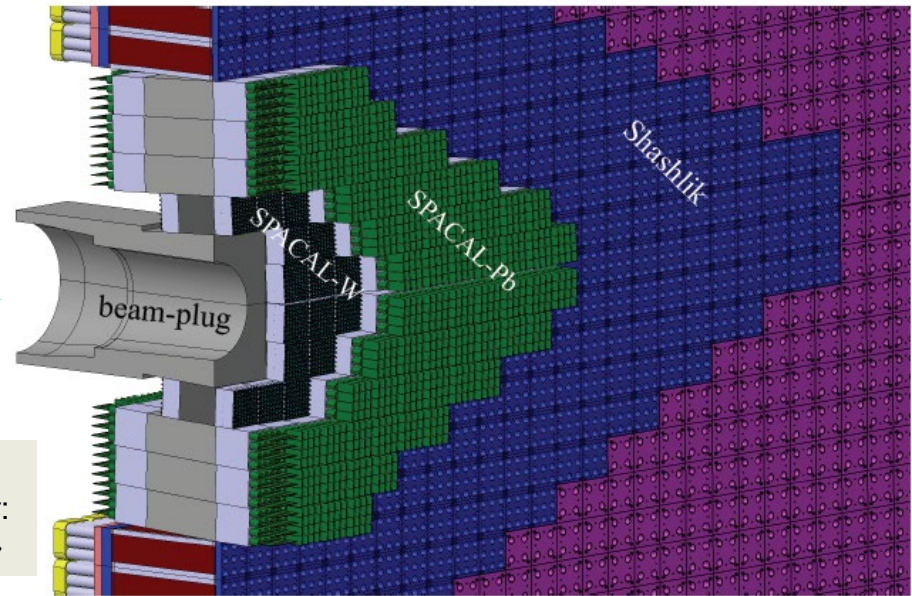
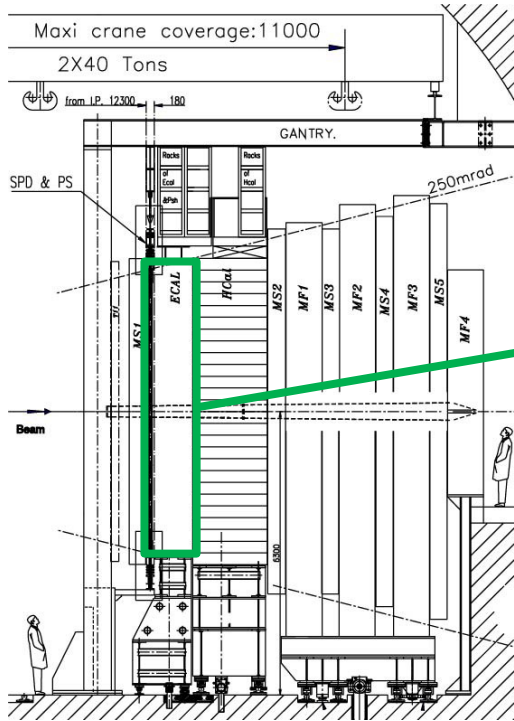
## 4D FOR CALO CHALLENGES: FOCUS ON LHCb ECAL UPGRADE

**Dominique Breton, on behalf of LHCb upgrade team**

*CERN, March 14<sup>th</sup> 2023*

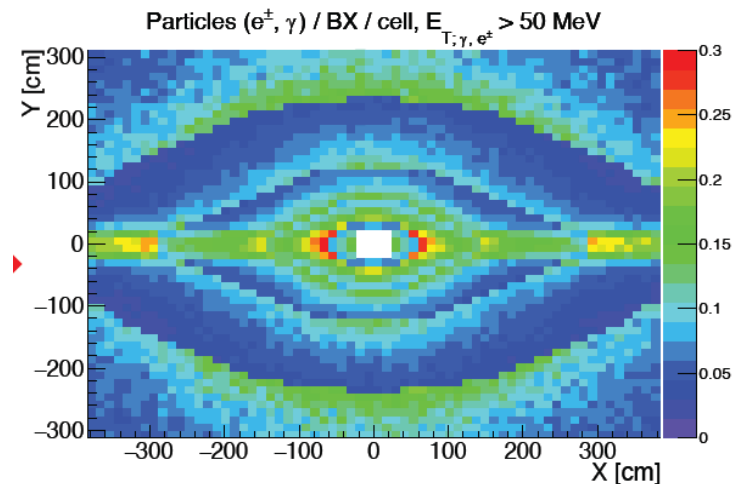


# THE UII DETECTOR



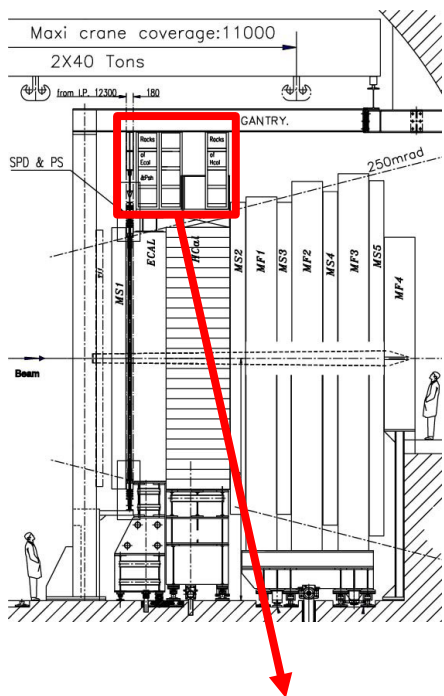
The future UII detector: « PicoCal »

- For the phase 2 upgrade, the central part of the detector will be equipped with SPACAL modules to deal with radiation (up to 1MGy).
- Shashlik will remain in the outer part (< 40kGy).
- In order to limit the occupancy, the size of the modules will be reduced thus their number increased
  - ⇒ from 6,000 to ~ 15,000 channels
- Introduction of longitudinal segmentation and double sided readout => ~ 30,000 channels (baseline option)



UII detector occupancy

# THE ELECTRONICS

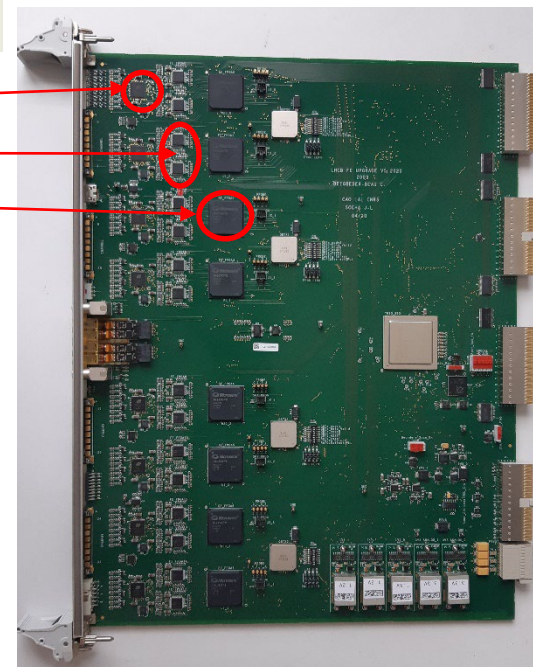
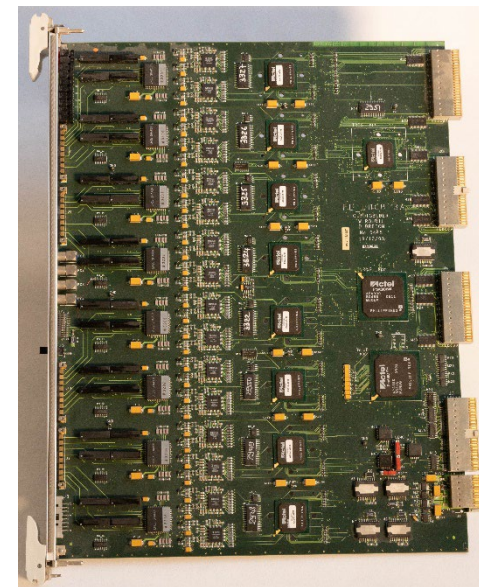


The original front-end board (2008-2020)

The 10 electronics racks are located on the platform => 12 to 20m cables but low radiation level (400 Gy for UII)

- 18 crates
- Currently 256 front-end boards (32-channel each)

The new front-end board since phase1 upgrade in 2020



IceCal ASIC

12-bit ADCs

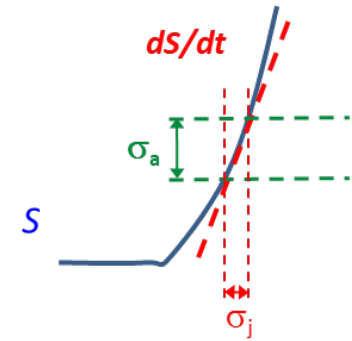
FE FPGA



# REQUIREMENTS FOR NEW TIMING PATH

- Target time resolution of **15ps rms** to distinguish multiple interactions
- Target energy range for time measurement =>  $E_T = [50\text{MeV}-5\text{GeV}]$  => **range of 100 ...**
- Deal with **maximum possible channel occupancy**

Theoretical electronics time resolution: 
$$\delta_t = \frac{t_{\text{rise time}}}{\text{SNR}} = \frac{\text{Noise}}{\text{Slope}}$$



- If you look at the current modules and electronics: rise time of 5ns with 1mV rms noise → jitter of 250ps rms !

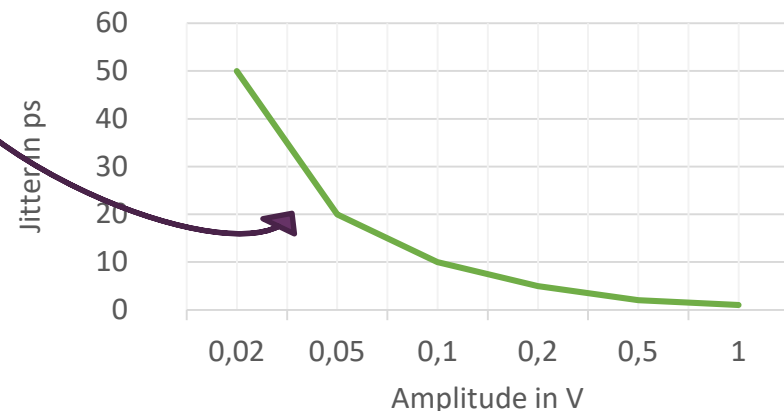
⇒ We have to reduce **both rise time and noise**

⇒ To give an idea, to get a resolution of 20ps rms with a rise time of 1ns and a noise of 1mV rms, you need a 50 mV pulse

- 1ns seems to be a (below the ?) limit for the PMTs so we have to do our best concerning the noise to get the largest possible dynamic range

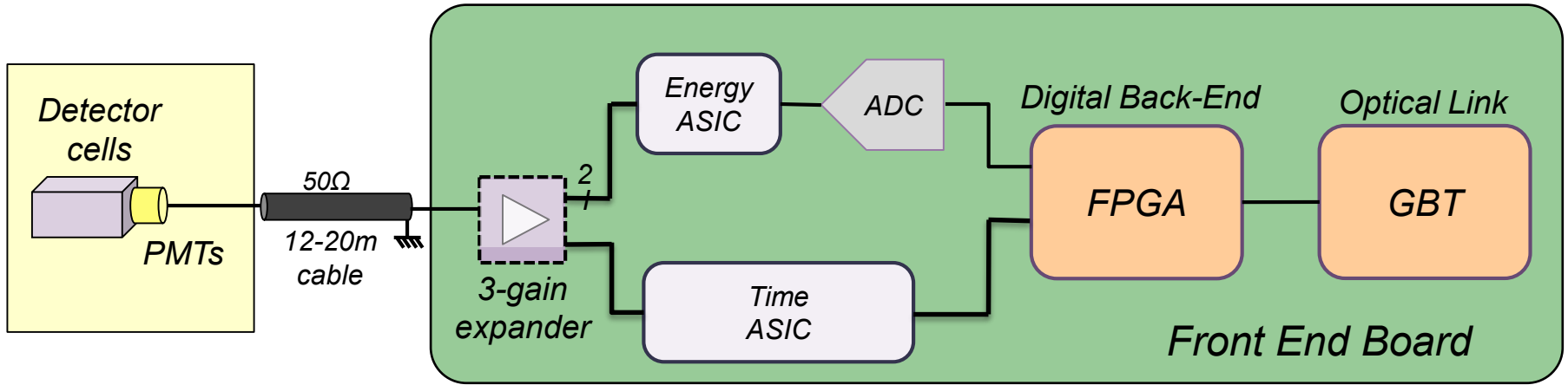
- Noise is **the sum of detector and electronics contributions**

Evolution of the jitter with the signal amplitude (rise time = 1 ns, noise = 1mV )



# NEW ELECTRONICS CHAIN

➤ Chosen architecture: this choice will be explained in the following slides...



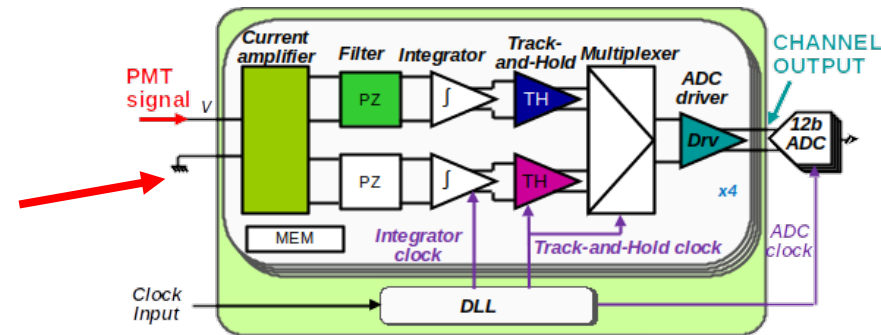
➤ Two separated processing paths with dedicated ASICs in the same technology: **CMOS 65 nm**

➤ **Energy path** close to the current ICECAL scheme (mostly analog processing)

➤ **Independent timing path** based on SPIDER waveform TDC  
=> can be used for other application or type of detector

➤ For dynamic range compatibilities, **3 different gains** must be provided

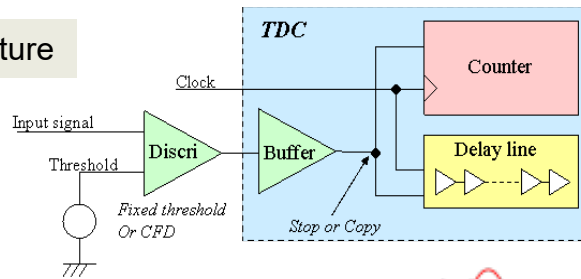
- 50MeV to 100GeV over 2 gains for energy measurement
- 50MeV to 5GeV (single gain) for time measurement



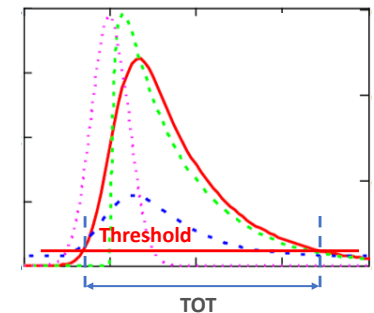
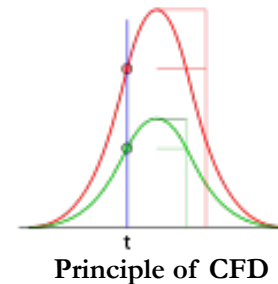
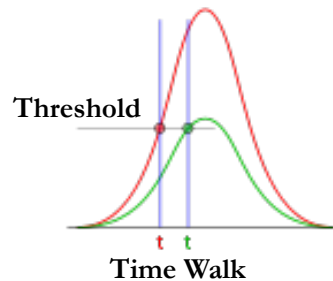
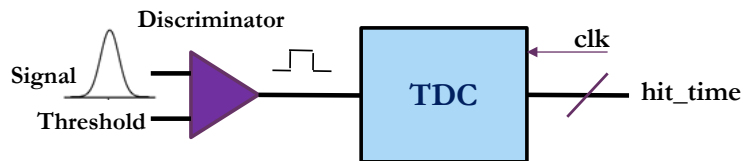
# DRAWBACKS OF TDC-BASED CHAINS

- **Time to Digital Converters (TDCs)** are the usual candidates for time stamping of fast signals. They are designed either in the form of **dedicated ASIC** or integrated inside **high-end FPGAs**.
- They are self-triggering and can withstand high counting rates
- A TDC has a strictly digital input => a **discriminator** has to be present to transform the **analog signal into digital**. It introduces **additional jitter and residues of time walk** => the overall timing resolution is degraded to **the quadratic sum of the discrimination and TDC contributions**.

Usual TDC structure



When sending a signal to a discriminator, the time instant "t" of the output level toggling will depend on the amplitude of the signal  
=> **"Time Walk"** effect

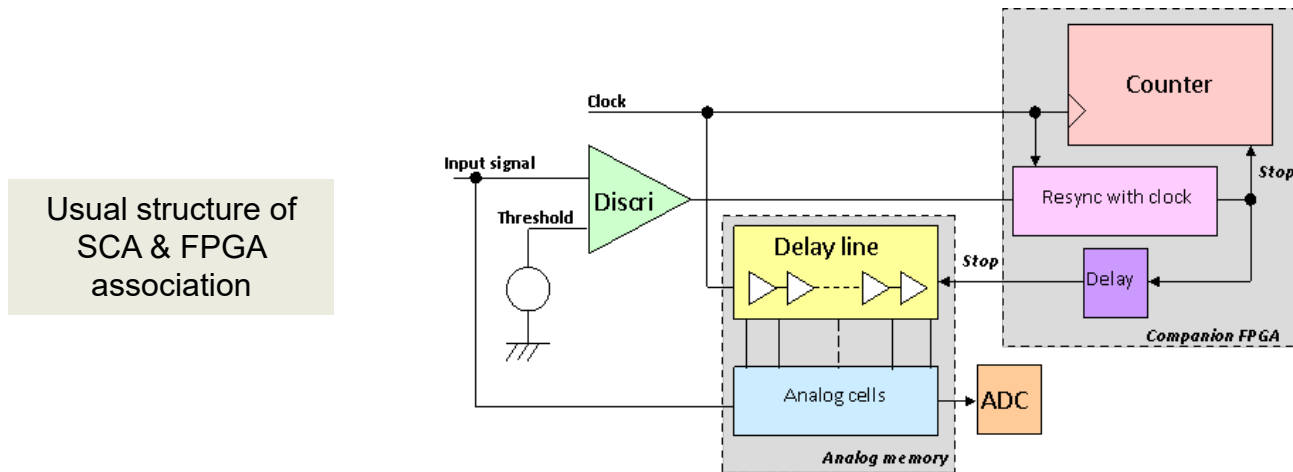


To avoid the Time Walk effect, one has to use a **Constant Fraction Discriminator (CFD)**

- But this implies that **you need to know the value of the peak** to apply the threshold !
- **Ok for firmware or software** when the signal has been digitized but **not in a TDC which does not provide information on waveform**, except under the derivate form of time over threshold (TOT) thus with a rather poor precision (especially because of the asymmetry of the signal edges).

# FAST DIGITIZERS: ANALOG MEMORIES...

- Time measurement can also be based on **Waveform Digitizing**.
- **Analog memories using Switched Capacitor Arrays (SCAs) associated with FPGAs** offer a smart solution for **replacing ADCs**, especially in terms of power, space and money budgets.
- **The discriminator is not anymore in the critical timing path.** Time information is given by association of the Timestamp Counter (few ns step), of the DLL locked on the clock to define region of interest (100 to a few 100's picoseconds minimum step), and finally of the samples of the waveform: their interpolation will give a precision of **a few picoseconds rms**.



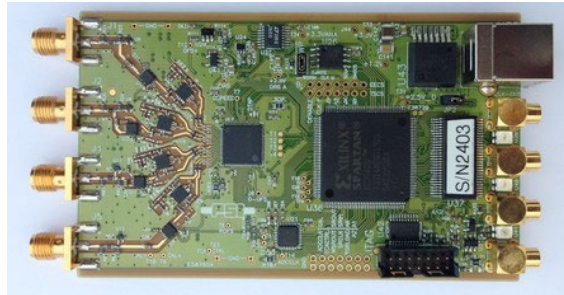
- This requires a precise **calibration of the Time Integral Non-Linearity** (like for ADCs). A very good time resolution can be reached even on small analog signals (a few tens of mV).
- The main drawback of the SCAs is their **readout dead-time** (a few tens to  $\sim 100 \mu\text{s}$  depending on the number of samples read), which becomes a limitation at high rates. Moreover, the channels are **usually commonly triggered and readout like in an oscilloscope**.

# EXAMPLES OF SCA-BASED FAST DIGITIZERS



4-channel Evaluation Module

DRS4 ASIC and modules  
(S.Ritt, PSI)



CAEN version  
(V1742)



**Currently used for LHCb upgrade test beams**

8-channel Module



WaveCatcher modules (IJCLab & IRFU)  
Based on SAMLONG ASIC

CAEN version  
(V1743)



16+2-channel Module



16+2-channel board

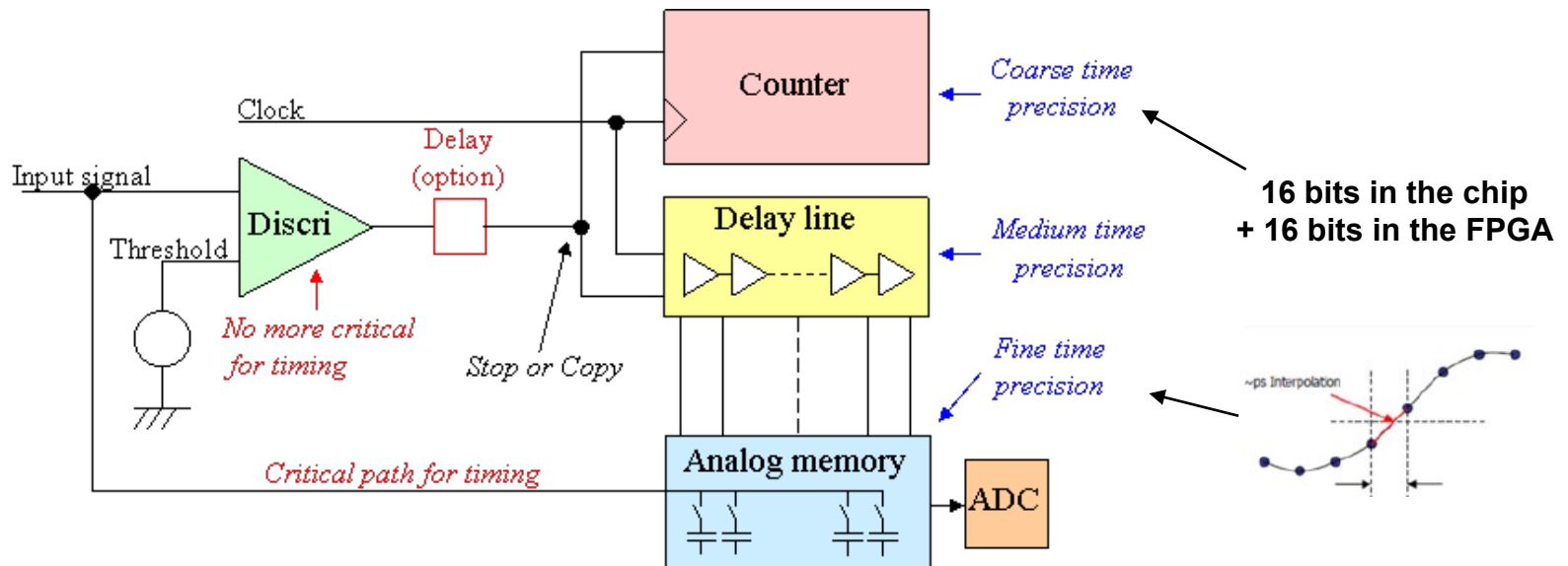
64-channel mini-crate





# THE « WAVEFORM TDC » STRUCTURE

- Introduced by LAL/IRFU in 2009: **mix of DLL-based TDC and of analog-memory based Waveform Digitizer**
- **All channels are self-triggering**
- The TDC gives the time of the samples and the samples give the final time precision after **CFD interpolation** => **resolution of a few ps rms**
- Digitized waveform gives **access to signal shape...**
- Conversely to TDC, discriminator is used only for triggering, **not for timing**

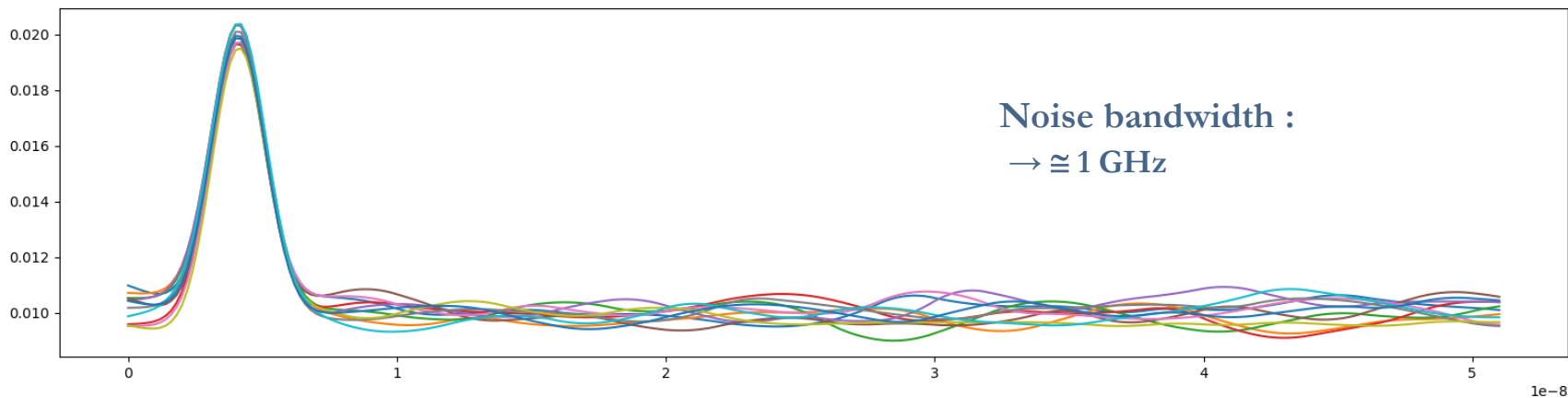
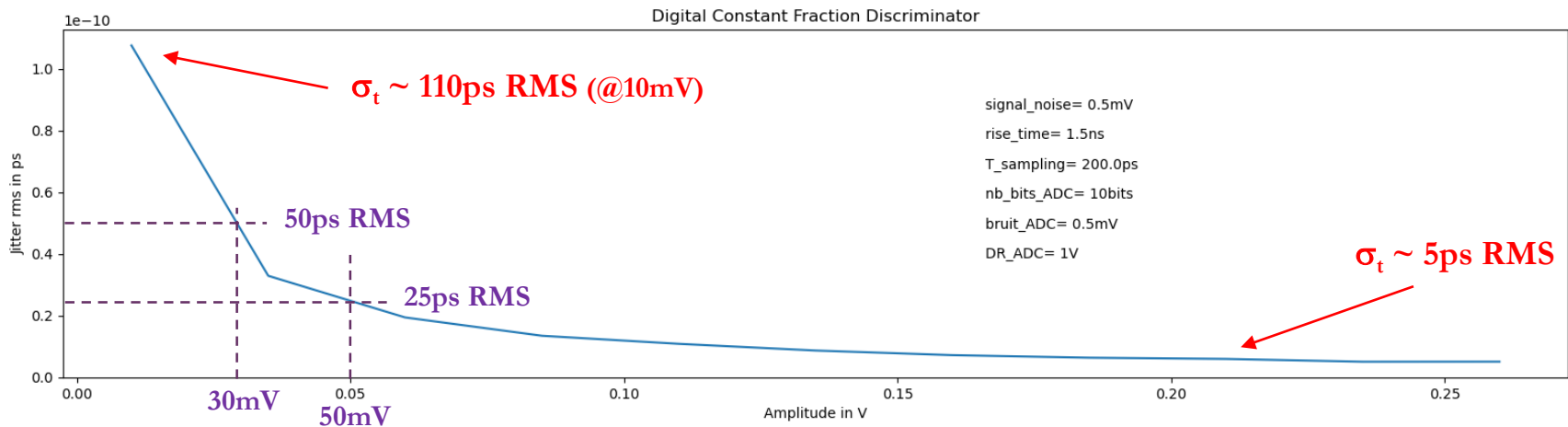


# SIMULATIONS OF DIGITAL CFD (1)

## Timing jitter versus signal amplitude :

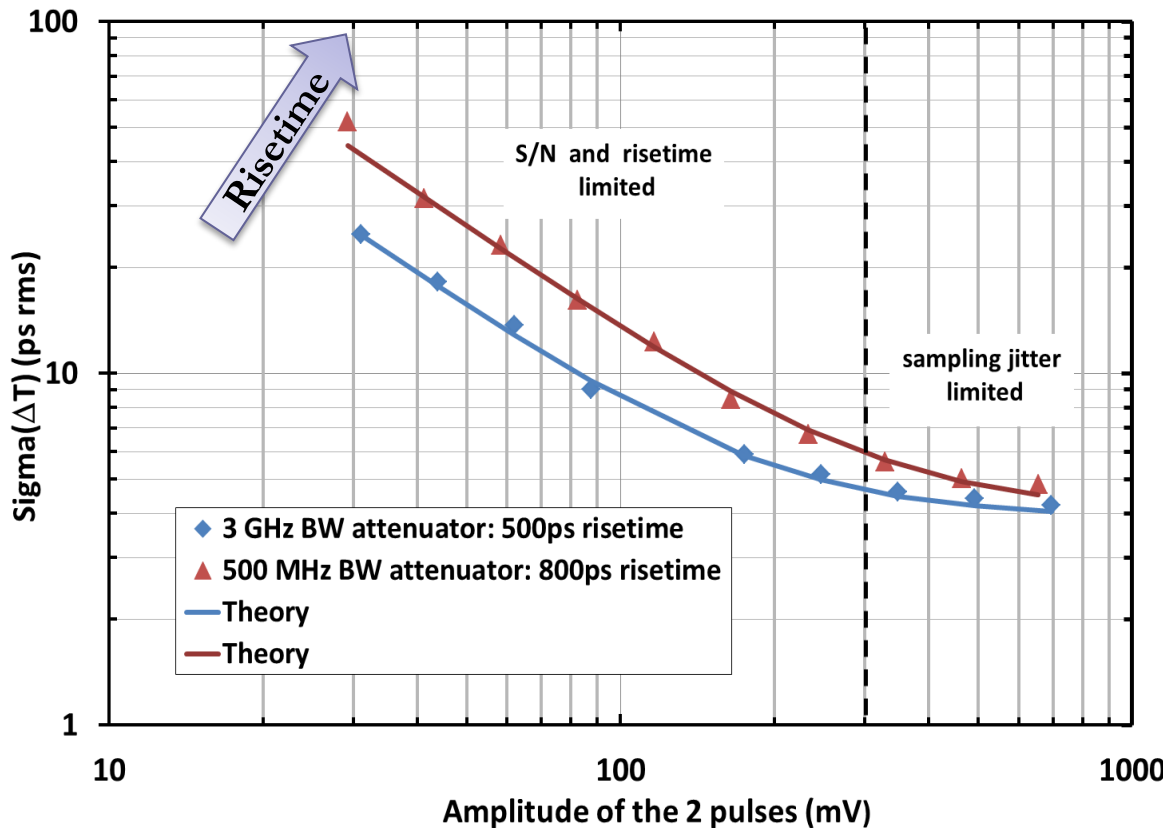
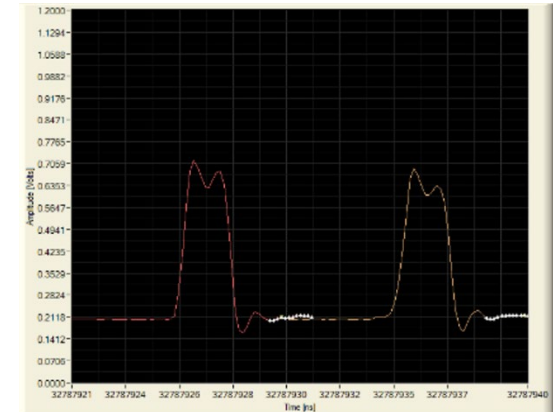
rise time = 1.5ns ;  $\sigma_{\text{noise}} = 500\mu\text{V}_{\text{RMS}}$  ;  $\sigma_{\text{SCA}} = 500\mu\text{V}_{\text{RMS}}$

Here we use a **dynamic range of 100**, as required for ECAL:  
=> Vin ranges from **10mV to 1V** (limited by technology)



# REAL MEASUREMENTS WITH DIGITAL CFD

Measurements performed with a **SAMPIC** module (Waveform TDC, designed by IJCLab & IRFU) : two pulses with 1nS FWHM - 15 ns delay, digital CFD algorithm



Measurements consistent with the theoretical formula:

$$\sigma(\Delta t) = \sqrt{2} \times \sqrt{\sigma_j^2 + \alpha \times \left(\frac{\sigma_n}{Slope}\right)^2}$$

Assuming: :

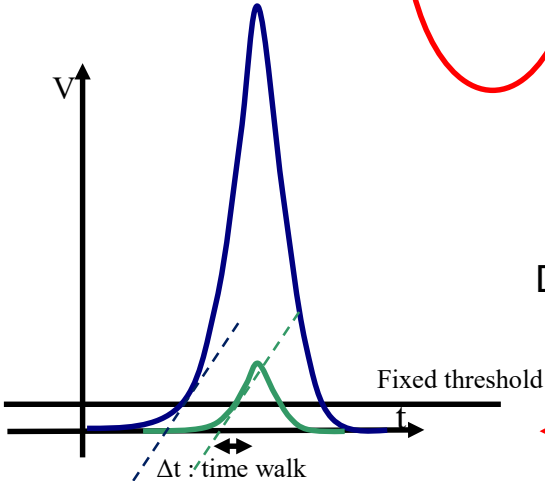
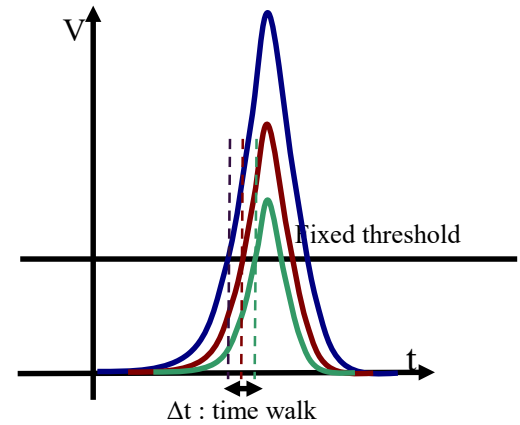
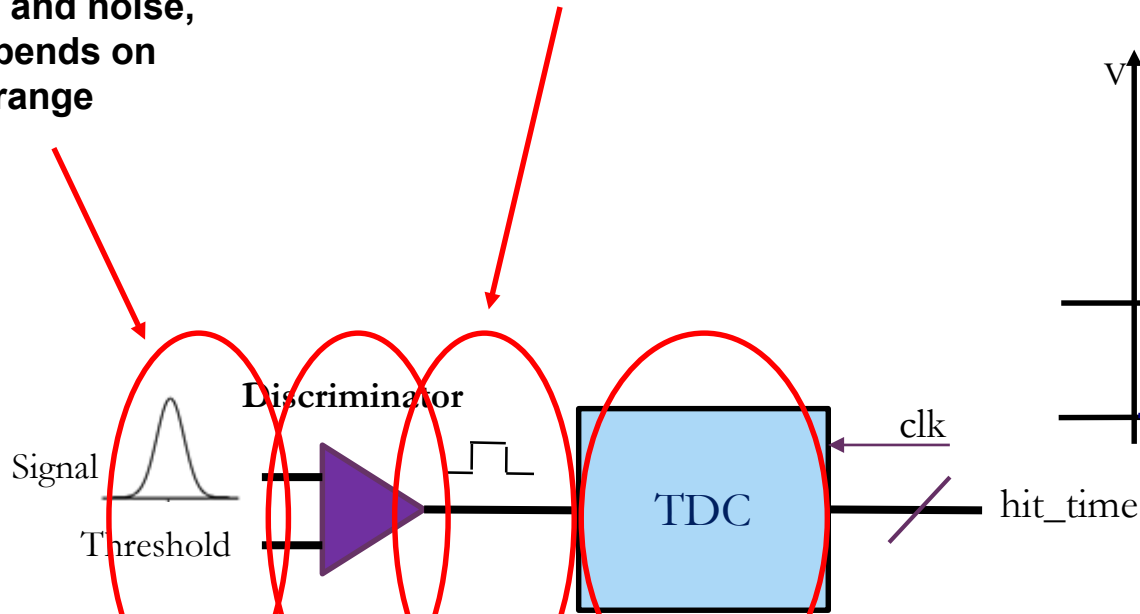
- \* Voltage noise  $\sigma_n = 1.1$  mV RMS
- \* Sampling jitter  $\sigma_j = 2.8$  ps RMS
- \*  $\alpha = 2/3$  (theory for perfect CFD)

[arXiv:1606.05541v1](https://arxiv.org/abs/1606.05541v1)

# JITTER CONTRIBUTIONS IN A TDC CHAIN

Jitter from comparison signal vs threshold: **depends on signal slope and noise, threshold depends on dynamic range**

Effect of time walk: depends on signal dynamic range. Can be partly corrected thanks to amplitude or charge measurement



TDC jitter (depends on time LSB, time INL residue, ...)

Discriminator's own jitter

← The key element is **the slope at threshold crossing** ...

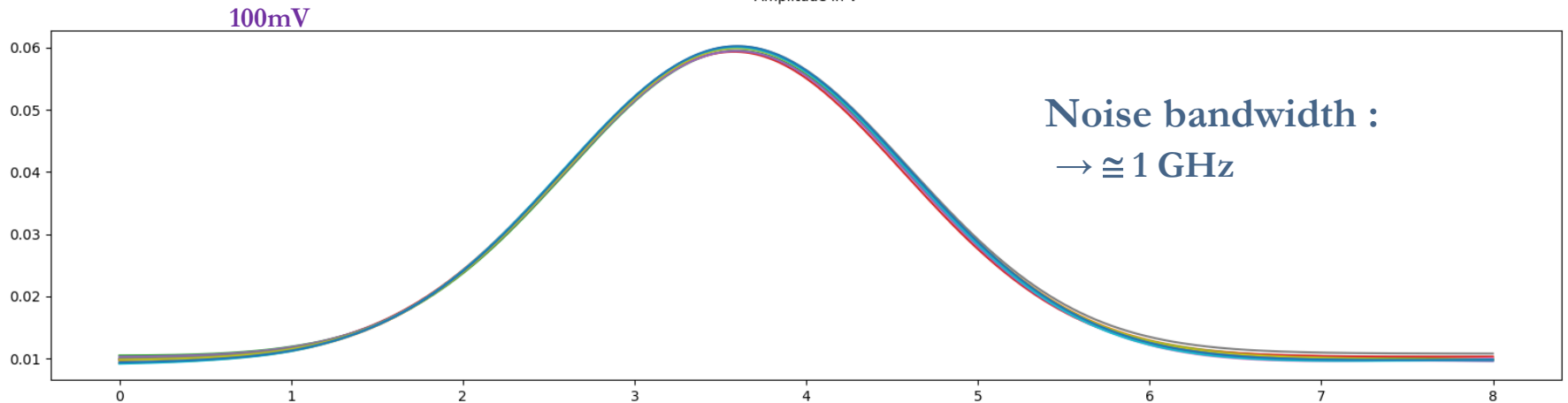
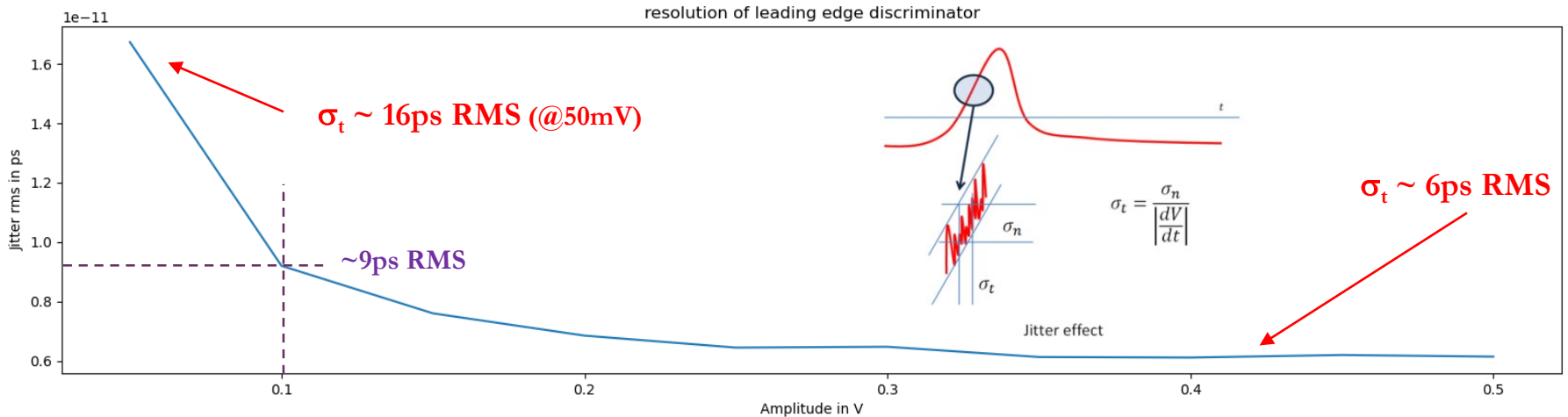
# SIMULATIONS OF SOLE LEADING-EDGE DISCRIMINATOR (1)

Timing jitter versus signal amplitude : rise time = 1.5ns ;  $\sigma_{\text{noise}} = 500\mu\text{V RMS}$

If the dynamic range was of only 20:

$V_{\text{in}}$  ranges from 50mV to 1V

=> discriminator threshold is set to **25mV** (half the minimum signal)



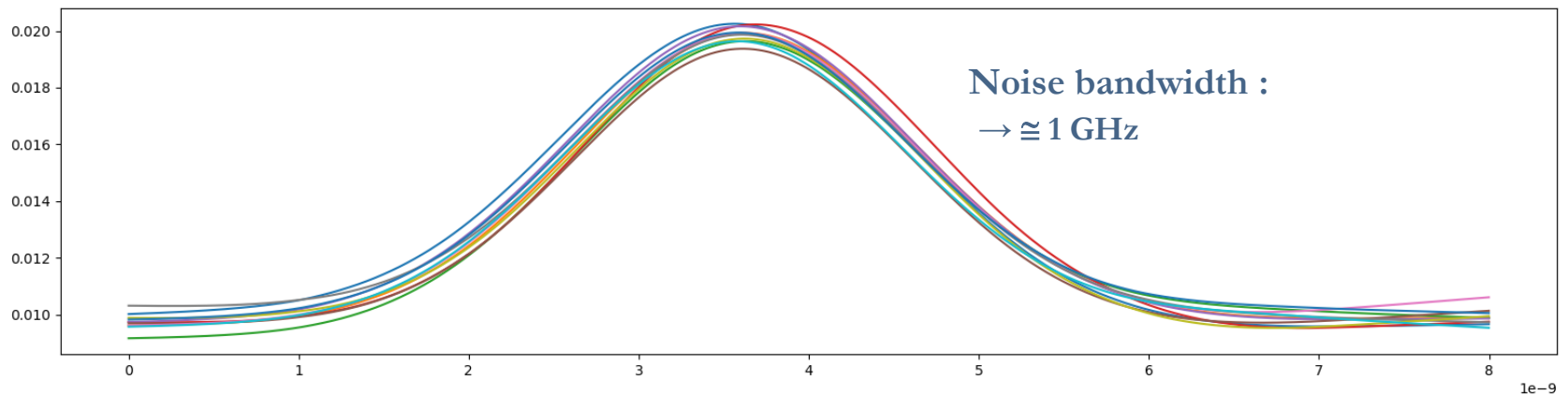
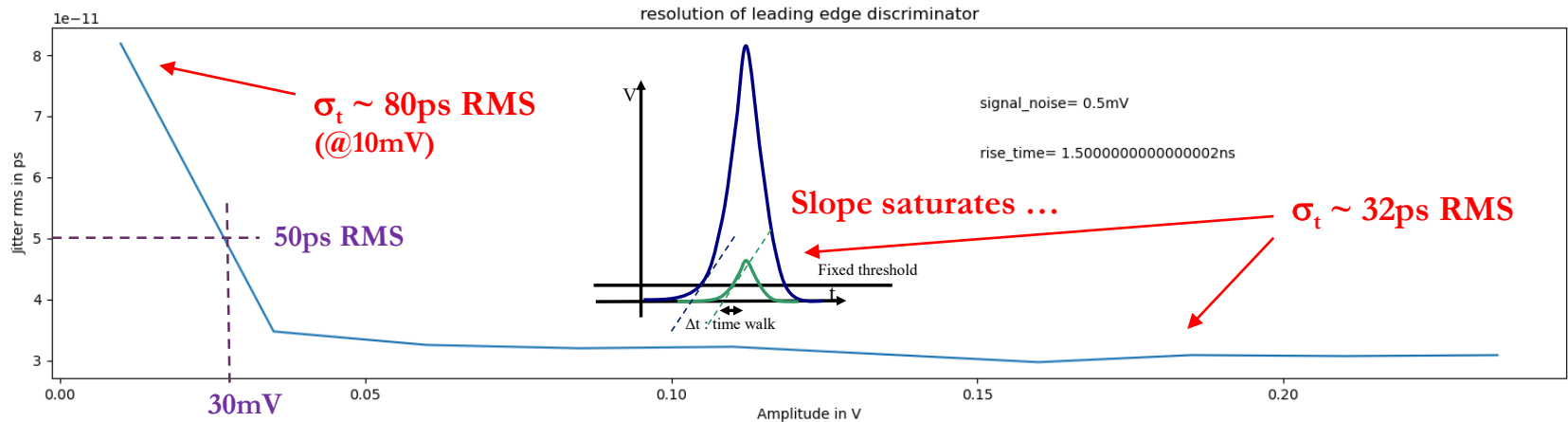
# SIMULATIONS OF SOLE LEADING-EDGE DISCRIMINATOR (2)

Timing jitter versus signal amplitude : rise time = 1.5ns ;  $\sigma_{\text{noise}} = 500\mu\text{VRMS}$

But with a dynamic range of 100:

$V_{\text{in}}$  ranges from 10mV to 1V

=> discriminator threshold is set to 5mV (half the minimum signal)

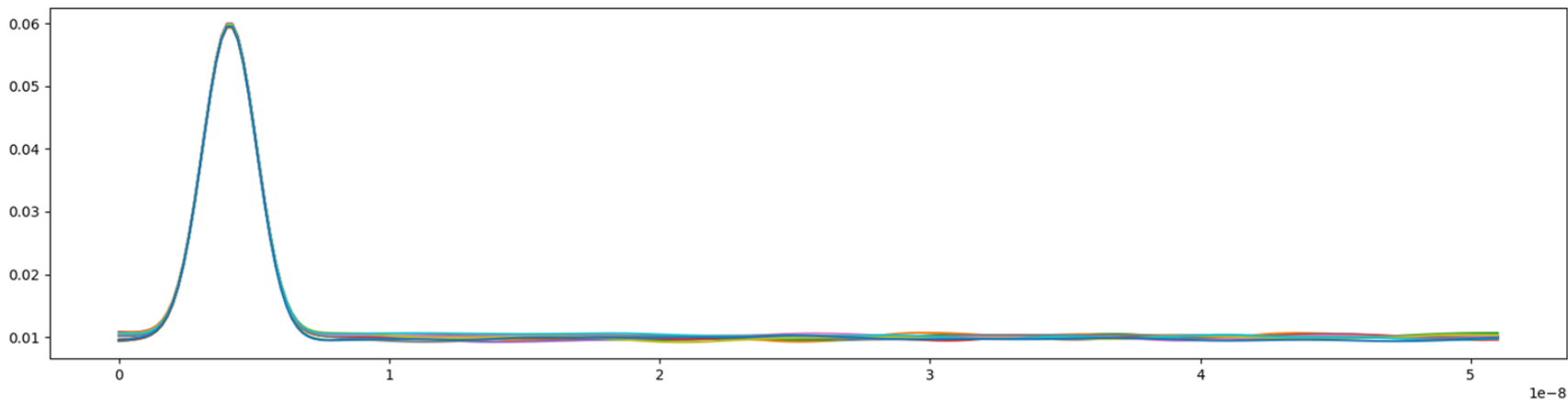
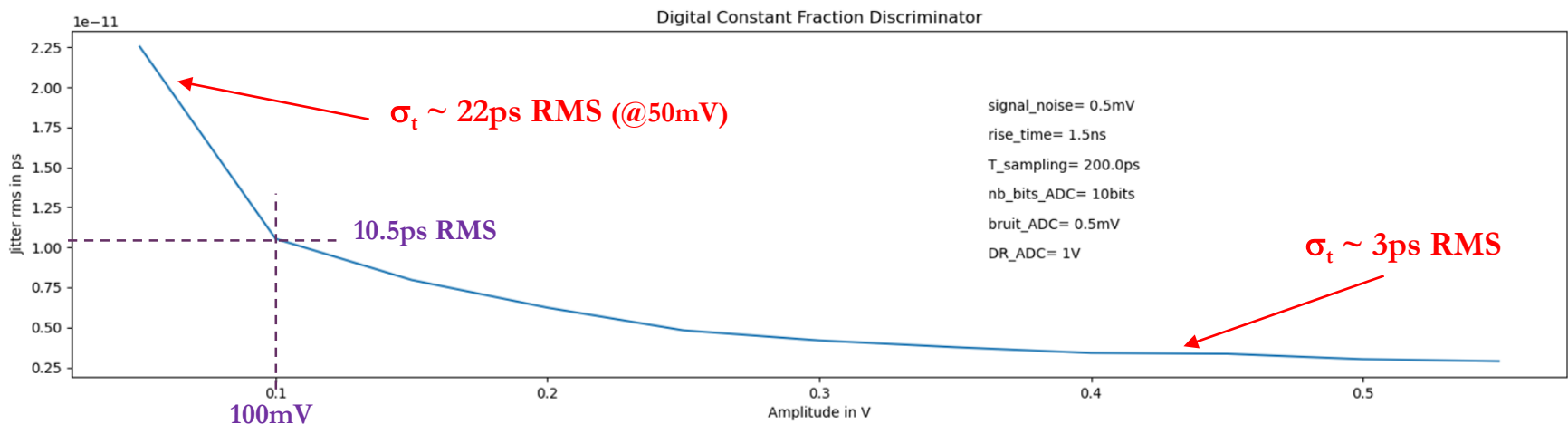


# SIMULATIONS OF DIGITAL CFD (2)

Timing jitter versus signal amplitude :

rise time = 1.5ns ;  $\sigma_{\text{noise}} = 500\mu\text{VRMS}$  ;  $\sigma_{\text{SCA}} = 500\mu\text{VRMS}$

Just to compare, here we use a reduced dynamic range of 20  
=>  $V_{\text{in}}$  ranges from 50mV to 1V



# SUMMARY ABOUT DISCRIMINATOR + TDC CHAINS

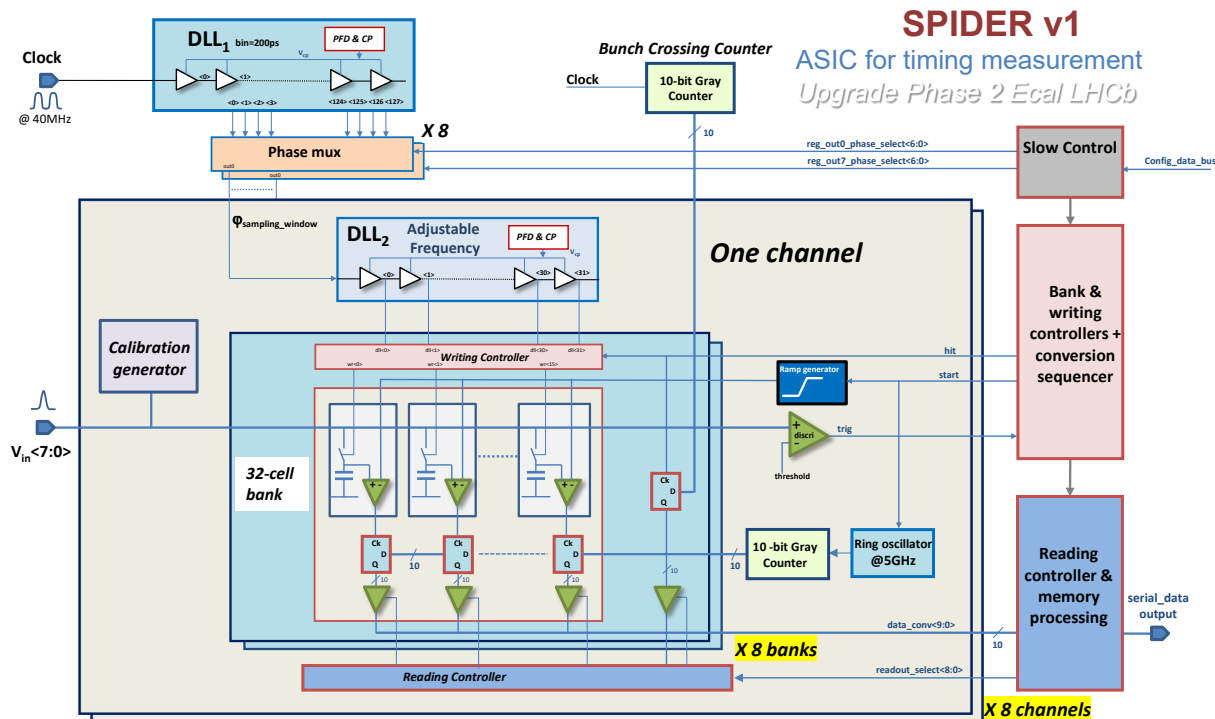
- The **discriminator + TDC chain** is well adapted for small or medium dynamic ranges, not for large ones
  - **Very sensitive to input noise:** the contribution of the sole discriminator is already higher than the electronics target ( $< 20\text{ps rms}$ ) even for large signals if input noise is  $> 350\ \mu\text{V rms}$ .
  - **Very sensitive to Time Walk correction**, especially with asymmetric edges (much slower falling edge which introduces jitter in TOT)
    - In the case of LHCb, we have the separate energy measurement which could help in this field (but its correction requires a cross calibration of energy and time) => hard to predict precisely
- **This kind of problems has clearly been seen on ATLAS HGTD and CMS HGAL**, even with smaller dynamic ranges than the one required for UII ECAL
  - They seem to induce non negligible limitations to the time resolution
- The **other contributions** still and always have to be added (in quadrature):
  - The **discriminator noise** => low
  - The **TDC's own time resolution** => depends on the chosen solution (FPGA or ASIC), and of the complexity of its calibration





# ARCHITECTURE OF SPIDER

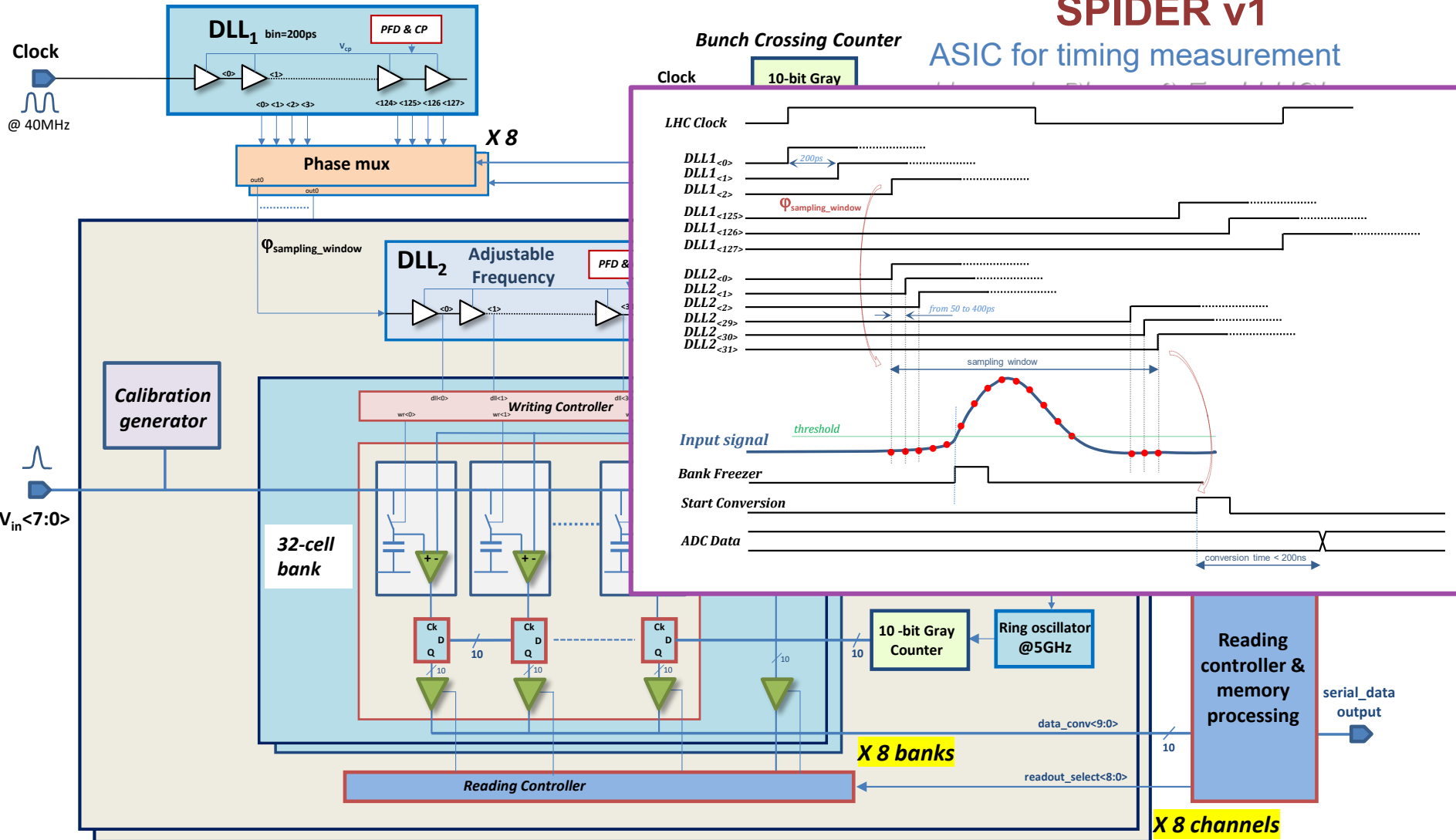
- Each channel is **self-triggering** (based on individual discriminators)
- There are **8 banks per channel** and they can trigger on consecutive BCs: **analog derandomizer**
  - The sampling window covers a **subset of the clock period** based on the time of flight of particles
- **ADC is massively parallel** so it can convert all the banks which have already triggered
  - => this permits increasing the mean occupancy ( up to ~ 50% at the ADC level)
  - => the bottleneck is pushed towards the output dataflow capacity (up to ~2Gbit/s/ch)



# ROUGH SEQUENCING OF ACQUISITION

## SPIDER v1

ASIC for timing measurement



# SPIDER CHARACTERISTICS

- Technology: **TSMC CMOS 65nm** (the most lasting technology, 10 years (?)), but only **1.2V of power supply** (2.5V transistors are also available)
  - ⇒ hard for analog design => smart use of 2.5V transistors
  - ⇒ nice for digital blocks
- Input signal: rise time ~ 1ns / 1.5ns, dynamic range  $V_{in}=[10mV-1V]$

To achieve the time resolution of **15ps rms** over the largest possible energy range, we need :

- a memory cell (switches & capacitor) with **~1V of dynamic range** and a noise voltage around or below **0.5mV rms**
- a resolution of 10 bits for the conversion: **10-bit Wilkinson ADC running at 5GHz** to reduce the conversion time (200ns max for full 10-bit range, i-e 8 clock periods max)
- a 128-delay-cell DLL1 running @40MHz → bin  $\approx$  200ps to define **the beginning and the width** of the sampling window
- a 32-delay-cell DLL2 running from 80MHz to 640 MHz → bin  $\approx$  50ps to 400ps to fix the **sampling frequency** between **2.5GS/s and 20GS/s**

# FIRST PROTOTYPE ARCHITECTURE

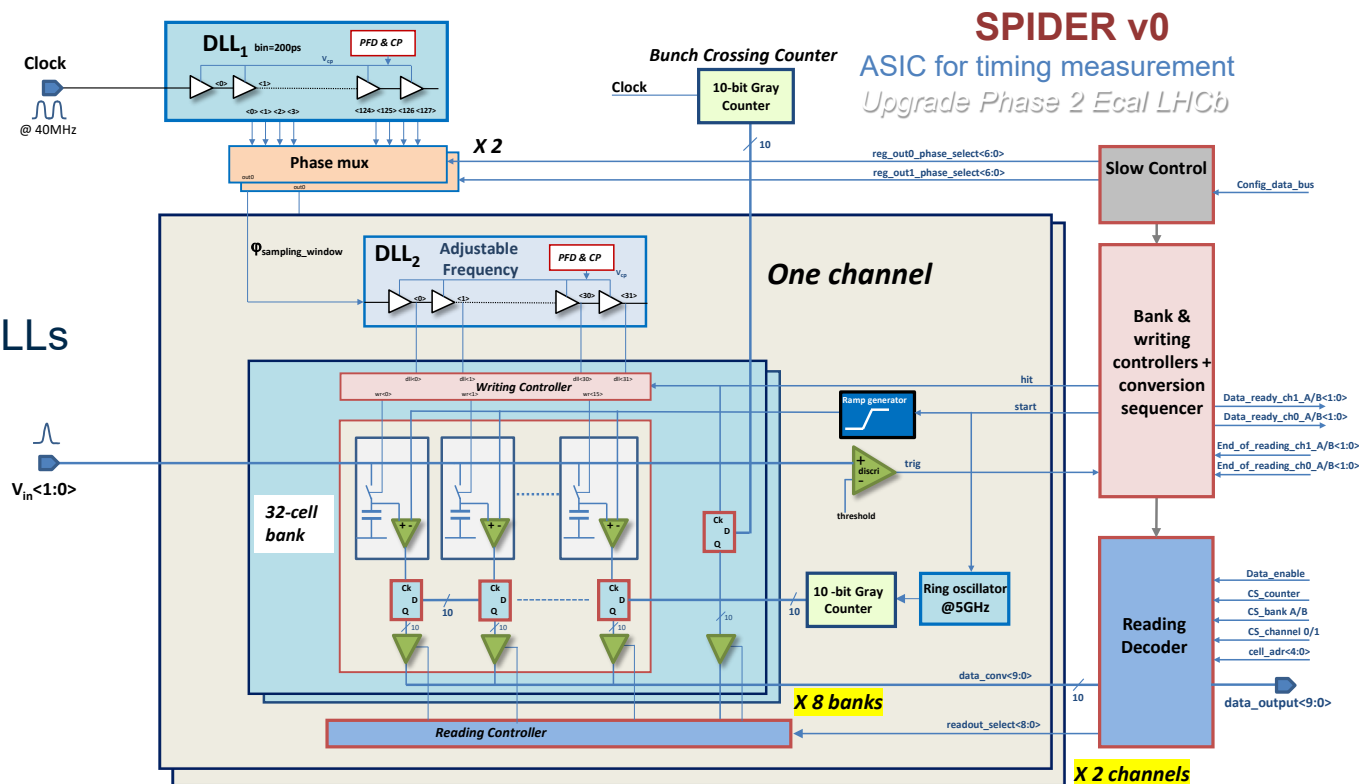
➤ Architecture: «two eight-bank channels»

SPIDER first prototype:  
contains all critical  
blocks



Proof of concept :

- ✓ Clock distribution & DLLs
- ✓ Memory cell in 65nm
- ✓ Self-triggering
- ✓ Multi-bank operation
- ✓ 10-bit Wilkinson ADC @5GHz



# DEVELOPMENT STATUS

- Collaboration of **4 IN2P3 labs** (Orsay, Clermont-Ferrand, Caen, Lyon) led by IJCLab and LPC Clermont.
- Very challenging design! Has started six months ago.
- Repartition in **work packages** for:
  - 1) Delay Locked Loop (DLL1 & DLL2)
  - 2) Analog part (memory cell, trigger comparator, ADC comparator, ramp generator) + Sampling & ADC management (bank & write controller + conversion sequencer)
  - 3) Counting digital part for “10-bit Wilkinson ADC & coarse time” (Gray counters, ring oscillator )
  - 4) Slow control & Readout management part (read decoder)
  - 5) Phase Locked Loop (not critical for first prototype)

 The first prototype submission is expected at the **end of 2023**

The idea is to start with 3,500 channels of new electronics in the inner detector for run 4. Including the new front-end boards housing SPIDER...



# SUMMARY

- For 4D calorimetry, we need to develop electronics with **large dynamic range** and **very good time resolution**
  - As shown, the association of the two requirements is **a challenge** which seems to be in the spirit of DRD7 ...
- Based on our long experience in the design of **analog memories**, we feel like the **Waveform TDC** can be an adequate solution to face this challenge
  - Waveform indeed contains all information
  - A low threshold has **no impact on time resolution**
  - Extracting only the most useful samples for the time extraction limits the readout time
  - There is **a lot of bandwidth margin for faster signals** which may directly reduce the jitter
  - This solution can work for **many other types of detectors** ...
- Our main targets:
  - **Short term:**
    - Reduce the electronics noise and increase the dynamic range
    - Reduce the conversion time while keeping the massive parallelism of the ADC
    - Get the best possible time INL and jitter for the analog memory
    - Optimize the output dataflow
  - **Longer term:**
    - Perform on-chip data compression still allowing external feature extraction
    - Get closer to 100% occupancy
    - Measure **both energy and time** ...