ECFA DRD7.3 - 4D Techniques - Pre-identified Challenges for future detectors

Timing ASICs for low-jitter & highly deterministic Front-End and Back-End

Methodology to Simulate Timing Determinism

Universal Time distribution in detectors

White Rabbit 2 Front-End

In-chip high quality clock distribution techniques

TSV for accurate distribution of global lines and data extraction

System-level issues

Distributed clock filtering and re-phasing circuits

Fast front-end amplifiers and limited power budget

high performance TDC and ADC blocks

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Large dynamic range for energy

Precise time calibration

Contact us !
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High Precision Timing Distribution *Trackers / Novel on-chip architectures* *Calo / High Performance Sampling*