Monolithic sensors in ALICE

Magnus Mager (CERN)

DRD7 — 15.03.2023

Monolithic sensors in ALICE

ALICE ITS2:

- 7 layers
- 10 m^2 MAPS
- 12.5 GPixel
- installed in Sep'21 (LHC LS2)

ALICE

Pb-Pb 5.36 TeV

LHC22s period
18th November 2022
16:52:47.893

Magnus Mager (CERN)
DRD7 — 15.03.2023

Executive summary

- **ALICE** is pushing **MAPS** technology since some 10 years:
  - **expertise** in design, characterisation, integration is built up at several institutes within the collaboration
  - **large workforce** >100 people, >20 institutes participate
  - long-standing **relation** with the foundry

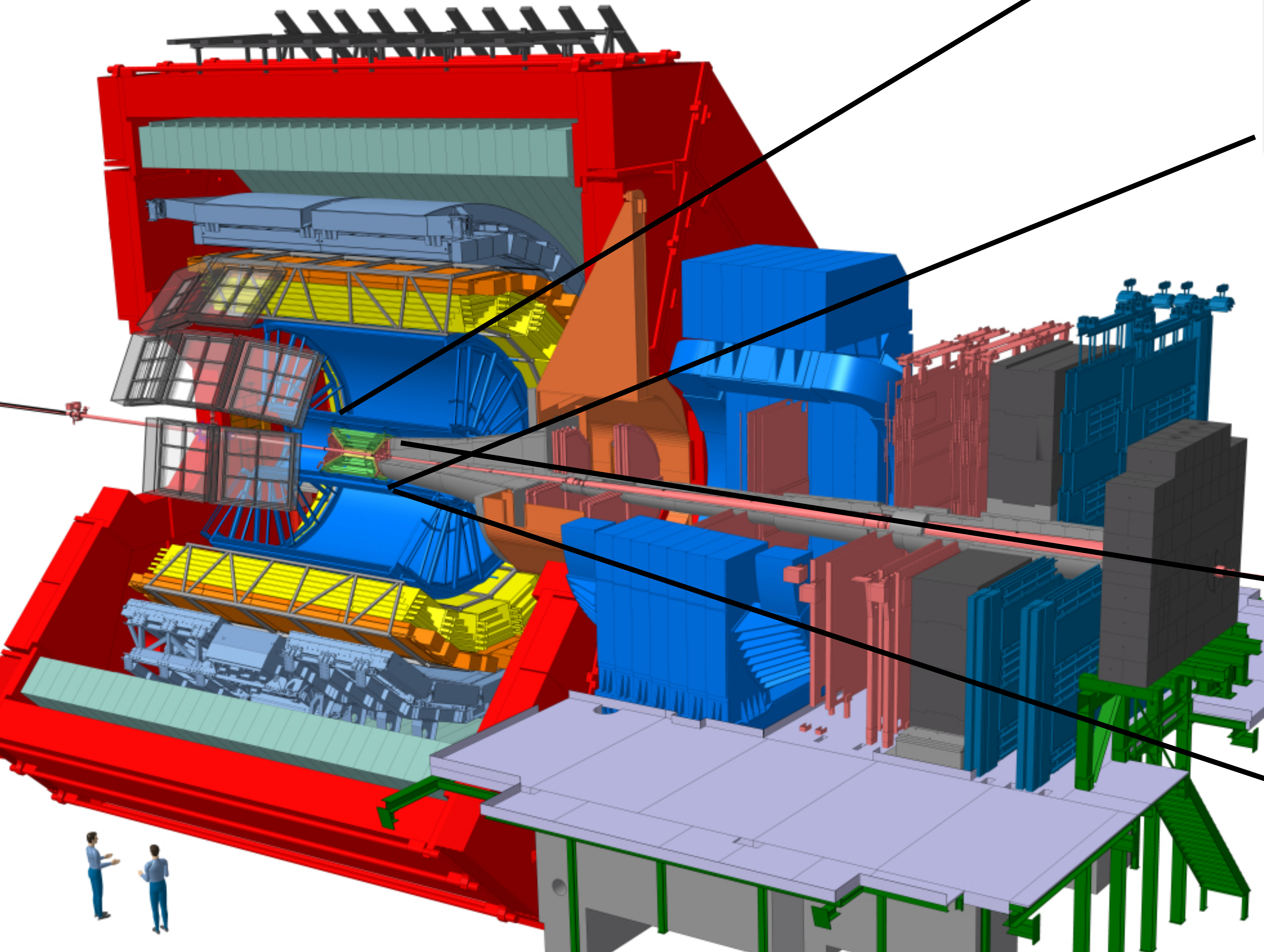
- Driven by clear goals and timelines:
  - **ITS2+MFT** (LHC LS2, 2021): new 10 m^2 7-layer monolithic Inner Tracking System and Forward Muon Tracker
    Tower Semiconductor 180 nm CIS (ALPIDE)
  - **ITS3** (LHC LS3, 2028): new inner-most 3 layers, wafer-scale, bent, stitched sensors
    Tower Partner Semiconductor 65 nm CIS
  - **ALICE 3** (LHC LS4, 2034): 60 m^2 silicon-only vertexer and tracker
    Tower Partner Semiconductor 65 nm CIS (baseline, tbc)

- R&D is exploring the technology far beyond the strict ALICE needs:
  - e.g. using process options to improve on radiation hardness and timing performance
  - gives a lot of **confidence** for the concrete ALICE application, **serves** the community as a whole, and also paves the way for the **future** ALICE plans

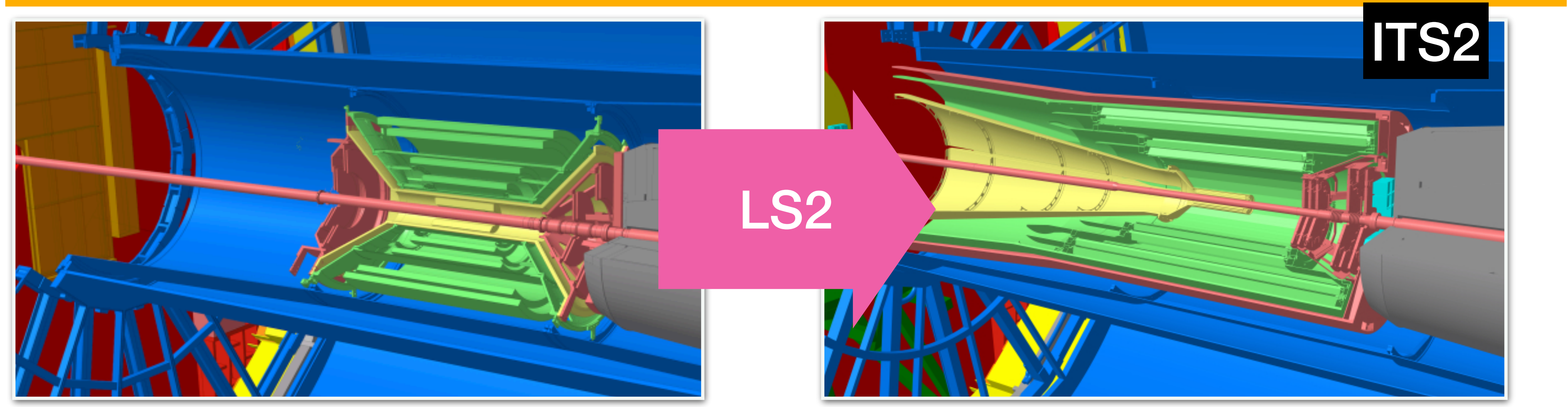
- Developed technology is used for several **off-spring** experiments (HEP, medical, …)
  - several (smaller, but not necessarily small) experiments have adopted ALPIDE
  - 180 nm technology is now widely used

ITS2+MFT

ALICE LS2 upgrades with Monolithic Active Pixel Sensors (MAPS)



Inner Tracking System



6 layers:
2 hybrid silicon pixel
2 silicon drift
2 silicon strip

Inner-most layer:
radial distance: 39 mm
material: $X/X_0 = 1.14\%$
pitch: $50 \times 425\ \mu m^2$

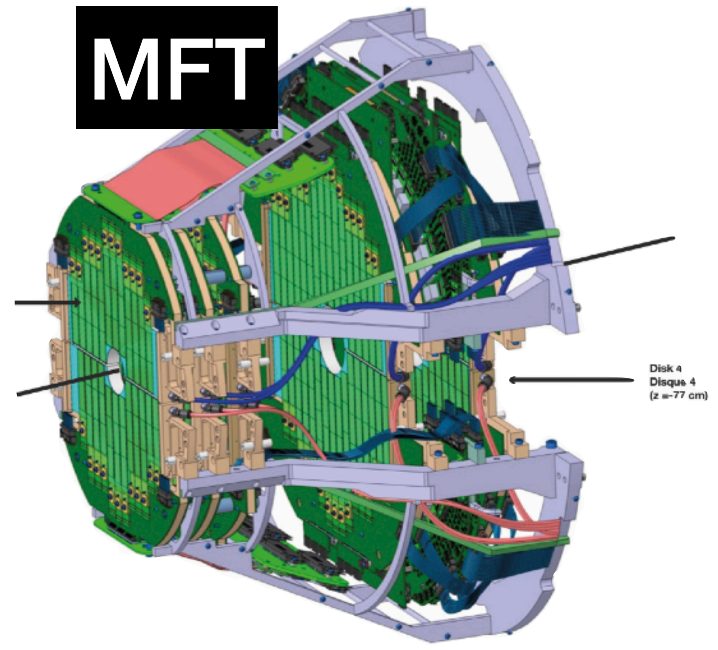
rate capability: 1 kHz

7 layers:
all MAPS
10 m^2, 24k chips, 12.5 Giga-Pixels

Inner-most layer:
radial distance: 23 mm
material: $X/X_0 = 0.35\%$
pitch: $29 \times 27\ \mu m^2$

rate capability: 100 kHz (Pb-Pb)

Muon Forward Tracker

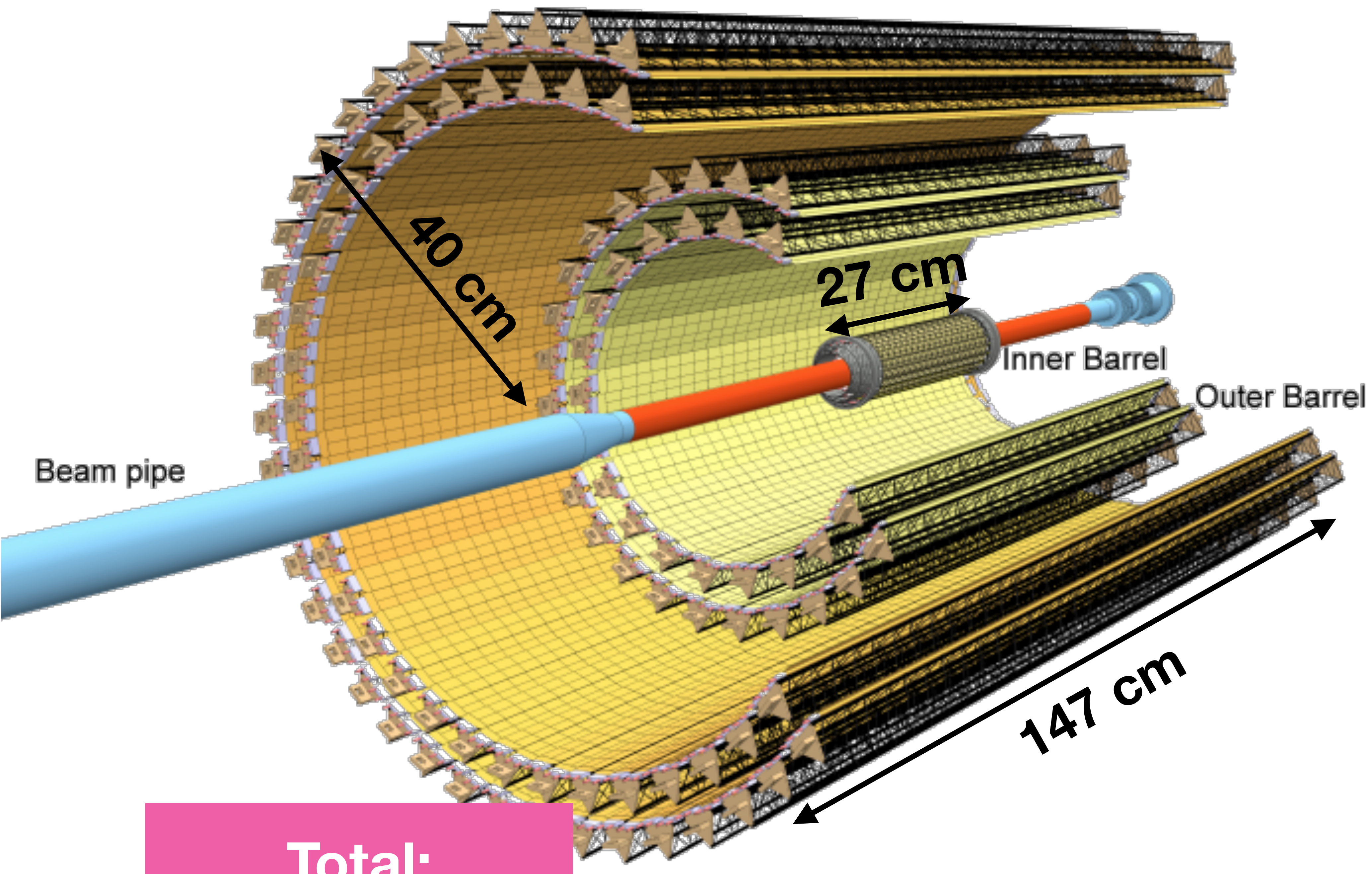


new detector

5 discs, double sided:
based on same technology as ITS2

ITS2: overview

Layout



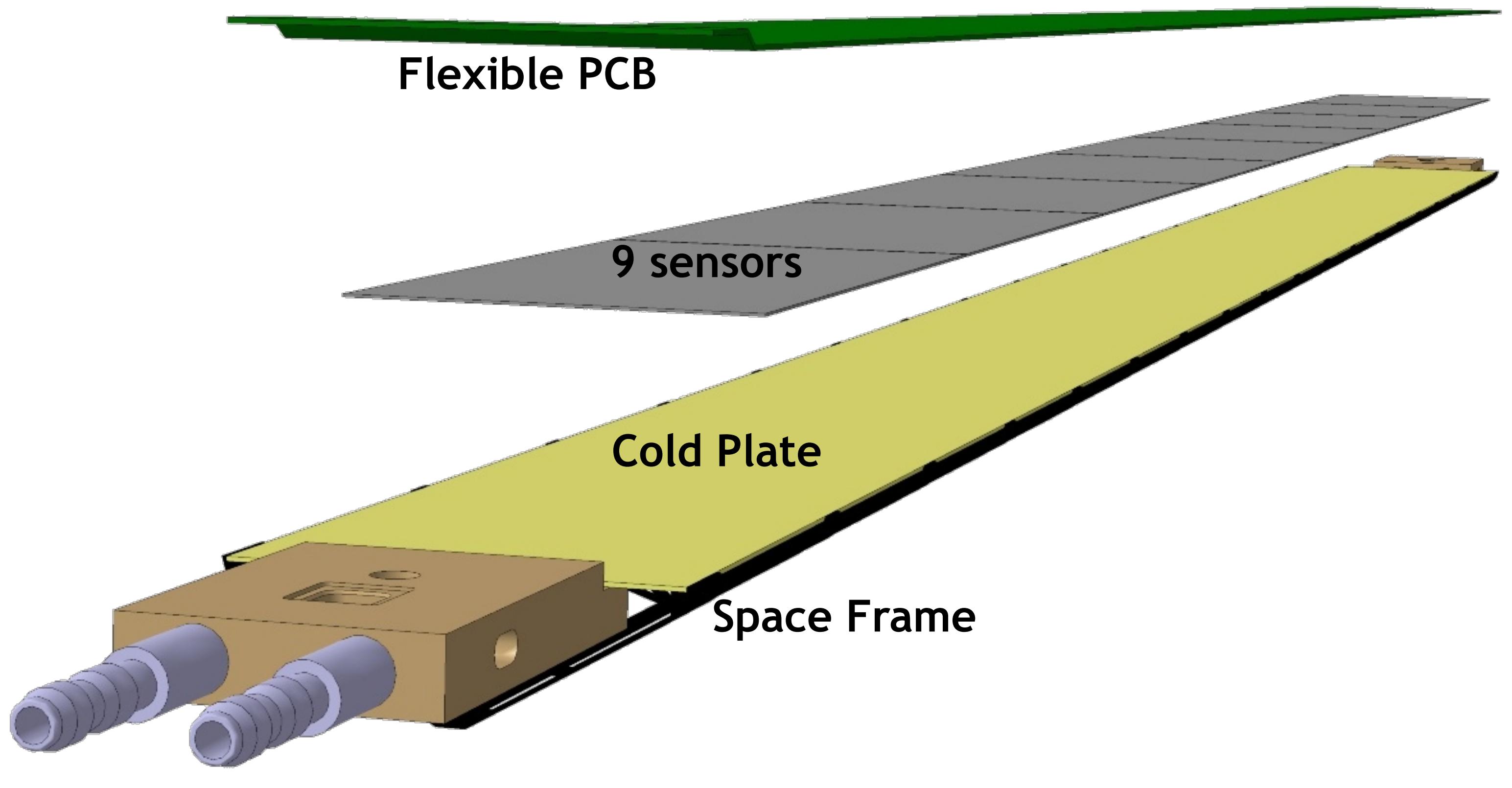
Total:
- 24k chips
- 10 m²
- 12.5 GPixel

Inner Barrel (IB)

3 Inner Layers: 12+16+20 Staves
1 Module / Stave

9 sensors per Module

96 Modules to be produced (including one spare barrel)

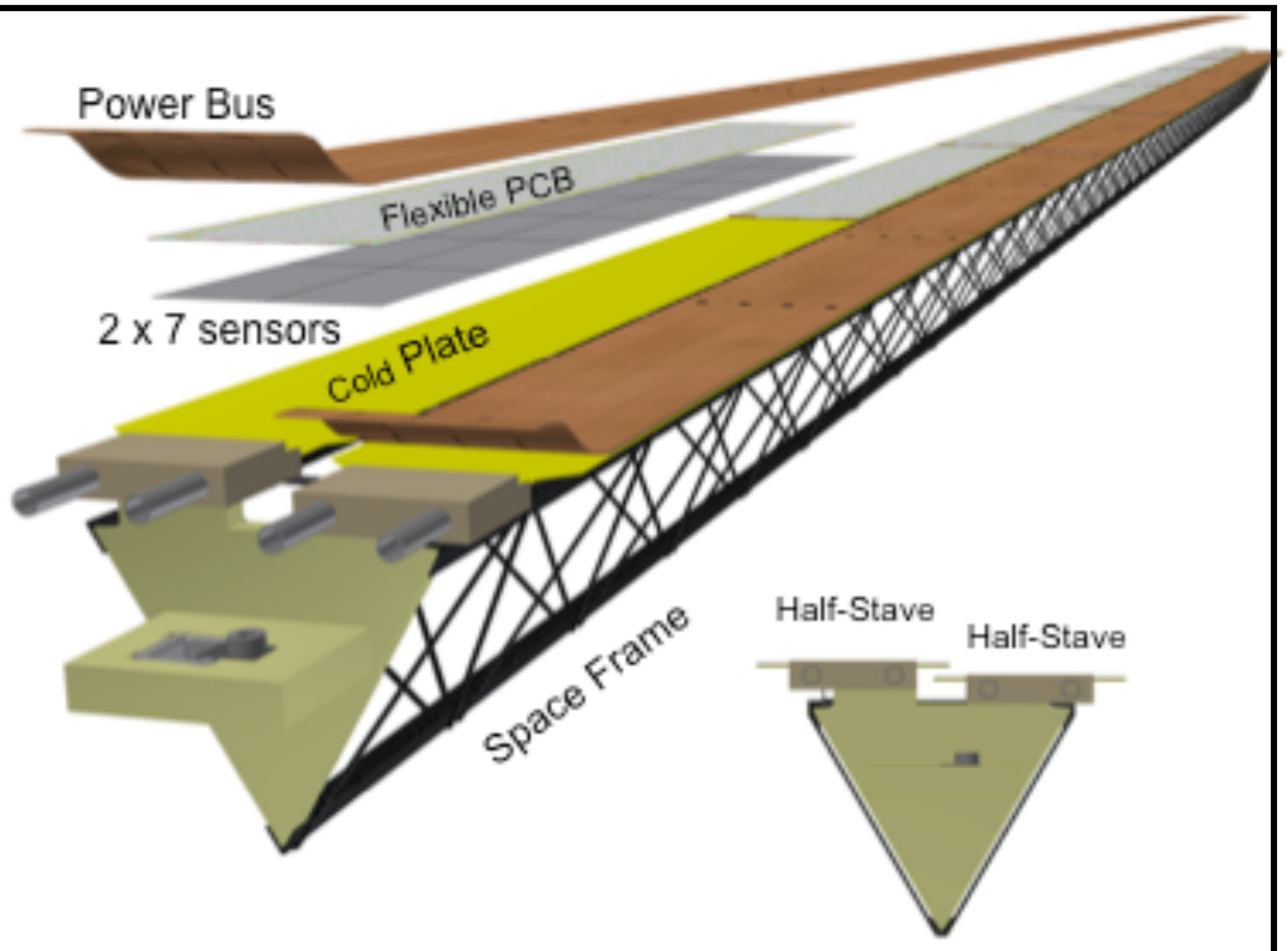


Outer Barrel (OB)

2 Middle Layers: 30+24 Staves
2×4 Modules / Stave
2 Outer Layers: 42+48 Staves
2×7 Modules / Stave

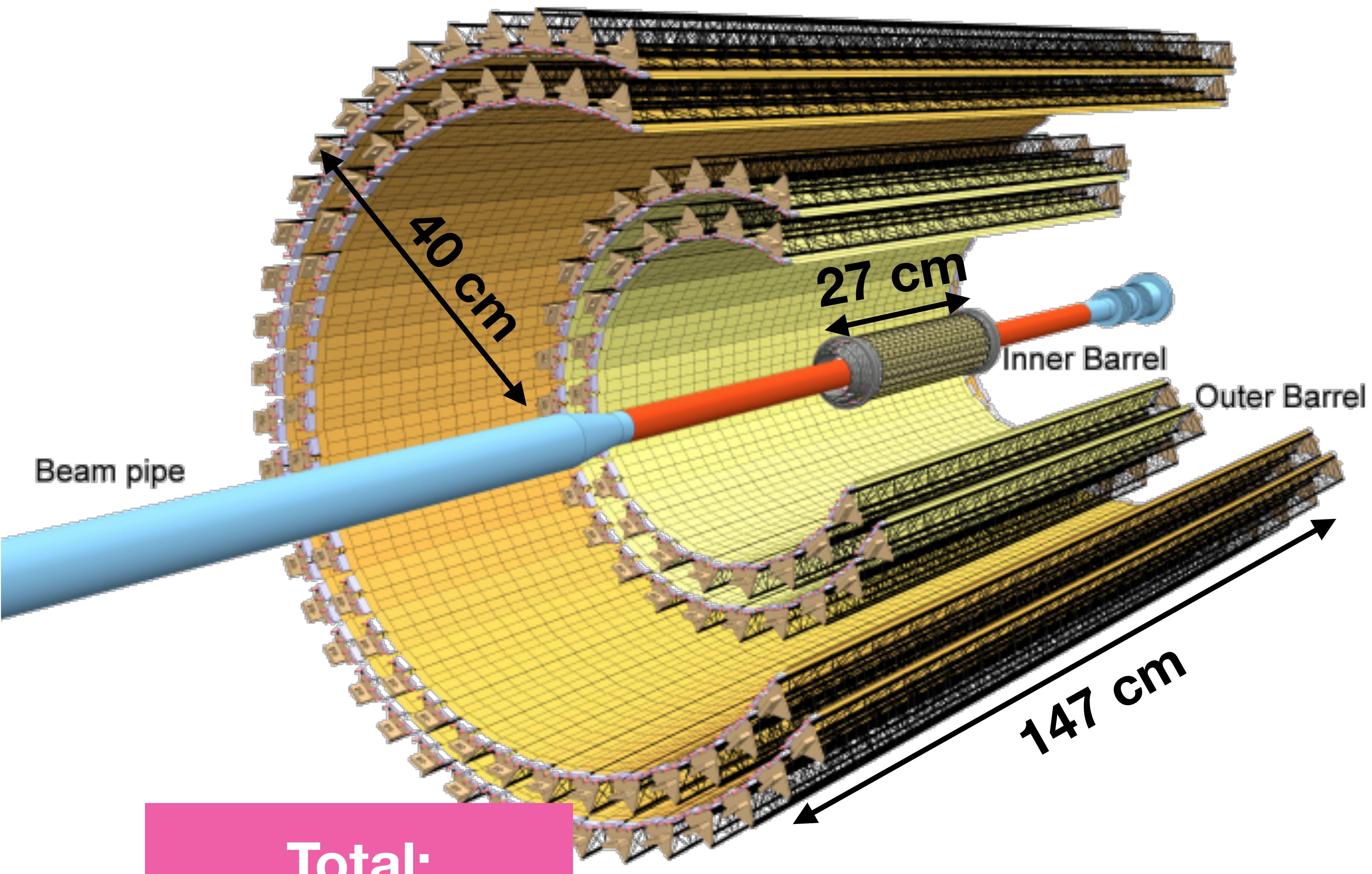
2×7 sensors / Module (Middle and Outer Layers are equipped with the same Module Type)

1880 Modules to be produced (including spares)

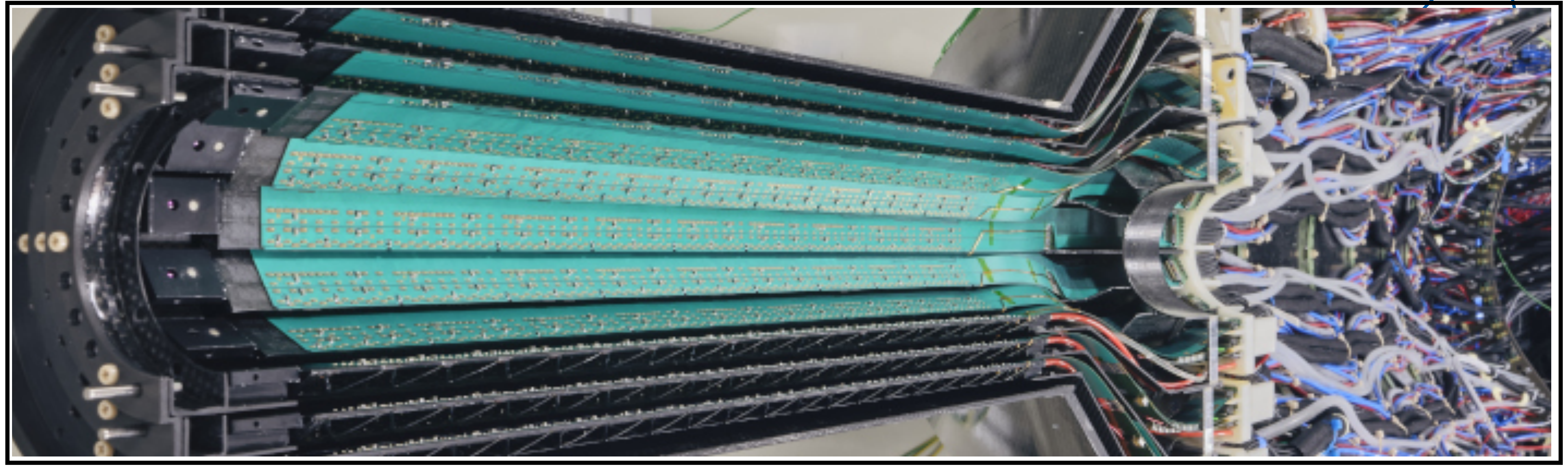


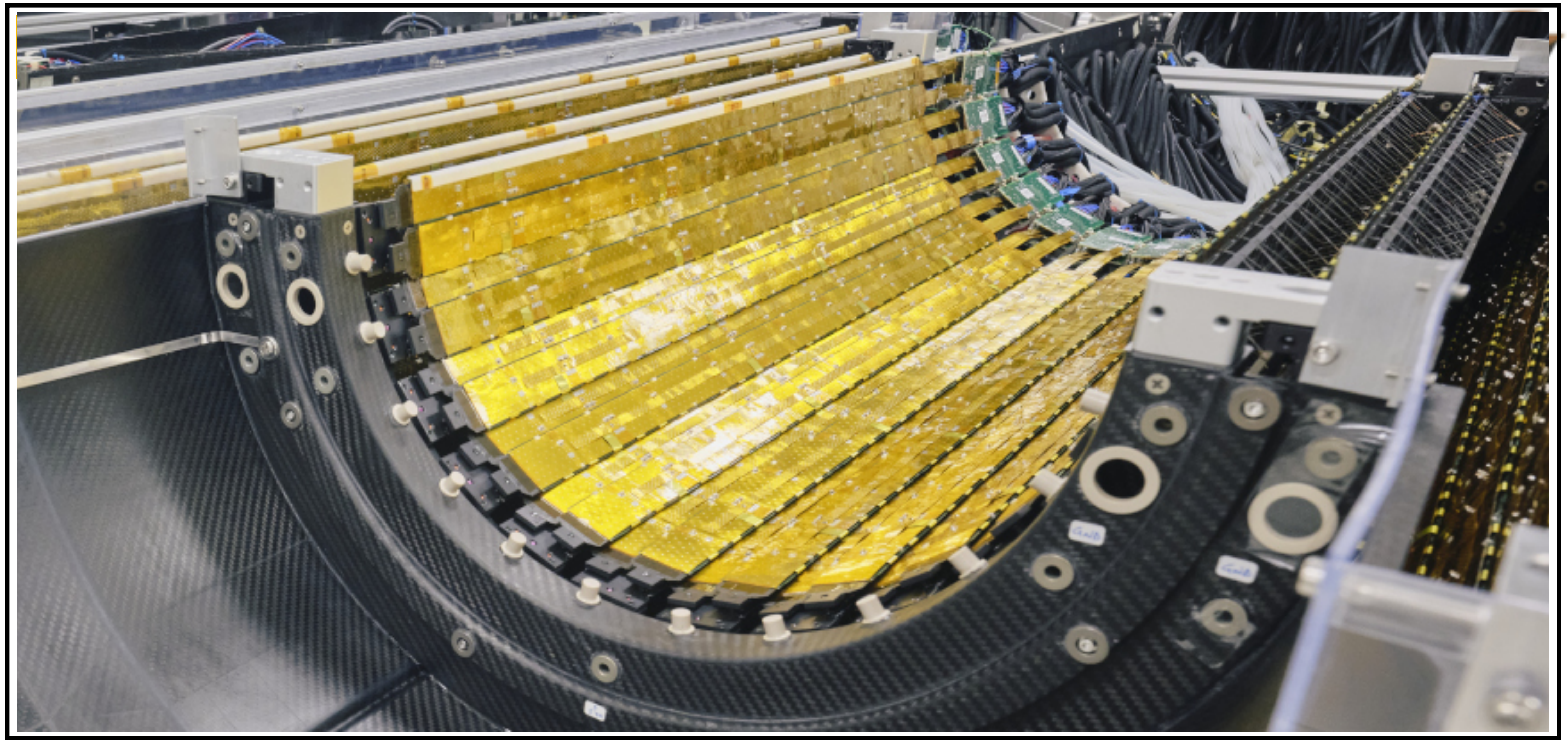
ITS2: overview

Layout

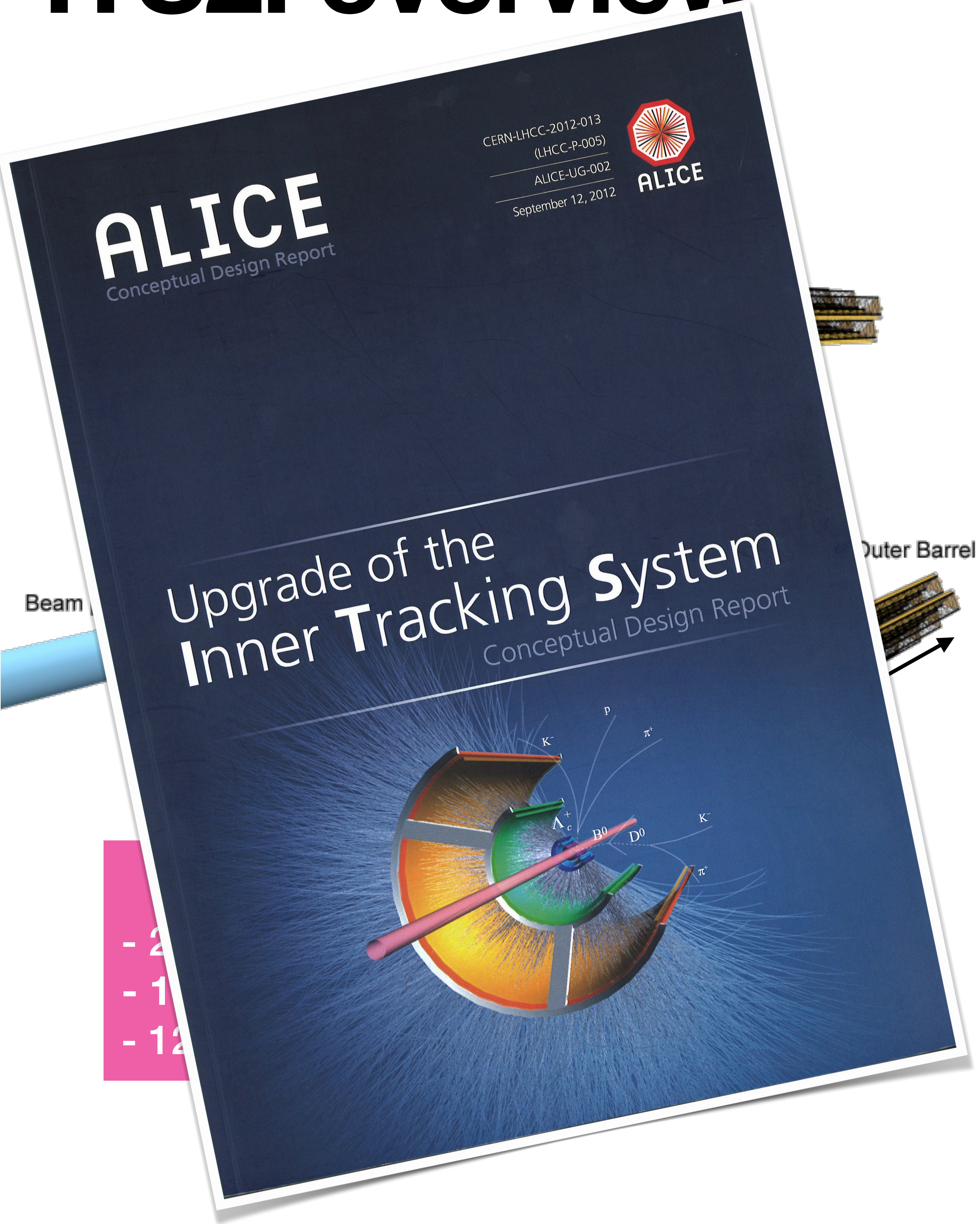


Total:
- 24k chips
- 10 m²
- 12.5 GPixel





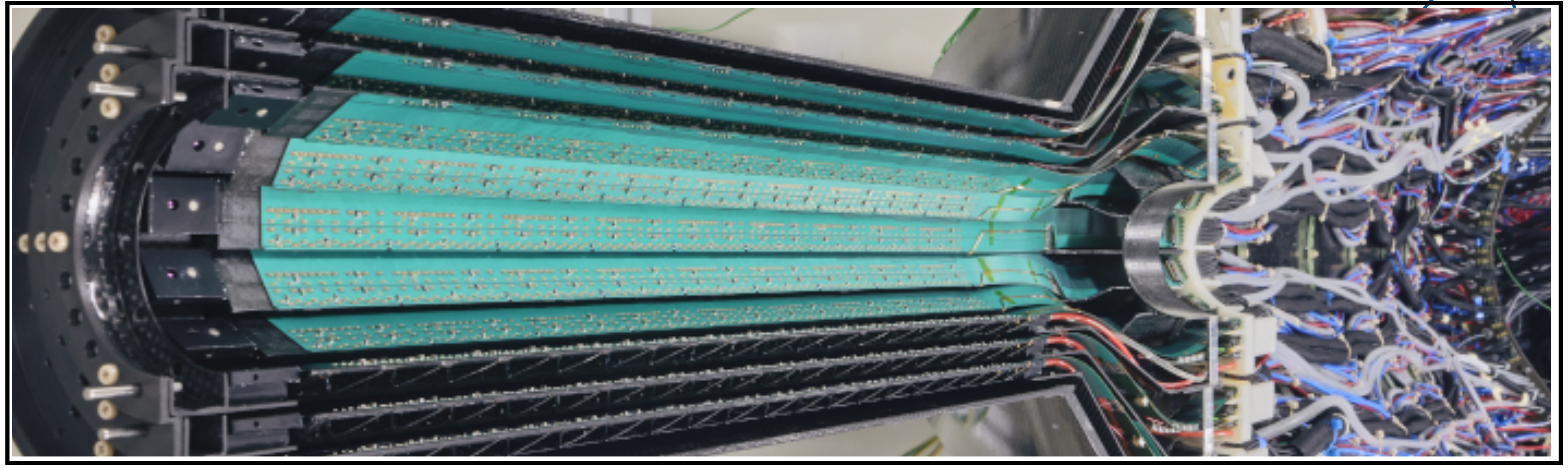
ITS2: overview

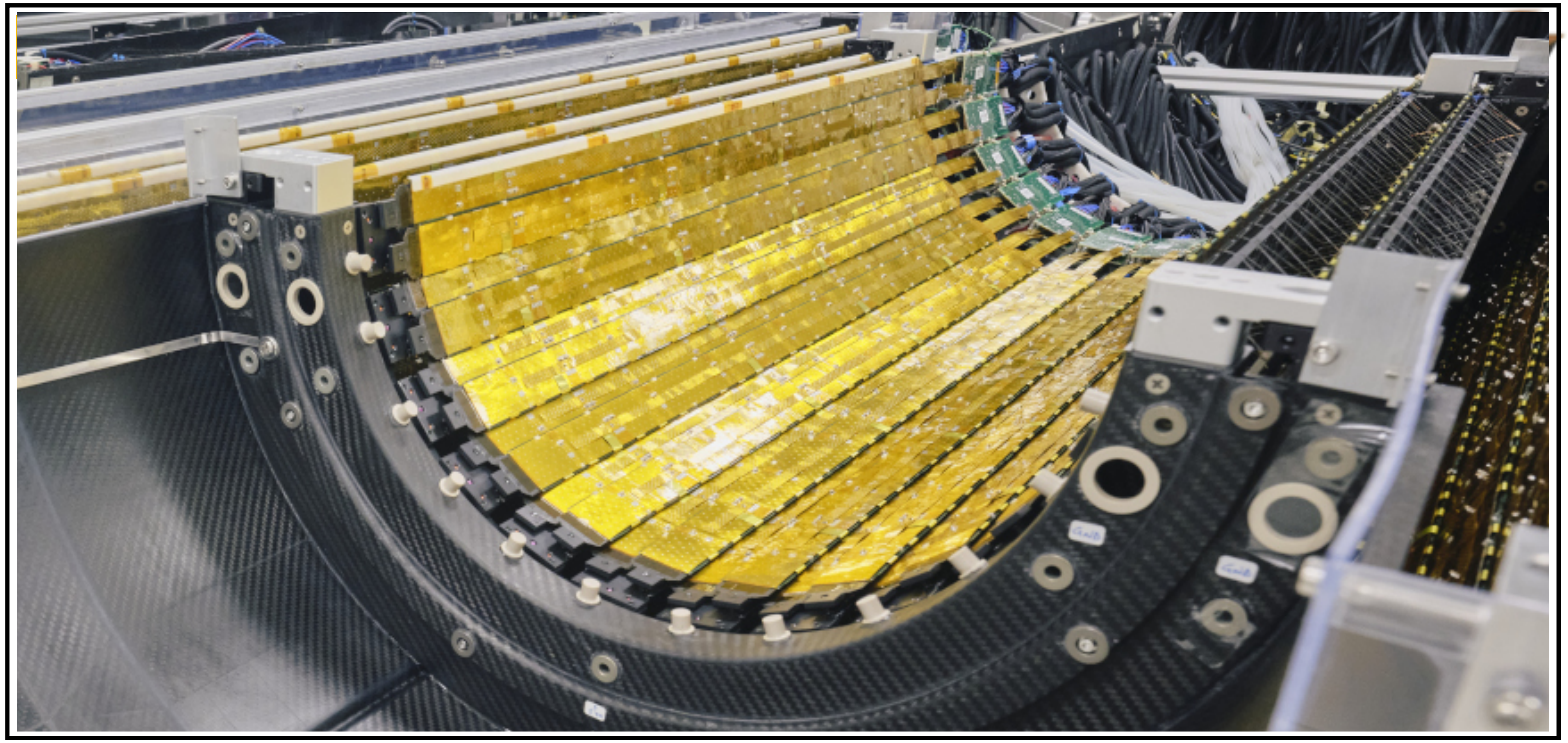


CERN-LHCC-2012-013
(LHCC-P-005)
ALICE-UG-002
September 12, 2012

ALICE
Conceptual Design Report

Upgrade of the
Inner Tracking System
Conceptual Design Report





ITS2: overview

Beam

- 2
- 1
- 12

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Conceptual Design Report

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ALICE
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CERN-LHCC-2013-024
ALICE-TDR-017
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CERNCOURIER
July/August 2021 cerncourier.com
Reporting on international high-energy physics

PIXEL
PERFECT

Exploring the Hubble tension
A CERN for climate change
Medical technologies

Beam

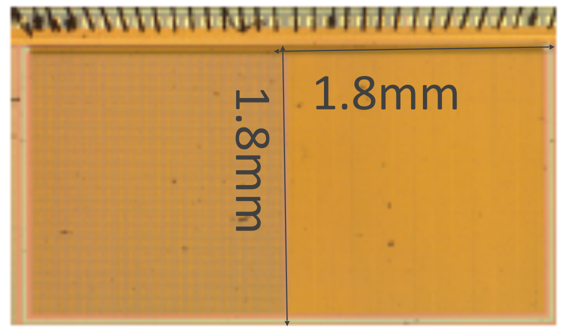
- 2
- 1
- 12

ITS2: sensor development

R&D path

2012	Explorer	- study of technology - detection diode geometry - starting materials - radiation hardness
2013	pALPIDEss	- digital front-end - priority-encoder readout
May 2014	**pALPIDE-1**	- full-scale sensor - simplified interface
Apr 2015	**pALPIDE-2**	- chip-chip communication interface - module integration - *slow-speed serial link*
Oct 2015	**pALPIDE-3**	- multiple-hit memory, final interfaces - last optimisation of pixel - *high-speed serial link (jitters)*
Aug 2016	**ALPIDE**	- final chip

Explorer



pALPIDEss

ITS2: ALPIDE

Parameter	Req.	ALPIDE
Spatial resolution (µm)	≈ 5	≈ 5
Integration time (µs)	< 30	< 10
Fake-hit rate (/pixel/event)	$< 10^{-6}$	$<< 10^{-6}$
Detection efficiency	> 99%	>>99%
Power density (mW/cm^2)	< 100	< 40
TID (krad)	> 270 (IB)	OK
NIEL (1 MeV n_{eq} / cm^2)	$> 1.7x10^{12}$	OK

ITS2: ALPIDE

> 70k chips produced and tested

24k in continuous operation on ITS2

+ several other applications

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Spatial resolution (µm)	≈ 5	≈ 5
Integration time (µs)	< 30	< 10
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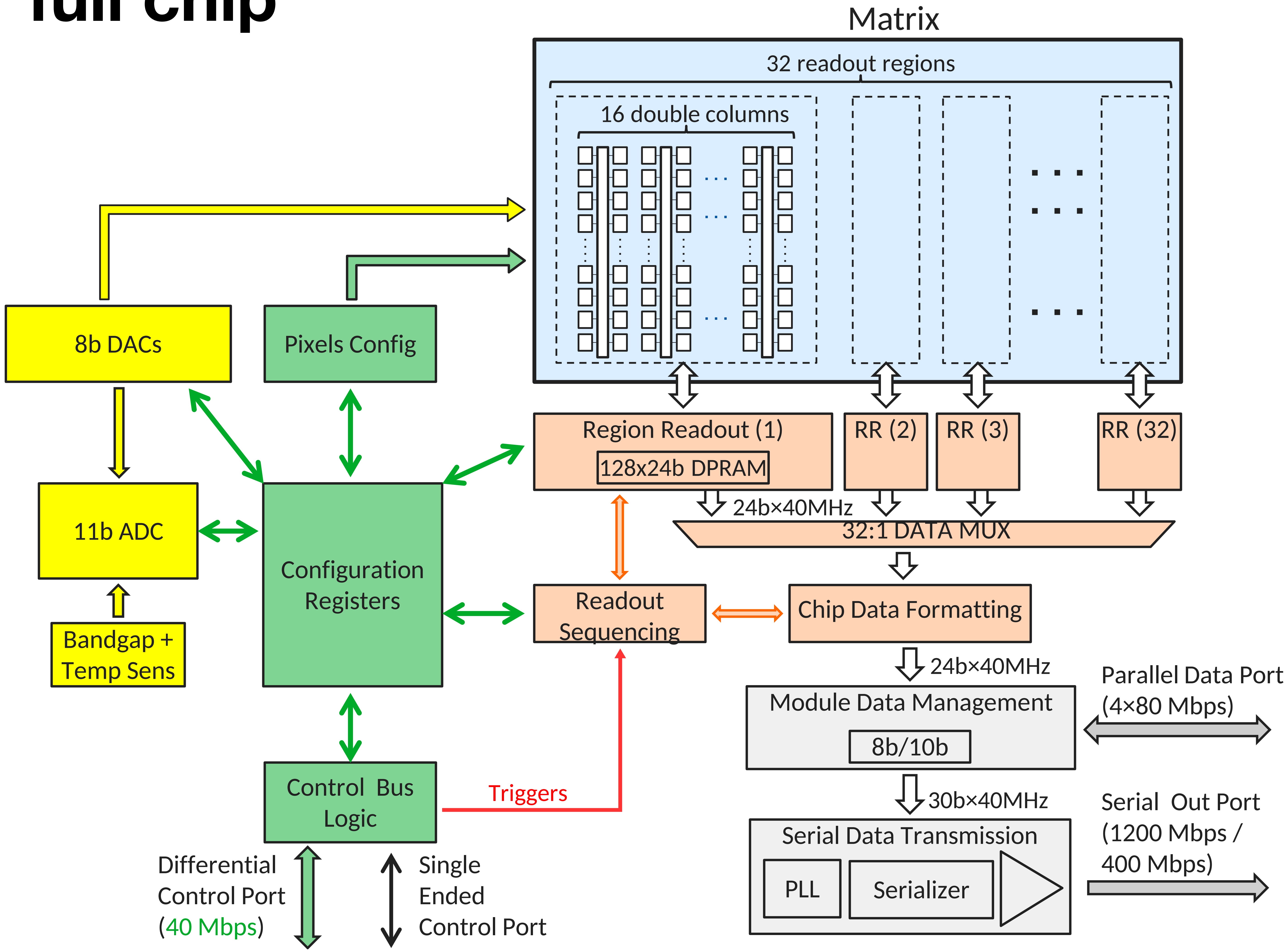
ITS2: ALPIDE

full chip



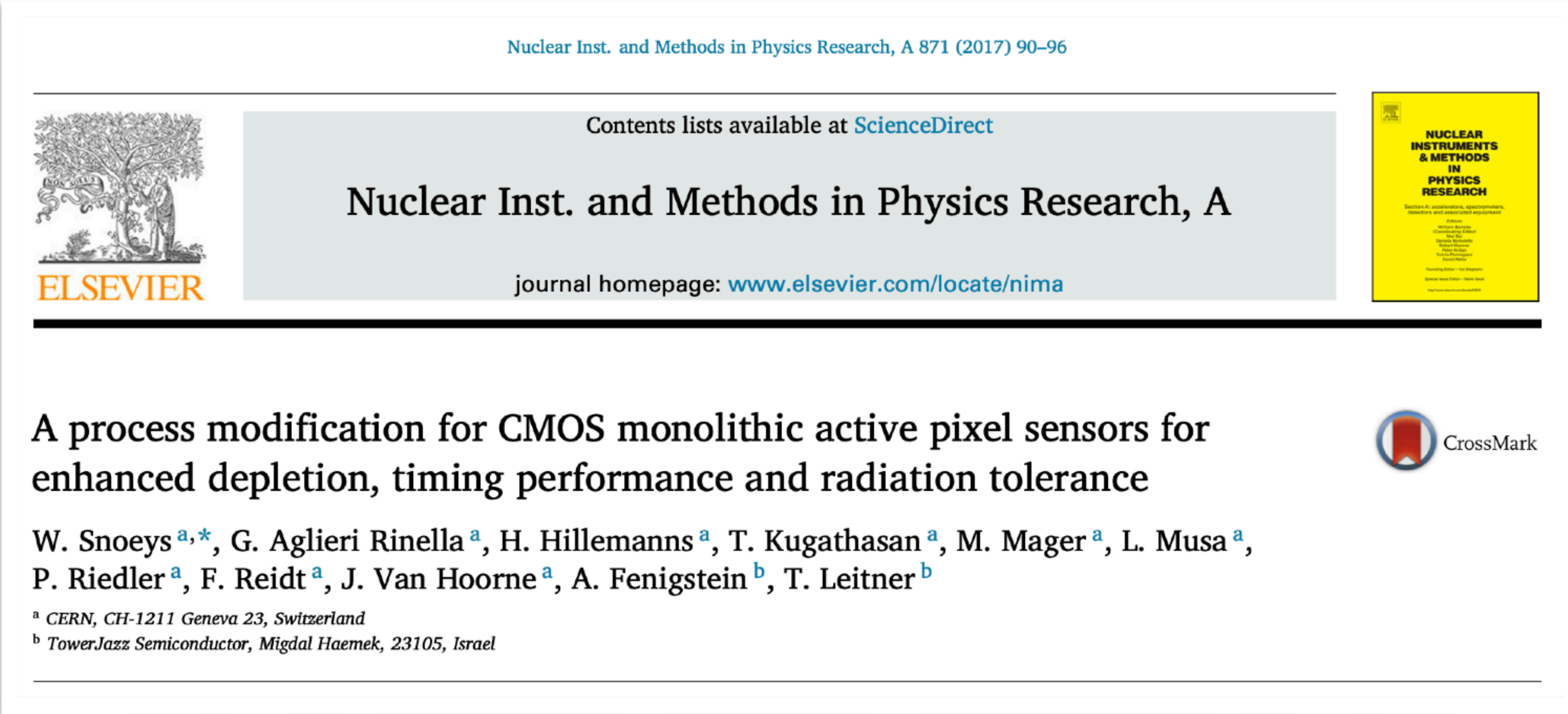
- **Fully integrated:**
  - next active circuit ≳ 8 m away off-detector
- **Strobing:**
  - global shutter
  - either triggered or in continuous sequence
- **Data interface:**
  - high-speed serial link using copper cables

much more than “just” the sensor matrix

ITS2 R&D: process modification

full depletion as “side development”

- Addition of a **low-dose n-implant**
  - developed together with foundry
- Opens up new applications
  - higher radiation hardness
  - faster charge collection
- Now crucial for the 65 nm development (it paid off also for ALICE!)



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journal homepage: www.elsevier.com/locate/nima

ELSEVIER

A process modification for CMOS monolithic active pixel sensors for enhanced depletion, timing performance and radiation tolerance

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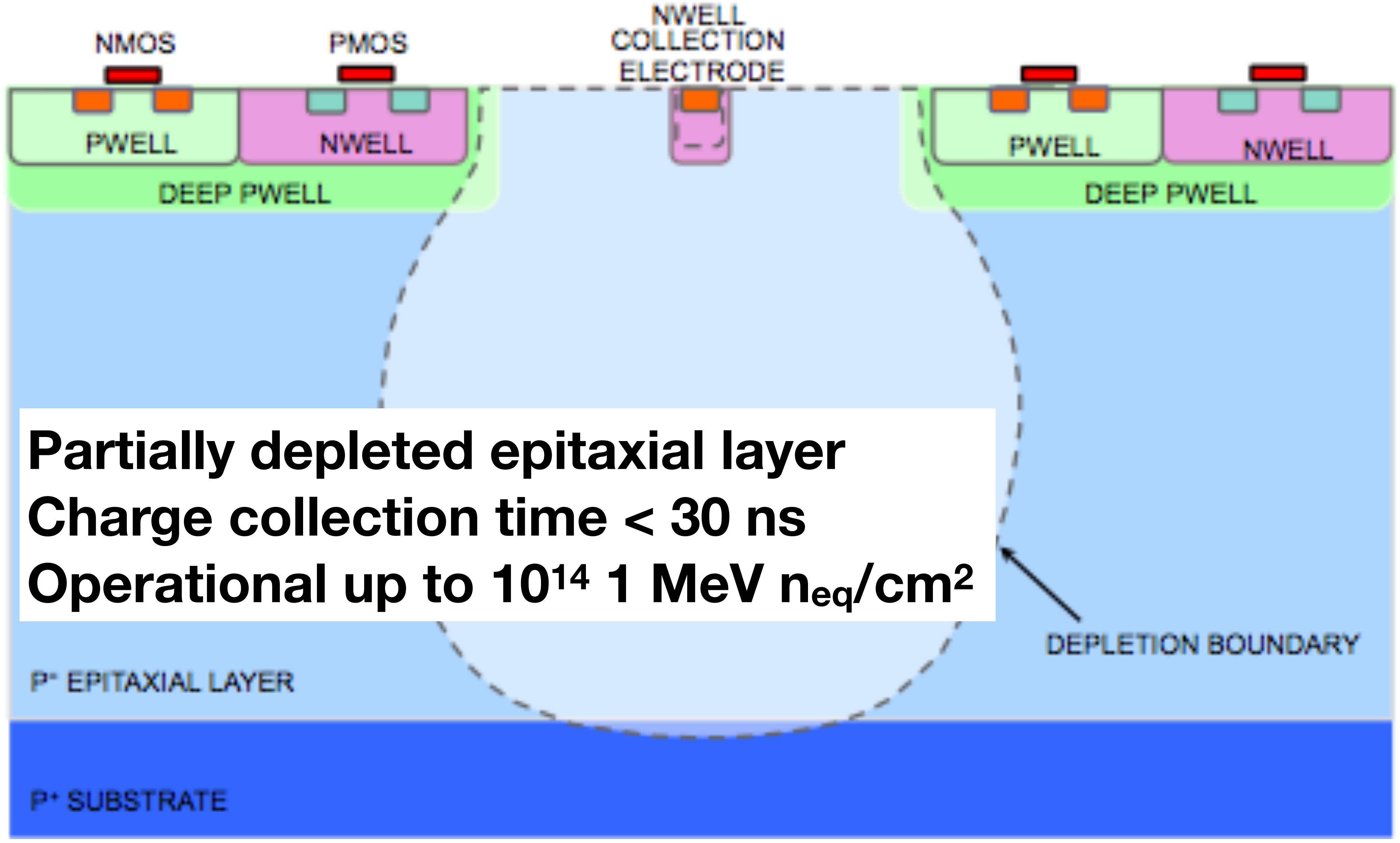
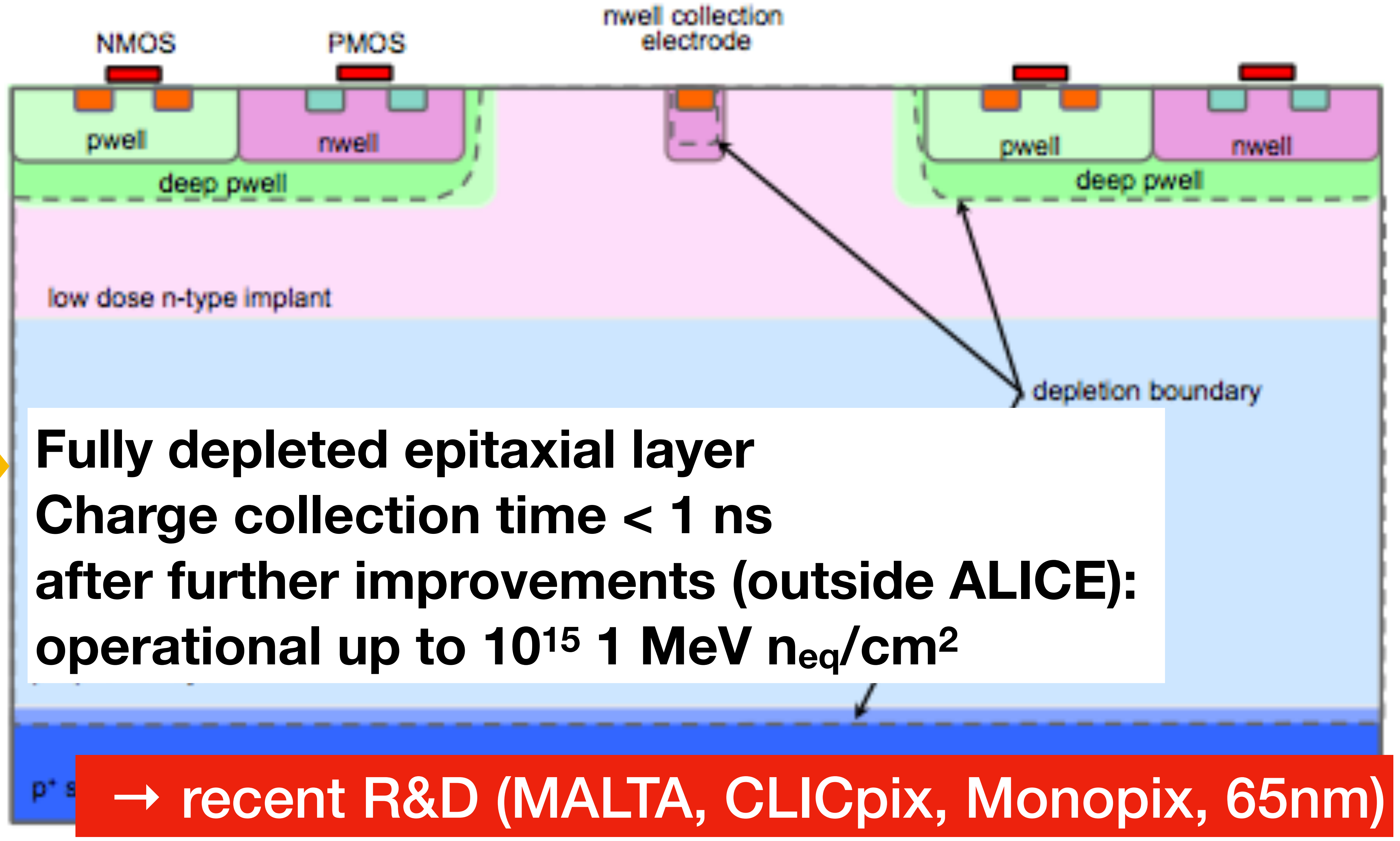
[doi:10.3390/s8095336]



Partially depleted epitaxial layer
Charge collection time < 30 ns
Operational up to 10^{14} 1 MeV n_{eq}/cm^2

Developed and prototyped within ALPIDE R&D

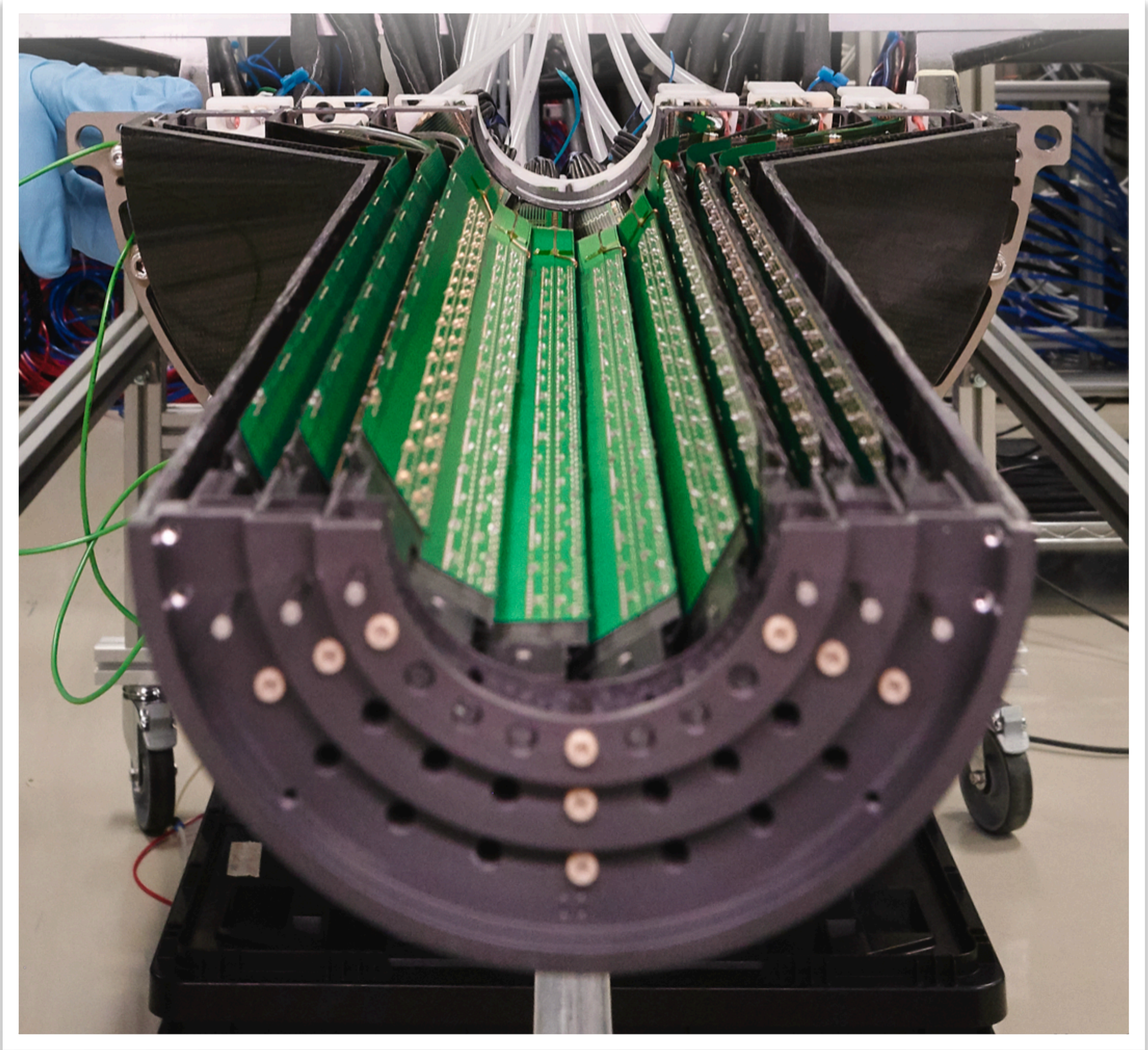


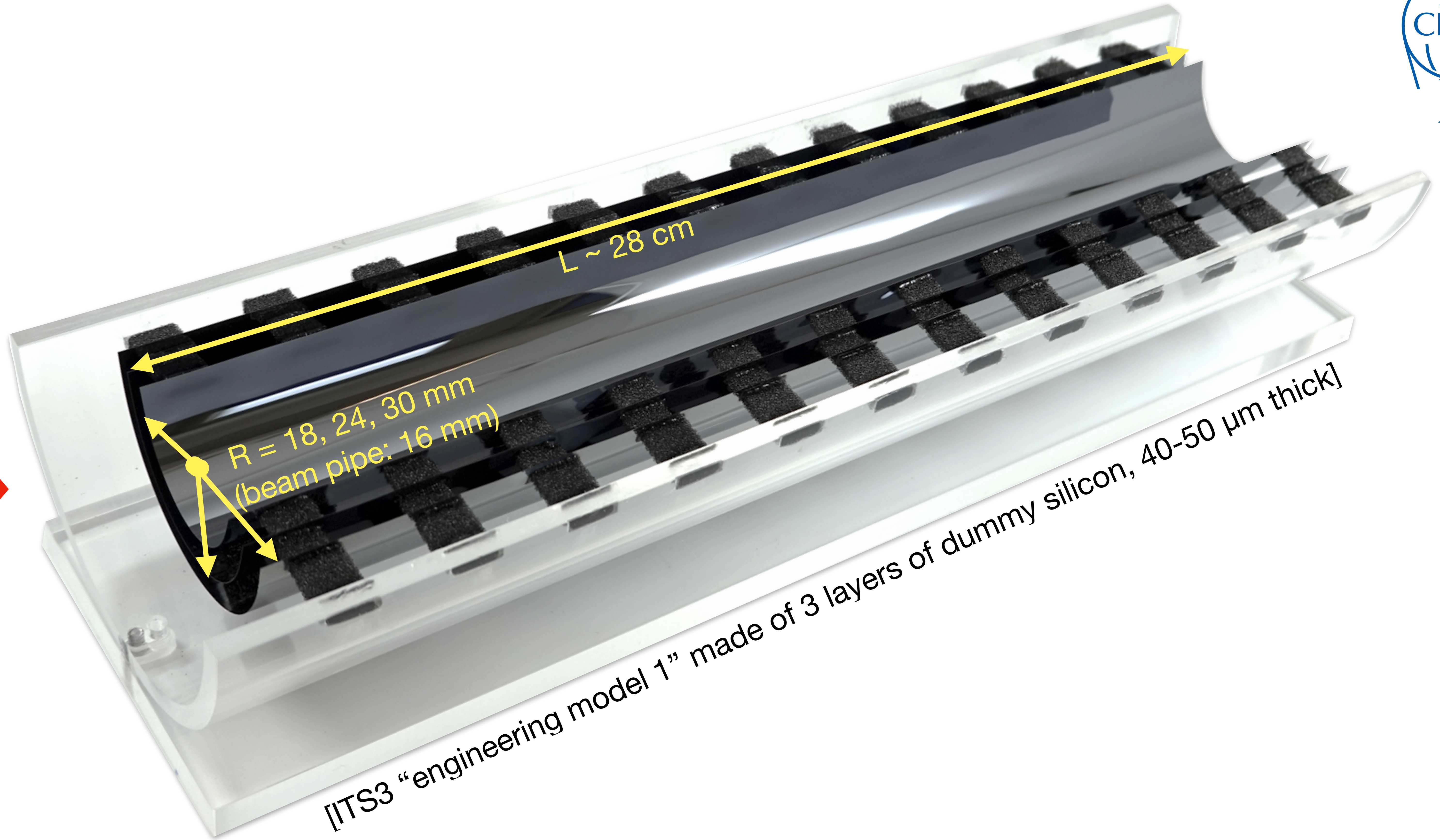
Fully depleted epitaxial layer
Charge collection time < 1 ns
after further improvements (outside ALICE):
operational up to 10^{15} 1 MeV n_{eq}/cm^2

→ recent R&D (MALTA, CLICpix, Monopix, 65nm)

ITS2 → ITS3

the concept





[ITS3 “engineering model 1” made of 3 layers of dummy silicon, 40-50 µm thick]

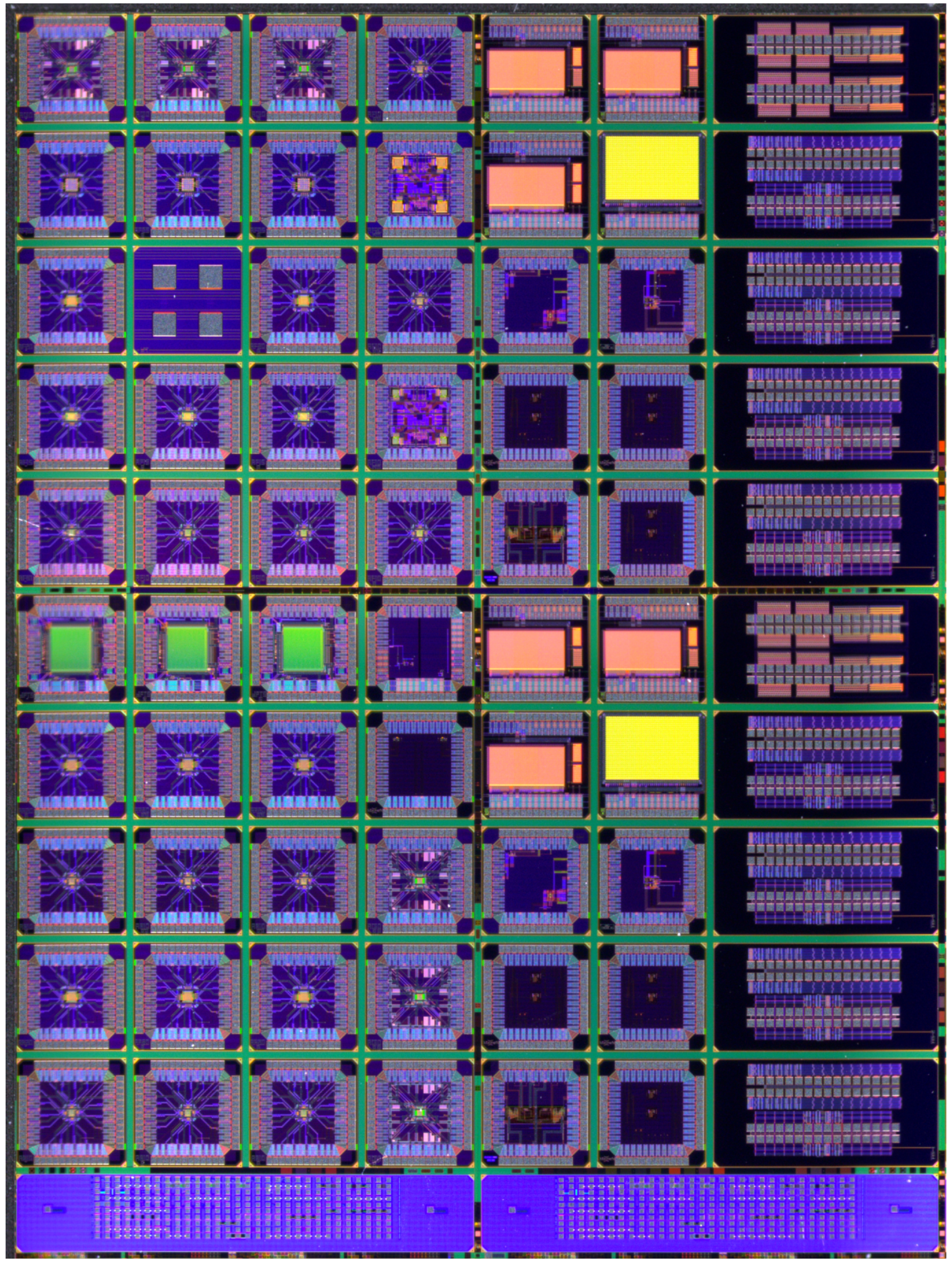
- Replacing the barrels by real half-cylinders (of **bent, thin** silicon)
- Rely on **wafer-scale sensors** (1 sensor per half-layer)
- Minimised material budget and distance to interaction point
  → large improvement of vertexing precision and physics yield (“**ideal detector**”)

Relies on the development of wafer-scale sensors

ITS3: 180 nm → 65 nm

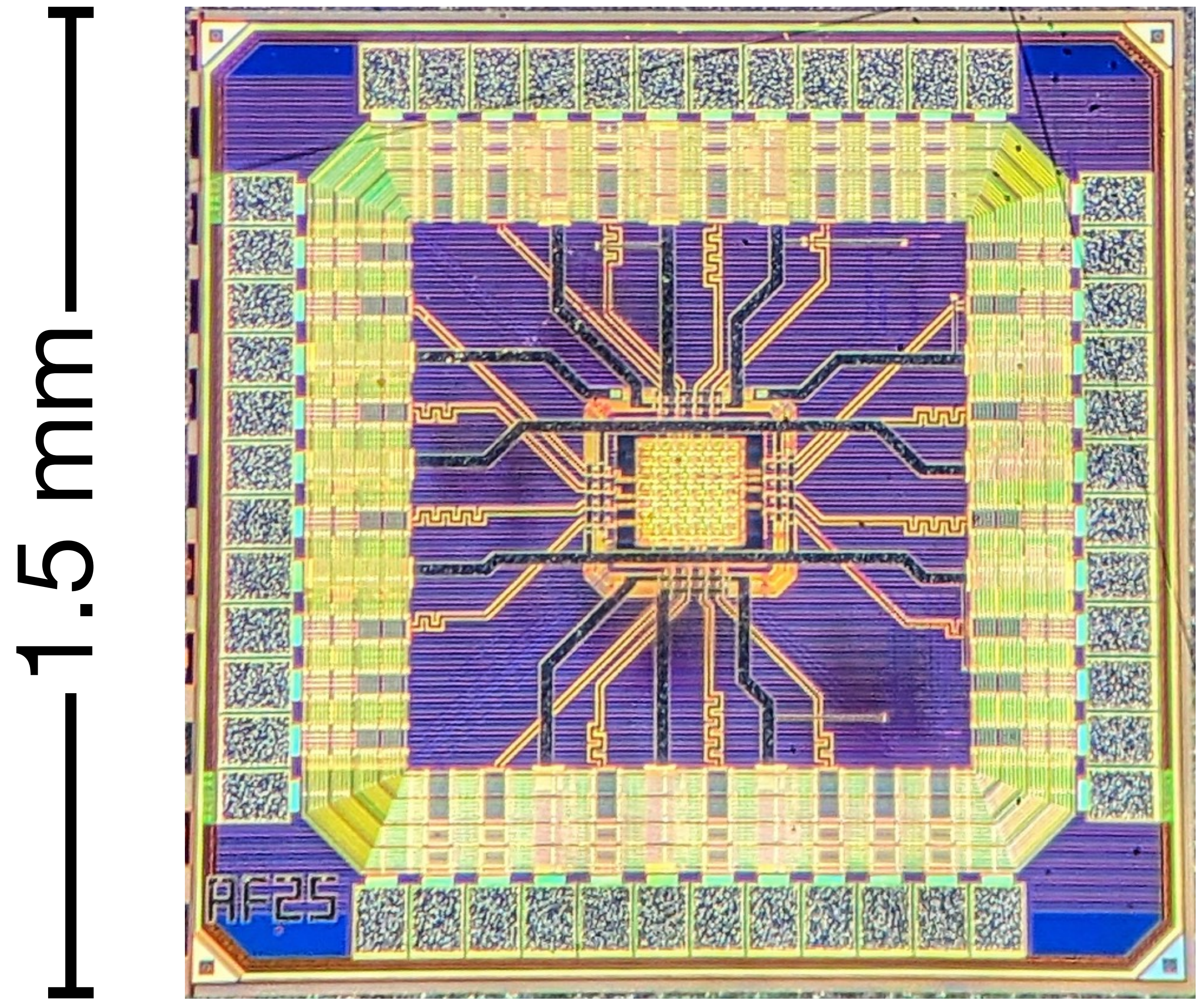
qualifying the TPSCo 65 nm CMOS Imaging Technology

- **Key benefits**
  - smaller features/transistors: higher integration density
  - smaller pitches
  - lower power consumption
  - **larger wafers** (200→300 mm)
- **Similar R&D plan as for 180 nm:**
  - small prototypes to characterise technology
  - then larger chips
  - **BUT:** technology node is more advanced, “larger” is larger by 1-2 orders of magnitude (stitching)
- **MLR1:** concentrated effort **ALICE ITS3** together with **CERN EP R&D**
  - leverages on experience with 180 nm (ALPIDE)
  - excellent links to foundry
  - large support form **CERN** (EP department and EP/ESE group)
  - Comprehensive *first* submission: **55** prototype chips
  - goal: qualify the technology (achieved)



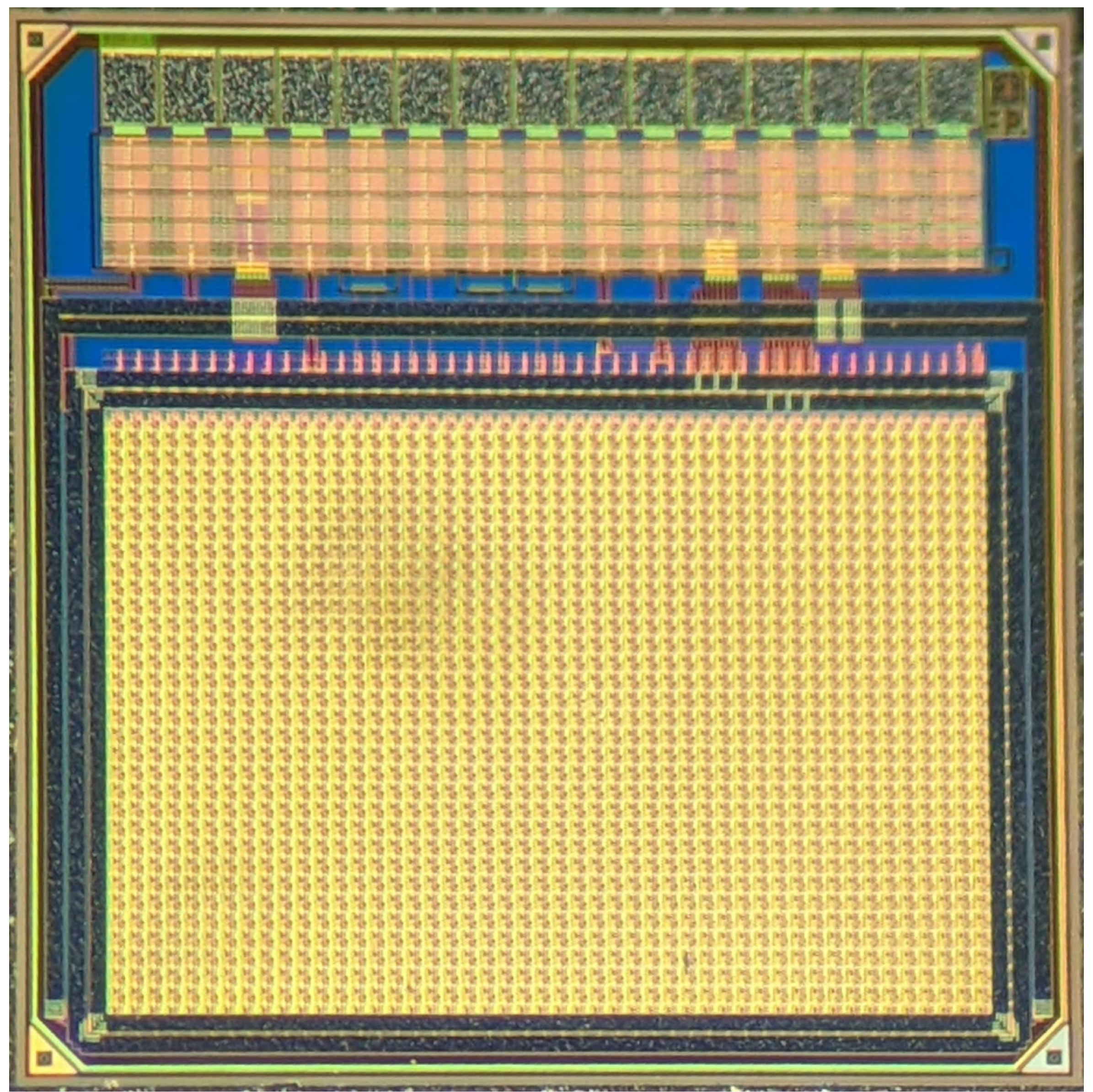
ITS3: pixel prototype chips (selection)

APTS



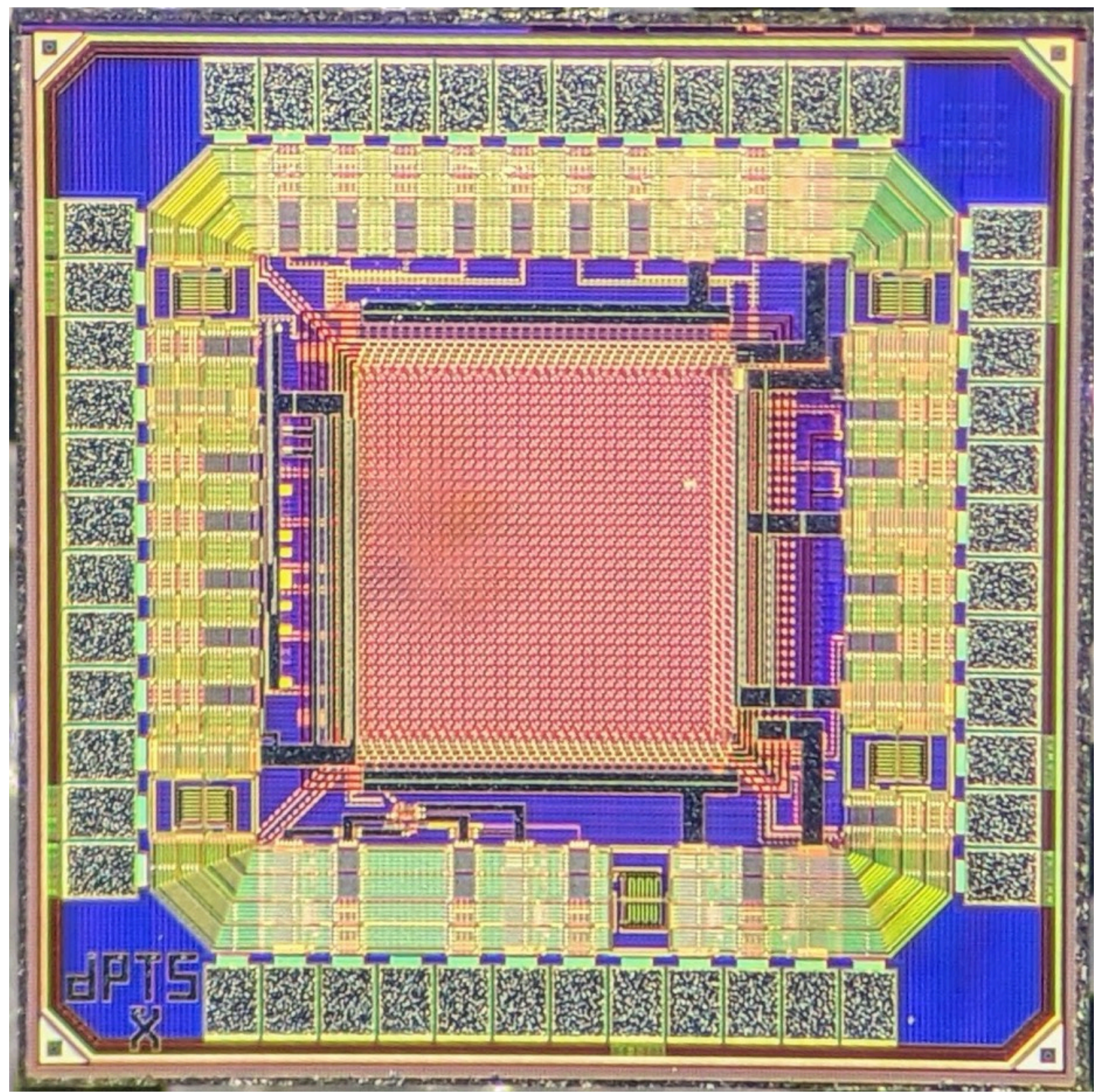
- **matrix:** 6x6 pixels
- **readout:** direct analog readout of central 4x4
- **pitch:** 10, 15, 20, 25 µm
- **total:** 34 dies

CE65



- **matrix:** 64x32, 48x32 pixels
- **readout:** rolling shutter analog
- **pitch:** 15, 25 µm
- **total:** 4 dies

DPTS



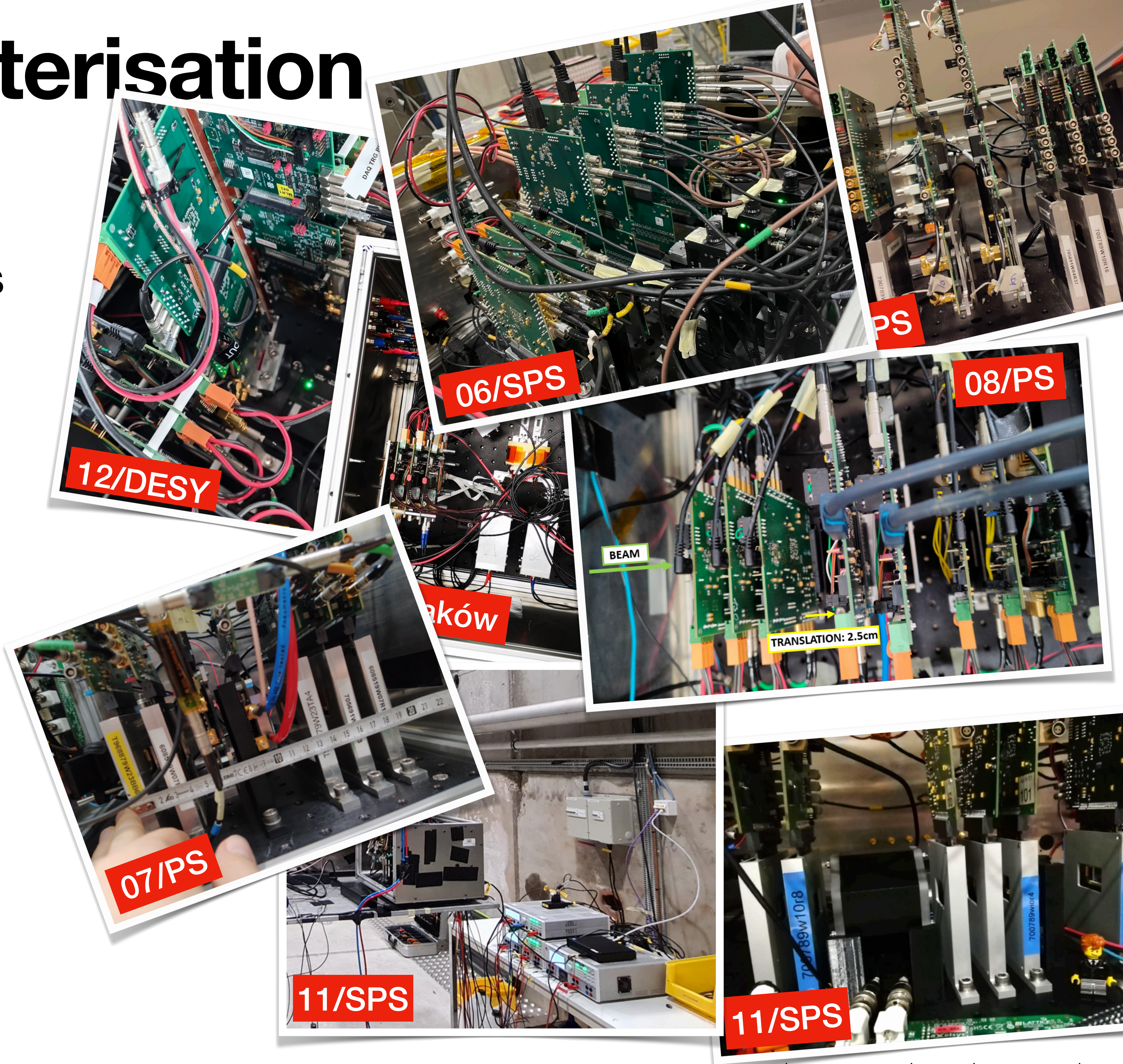
- **matrix:** 32x32 pixels
- **readout:** async. digital with ToT
- **pitch:** 15 µm
- **total:** 3 dies

Comprehensive set of (small) prototypes and variants to explore the technology for particle detection

ITS3: sensor characterisation

example: test beams

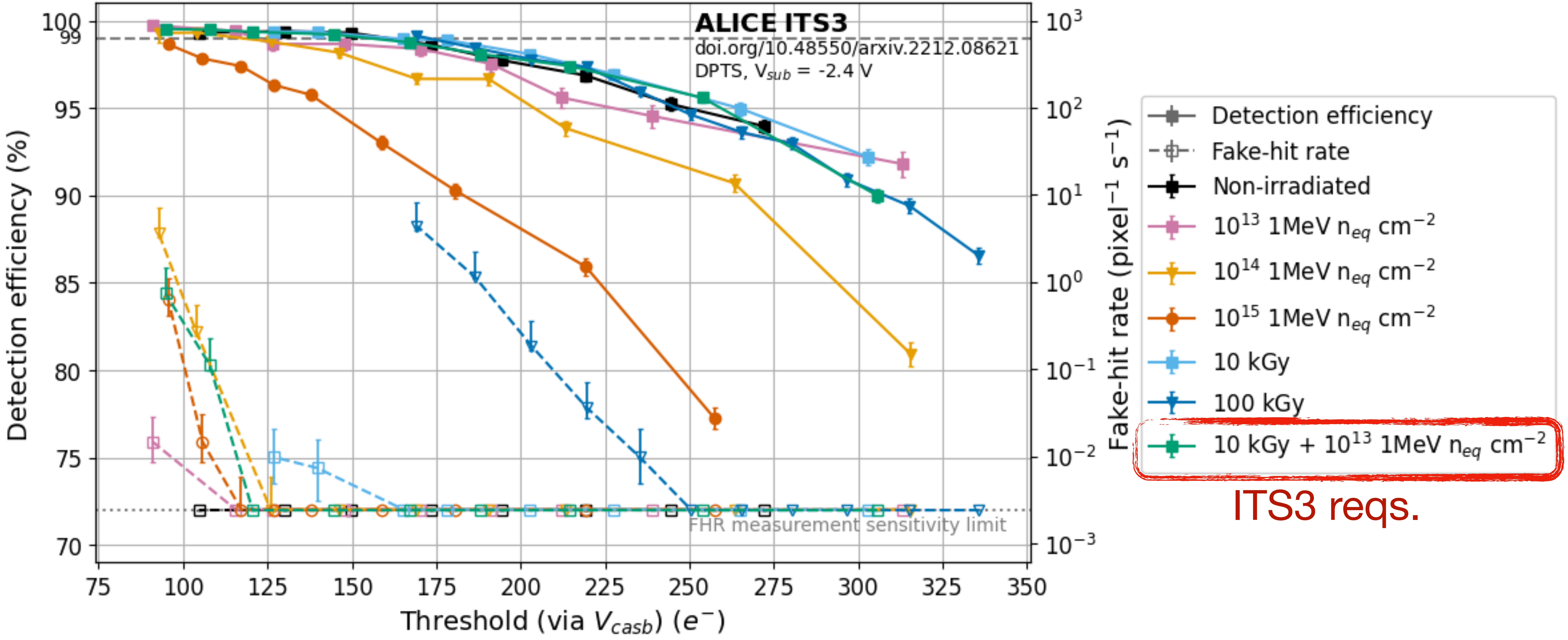
- Large effort by several ALICE groups
  - groups/links/education
- Test beams with a cadence of > 1/month
  - several facilities
  - several groups
  - unified test system (in-house, targeted development)
- comprehensive datasets
  - including less standard configurations (e.g. beam energies)



ITS3: DPTS paper (65 nm)

[doi:10.48550/arXiv.2212.08621]

highlights



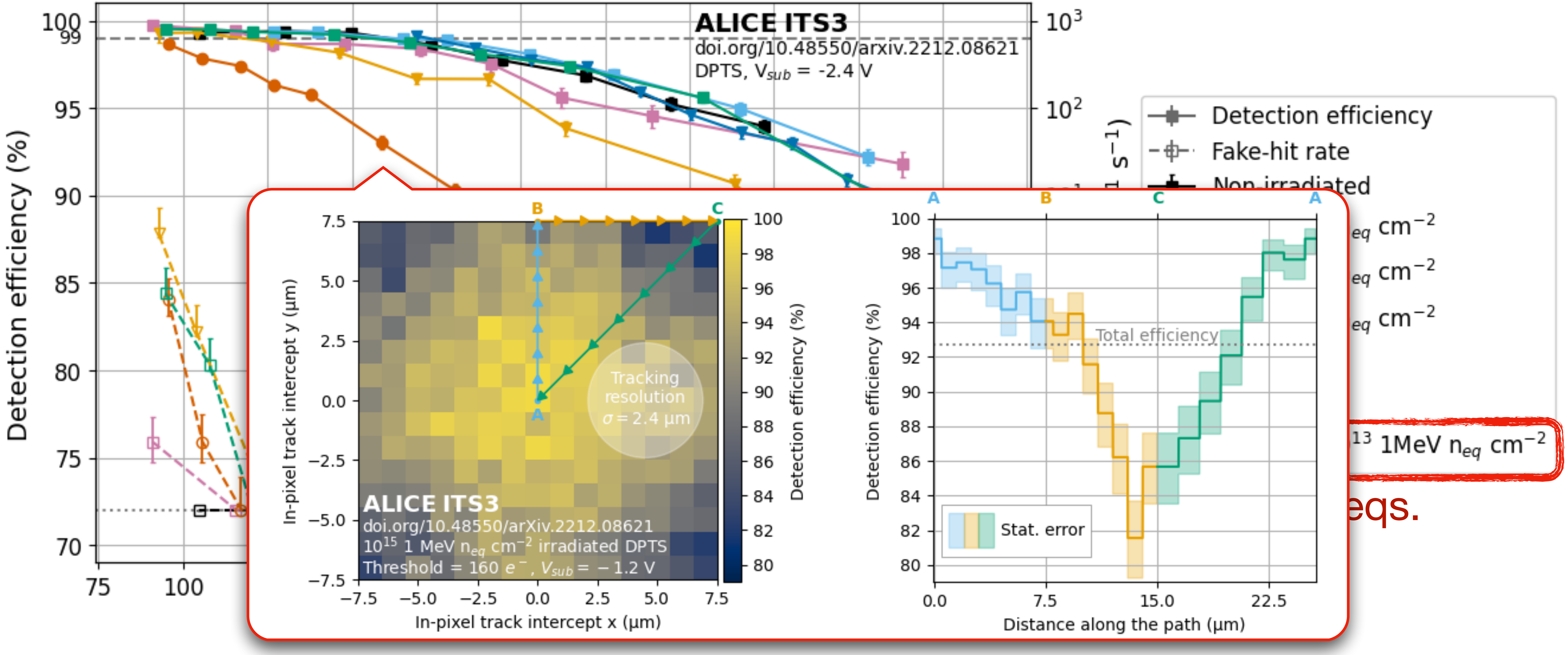
ITS3 reqs.

First comprehensive paper on 65 nm — summarises 1 year of mesaurements

ITS3: DPTS paper (65 nm)

[doi:10.48550/arXiv.2212.08621]

highlights

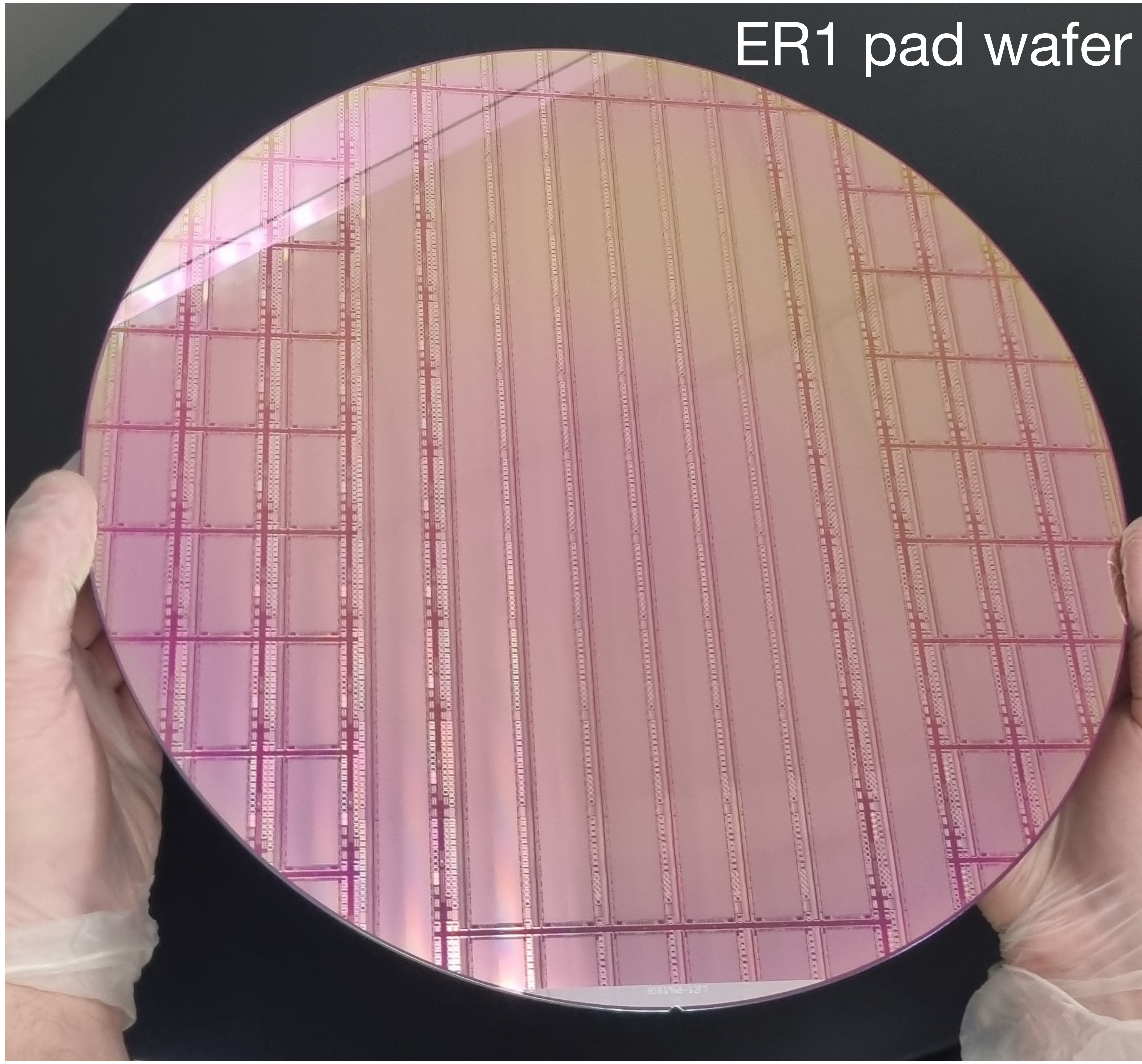


First comprehensive paper on 65 nm — summarises 1 year of mesaurements

ITS3: Wafer-scale sensors

Engineering Run 1 (ER1)

- Submitted in Dec’22
  - pad wafers: beg. Mar
  - processed wafers: end Mar (tbc)
- “**MOSS**”: 14 x 259 mm, 6.72 MPixel (22.5 x 22.5 and 18 x 18 μm²)
  - conservative design, different pitches
- “**MOST**”: 2.5 x 259 mm, 0.9 MPixel (18 x 18 μm²)
  - more dense design
- Plenty of small chips (like MLR1)


ER1 pad wafer

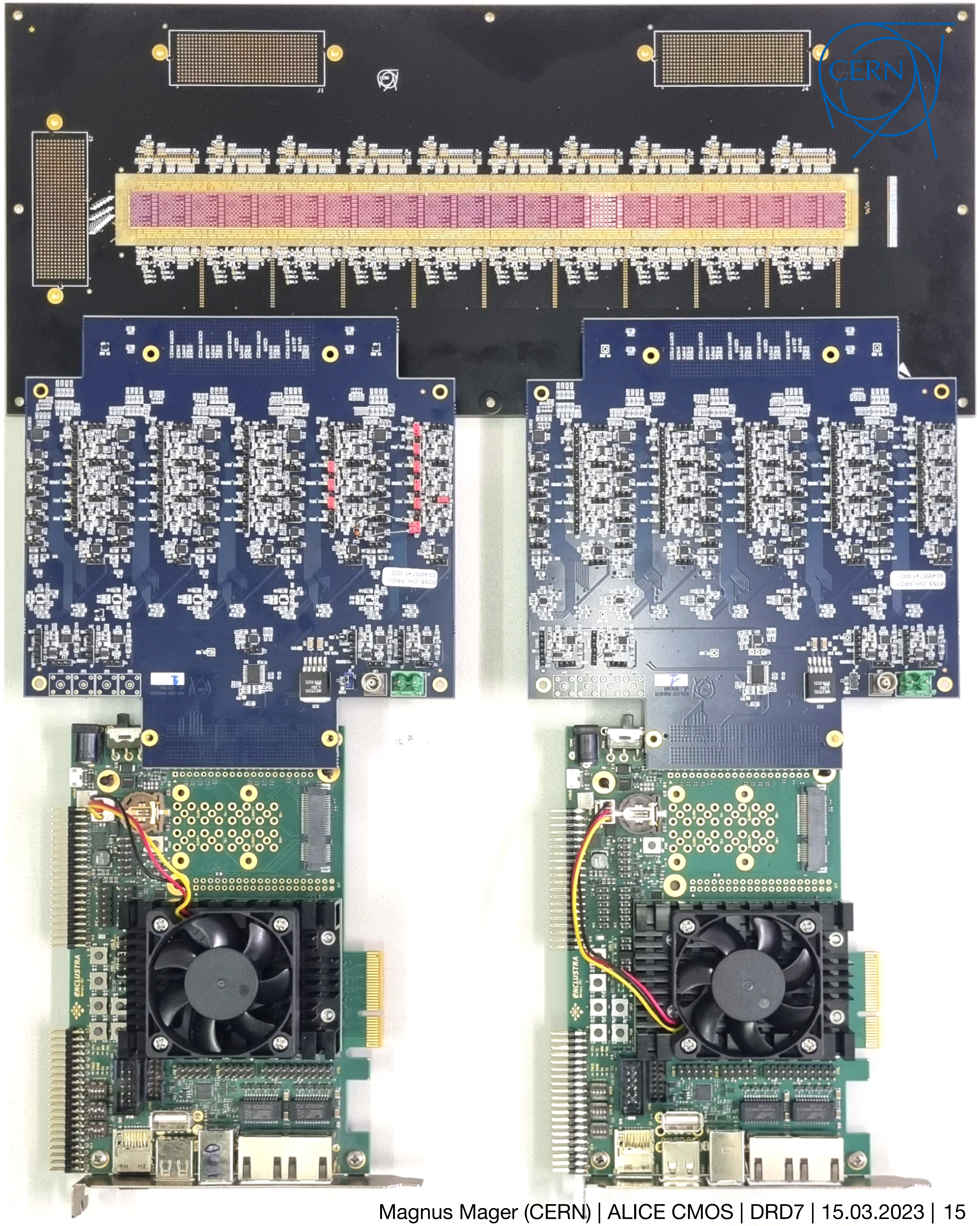
ITS3: ER1 testing preparation

MOSS test system

- In-house development
  - tailored to MOSS chip

- Based on:
  - carrier card (passive; custom made)
  - 5x proximity card (active; custom made)
  - 5x FPGA board (commercial: enclustra Mercury+ AA1+PE1)

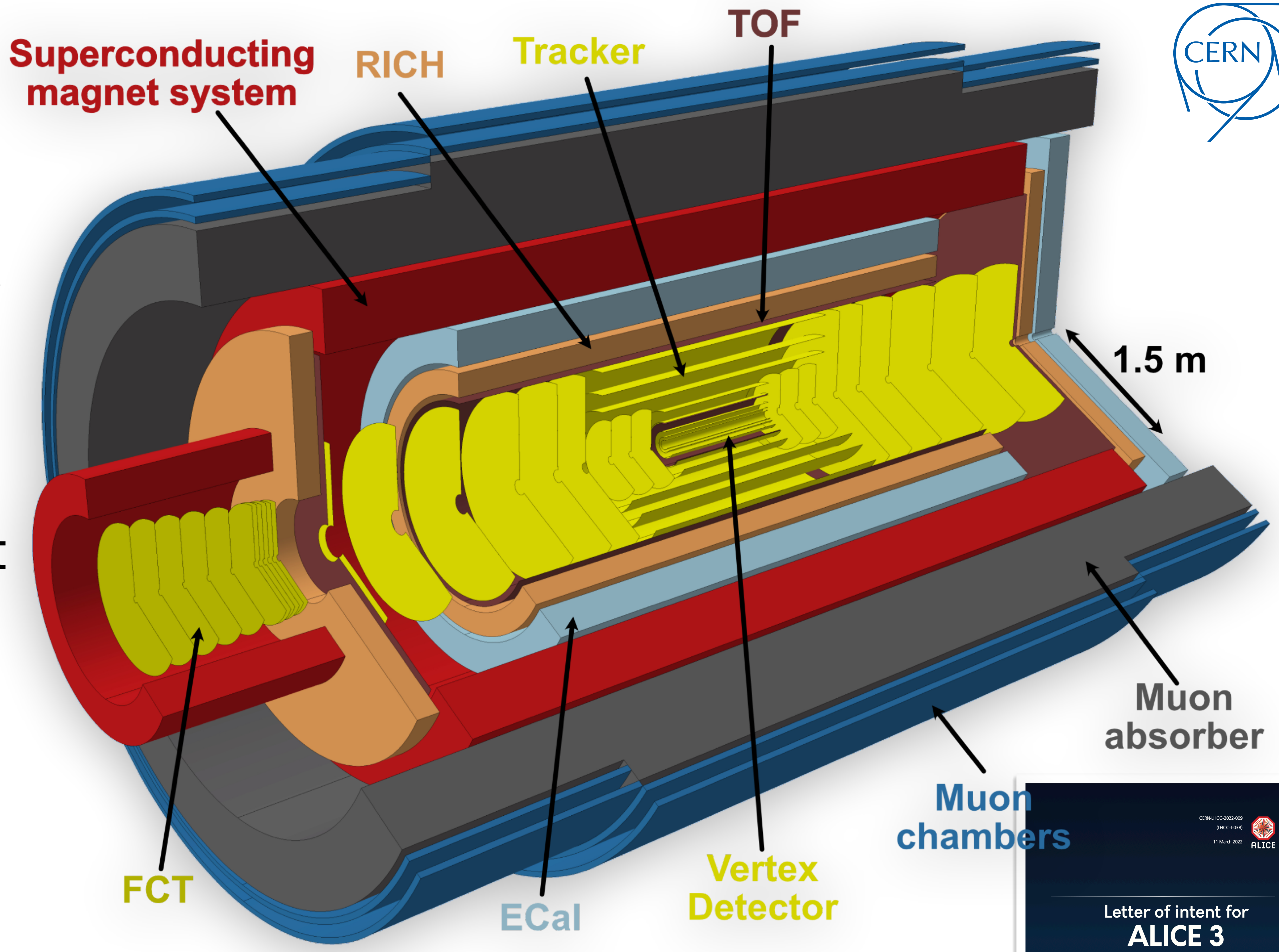
- Crucial activity involving quite a number of people

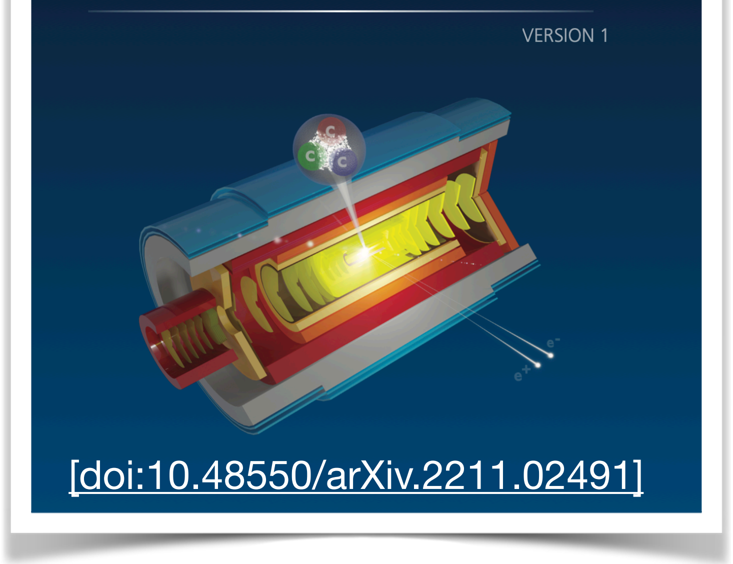


ALICE 3

outlook

- ALICE 3 is centred around a 60 m² MAPS tracker
  - innermost layers will be based on wafer-scale Silicon sensors “iris tracker”, similar to ITS3 (but in vacuum)
  - outer tracker will be based on modules like ITS2 (but order of magnitude larger)
- Also TOF and RICH based on CMOS technology (baseline)
- *This is the next big and concrete step for this technology*




CERN-LHCC-2022-009
(LHCC-I-038)
11 March 2022

ALICE

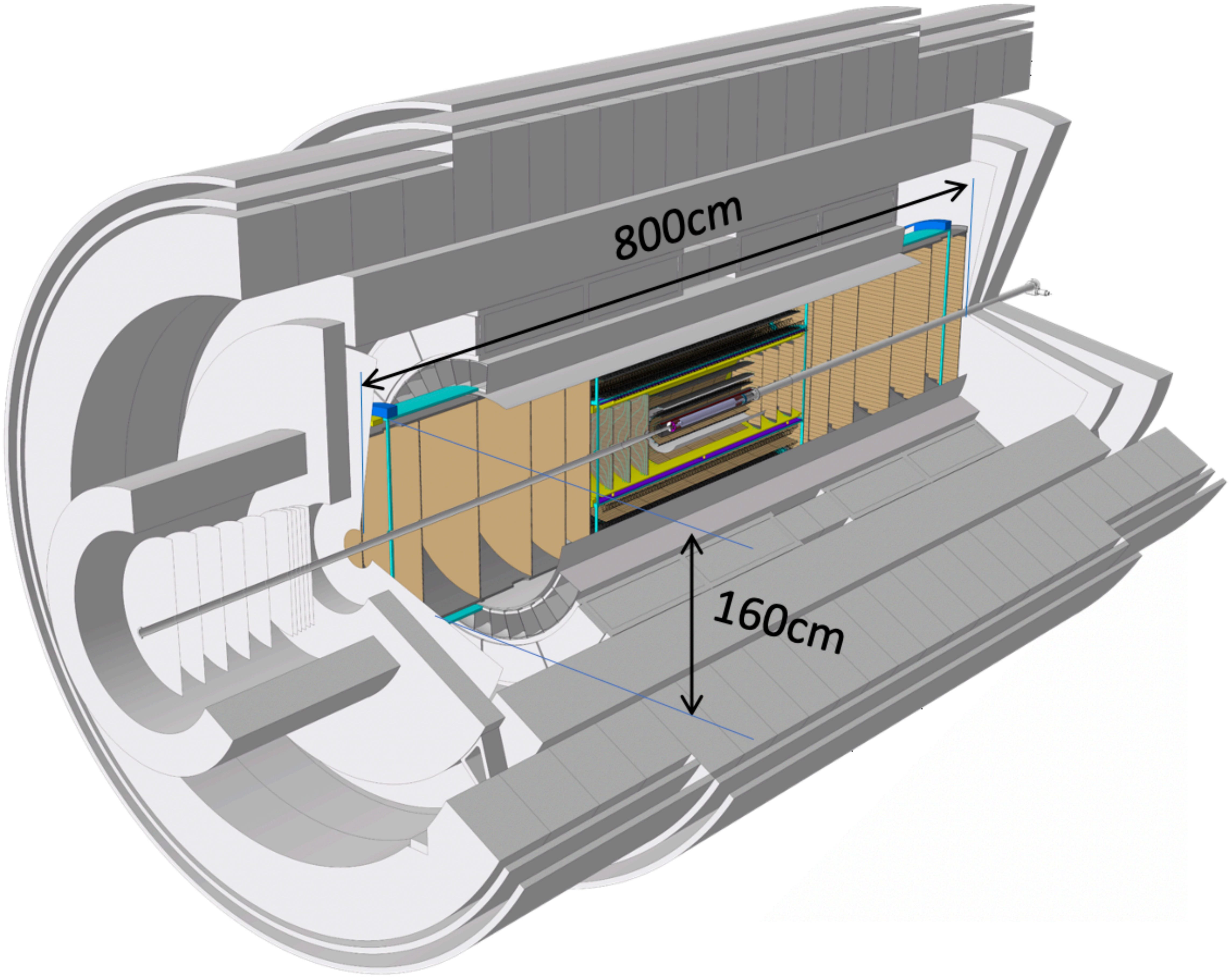
Letter of intent for
ALICE 3

VERSION 1

[doi:10.48550/arXiv.2211.02491]

ALICE 3

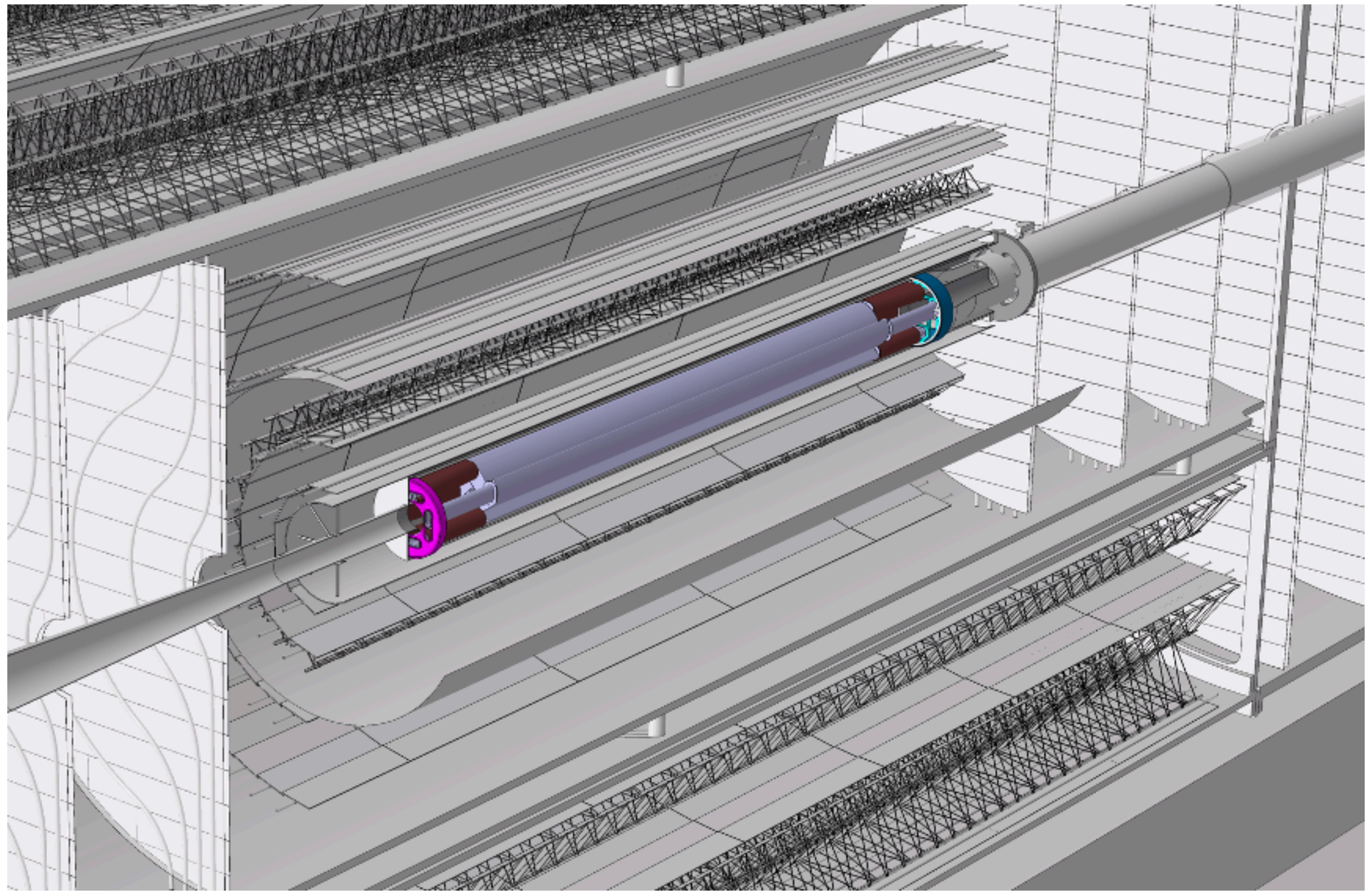
Outer tracker

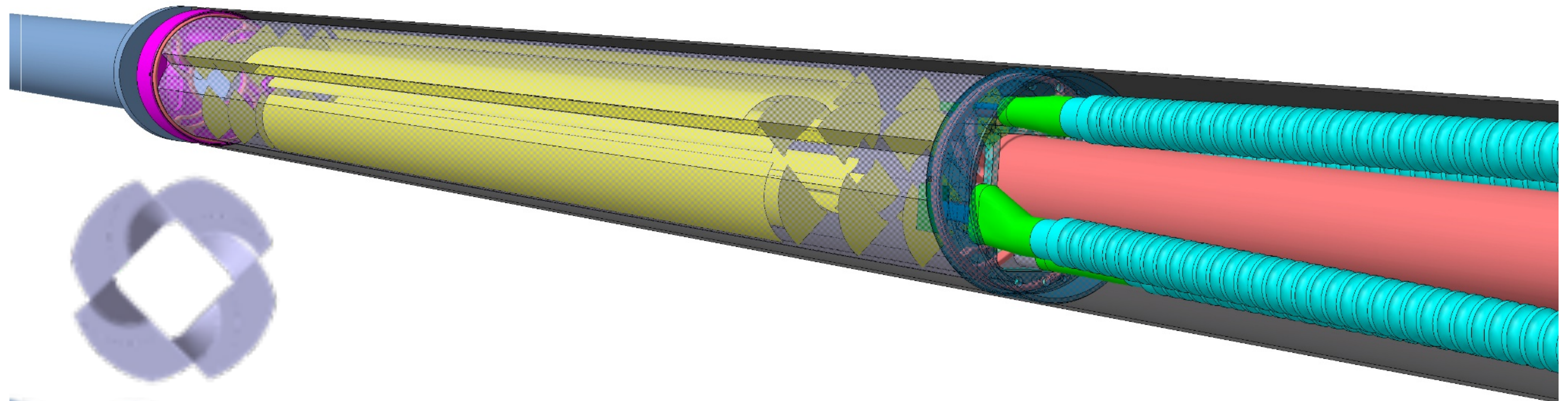


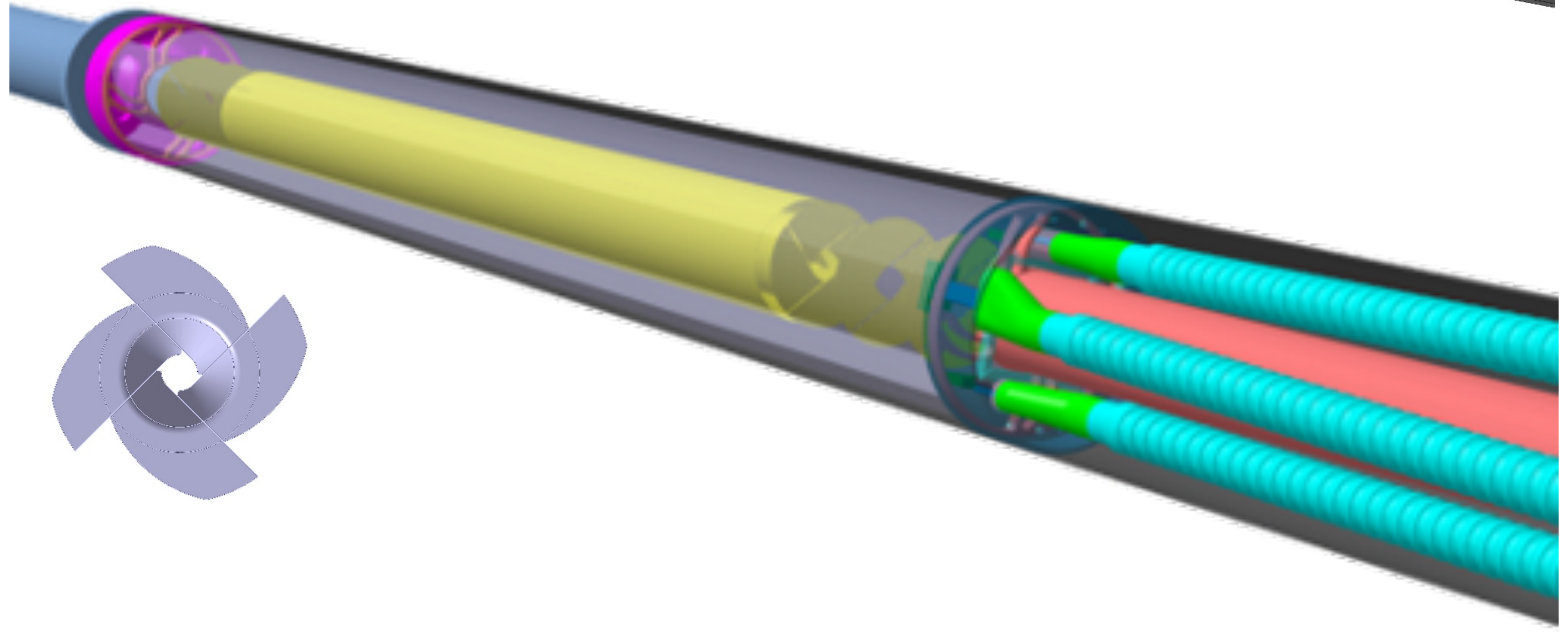
- **60 m² silicon pixel detector**
  - large coverage: ±4η
  - high-spatial resolution: ≈ 5 μm
  - very low material budget: X/X_0 (total) ≲ 10%
  - low power: ≈ 20 mW/cm²
- module (O(10 x 10 cm²)) concept based on industry-standard processes for assembly and testing

ALICE 3

Vertex detector



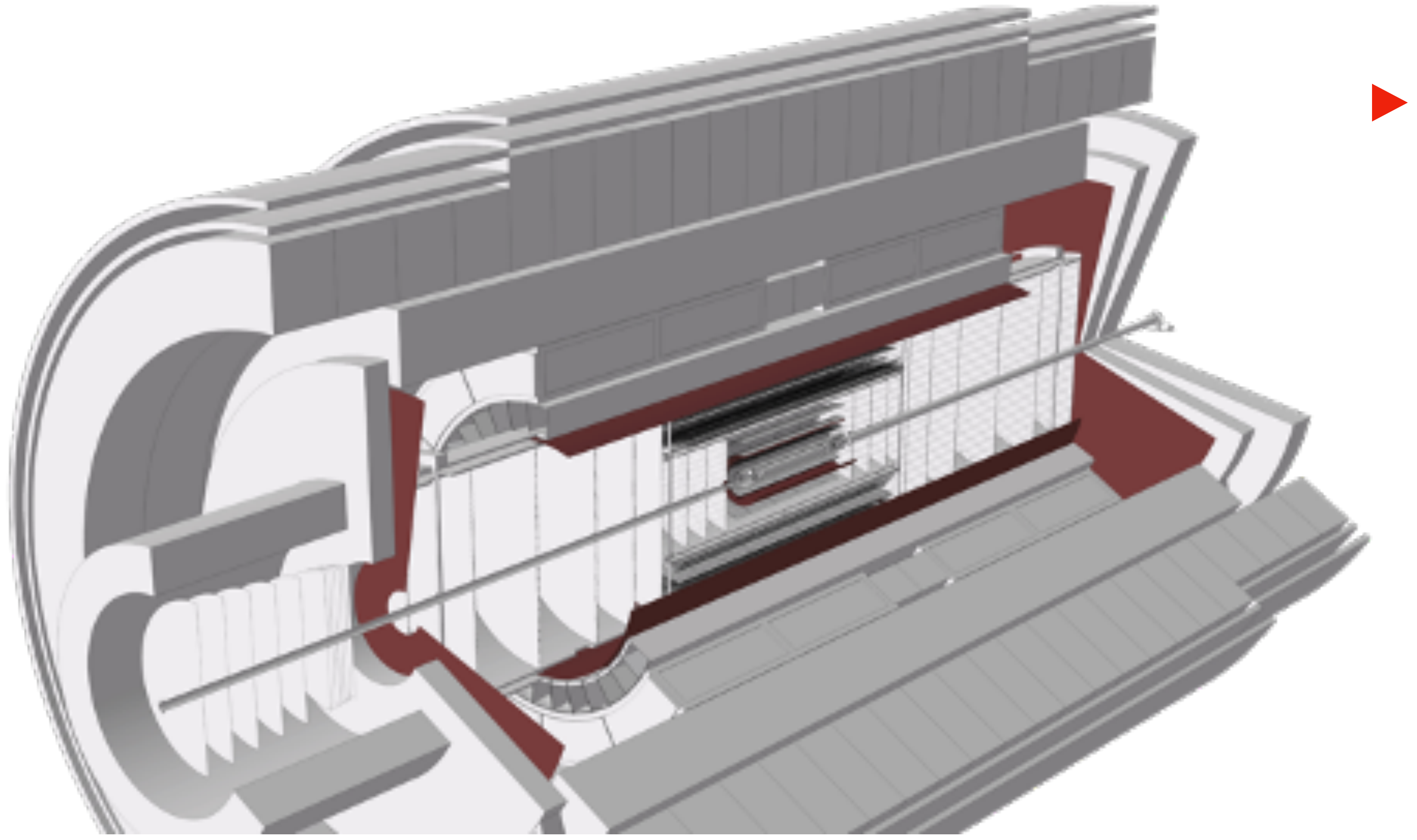




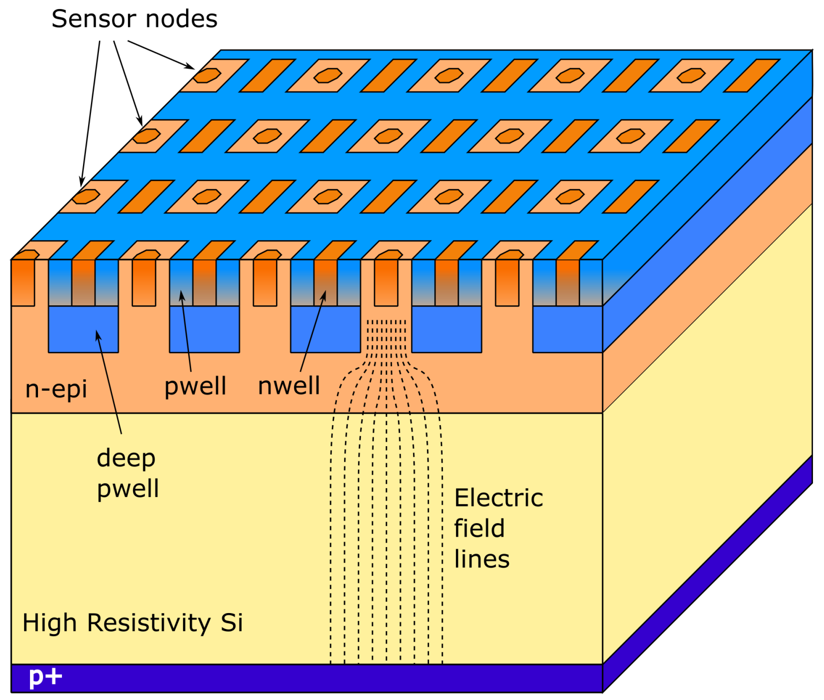
- Based on wafer-scale, ultra-thin, curved MAPS
  - radial distance from interaction point: 5 mm (inside beampipe, retractable configuration)
  - unprecedented spatial resolution: ≈ 2.5 µm
  - … and material budget: ≈ 0.1% X_0/layer
- Unprecedented performance figures
  - largely leverages on the ITS3 developments
  - pushes improvements on a number of fronts

ALICE 3

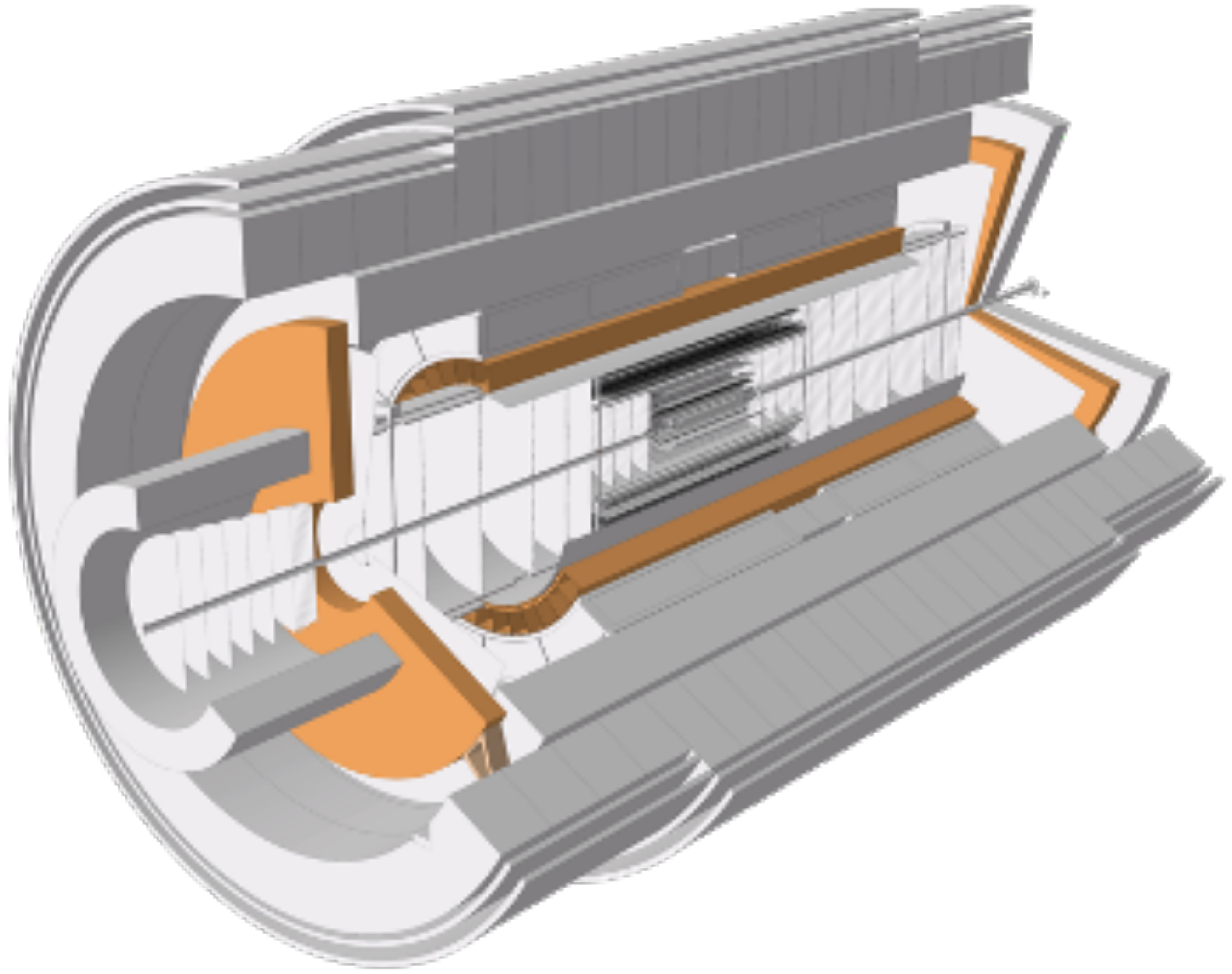
PID detectors TOF + RICH



- **TOF**
  - surface: O(45 m^2)
  - pitch: 1-5mm pitch
  - time resolution: <20 ps
  - CMOS LGADs



ARCADIA MAPS



- **RICH**
  - O(50m^2)
  - granularity: 3x3 mm
  - digital SiPM (hybrid as fallback)
- Main benefits in going integrated CMOS:
  - cost reduction
  - facilitation of system-level integration

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  - **expertise** in design, characterisation, integration is built up at several institutes within the collaboration
  - **large workforce** >100 people, >20 institutes participate
  - long-standing **relation** with the foundry
- Driven by <u>clear goals and timelines</u>:
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  - gives a lot of **confidence** for the concrete ALICE application, **serves** the community as a whole, and also paves the way for the **future** ALICE plans
  - ALICE follows an inclusive approach (open non-ALICE members welcome)
    significant support from CERN EP department and EP-ESE group!
- Developed technology is used for several **off-spring** experiments (HEP, medical, …)
  - several (smaller, but not necessarily small) experiments have adopted ALPIDE
  - 180 nm technology is now widely used

→ now Frederic's talk for technical details!

Thank you!