# ALICE ITS3 - The unfashionable but important bits

## The physical implementation of MAPS

# Outline

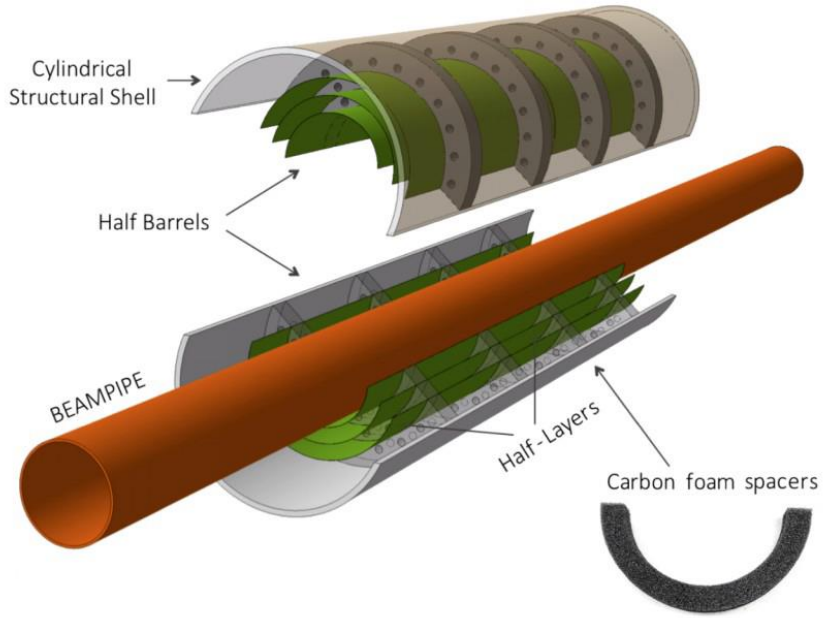
- Context
- Importance of hierarchical design
- Large design challenges
- Emerging needs
- Conclusion

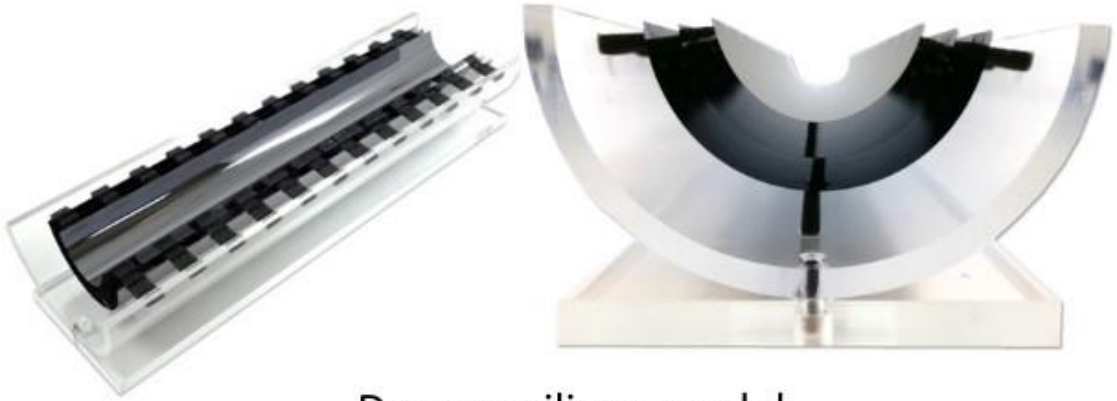
# ALICE ITS3

- Goal: Less material means better physics

- How is it achieved?
  - Lower power consumption allows for air cooling
  - On chip data transfer allows no flex
  - Bent Si wafers allow stable mechanical structure

- Proposal: Wafer-scale stitched particle detectors



Dummy silicon model

# MOSS and stitched sensors

- Stitching: technique that allows some parts of the reticule to be repeated across a wafer to create a unique circuit
- MOSS (Monolithic Stitched Sensor) prototype is a proof-of-concept of stitched MAPS
  - 1.4 by 26 cm wide
  - 1.67 million pixels
  - 736.3 million transistors
- How to achieved the design of such sensors?

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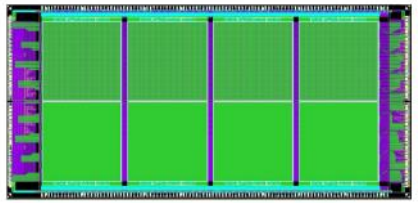
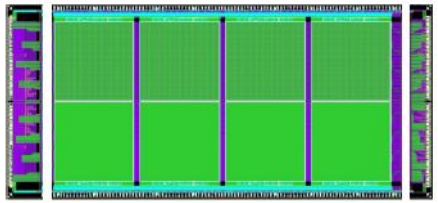
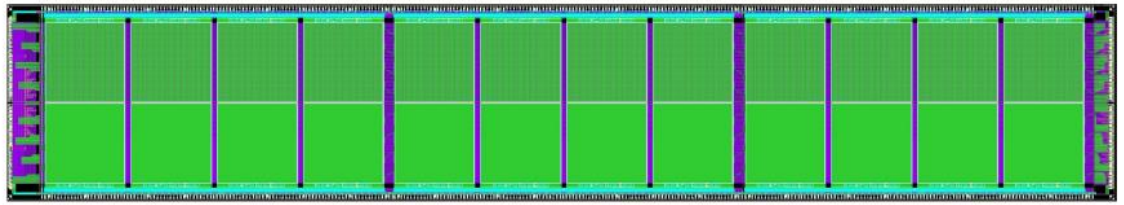


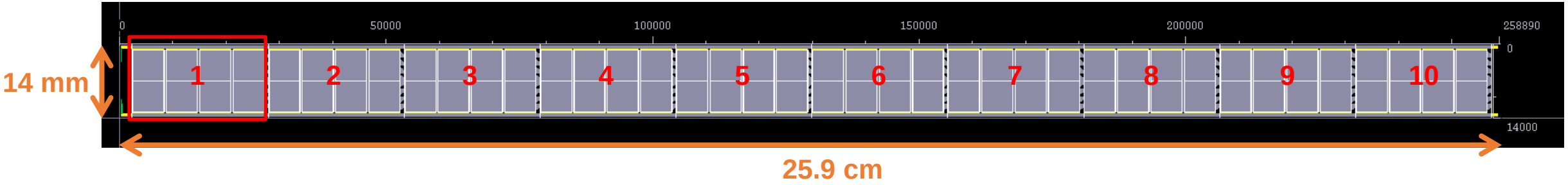
Reticule



Split

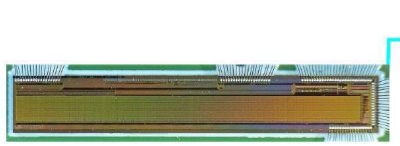


Stitched sensors (1x3)

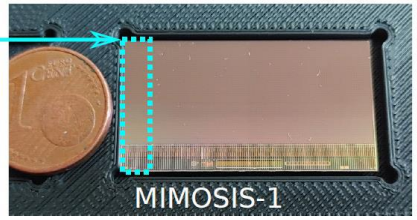


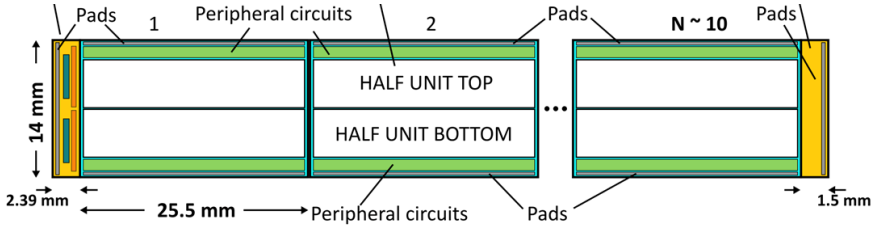
# How to build successful MAPS with Digital on Top?

- There are 4 aspects to master: Hierarchy, Granularity, Timing, and Power
  - The Learning Map @ C4Pi

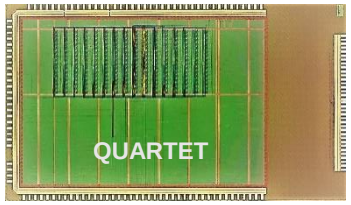


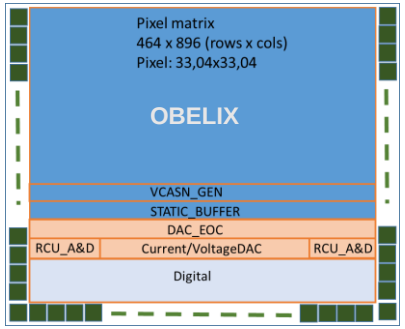
MIMOSIS-0




MOSS




Conformal ECO → MIMOSISFAST

| MIMOSIS-0 | MIMOSIS-1 | QUARTET | MIMOSIS-2 | MOSS | OBELIX | MOSS2 |
|---|---|---|---|---|---|---|
| 05-2017 | 03-2020 | 02-2022 | 11-2022 | 12-2022 | XX-2023 | XX-2023 |
| Mixed on Top | Digital on Top<br>Rough timing<br>No power | Hierarchical<br>Digital on Top | Digital on Top<br>Full timing + power | Coarse-grained<br>Digital on Top | Hierarchical floorplan<br>Digital on Top | |

Flowkit

# Hierarchical design: divide and conquer

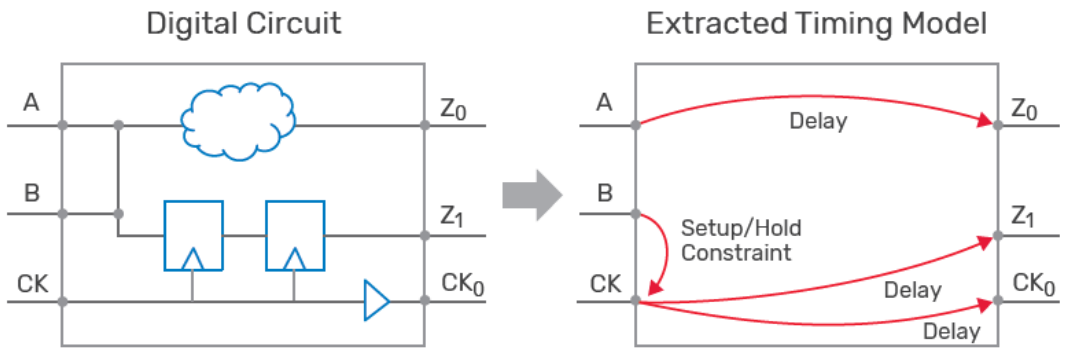
- Large and complex designs need a hierarchy to keep the submission on schedule
- 2 well known approaches:
  - Bottom-up
    - The design of each block is “independent” 
    - All the constraints are seen at the top, at the end of the flow 
  - Top-down
    - The top constraints of the system are pushed down to the blocks 
    - Need a dedicated flow 
    - Works at early stage with partially defined blocks 
- Hierarchical flow helps the designers with
  - Partitioning
    - Push floorplan constraints into blocks
  - Time budgeting
    - The timing constraints are allocated between top and partitions
- Hierarchy could be nested

# Granularity is crucial

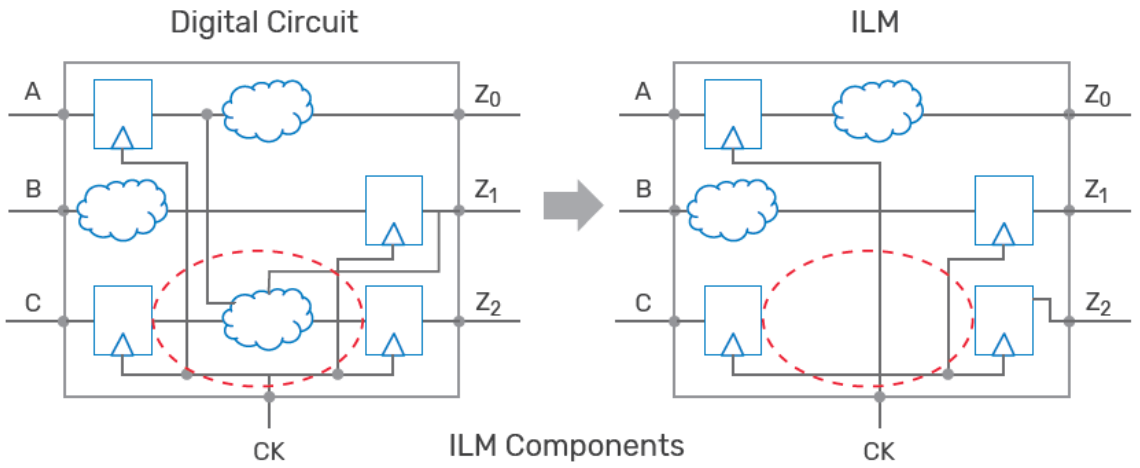
- Digital flow is based on abstraction of cells
  - Liberty file: timing and power model
  - Abstract: physical view
  - Power Grid View (PGV): extracted power network
- Granularity is related to the size of the blocks in the hierarchy
  - Which is the best: Pixel, column, sub-array or matrix level?
  - Need to be in phase with functional verifications
- Runtime of the flow and verification accuracy are correlated to the granularity
  - Need to be flexible during the flow (place and route stages vs signoff stage)
- Generating the abstraction for coarse-grained blocks could be difficult
  - On a huge block it could take days or did not converge at all
  - It is much easier for the blocks that come from Innovus than for those that come from Virtuoso

# Hierarchical Timing Analysis concepts

- Need to model the timing of digital hierarchical blocks at high level to reduce the runtime
- 2 types of modelling: ETM (Extracted Timing Model) and ILM (Interface Logic Model)
  - ETM generates a liberty file of the block
  - ILM works on a reduced netlist
- ETM can be long and difficult to generate and has many drawbacks
- ILM is more efficient but still has some limitations




**ETM**




**ILM**

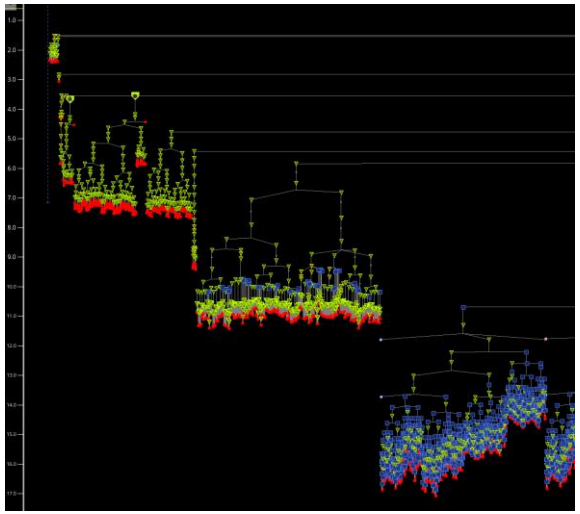
# Full Flat Verifications is mandatory

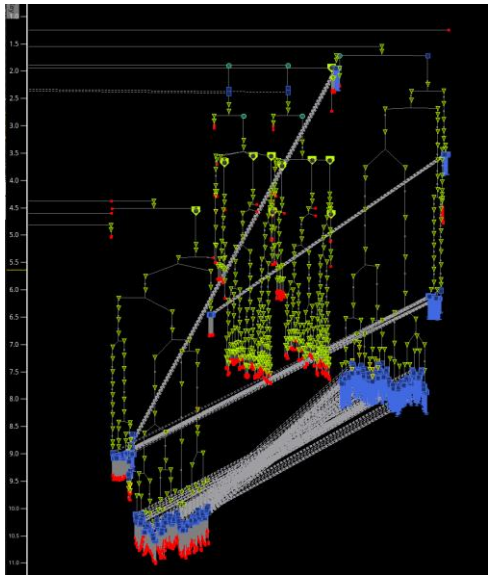
- A full flat signoff analysis is required to avoid missing failed paths with hierarchical timing
  - Not all corners are used during place and route steps
  - Problems with interactions between blocks and top
- Knowledge of the tools is essential for success in a reasonable time
  - Flatten the design using advanced capability of Tempus
  - Distributed timing verification
    - Careful tuning between corners and remote hosts is needed to get the best performance
  - Use hierarchical ECO flow to fix remaining fall paths
- Similar techniques are available for power verifications

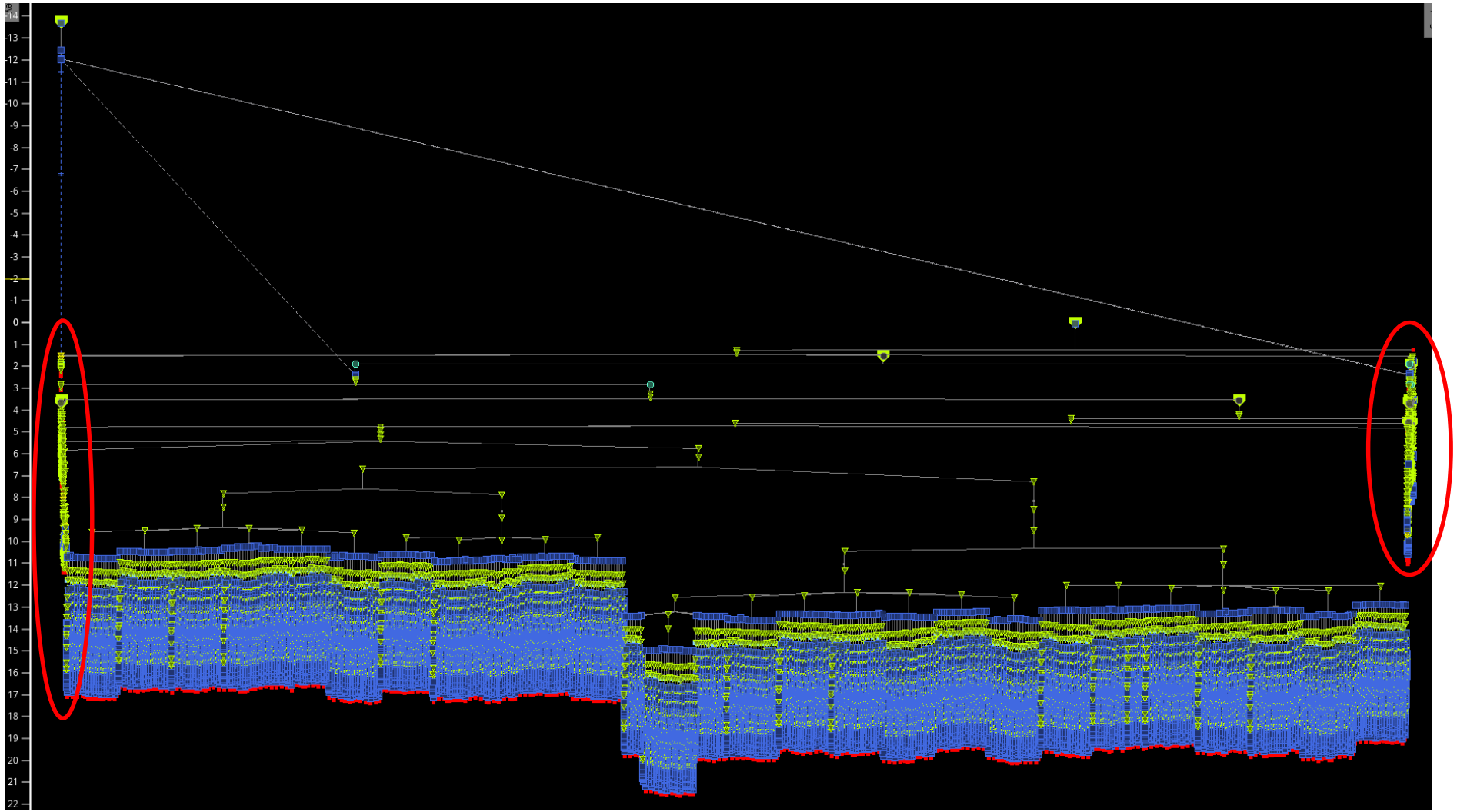
**MIMOSIS2**
**full flat timing analysis**
**Reticule size chip**
**in 0.18 µm**

| | Local hierarchical 1 CPU | Local no physical 16 CPU | Local physical 16 CPU | Distributed physical 4 hosts with 4 CPU |
|---|---|---|---|---|
| **Total Time (h)** | 0.3 | 4 | 4.2 | 4.5 |
| **CPU Time (h)** | 0.3 | 32.5 | 32.75 | 52 |
| **Peak Memory (GB)** | 20 | 110 | 120 | 47 for each host |

# Full flat timing results: Clock tree of MIMOSIS2

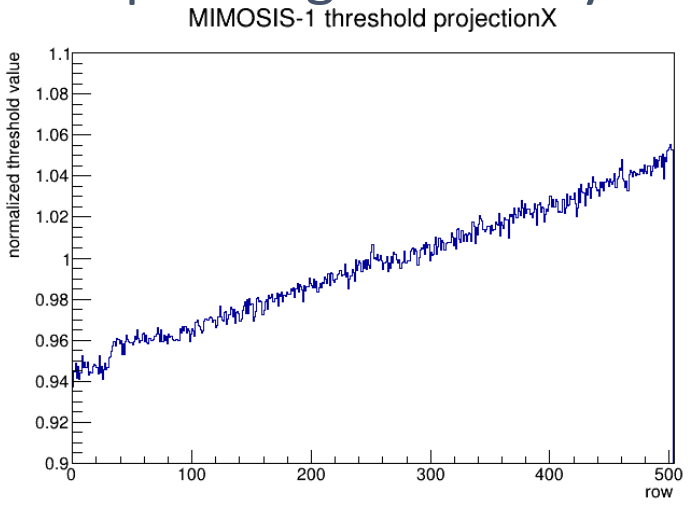


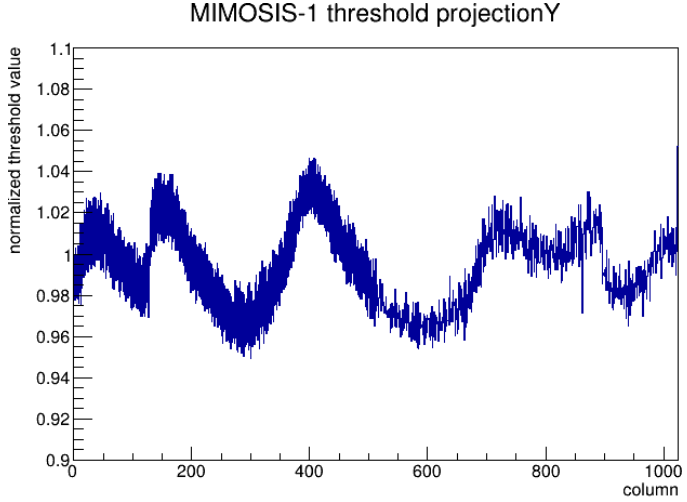




# Full flat power results: IR drop of MIMOSIS2

- The power grid is a key factor for the threshold uniformity




**Threshold shift of MIMOSIS-1 projection (measurements)**

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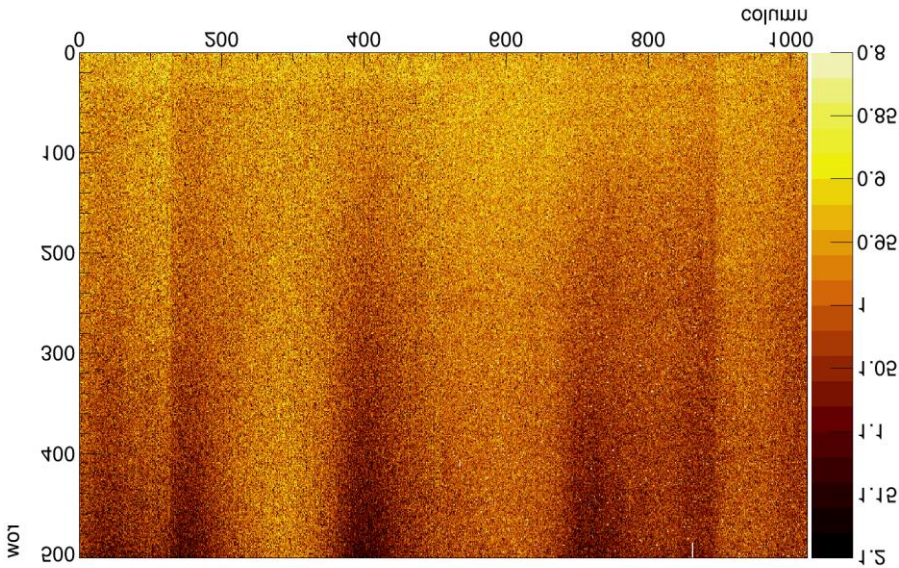
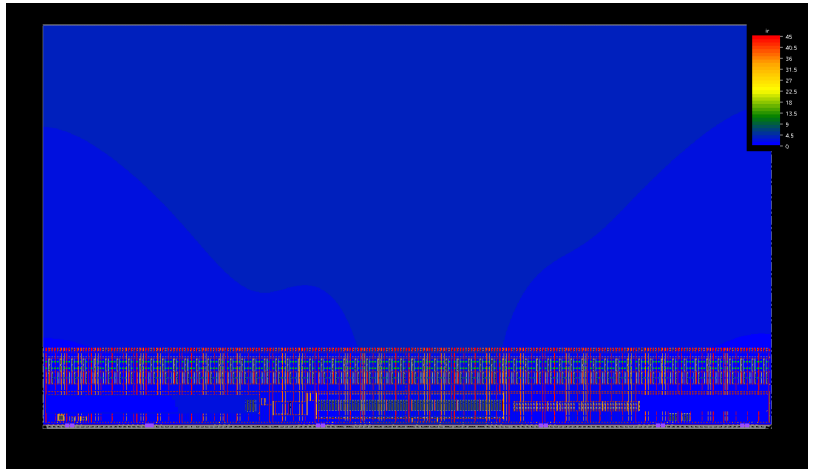
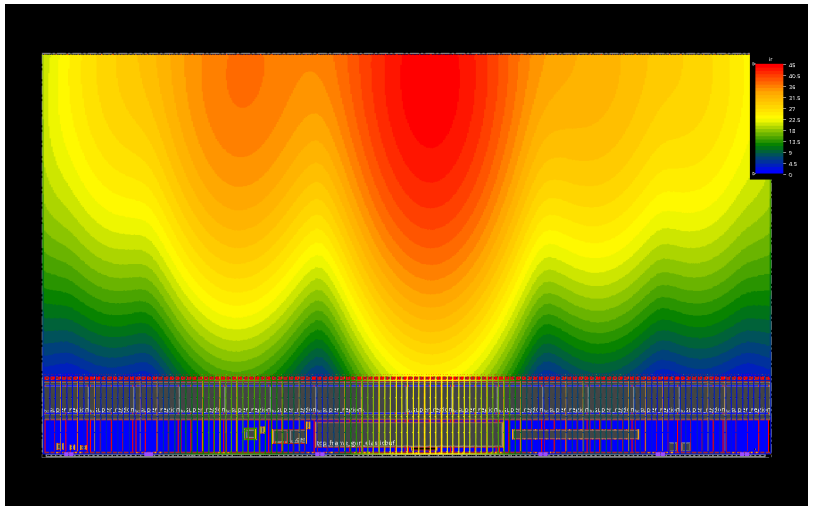




**IR drop on AVDD (simulations)**
**0-45 mV scale**

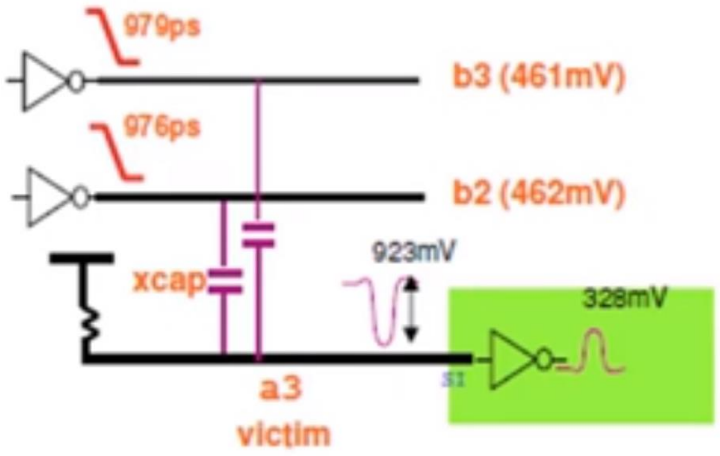
**MIMOSIS-1**
**Mean= 26 mV**

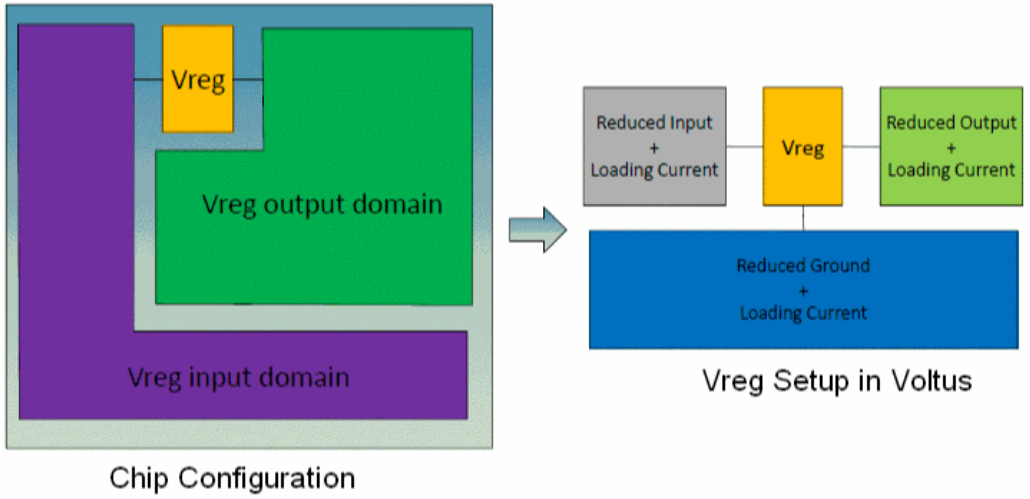
**MIMOSIS-2**
**Mean = 3 mV**



# Convergence between digital and analogue world

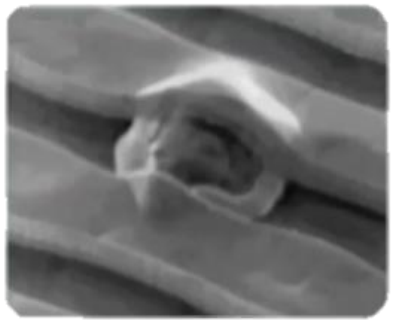
- Signal Integrity glitch analysis for analogue nets
  - Estimation of the injection peak on an analogue net and make the corrections on violated nets
  - High-precision simulations (spectre)
- Dynamic Rail Analysis for On-Chip Voltage Regulators with Voltus
  - Simulate a reduced circuit with spectre
  - Inject the simulated voltage waveforms into Voltus rail solver



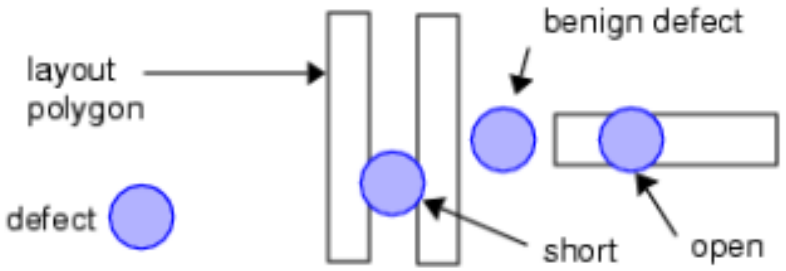
# To further improve the quality of design: new tools are needed

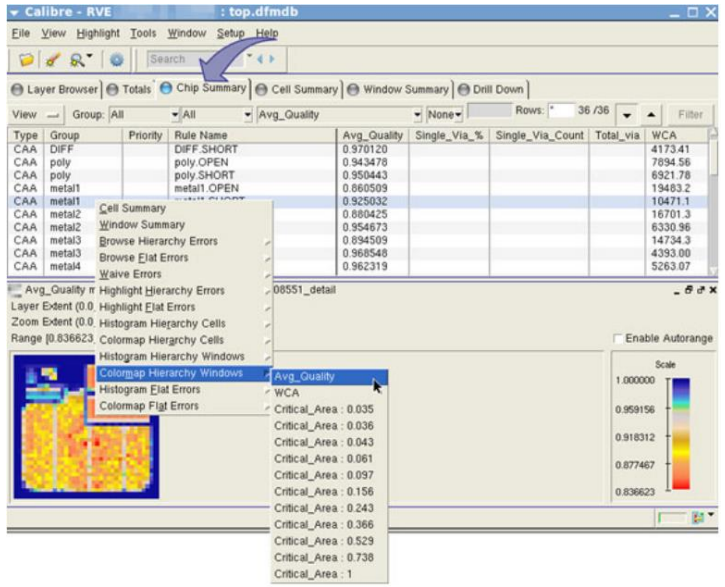
- Need to use new tools to ensure good yield of stitched sensors
  - DRC clean and traditional filling is not sufficient (recommended rules and smart filling)
  - Yield dominated by a few hotspots
- Calibre DFM provides access to a set of analyses
  - For some analyses, foundry rules are mandatory
  - For some analyses, some basic self check could be performed to identify the weakest points



Another particles detector

**Figure 11-1. Manufacturing Defects**



# Conclusion

- Design methodologies are essential to produce high quality sensors on time
- The sensor is part of an overall system ➔ Do we need to go for digital twins?
- Relationships with foundries and EDA vendors are critical
- Potential bottleneck in computing infrastructure