TSI

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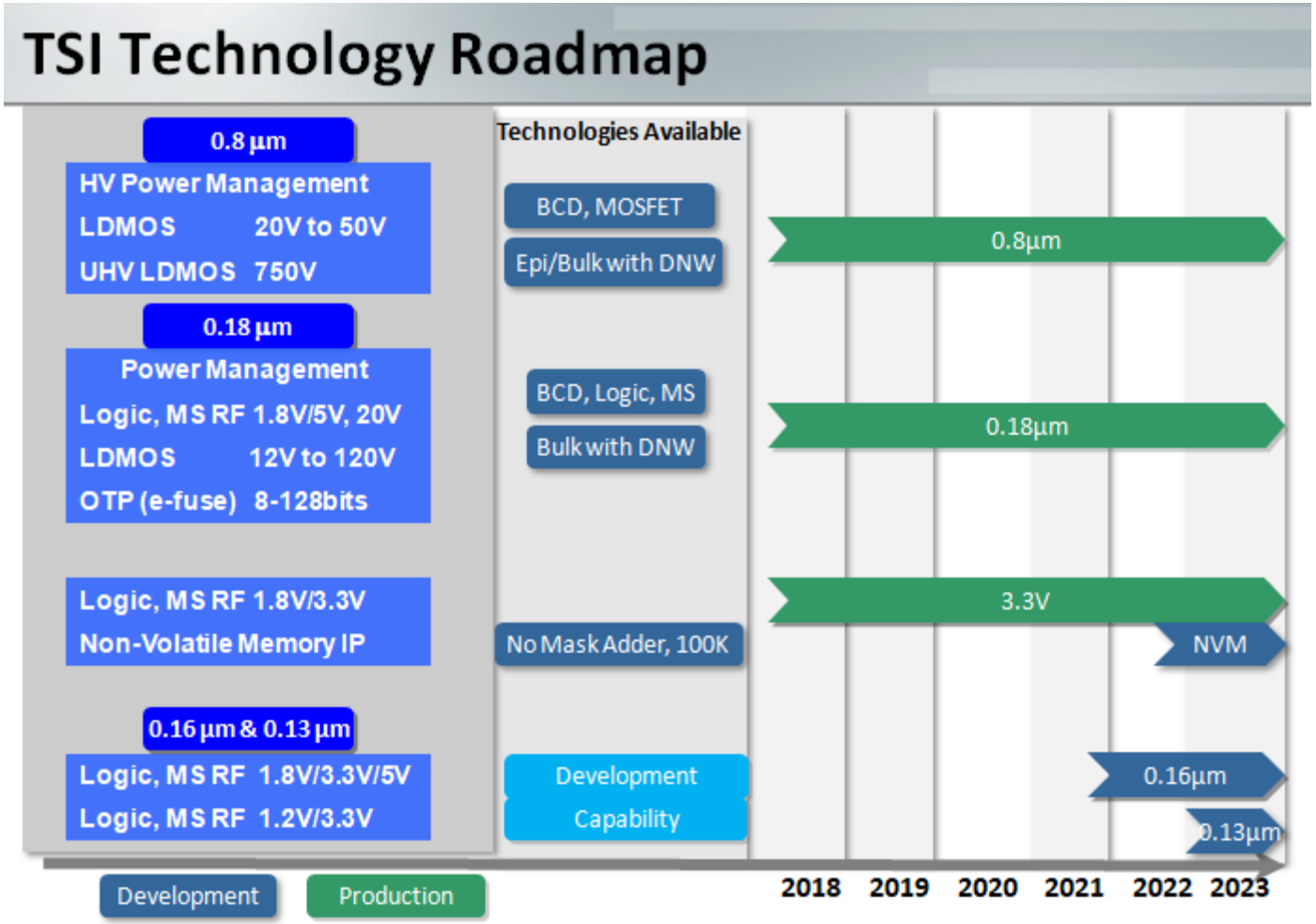
- TSI semiconductors
- https://www.tsisemi.com/
- Roseville, California, USA

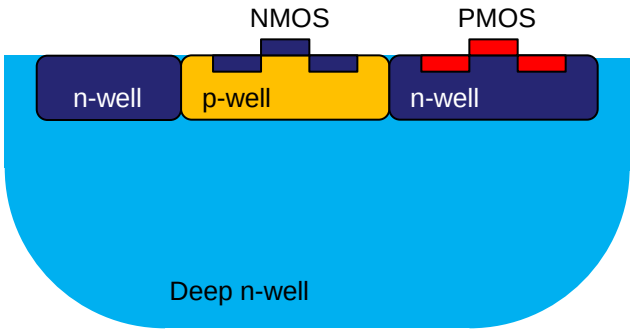
Capabilities

- Production grade tools in Class 3 Clean Rooms
- 24/7 Engineering, Operations & Maintenance
- Manufacturing Execution Systems (MES)
- IP Secure Environments
- Robust Quality Systems
- Automotive Registered
- ITAR Certified
- Trusted Accreditation
- Onsite Analytical Tools & Labs
- Lithography Capable to 110nm
- Aluminum BEOL Interconnect
- Engineering Specialists and Program Managers
- Process Library
- Novel Materials
- Emerging Technology Capabilities

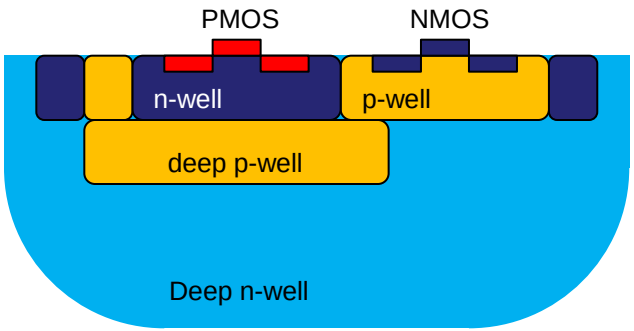
- Technologies from 0.8µm – 0.13µm
- My focus on: 180nm HVCMOS process



- The 180nm TSI HVCMOS process offers:
- Low voltage CMOS transistors that are placed within n deep-nwell.
- High deep n-well to p-substrate voltages possible (>500V according to TCAD)



Standard



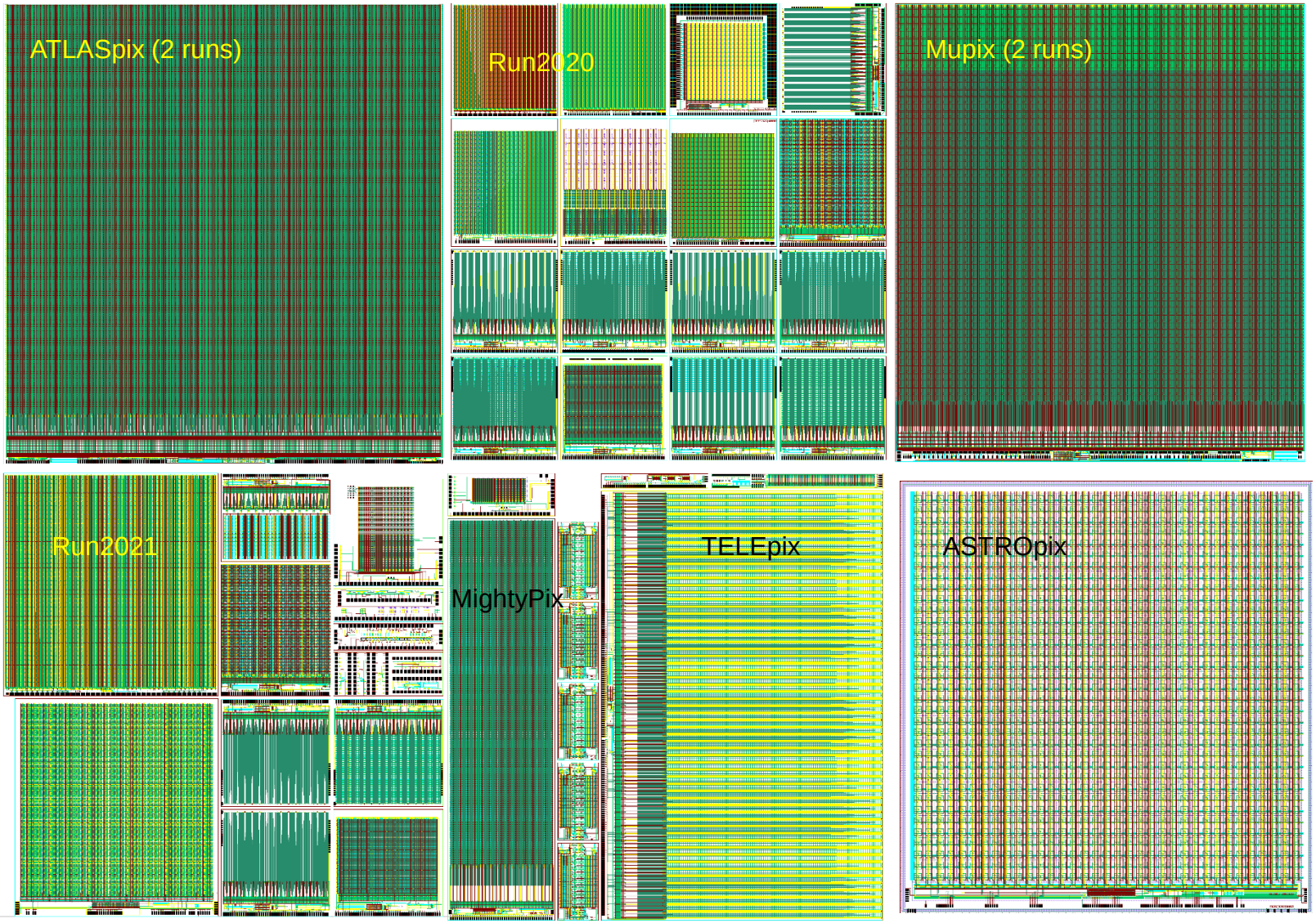
With deep p-well

- Several flavors of low voltage transistors: with regular and high, super high threshold, 1.8V, 3.3V, 5V…
- High voltage transistors (NFET and PFET) that can have Vds up to 120V
- In particular: 12V, 20V, 25V, 50V, 120V NFET/PFET transistors
- Comment: There are several high voltage processes on the market but to my knowledge only very few processes with 180nm feature size offer devices with >100V Vds, one of them is the TSI process
- Thin gate oxide*
- HV- bipolar transistors, mim and dual mim capacitors, resistors, LV forward diodes
- Largest reticle we produced: 20.7mm x 23.1mm
- TSI process offers up to 7 metal layers. 6 Layers are small feature size layer and the last layer is (optionally) 4µm thick and has very low sheet resistance.
- Never had issues with voltage drops in large matrices thanks to this layer

- TSI offers to use customer’s substrates
- Presently we use 18kOhm substrates from Topsil and 370Ohm substrates from Okmetic
- Standard TSI-substrate is also suitable for HVCMOS sensors
- TSI was ready to add additional implant to their process
- Reticle stitching possible

- The TSI design kit includes a standard cell library
- TCAD models available on request

- We started developing chips in TSI process in 2018
- We had so far 8 engineering runs
- We started also a production with 150 wafers for Mu3e
- 2018: Atlaspix3
- 2019: MuPix10
- 2020: Run2020, Atlaspix3v2
- 2021: Run 2021
- 2022: MuPix11, MightyPix/TELEpix, Astropix3, MuPix11 production


ATLASpix (2 runs)
Run2020
Mupix (2 runs)
Run2021
MightyPix
TELEpix
ASTROpix

- Excellent yield 80% for large chips after dicing and bonding
- Fast production time
- TSI colleagues are highly competent, respond fast, excellent support, helpful
- Engineering run costs were comparable to the costs in the case of UMC 180nm process
- Production time was 3 months, recently increased by a few months

- Before start: NDA and customer form
- Engineering run
- Tape out
- The design is checked by TSI for errors
- Design manufacturing form and waiver request form

Summary

- Excellent technology for HVCMOS sensors
- Features: Deep n-well, high resistivity substrates, deep p-well
- High voltage FETs available, up to 120V – use thin oxide
- Excellent for drivers, HV-generators, power regulation
- Excellent support, highly competent team, helpful, quick in responding
- Readiness to adjust and develop process according to customer needs
- Use of customer's substrates possible
- TCAD models shared
- TSI: “Our flexible approach to development and manufacturing allows customers to develop with a broader range of materials than other foundries.”