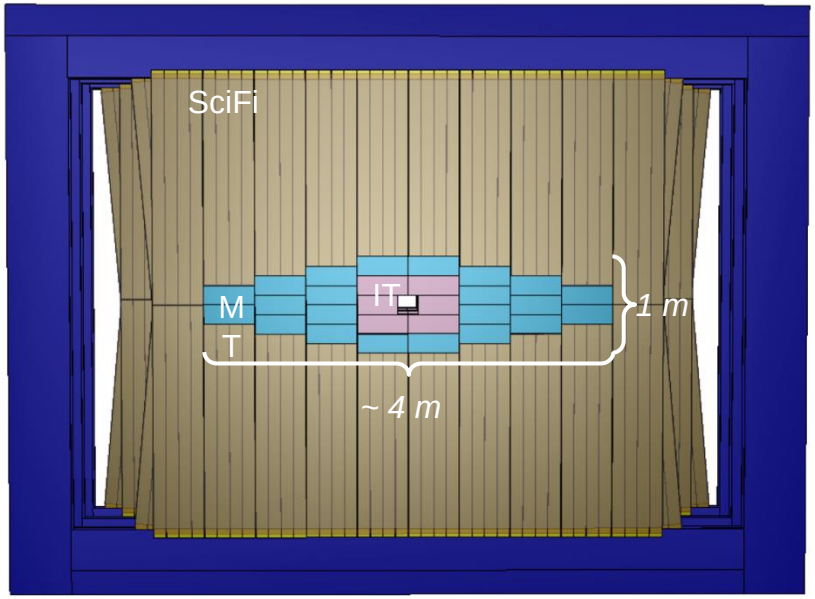
# MightyPix

Ivan Peric and MightyPix team

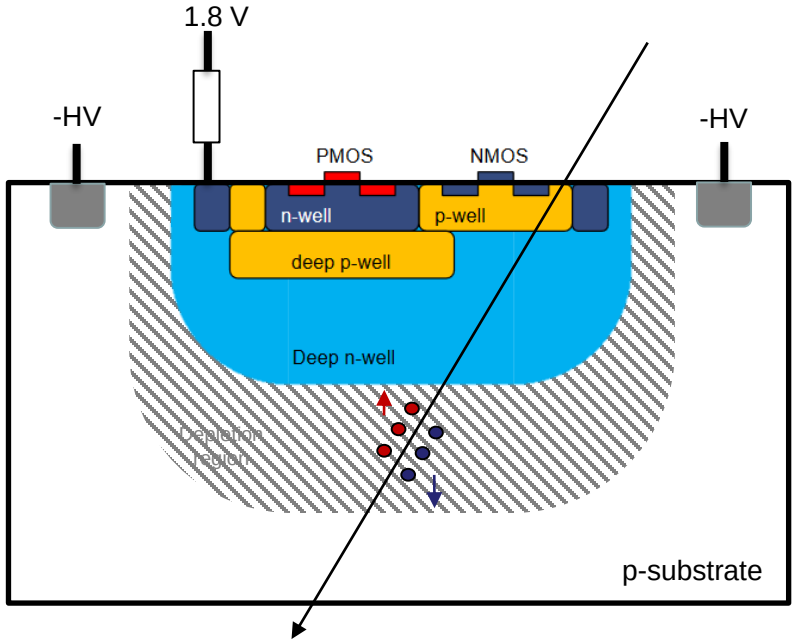
- Mighty Tracker
- SciFi Tracker
  - Scintillating fibres with SiPM readout
- Inner Tracker and Middle Tracker
  - Silicon sensors meet requirements of radiation hardness and granularity
  - Baseline technology: HV-CMOS pixel chip **MightyPix**
  - In total over 46000 silicon sensors to cover area of 18 $m^2$ (minus beam-pipe hole)




*Schematic of one layer of the Mighty Tracker. [1]*

# MightyPix

- HV-CMOS sensor
- Sensing element and readout circuit on same chip
- n-well/p-substrate diode acts as sensor
- Readout electronics isolated from high voltage by deep n-well
- High reverse bias creates thick depletion region between deep n-well and p-substrate
- Ionising particles create electron/hole pairs, collected via drift




*Working principle of HV-CMOS sensors.*

# MightyPix

- MightyPix is based on knowledge from ATLASPix[1] and MuPix[2]
- Final design parameters and requirements:
- First prototype: **MightyPix1**

| Parameter | Required Value | Notes |
|---|---|---|
| Chip size | $\sim 2\ \mathrm{cm} \times 2\ \mathrm{cm}$ | |
| Pixel size | $\sim 50\ \mu\mathrm{m} \times 150\ \mu\mathrm{m}$ | |
| Time resolution | $< 3\ \mathrm{ns}$ | Hit assigned to right BX |
| Power consumption | $< 0.15\ \mathrm{W/cm^2}$ | |
| NIEL[3] | $6 \times 10^{14}\ 1\ \mathrm{MeV}\ \mathrm{n_{eq}/cm^2}$ | Includes safety factor of 2 |
| Cooling | $< 0°\mathrm{C}$ | Test beam studies |

*[1] HV-CMOS pixel chip for the ATLAS experiment at CERN*
*[2] HV-CMOS pixel chip for the Mu3e experiment at PSI*
*[3] Non Ionising Energy Loss*

# MightyPix1: Overview

- Implemented in TSI 180 nm process
- Submitted in May 2022
- Chip size: ~ 2 cm × 0.5 cm → full column length, ¼ width
- Pixel matrix: 29 columns, 320 rows
- Pixel:
  - 165 µm × 55 µm
  - CMOS amplifier and CMOS comparator
- Data format: 2 × 32 bit words per hit trasmitted
- Data output rate: 1.28 Gbit/s going to lpGBT

*The first prototype: MightyPix1*

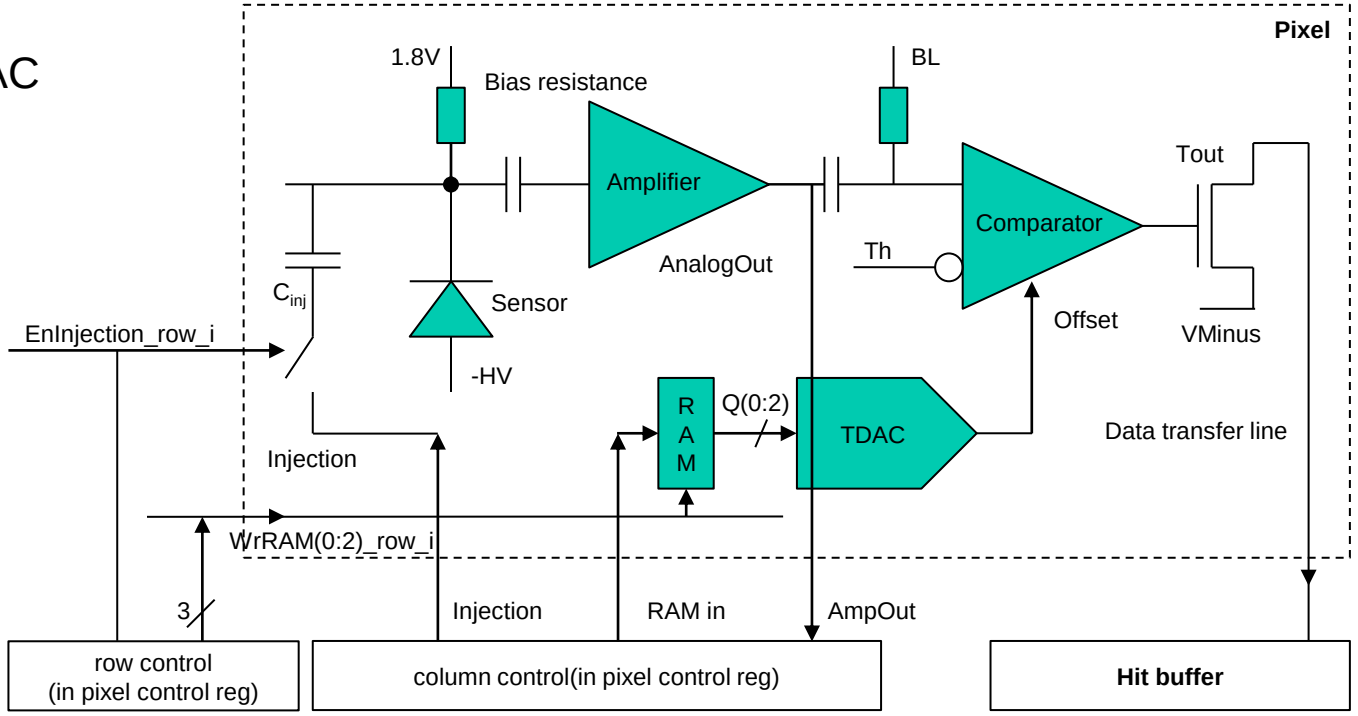
# MightyPix1: Overview

- Digital interfaces:
  - Timing and Fast Control (TFC)
  - Slow Control (I2C)
  - Configuration shift register (SR) interface
- Clock generation:
  - External: 40 MHz and 640 MHz coming from lpGBT
  - Internal: CML and CMOS PLL with 40 MHz reference clock
- Bias voltages:
  - Integrated 10 bit voltage DACs
  - Can be supplied externally

*The first prototype: MightyPix1*

**Pixel contains:**

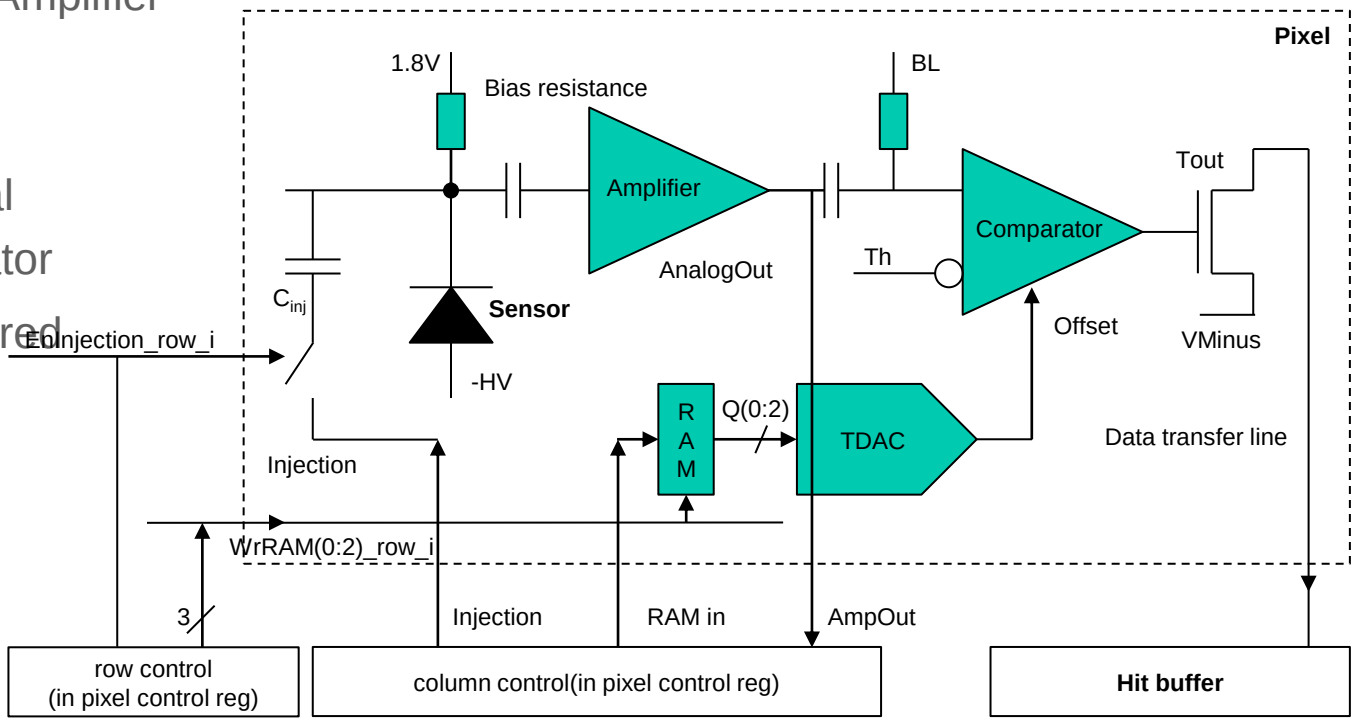
- Sensor diode
- Charge Sensitive Amplifier (CSA)
- Comparator
- Threshold tune DAC
- RAM for tune bits




*Source: Ivan Perić*

## Working principle:

1. Charge collected by pixel n-well
2. Converted to voltage signal by Charge Sensitive Amplifier
3. Analog voltage pulse shaped and converted to digital signal by comparator
4. Hit information stored in hit buffer

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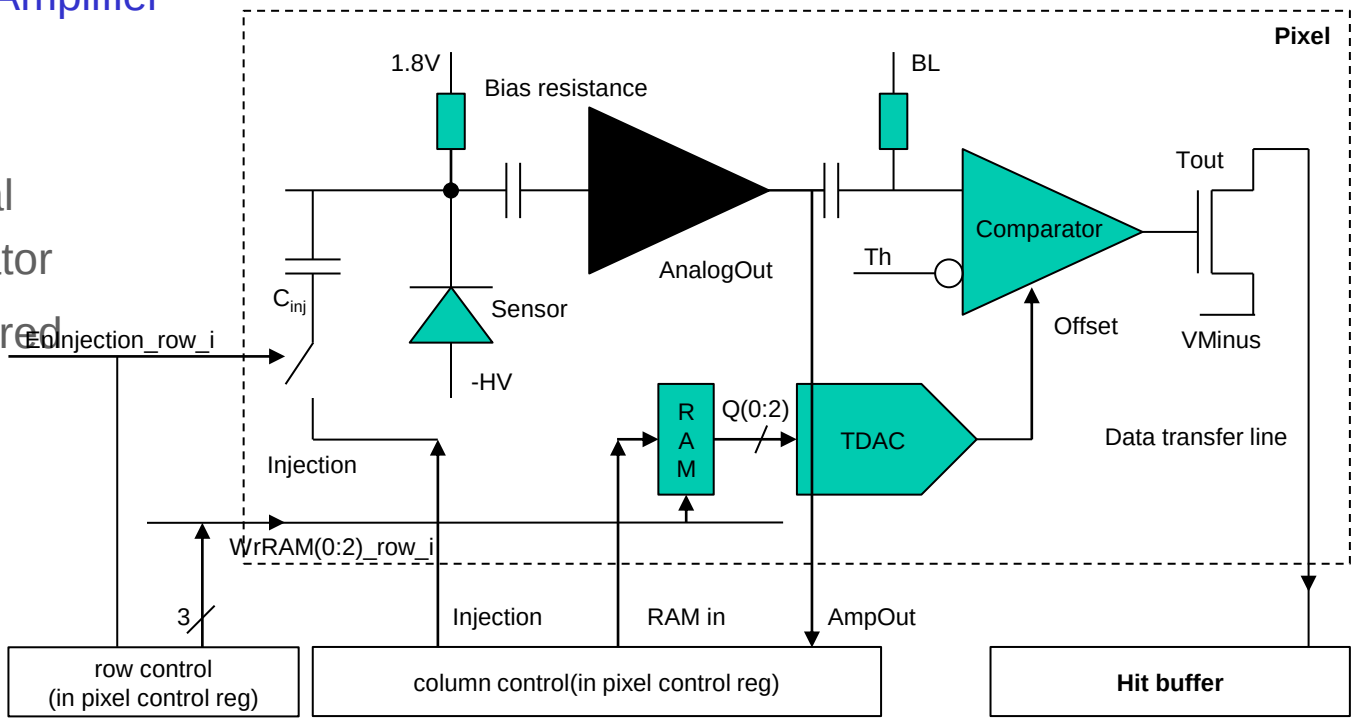


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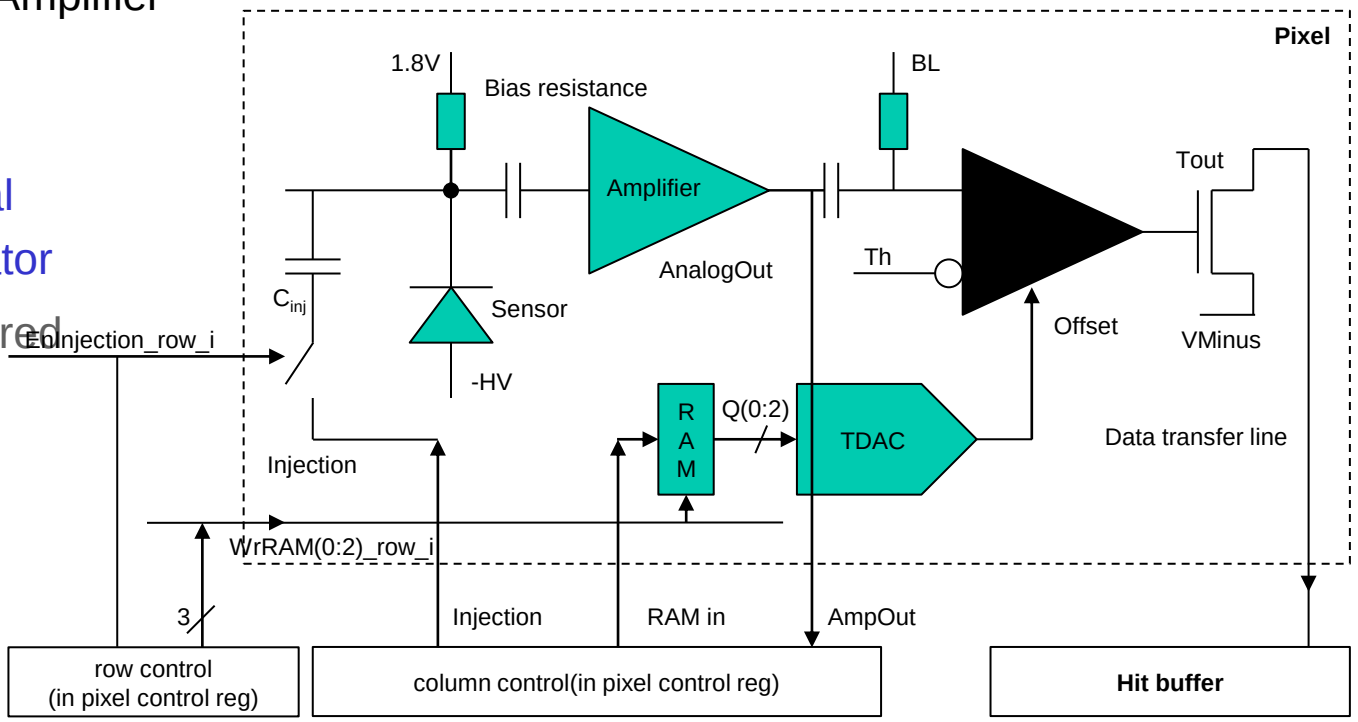


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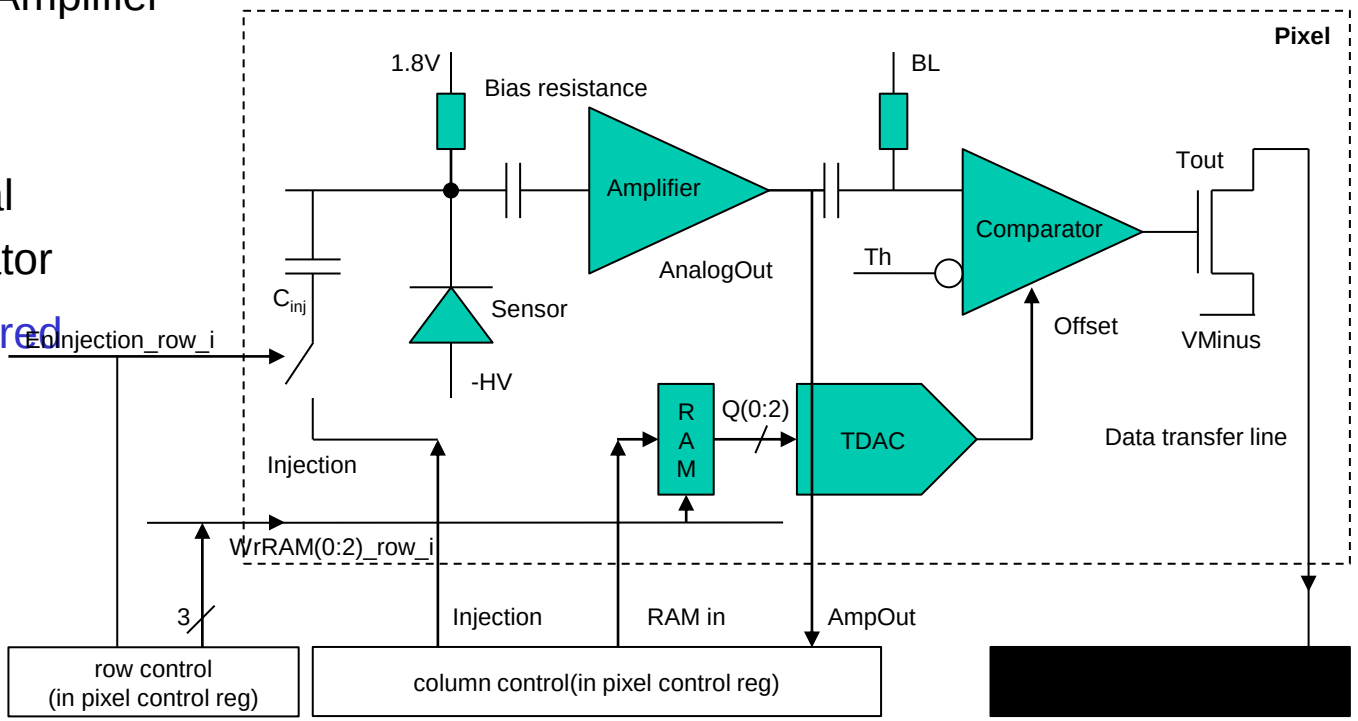


*Source: Ivan Perić*

# MightyPix1

- MightyPix1 has been produced – first results soon