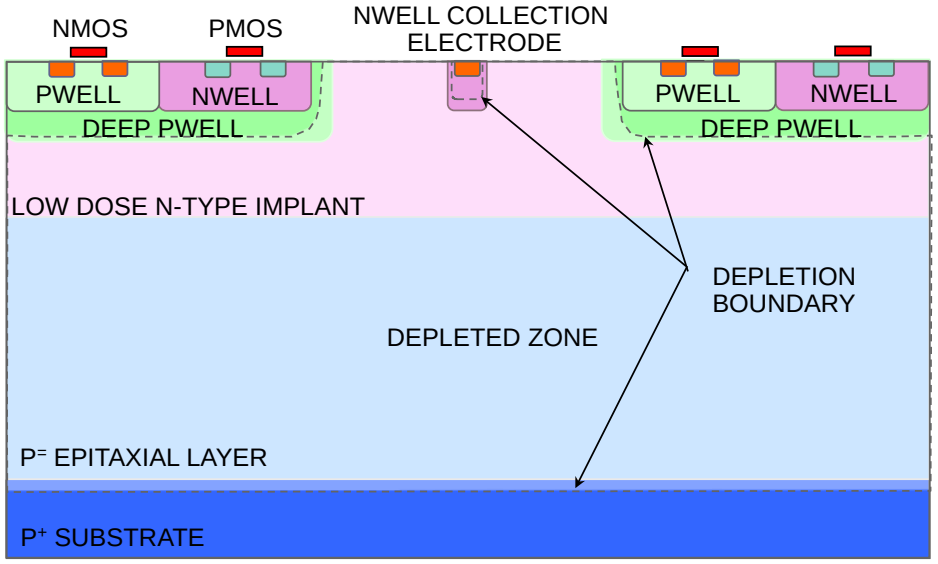
WP 7.6 Monolithic Sensor ASICS

Implementing DRD7 : R&D Collaboration on Electronics and On-detector Processing

CERN – Wednesday March 15th , 2023

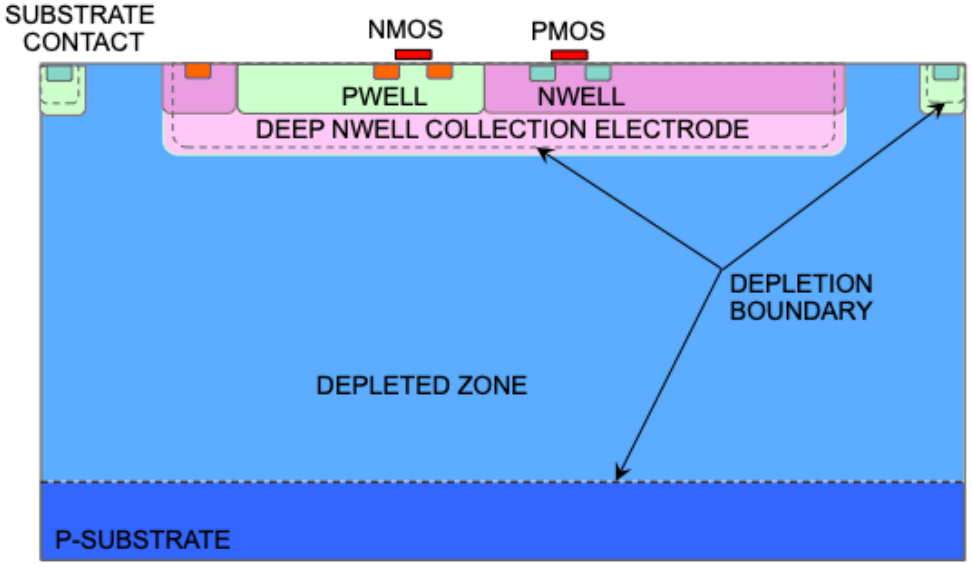
Marlon Barbero / Iain Sedgwick / Walter Snoeys

Developments in many technologies



Small collection electrode

Small capacitance (a few fF), radiation tolerance more challenging

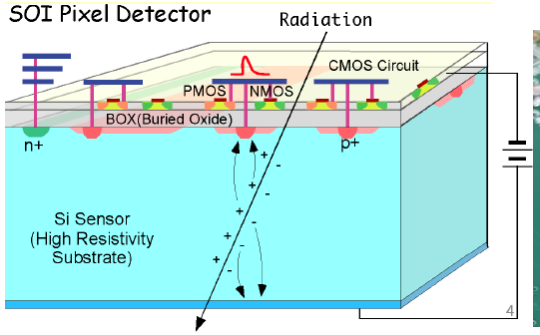


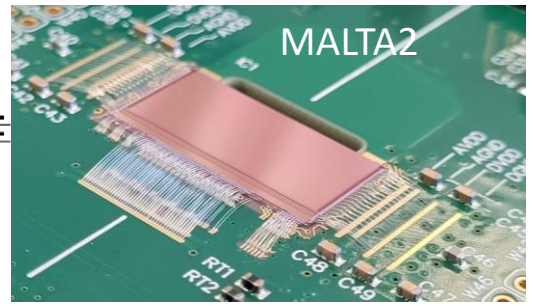
Large collection electrode

Radiation tolerant, but large capacitance (100s of fF)

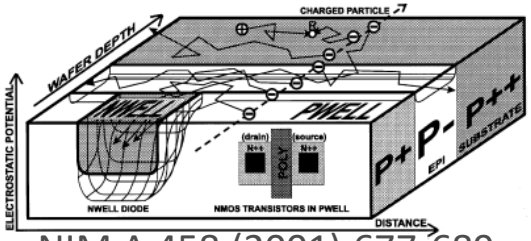
TPSCo 65 nm ISC and TSI180 already presented

Many others: LF150, LF110, SOI, XFAB, SiGe BiCMOS, with and without gain layer, TJ180 …





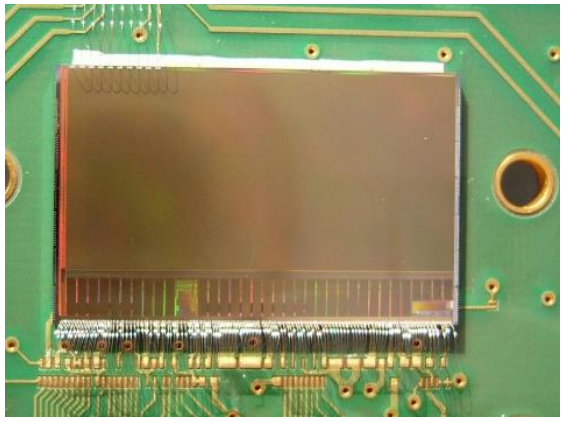
Mimosa series – IPHC Strasbourg



NIM A 458 (2001) 677-689

A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology

R. Turchetta[a,*], J.D. Berst[a], B. Casadei[a], G. Claus[a], C. Colledani[a], W. Dulinski[a], Y. Hu[a], D. Husson[a], J.P. Le Normand[a], J.L. Riester[a], G. Deptuch[b,1], U. Goerlach[b], S. Higueret[b], M. Winter[b]



Rolling shutter readout

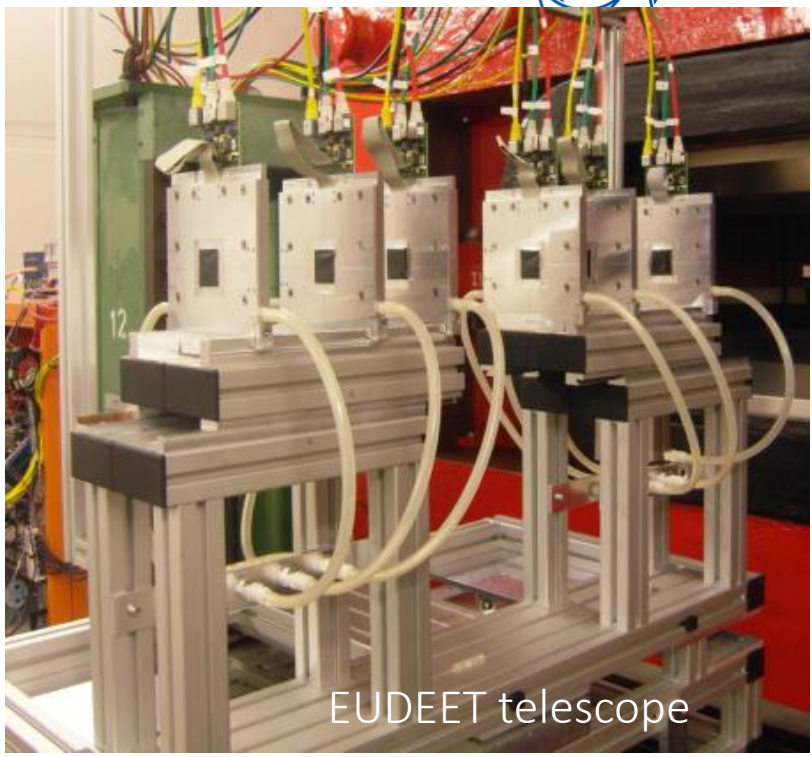
Mimosa26 – 2008

AMS 0.35 µm

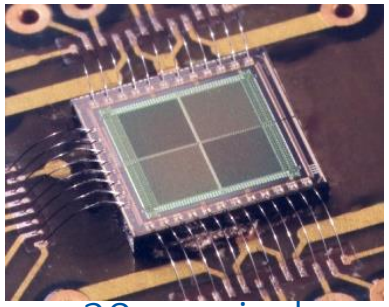
18.4 µm pixel pitch 576x1152 pixels

First MAPS with integrated zero-suppressed readout

First MAPS used for several applications, also for EUDEET telescope

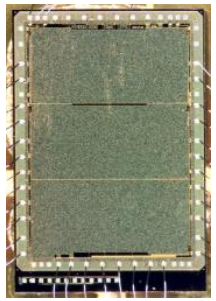


Mimosa1 – 1999
AMS 0.6 µm



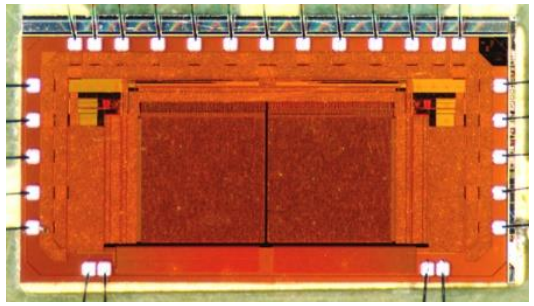
20µm pixel

Mimosa2 – 2000
MIETEC 0.35 µm



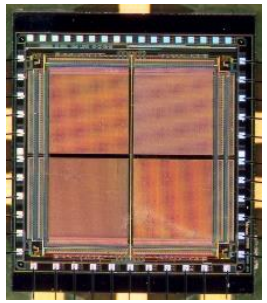
20µm pixel

Mimosa3 – 2001
IBM 0.25 µm



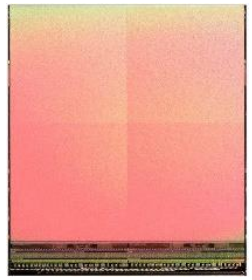
8µm pixel

Mimosa4 – 2001
AMS 0.35 µm



20 µm pixel

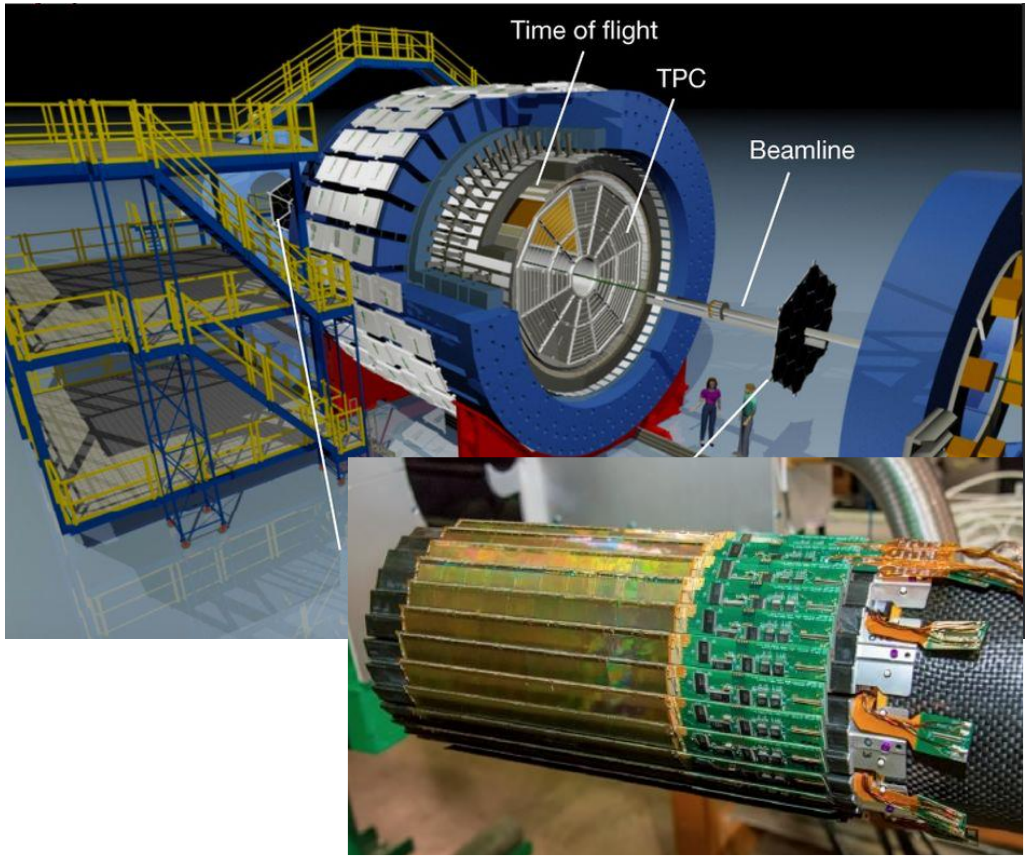
Mimosa5 – 2001
AMS 0.6 µm



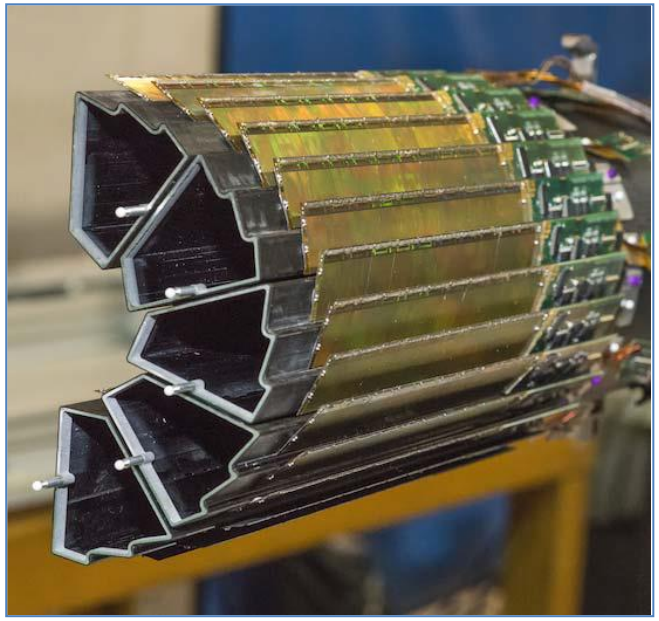
17 µm pixel

....

MIMOSA28 (ULTIMATE) in STAR PXL



courtesy of STAR Collaboration



356 M pixels on ~0.16 m² of silicon

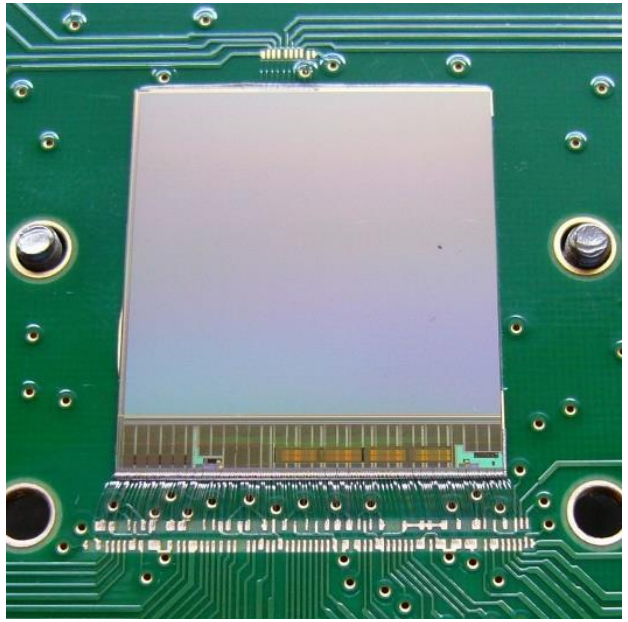
Full detector Jan 2014

Physics Runs in 2015-2016

- 2 layers (2.8 and 8 cm radii)
- 10 sectors total (in 2 halves)
- 4 ladders/sector
- Radiation length (1st layer)
- x/X0 = 0.39% (Al conductor flex)

Ladder with 10 MAPS sensors

2-layer kapton flex cable with Al traces



MIMOSA28 (ULTIMATE) – 2011

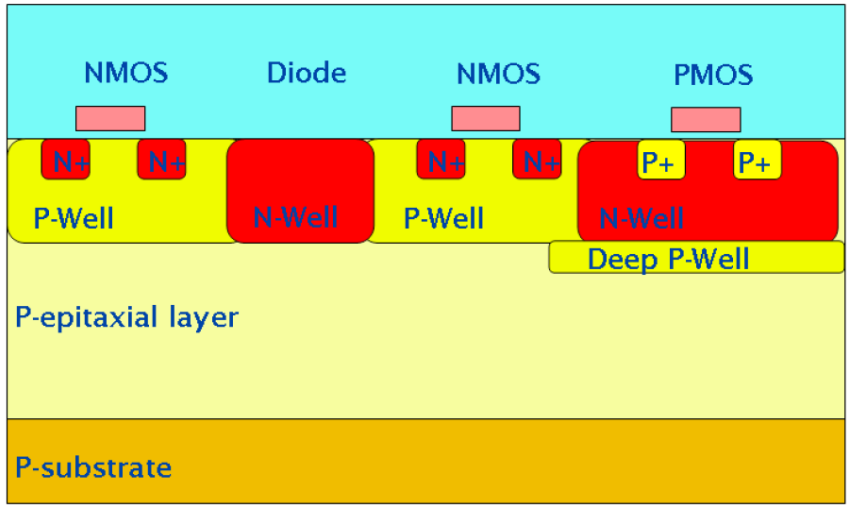
First MAPS system in HEP

Twin well 0.35 µm CMOS (AMS)

- 18.4 µm pitch
- 576x1152 pixels, 20.2 x 22.7 mm²
- Integration time 190 µs
- No reverse bias -> NIEL ~ 10^{12} n_{eq}/cm^2
- Rolling shutter readout

walter.snoeys@cern.ch

The INMAPS process: quadruple well for full CMOS in the pixel



STFC development, in collaboration with TowerJazz

Additional deep P-well implant allows complex in-pixel CMOS and 100 % fill-factor

New generation of CMOS sensors for scientific applications (TowerJazz CIS 180nm)

Also 5Gb/s transmitter in development

Sensors 2008 (8) 5336, DOI:10.3390/s8095336

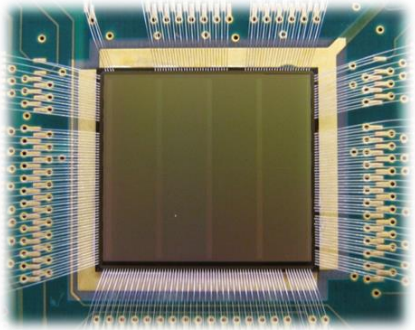
https://iopscience.iop.org/article/10.1088/1748-0221/7/08/C08001/meta

https://iopscience.iop.org/article/10.1088/1748-0221/14/01/C01006/meta

http://pimms.chem.ox.ac.uk/publications.php …

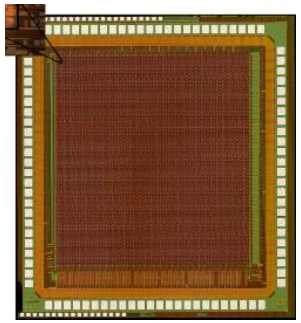
courtesy of N. Guerrini, STFC

TPAC
ILC ECAL (CALICE)



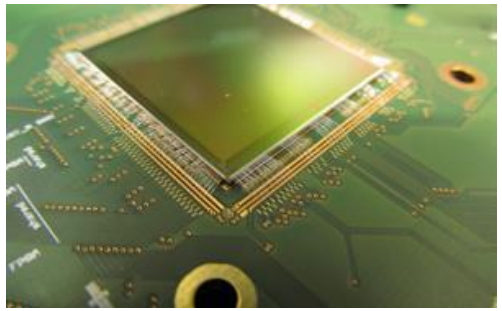
50μm pixel

DECAL
Calorimetry



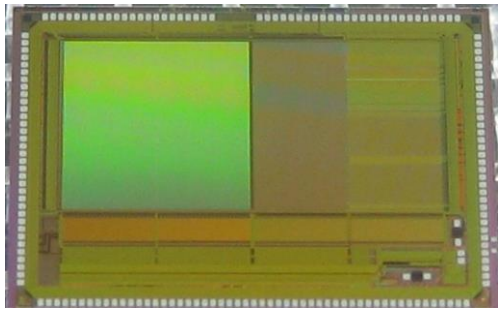
50μm pixel

PIMMS
TOF mass spectroscopy

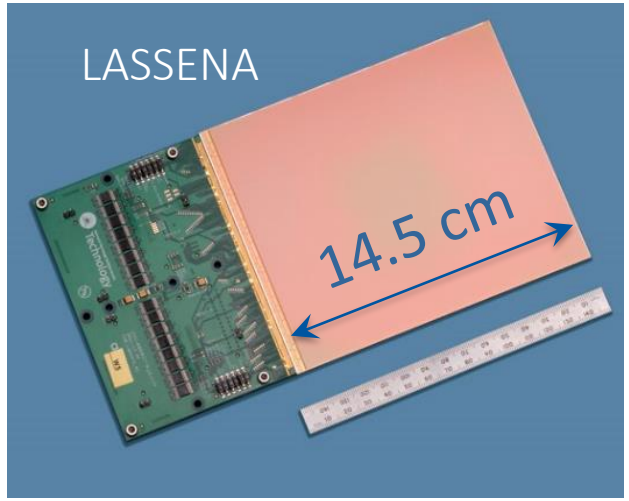


70μm pixel

CHERWELL
Calorimetry/Tracking



48 μm x 96 μm pixel



50μm pixel, waferscale

Also used for the ALPIDE (27 μm x 29 μm pixel), MALTA (36.4 x 36.4 μm pixel), and MIMOSIS (CBM)

Stitching in imaging technologies

Technique to cover areas with a single die larger than the reticle:

print several abutting fields from the reticle

Example: ER1 run in TPSCo 65nm ISC with two large **stitched** sensor chips (MOSS, MOST)

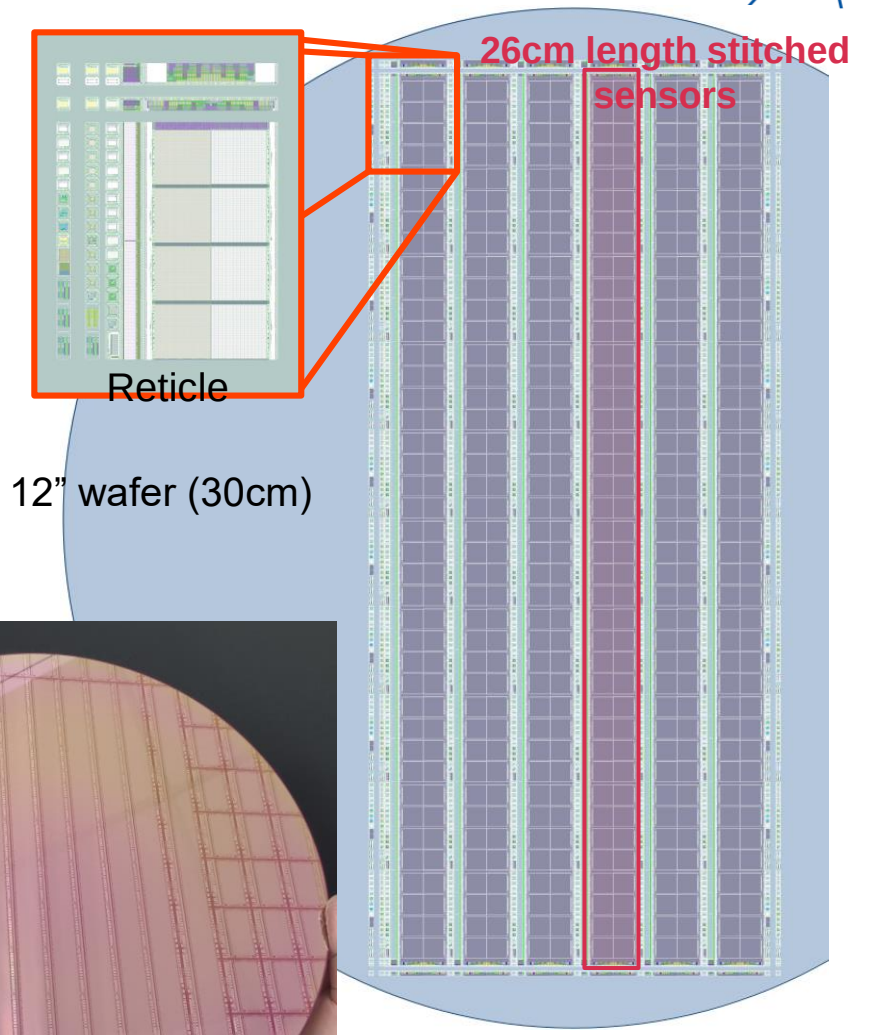
Different approaches for resilience to manufacturing faults

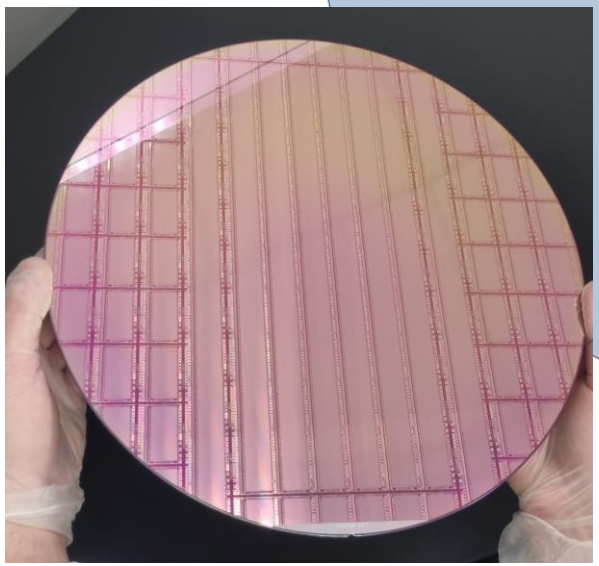
Challenges

Yield, power consumption andsupply drops, scale …

Available in several foundries

TSMC, Sony, Global foundries, …





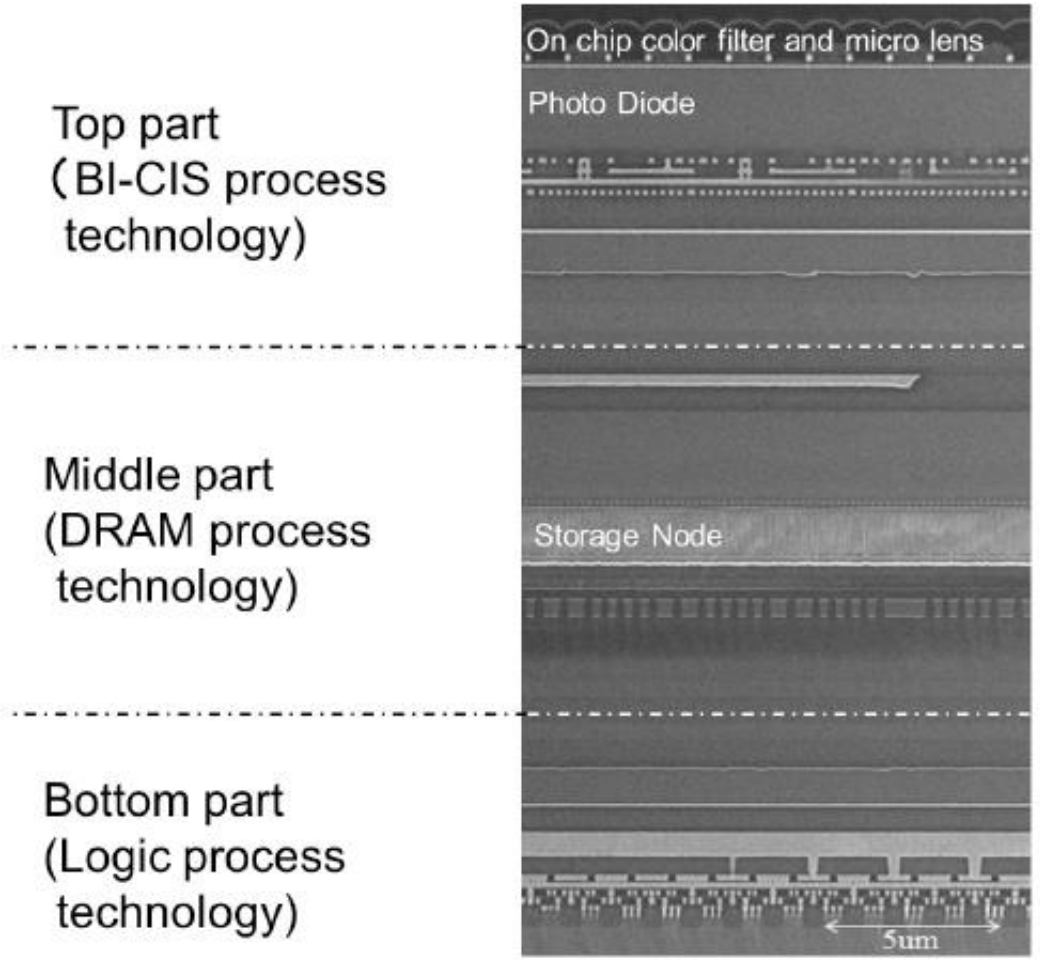
ER1 Pad wafer

Wafer stacking in CMOS imaging technologies

Several tiers (wafers) are stacked to assemble a full sensor, process is offered as a package in foundries

Is becoming available in several foundries or companies, mostly 2 layers only: SONY, TSMC, TJ180, TPSCo65nm…

Boundary between hybrid and monolithic becomes more vague



Example: SONY

Personal experience: TJ180nm and TPSCo65nm

Building knowledge about 65 nm for general interest

- Very significant contribution from the ALICE experiment
- Building on 10 year experience with 180 nm in the entire community (ALICE, ATLAS, CLIC, …)
- Towards full technology validation for our applications: full efficiency and SEU, TID according to expectations, further studies on sensor timing and NIEL:

  NIEL: 10^{15} n_{eq}/cm^2 at room temperature, investigating path to 10^{16} n_{eq}/cm^2
- Present stitching exercises will determine how we design silicon sensors in the future.

Features and outlook

- Performance superior in 65 nm compared to 180 nm technology, NRE cost high but 300 mm wafers….
- Specific imaging sensor features could still open further possibilities (only explored our ‘standard sensor’):
  - stacked photodiode
  - gain in the pixel
  - …
- Possibility of wafer stacking (65 nm imager wafer + 65 nm CMOS readout wafer)

Personal experience: TJ180nm and TPSCo65nm

The fine print: the unfashionable but important bits

- Interaction with the foundry requires care:
  - Need construction or production project to raise interest and obtain good support (good earlier experience with ALPIDE and ALICE ITS2), monolithic one of the areas with potentially large volume
  - No spurious requests, good follow up of requests and questions
  - Confidentiality of sensitive data (eg doping profiles)

- Significant effort to support community (pdk, drc, special layers, admin…).
- Complexity increases significantly, evolving towards digital-on-top to maintain manageability for verification, power analysis, etc.
- Cannot handle many technologies in parallel, need to concentrate resources

- EP R&D WP1.2 will in synergy with ALICE, community and other EP R&D workpackages, pursue TPSCo 65nm and contribute with relevant part of baseline program of Test, Design and Installing a common framework for the community for TPSCo 65 nm, and possibly join, as an opportunity to diversify, DRDT collaboration active in other promising areas (see presentation in EP R&D days)

DRDT 7.6 discussion:

- How to choose technological focus?
- How to avoid single technology source for “larger” projects?
- Should we go to deeper sub-micron than current?
- What model to manage relations to foundries?
- How to access sensible foundry information (NDAs, profiles for TCAD etc..)?
- Management of support?
- Design methodology? Digital tools and verification?

Cross-sections: