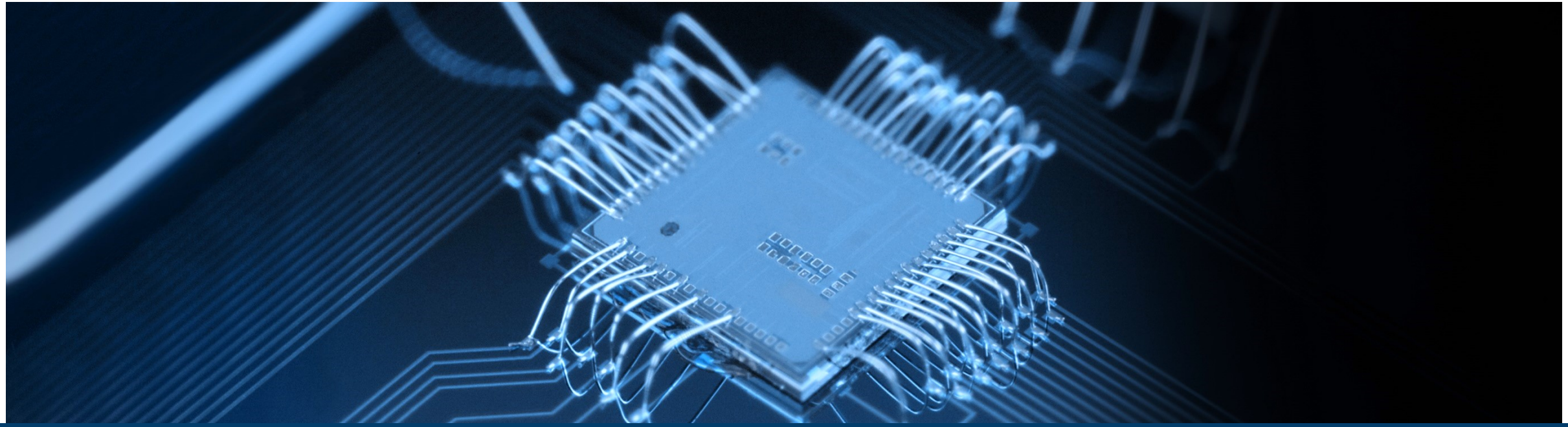


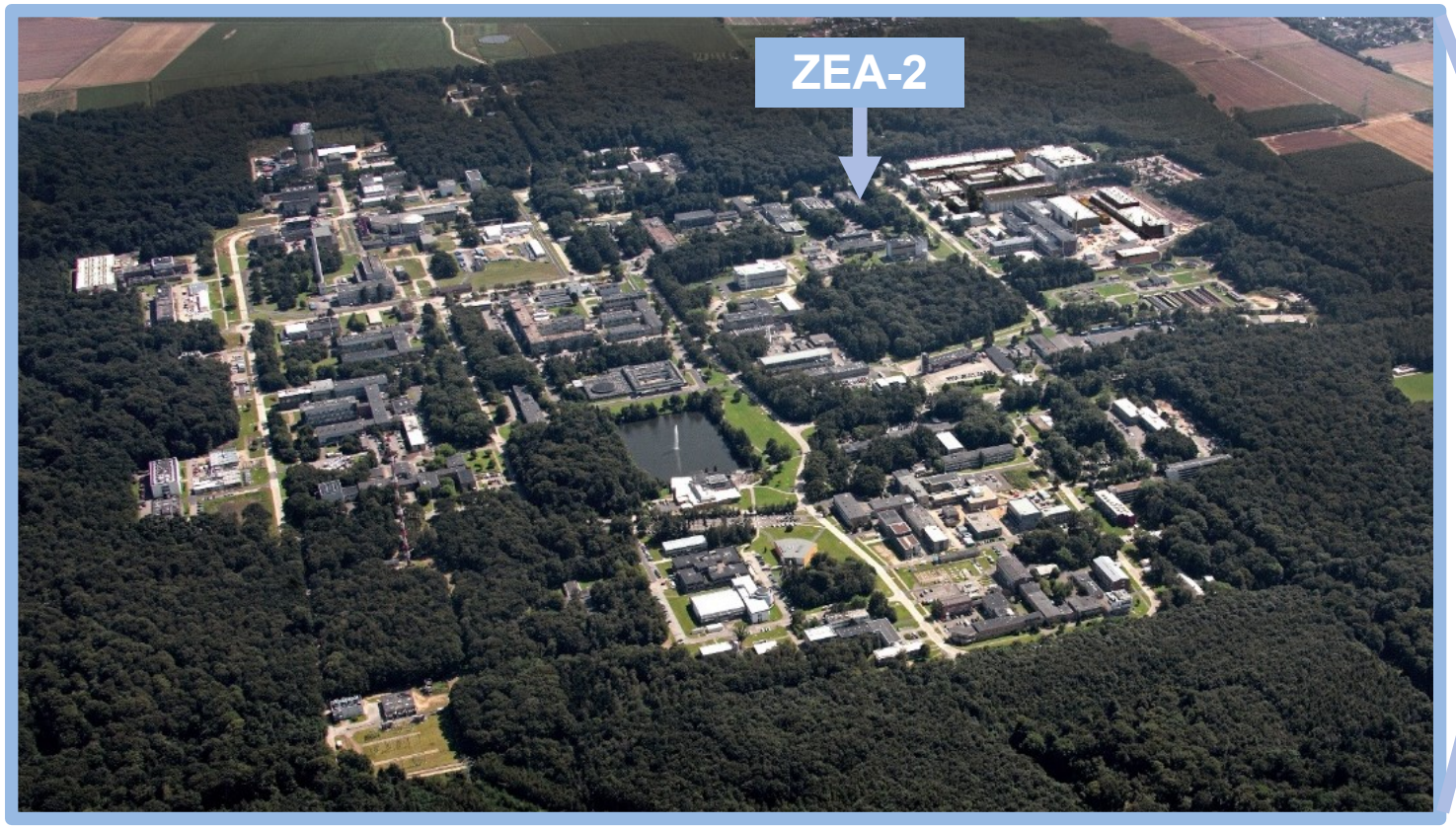
CRYOGENIC CMOS
POTENTIAL BEYOND QUANTUM

15.03.2023 | PATRICK VLIEX

JÜLICH Forschungszentrum | ZEA-2 Electronic Systems

ZEA-2 – ELECTRONIC SYSTEMS

Research Center Jülich



JÜLICH Forschungszentrum | ZEA-2 Electronic Systems

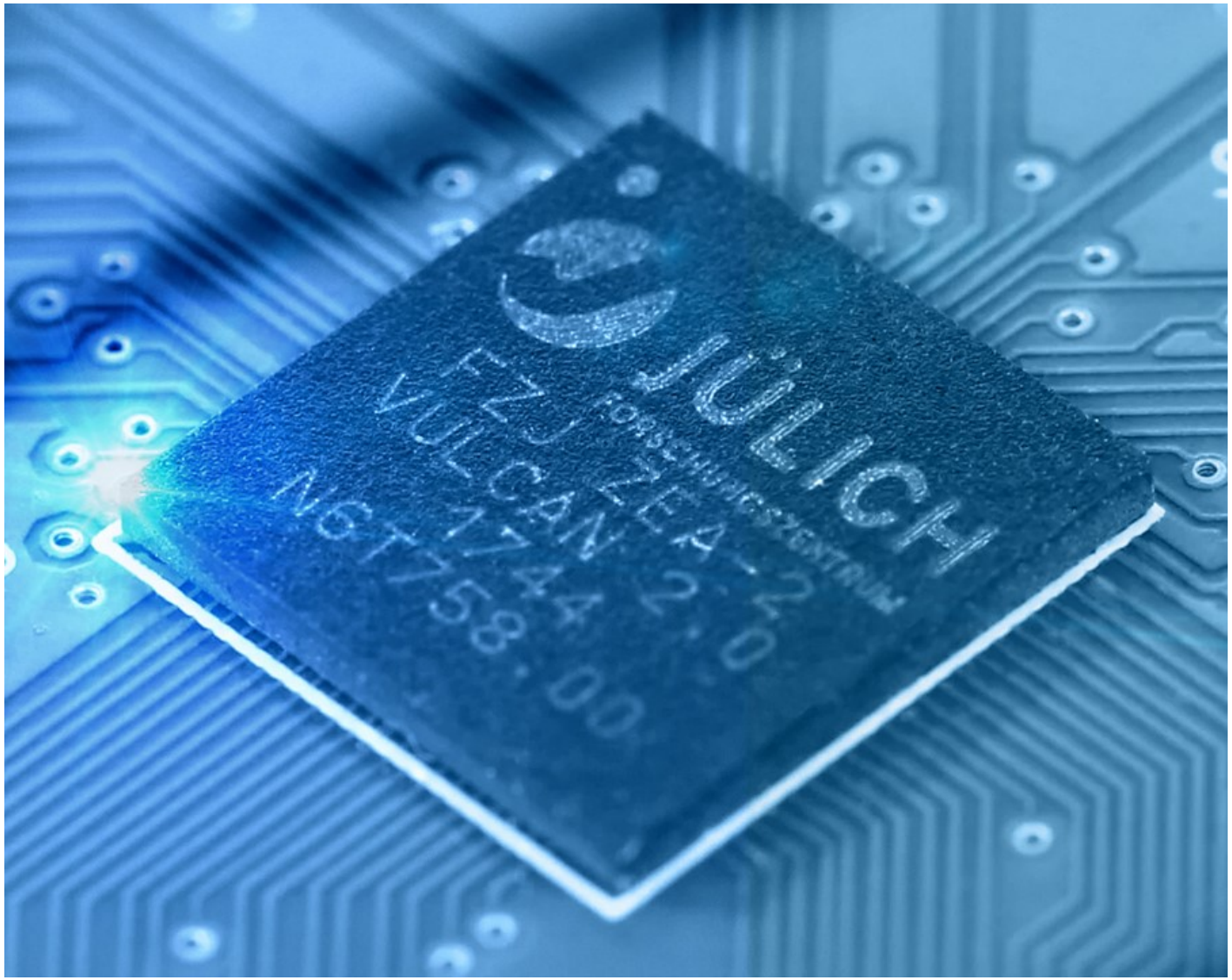
ZEA-2

Electronic Systems

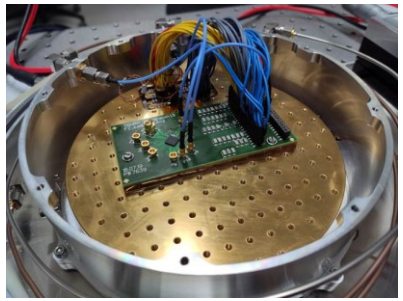
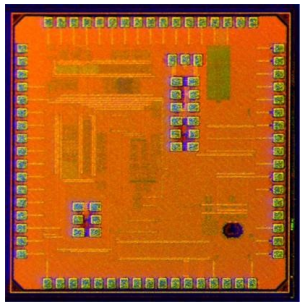
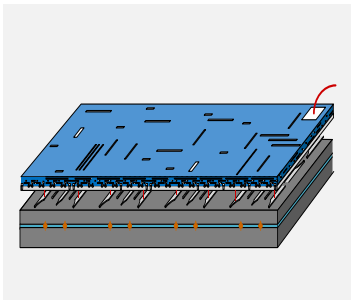
The **Central Institute of Engineering, Electronics and Analytics** - Electronic Systems (ZEA-2) is a **scientific institute** of Forschungszentrum Jülich GmbH performing **research and development** projects in **cooperation** with **institutes of the research center** as well as external **partners.**

Mission Statement of ZEA-2

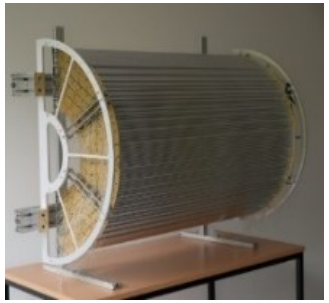
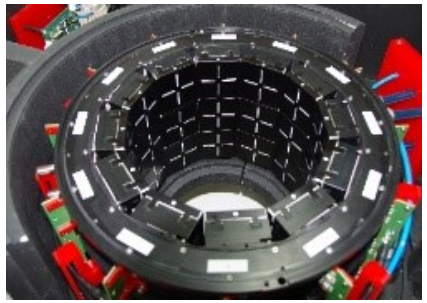
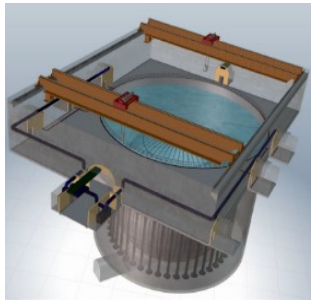
Focusing on interdisciplinary challenges, we research on **innovative, scalable SoC solutions** targeting efficient information extraction.



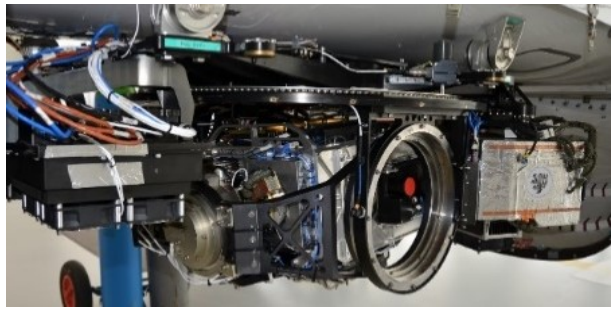
ZEA-2 – RESEARCH FIELDS

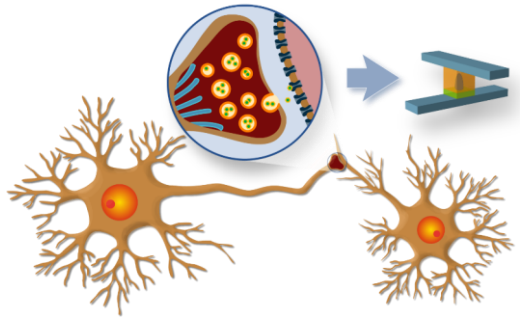
Electronic Systems for Quantum Computing
C. Degenhardt / C. Grewing

Detector Systems
C. Grewing

Measurement Systems
E. Zimmermann



Electronic Systems for Neuromorphic Computing
S. van Waasen

CRYOGENIC CMOS

A brief look into history

- Earliest IEEE publications: dating back to the early 1980's
- Single device characteristic at 77K
  - Focus on performance gains

Cryogenic behavior of scaled CMOS devices

Publisher: IEEE | Cite This | PDF

J.W. Schrankler ; J.S.T. Huang ; R.S.L. Lutze ; H.P. Vyas ; G.D. Kirchner All Authors

23 Paper Citations | 131 Full Text Views

Abstract | Authors | References | Citations | Keywords | Metrics

Abstract:
Performance enchancements of scaled CMOS devices are studied at room and liquid nitrogen temperatures. The extent of propogation delay improvement at low temperature is limited by velocity saturation as device channel lengths are decreased and or the supply voltage is increased. Liquid nitrogen temperature operation increases low field mobility by a factor of 4 while the saturation velocity increases only 30%. An analytical model is developed for device switching speed which includes velocity saturation effects. The model accurately predicts measured propogation delay on scaled CMOS delay chains with channel lengths down to 0.5 µm.

Published in: 1984 International Electron Devices Meeting

Date of Conference: 09-12 December 1984
DOI: 10.1109/IEDM.1984.190792
Date Added to IEEE *Xplore*: 09 August 2005
Publisher: IEEE
Conference Location: San Francisco, CA, USA

1984[1]

Investigation of cryogenic CMOS performance

Publisher: IEEE | Cite This | PDF

G. Gildenblat ; L. Colonna-Romano ; D. Lau ; D.E. Nelsen All Authors

25 Paper Citations | 536 Full Text Views

Abstract | Authors | References | Citations | Keywords | Metrics

Abstract:
The performance of cryogenic CMOS (CRYOCMOS) operation is investigated at the device, circuit and system levels. With the exception of saturation transconductance, device parameters are monotonic functions of the ambient temperature in the 10-300K range. Direct measurements demonstrate the absence of freezeout in the channel of enhancement type MOSFET's. CRYOCMOS scaling is discussed. The speed advantage is reduced for the non-ideal scaling. However, if the gate drive and device dimensions are scaled proportionally, the performance gain of CRYOCMOS remains unchanged. The switching time is a monotonic function of temperature down to 10K. The operation of a microcomputer with a CMOS-based CPU immersed in liquid nitrogen results in speed increase of about 100% as compared with room temperature operation.

Published in: 1985 International Electron Devices Meeting

Date of Conference: 01-04 December 1985
DOI: 10.1109/IEDM.1985.190948
Date Added to IEEE *Xplore*: 09 August 2005
Publisher: IEEE

1985[2]

[1] J. W. Schrankler, J. S. T. Huang, R. S. L. Lutze, H. P. Vyas and G. D. Kirchner, "Cryogenic behavior of scaled CMOS devices," *1984 International Electron Devices Meeting*, San Francisco, CA, USA, 1984, pp. 598-600, doi: 10.1109/IEDM.1984.190792.
[2] G. Gildenblat, L. Colonna-Romano, D. Lau and D. E. Nelsen, "Investigation of cryogenic CMOS performance," *1985 International Electron Devices Meeting*, Washington, DC, USA, 1985, pp. 268-271, doi: 10.1109/IEDM.1985.190948.

CRYOGENIC CMOS

A brief look into history

CMOS is typically specified to -40°C (233 K)
Cryogenic means <120 K for us

One year later: down to 10K

- Earliest IEEE publications: dating back to the early 1980's

- Single device characteristic at 77K
  - Focus on performance gains

Cryogenic behavior of scaled CMOS devices

Publisher: IEEE | Cite This | PDF

J.W. Schrankler ; J.S.T. Huang ; R.S.L. Lutze ; H.P. Vyas ; G.D. Kirchner All Authors

23 Paper Citations | 131 Full Text Views

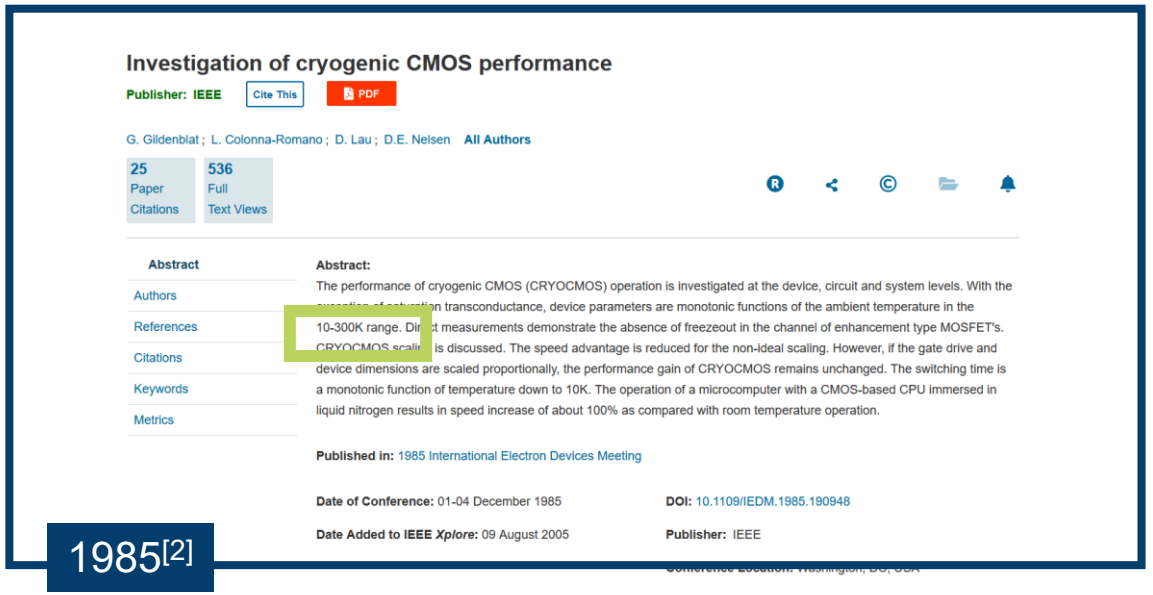
Abstract | Authors | References | Citations | Keywords | Metrics

Abstract:
Performance enchancements of scaled CMOS devices are studied at room and liquid nitrogen temperatures. The extent of propogation delay improvement at low temperature is limited by velocity saturation as device channel lengths are decreased and or the supply voltage is increased. Liquid nitrogen temperature operation increases low field mobility by a factor of 4 while the saturation velocity increases only 30%. An analytical model is developed for device switching speed which includes velocity saturation effects. The model accurately predicts measured propogation delay on scaled CMOS delay chains with channel lengths down to 0.5 µm.

Published in: 1984 International Electron Devices Meeting

Date of Conference: 09-12 December 1984
DOI: 10.1109/IEDM.1984.190792
Date Added to IEEE *Xplore*: 09 August 2005
Publisher: IEEE
Conference Location: San Francisco, CA, USA

1984[1]



Investigation of cryogenic CMOS performance

Publisher: IEEE | Cite This | PDF

G. Gildenblat ; L. Colonna-Romano ; D. Lau ; D.E. Nelsen All Authors

25 Paper Citations | 536 Full Text Views

Abstract | Authors | References | Citations | Keywords | Metrics

Abstract:
The performance of cryogenic CMOS (CRYOCMOS) operation is investigated at the device, circuit and system levels. With the [illegible] transconductance, device parameters are monotonic functions of the ambient temperature in the 10-300K range. Direct measurements demonstrate the absence of freezeout in the channel of enhancement type MOSFET's. CRYOCMOS scaling is discussed. The speed advantage is reduced for the non-ideal scaling. However, if the gate drive and device dimensions are scaled proportionally, the performance gain of CRYOCMOS remains unchanged. The switching time is a monotonic function of temperature down to 10K. The operation of a microcomputer with a CMOS-based CPU immersed in liquid nitrogen results in speed increase of about 100% as compared with room temperature operation.

Published in: 1985 International Electron Devices Meeting

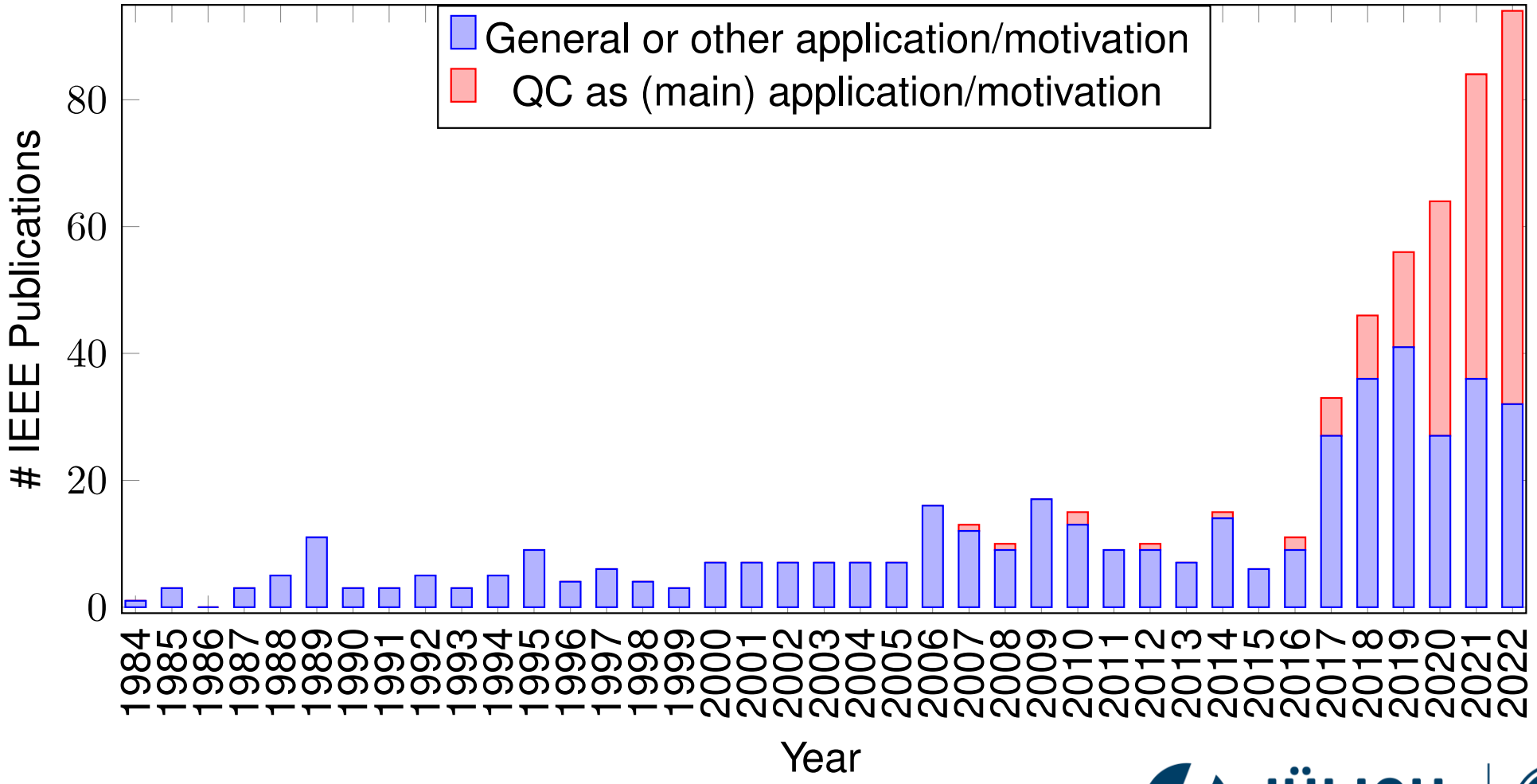
Date of Conference: 01-04 December 1985
DOI: 10.1109/IEDM.1985.190948
Date Added to IEEE *Xplore*: 09 August 2005
Publisher: IEEE

1985[2]

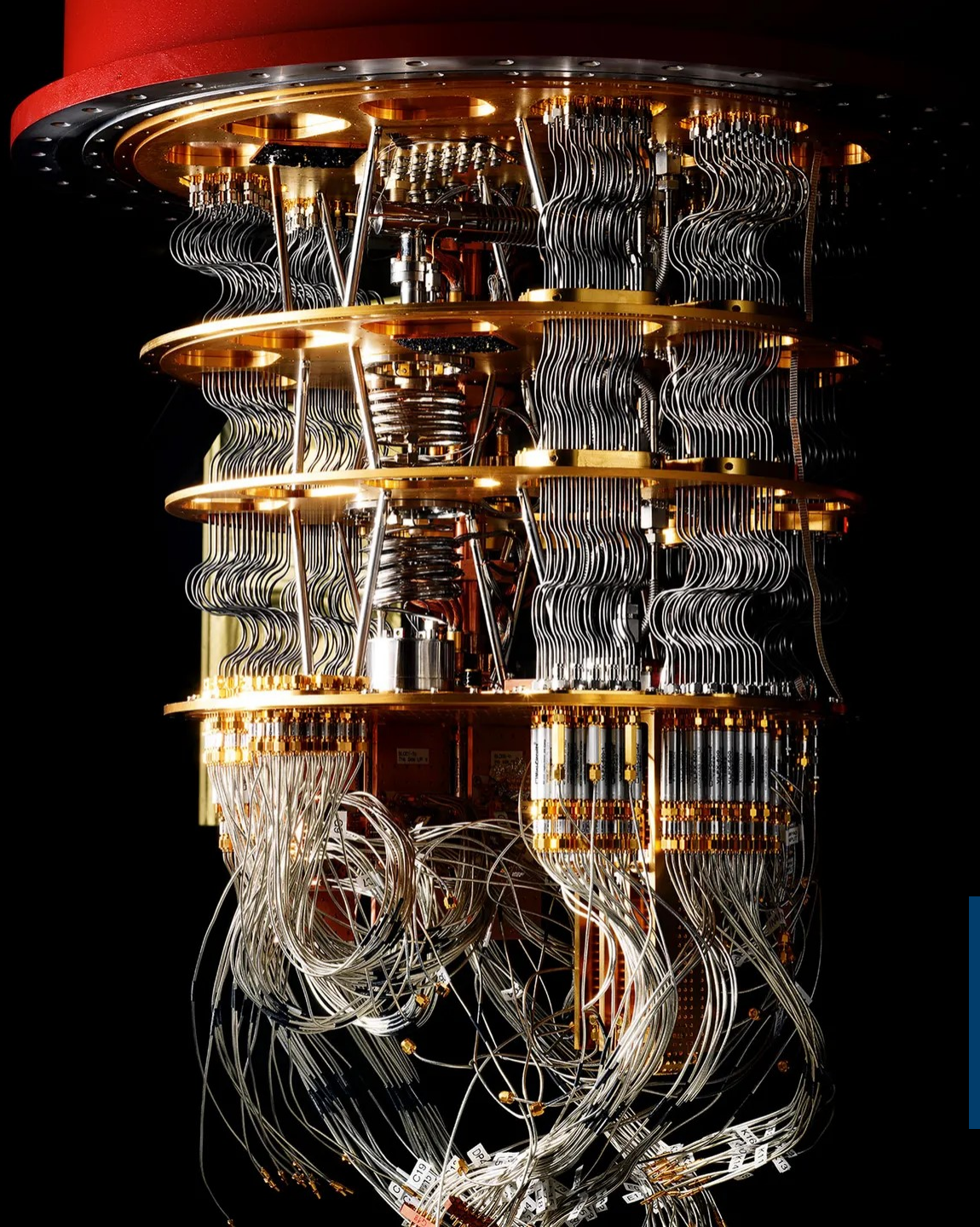
[1] J. W. Schrankler, J. S. T. Huang, R. S. L. Lutze, H. P. Vyas and G. D. Kirchner, "Cryogenic behavior of scaled CMOS devices," *1984 International Electron Devices Meeting*, San Francisco, CA, USA, 1984, pp. 598-600, doi: 10.1109/IEDM.1984.190792.
[2] G. Gildenblat, L. Colonna-Romano, D. Lau and D. E. Nelsen, "Investigation of cryogenic CMOS performance," *1985 International Electron Devices Meeting*, Washington, DC, USA, 1985, pp. 268-271, doi: 10.1109/IEDM.1985.190948.

CRYOGENIC CMOS

Focus of accelerated research for Quantum Computing (QC)



JÜLICH Forschungszentrum | ZEA-2 Electronic Systems



Cryostat for Quantum Computing at Google

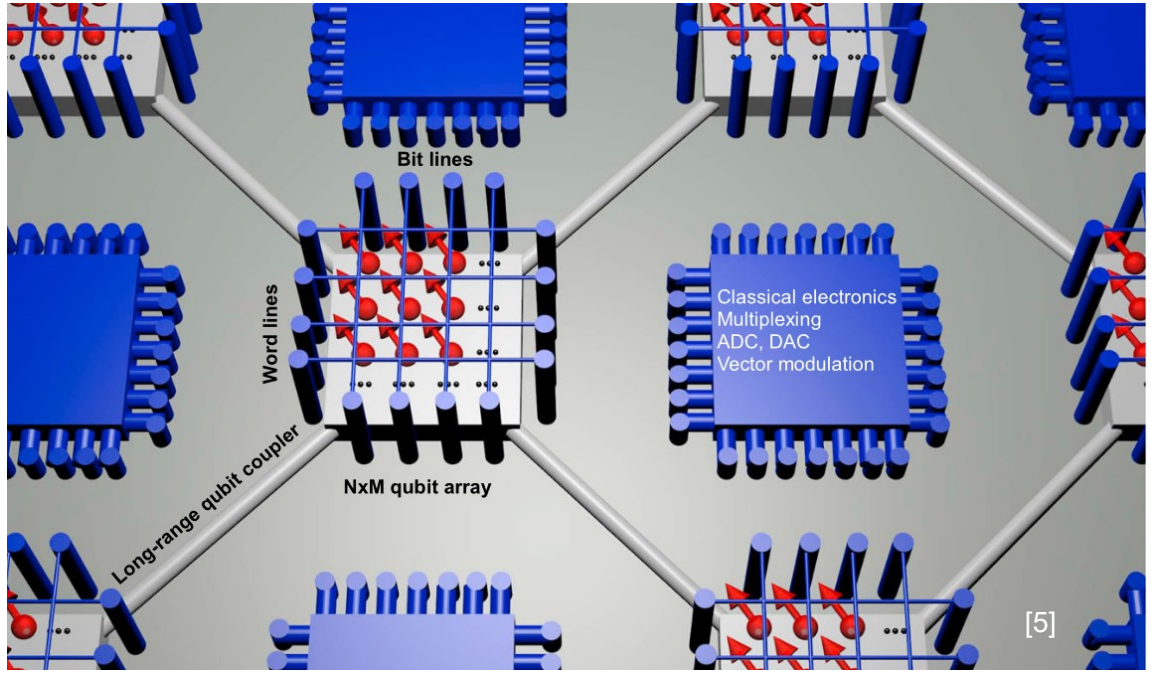
https://www.wired.co.uk/article/quantum-supremacy-google-microsoft-ibm

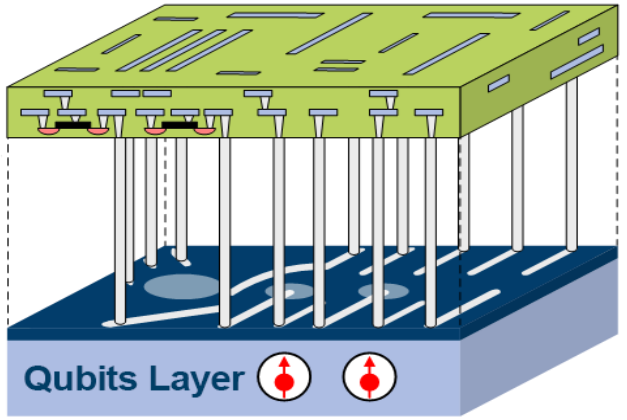
THE WIRING BOTTLENECK

Cryogenic CMOS as scaling solution

- How to scale into millions of qubits?
  - Cables from room temperature are unlikely

- **Solution concept: use of cryogenic CMOS**
  - **2007:** Avoid parasitics of long cables[3]
  - **2016:** Local control loops inside the fridge[4]
  - **2017:** Sparse qubit array & full 3D integration[5]





Classical CMOS IC Layer

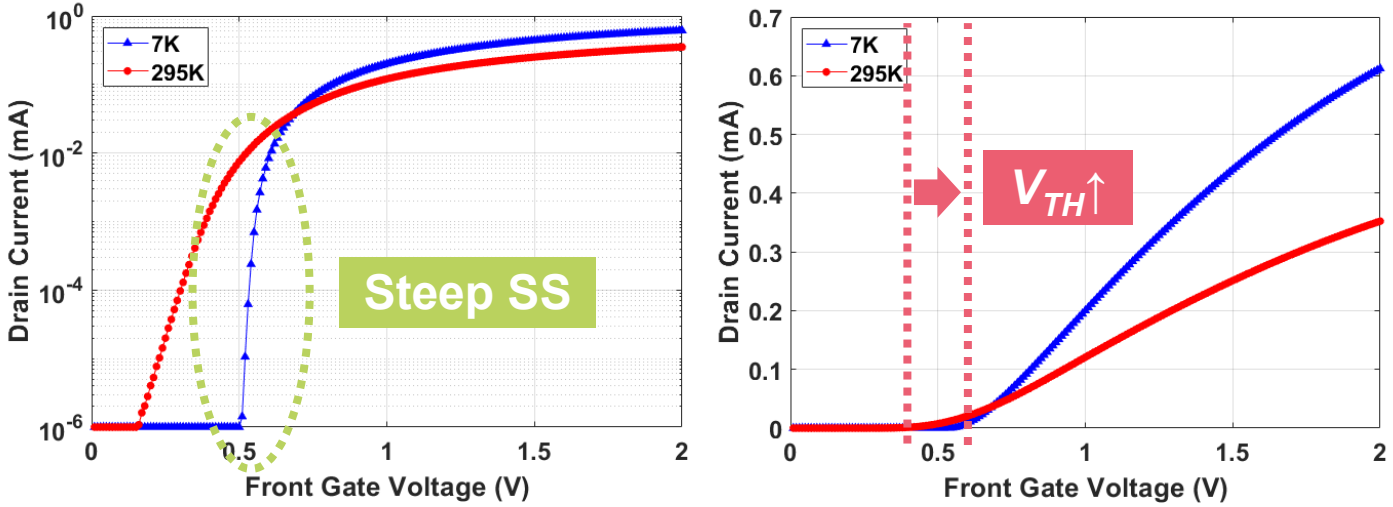
Through-Silicon Vias (TSVs)

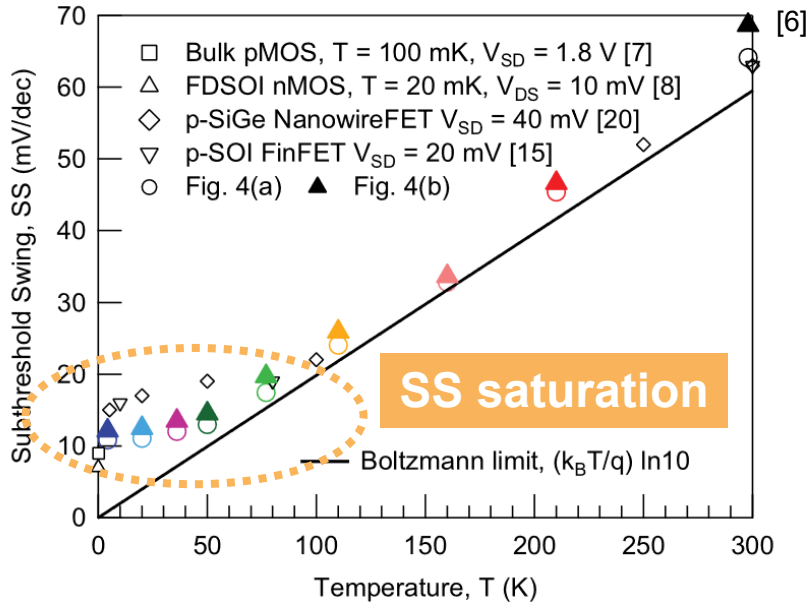
[3] S. R. Ekanayake, T. Lehmann, A. S. Dzurak and R. G. Clark, "Quantum bit controller and observer circuits in SOS-CMOS technology for gigahertz low-temperature operation," *2007 7th IEEE Conference on Nanotechnology (IEEE NANO)*, Hong Kong, China, 2007, pp. 1283-1287, doi: 10.1109/NANO.2007.4601417.
[4] E. Charbon *et al.*, "Cryo-CMOS for quantum computing," *2016 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2016, pp. 13.5.1-13.5.4, doi: 10.1109/IEDM.2016.7838410.
[5] Vandersypen, L.M.K., Bluhm, H., Clarke, J.S. *et al.* Interfacing spin qubits in quantum dots and donors—hot, dense, and coherent. *npj Quantum Inf* **3**, 34 (2017). https://doi.org/10.1038/s41534-017-0038-y

CRYOGENIC CMOS

Behavior from RT compared to cryo

- Reduced Johnson–Nyquist noise
- Increased subthreshold swing *SS* ☺
  - Negligible leakage currents ☺
  - Saturating at ~20 mV/dec for T≲70K 😐
- Increased mobility *μ* ☺
- Increased threshold voltage V_{TH} ☹





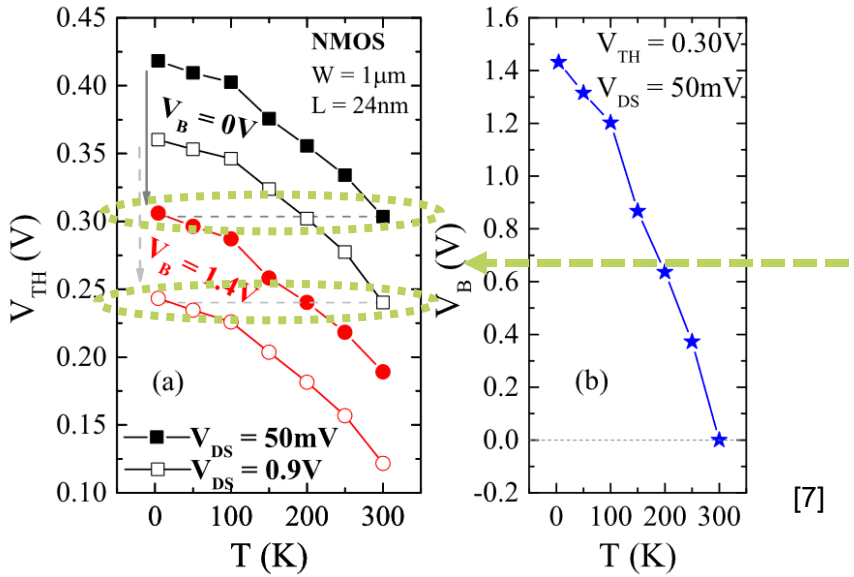
[6] A. Beckers, F. Jazaeri and C. Enz, "Theoretical Limit of Low Temperature Subthreshold Swing in Field-Effect Transistors," in *IEEE Electron Device Letters*, vol. 41, no. 2, pp. 276-279, Feb. 2020, doi: 10.1109/LED.2019.2963379.

CRYOGENIC CMOS

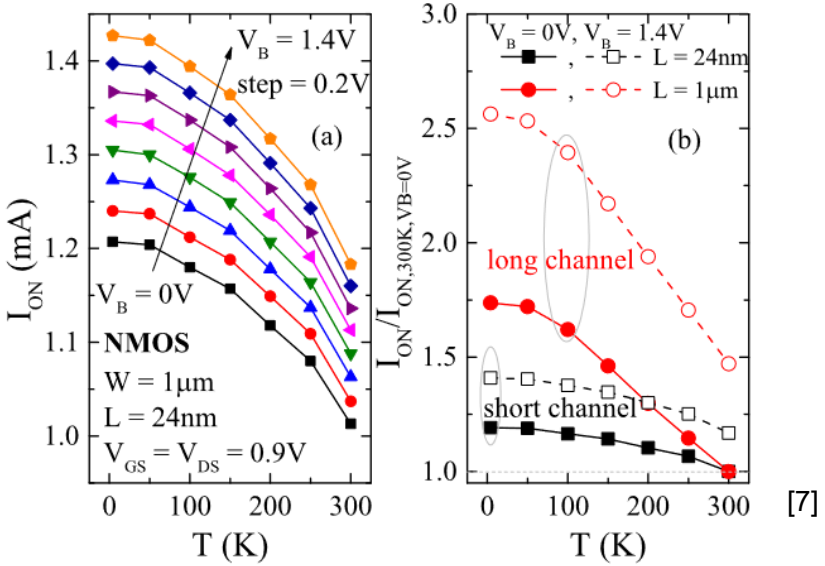
Behavior from RT compared to cryo

- Increased threshold voltage V_{TH} ☹

→ SOI*: Compensate with backgate voltage V_B ☺



- Increased ON-state current I_{ON} ☺



*silicon on insulator (SOI)

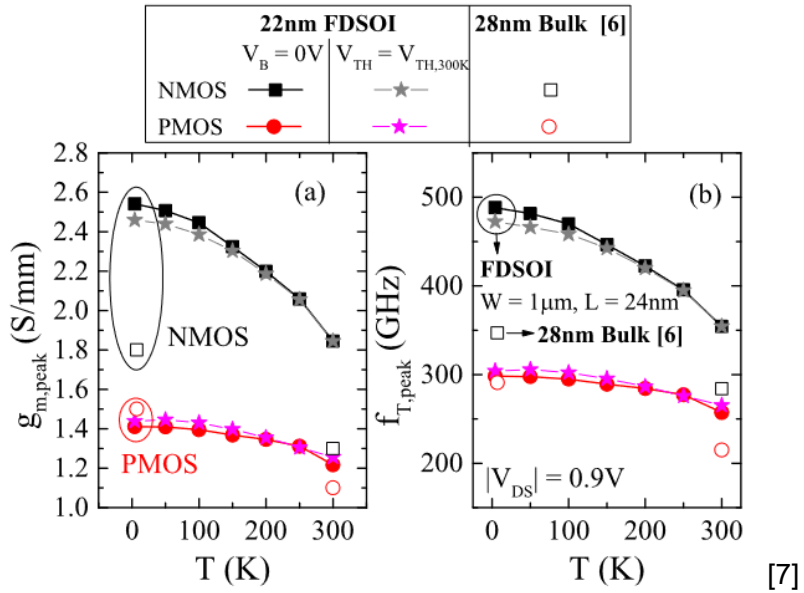
[7] B. Cardoso Paz *et al.*, "Performance and Low-Frequency Noise of 22-nm FDSOI Down to 4.2 K for Cryogenic Applications," in *IEEE Transactions on Electron Devices*, vol. 67, no. 11, pp. 4563-4567, Nov. 2020, doi: 10.1109/TED.2020.3021999.

CRYOGENIC CMOS

Behavior from RT compared to cryo

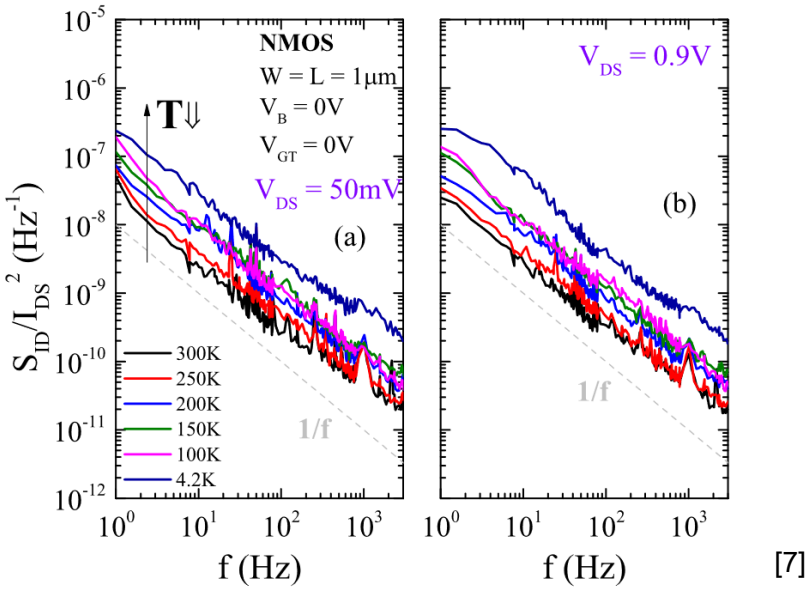
- ~~Kink, hysteresis and overshoot~~
- Not observed in modern nodes in operation range

- Increased $g_{m,peak}$ ☺
- Increased $f_{T,peak}$ ☺



[7]

- Increased 1/f Noise ☹
- Increased mismatch[8] ☹



[7]

[7] B. Cardoso Paz et al., "Performance and Low-Frequency Noise of 22-nm FDSOI Down to 4.2 K for Cryogenic Applications," in IEEE Transactions on Electron Devices, vol. 67, no. 11, pp. 4563-4567, Nov. 2020, doi: 10.1109/TED.2020.3021999.
[8] P. A. 'T Hart, M. Babaie, E. Charbon, A. Vladimirescu and F. Sebastiano, "Characterization and Modeling of Mismatch in Cryo-CMOS," in IEEE Journal of the Electron Devices Society, vol. 8, pp. 263-273, 2020, doi: 10.1109/JEDS.2020.2976546.

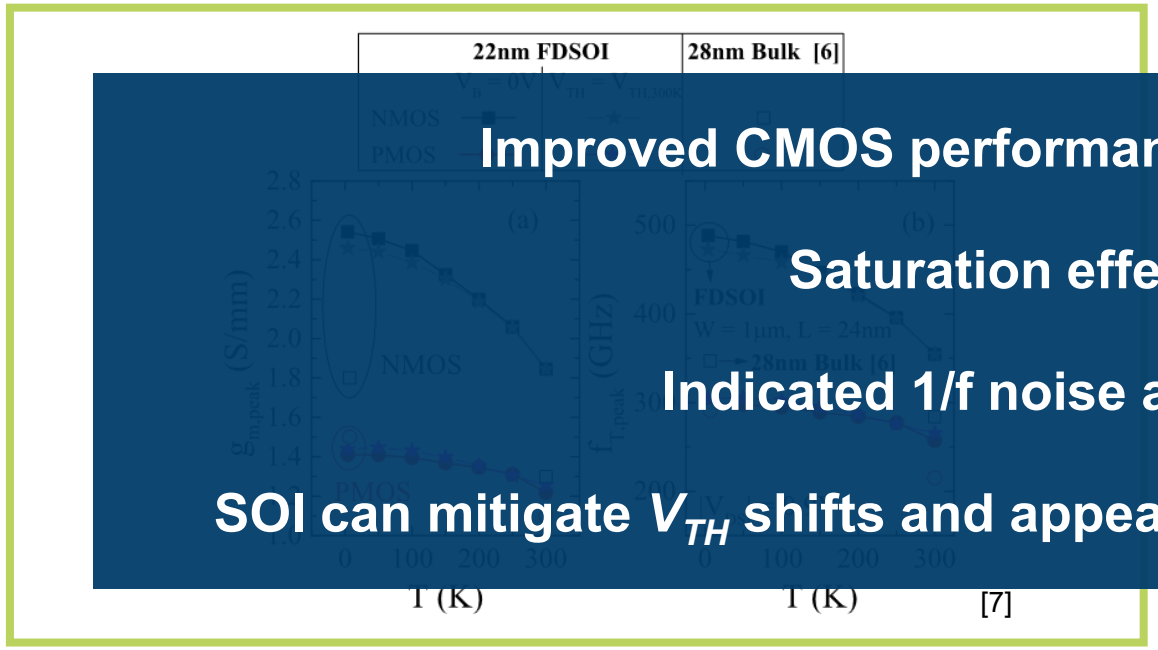
CRYOGENIC CMOS

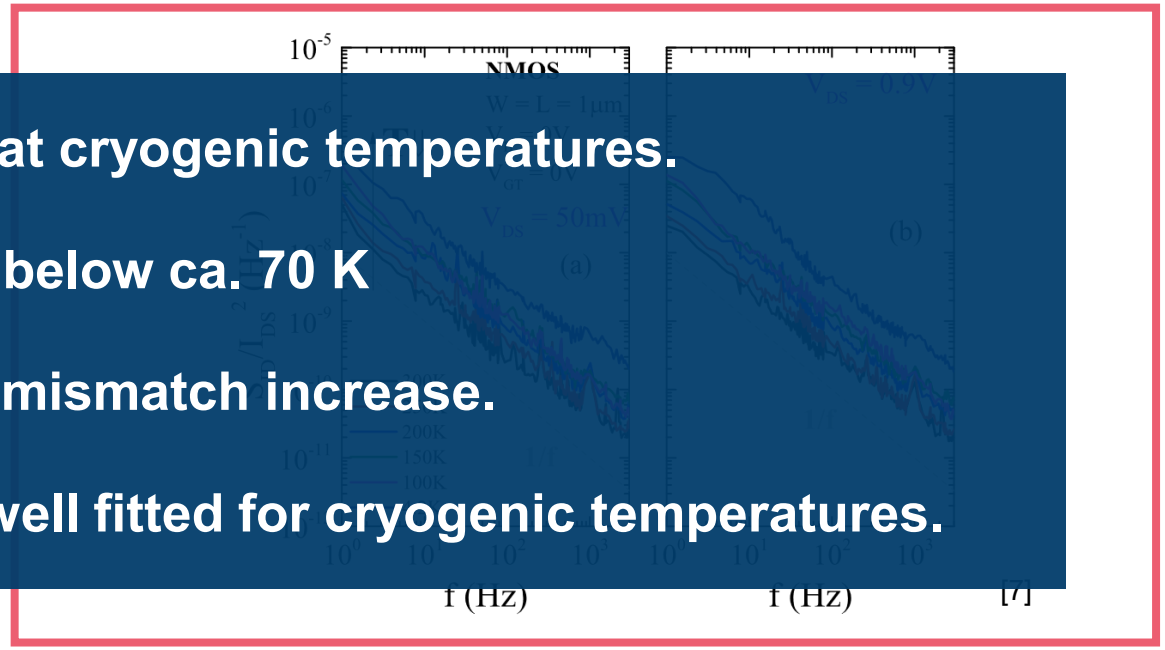
Behavior from RT compared to cryo

- ~~Kink, hysteresis and overshoot~~
- Not observed in modern nodes in operation range

- Increased $g_{m,peak}$ ☺
- Increased $f_{T,peak}$ ☺

- Increased 1/f Noise ☹
- Increased mismatch[8] ☹





Improved CMOS performance at cryogenic temperatures.

Saturation effects below ca. 70 K

Indicated 1/f noise and mismatch increase.

SOI can mitigate V_{TH} shifts and appears well fitted for cryogenic temperatures.

[7] B. Cardoso Paz et al., "Performance and Low-Frequency Noise of 22-nm FDSOI Down to 4.2 K for Cryogenic Applications," in IEEE Transactions on Electron Devices, vol. 67, no. 11, pp. 4563-4567, Nov. 2020, doi: 10.1109/TED.2020.3021999.
[8] P. A. 'T Hart, M. Babaie, E. Charbon, A. Vladimirescu and F. Sebastiano, "Characterization and Modeling of Mismatch in Cryo-CMOS," in IEEE Journal of the Electron Devices Society, vol. 8, pp. 263-273, 2020, doi: 10.1109/JEDS.2020.2976546.

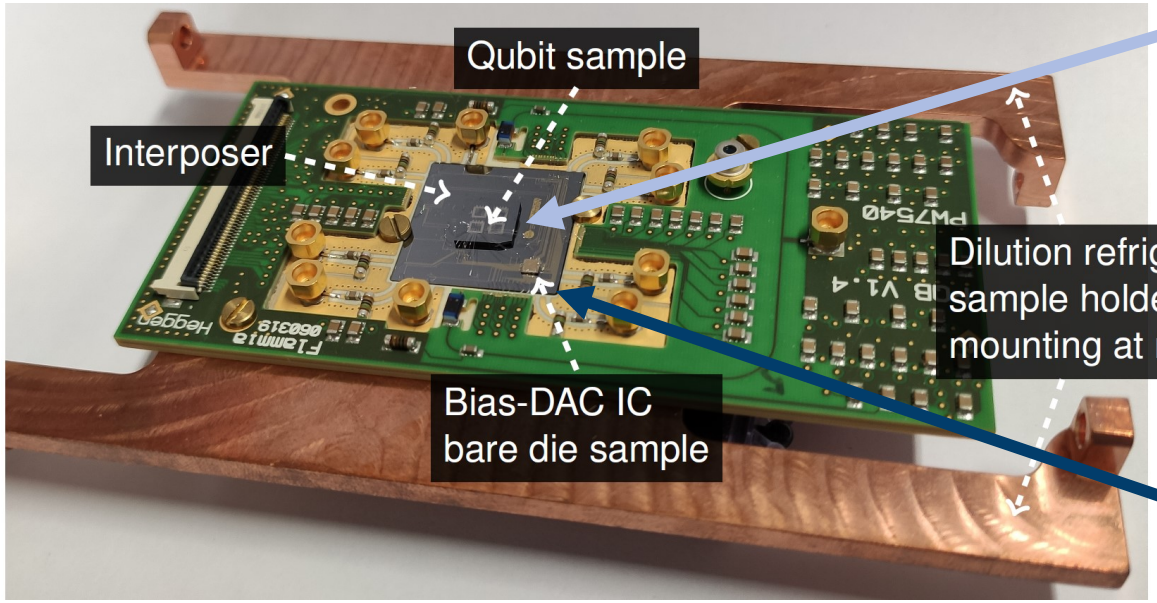
JÜLICH Forschungszentrum | ZEA-2 Electronic Systems

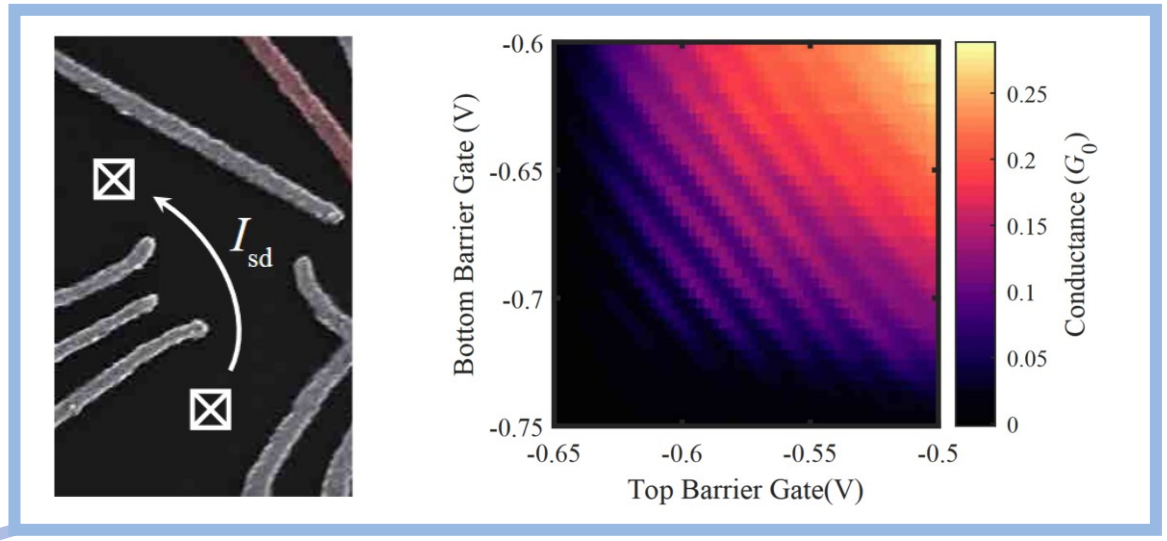
CMOS DEMONSTRATOR

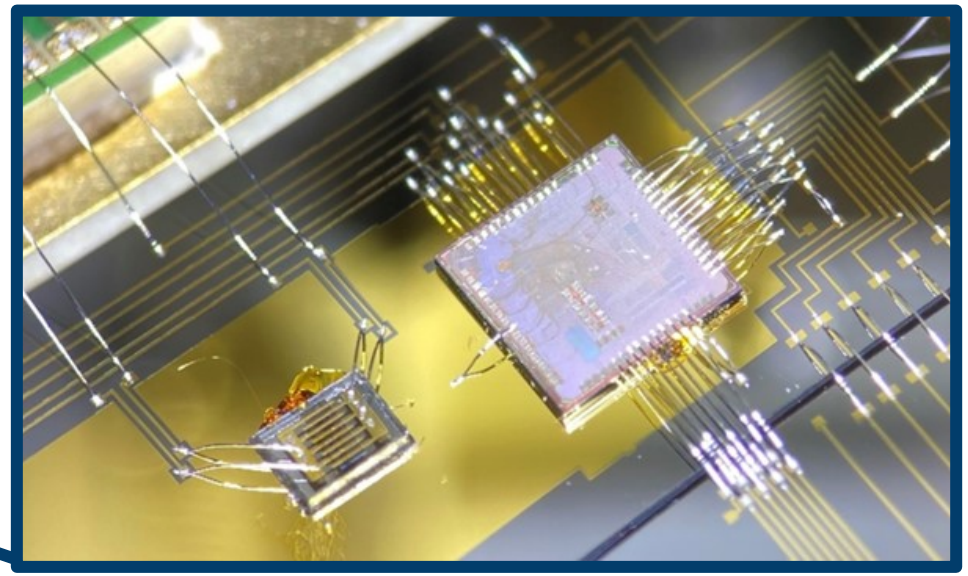
Operating CMOS IC sub-1K

- Bias-DAC in 65nm bulk CMOS[9]
- Low power consumption of 3µW per channel
- Demonstrate local SET* biasing at <1 K[10]

*single electron transistor (SET)





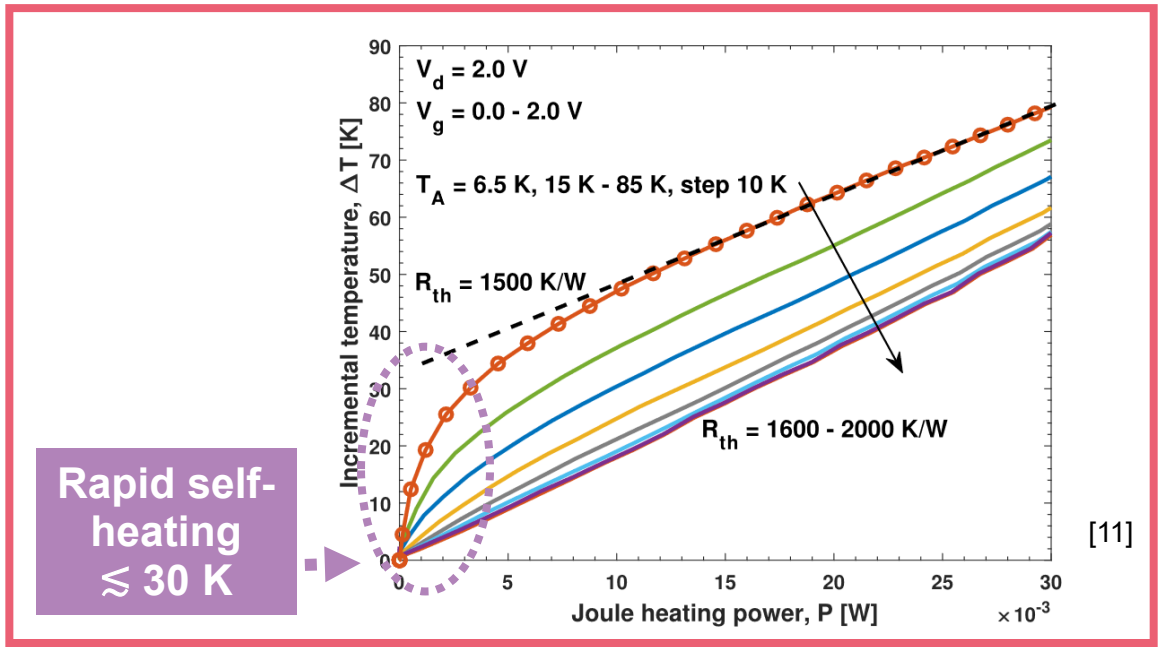


[9] P. Vliex *et al.*, "Bias Voltage DAC Operating at Cryogenic Temperatures for Solid-State Qubit Applications," in *IEEE Solid-State Circuits Letters*, vol. 3, pp. 218-221, 2020, doi: 10.1109/LSSC.2020.3011576.
[10] R. Otten, L. Schreckenberg, P. Vliex *et al.*, "Qubit Bias using a CMOS DAC at mK Temperatures," *2022 29th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Glasgow, United Kingdom, 2022, pp. 1-4, doi: 10.1109/ICECS202256217.2022.9971043.

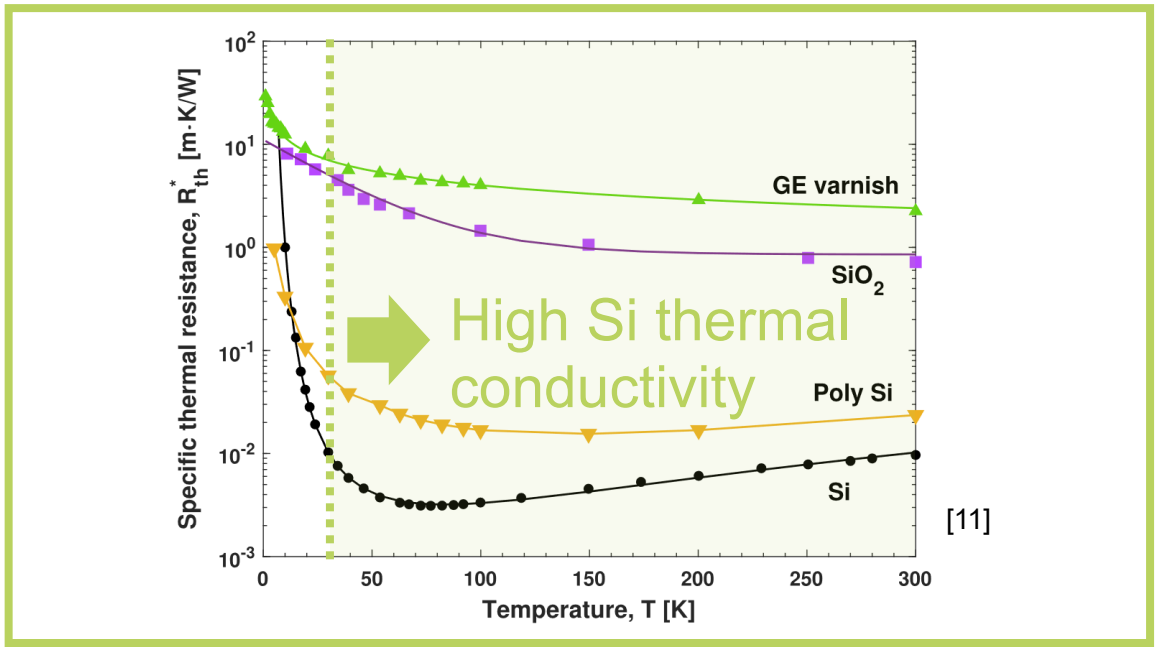
ONGOING RESEARCH

Cryogenic CMOS

- **Thermal management**
  - Further optimizing Bias-DAC thermals
- **Self-heating**
  - Decreased Si thermal conductivity ≲ 30 K



- **Cryogenic CMOS Process-Development-Kit**
  - Accurate device models in simulations
- **Cryogenic CMOS process optimization**
  - No leakage → Lower V_{TH} → Lower V_{DD}
  - Improve power efficiency



[11] A. A. Artanov *et al.*, "Self-Heating Effect in a 65 nm MOSFET at Cryogenic Temperatures," in *IEEE Transactions on Electron Devices*, vol. 69, no. 3, pp. 900-904, March 2022, doi: 10.1109/TED.2021.3139563.

SOLID

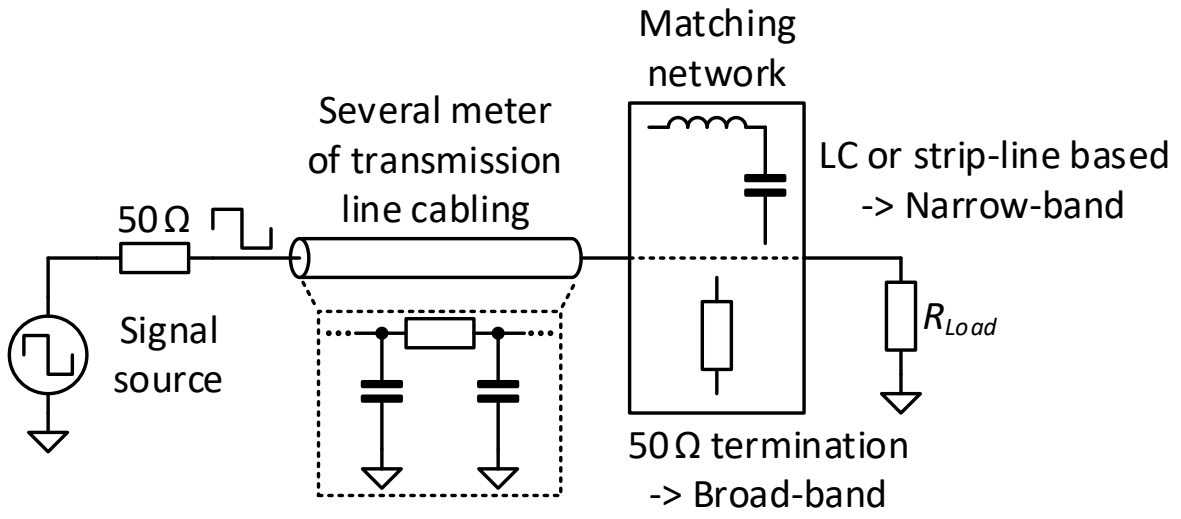
JÜLICH Forschungszentrum | ZEA-2 Electronic Systems

POTENTIAL BEYOND QUANTUM

What has cryogenic CMOS to offer

- Signals without wave characteristic
  - **Limited bandwidth by wire capacitance** ☹
- Signals with wave characteristic
  - Matching network required ☹
  - **Power consumption by 50 Ω matching** ☹

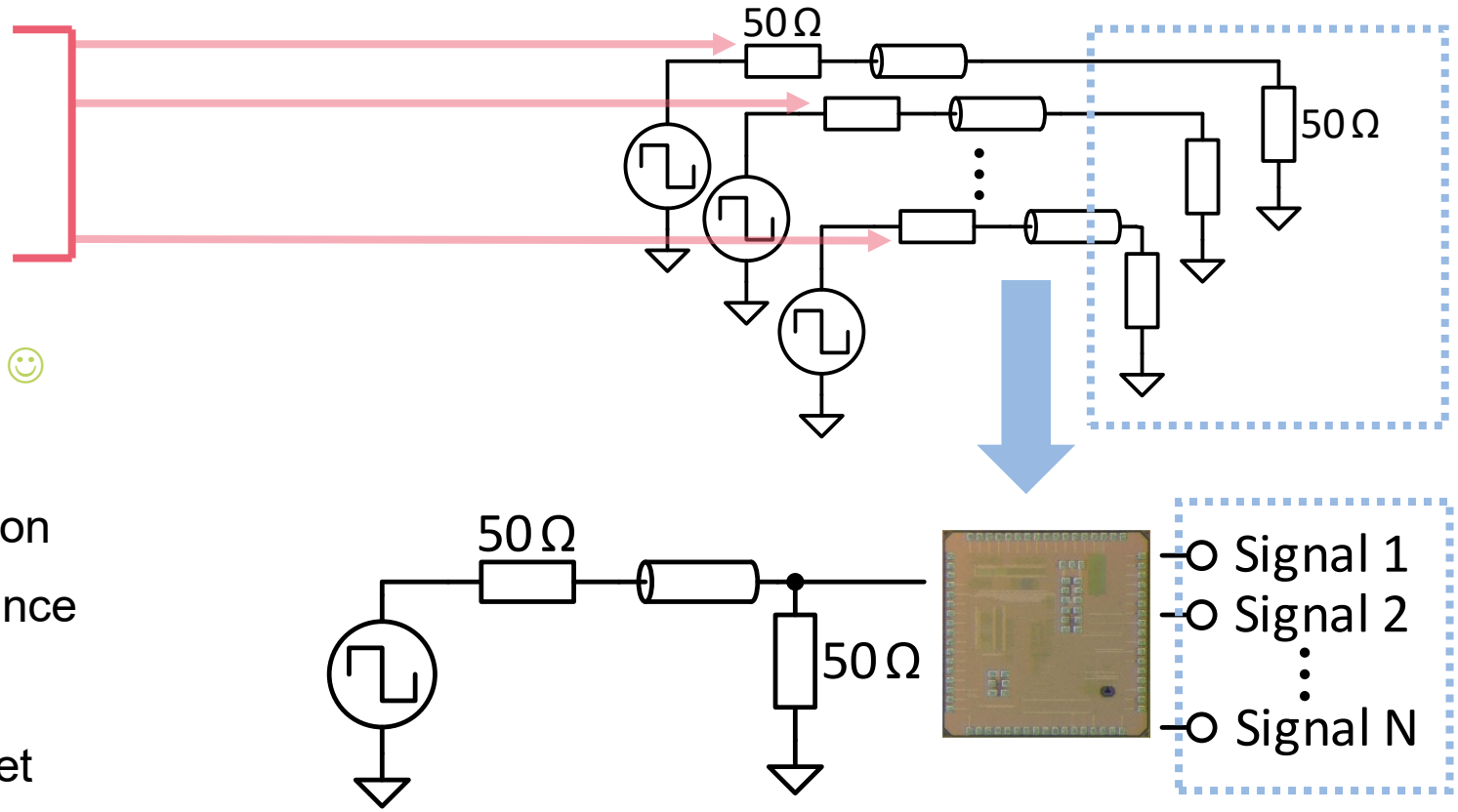
- **Avoid cable capacitance and parasitics** ☺
  - No 50 Ω matching needed (short wires)
  - Increased bandwidths available
  - No need for compensation of parasitics



POTENTIAL BEYOND QUANTUM

What has cryogenic CMOS to offer

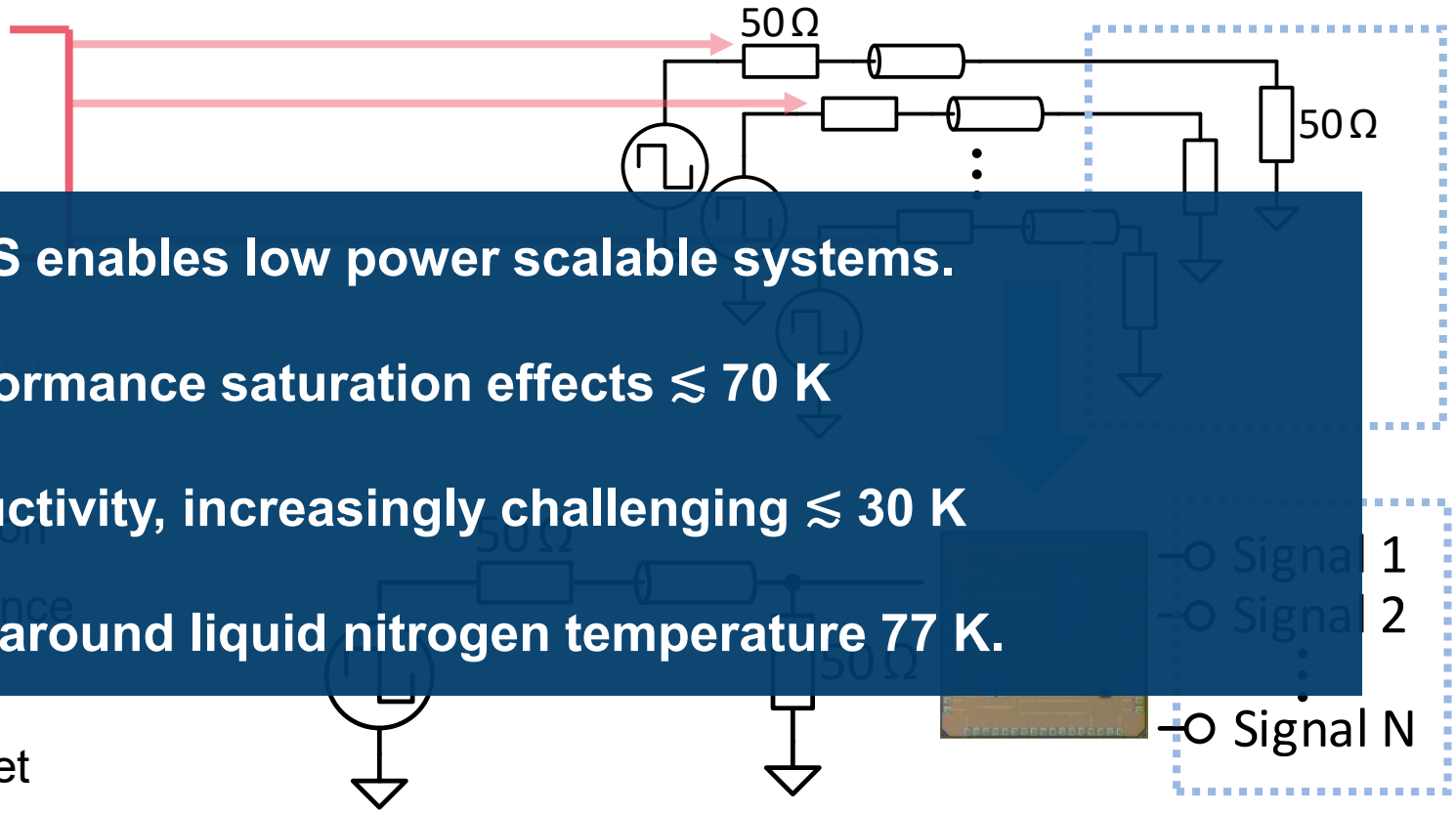
- **Wiring bottlenecks**
  - One (matched) wire per signal ☹
  - High thermal load due to wires ☹
- **CMOS chip providing multiple signals ☺**
  - Avoiding 50 Ω matching per signal
  - Local processing and signal generation
  - Improved cryogenic CMOS performance
  - Build low power systems
  - More cooling capacity & power budget



POTENTIAL BEYOND QUANTUM

What has cryogenic CMOS to offer

- **Wiring bottlenecks**
  - One (matched) wire per signal ☹
  - High thermal load due to wires ☹
- **CMOS chip providing multiplexing**
  - Avoiding 50 Ω matching per signal
  - Local processing and signal generation
  - Improved cryogenic CMOS performance
  - Build low power systems
  - More cooling capacity & power budget



Cryogenic CMOS enables low power scalable systems.

CMOS performance saturation effects ≲ 70 K

Si thermal conductivity, increasingly challenging ≲ 30 K

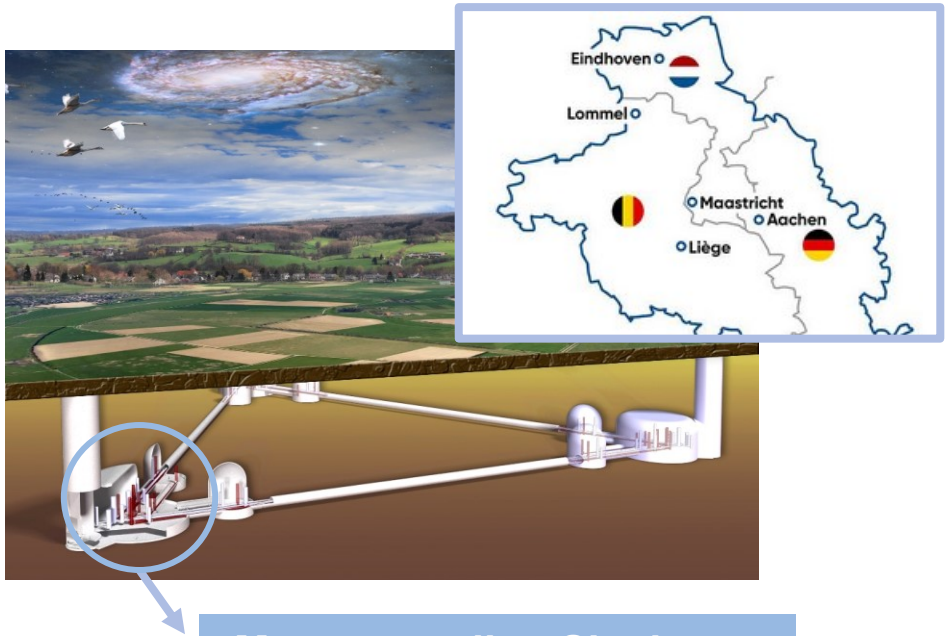
Biggest promises around liquid nitrogen temperature 77 K.

POTENTIAL BEYOND QUANTUM

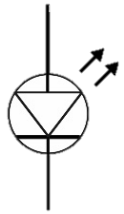
Einstein telescope

- Third-generation, gravitational-wave observatory
- 10km triangular interferometer at a depth of 200m

- Vibration free communication and power transfer
- High vacuum isolated cryogenic system to compensate thermal noise



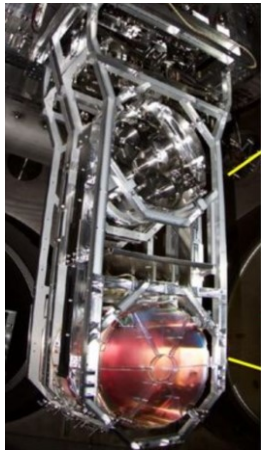
Monocrystaline Si mirrors



Laser will be used for power and data transmission

Fluorescence of the solar cell modulated to transmit data

Solar cells mounted inside the cryoshield



lowest power IC based system to operate the sensors and actuators

JÜLICH Forschungszentrum | ZEA-2 Electronic Systems


How can we transfer cryogenic CMOS to future experiments?
Utilize cryogenic CMOS performance gains.

REFERENCES

[1] J. W. Schrankler, J. S. T. Huang, R. S. L. Lutze, H. P. Vyas and G. D. Kirchner, "Cryogenic behavior of scaled CMOS devices," *1984 International Electron Devices Meeting*, San Francisco, CA, USA, 1984, pp. 598-600, doi: 10.1109/IEDM.1984.190792.

[2] G. Gildenblat, L. Colonna-Romano, D. Lau and D. E. Nelsen, "Investigation of cryogenic CMOS performance," *1985 International Electron Devices Meeting*, Washington, DC, USA, 1985, pp. 268-271, doi: 10.1109/IEDM.1985.190948.

[3] S. R. Ekanayake, T. Lehmann, A. S. Dzurak and R. G. Clark, "Quantum bit controller and observer circuits in SOS-CMOS technology for gigahertz low-temperature operation," *2007 7th IEEE Conference on Nanotechnology (IEEE NANO)*, Hong Kong, China, 2007, pp. 1283-1287, doi: 10.1109/NANO.2007.4601417.

[4] E. Charbon *et al*., "Cryo-CMOS for quantum computing," *2016 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2016, pp. 13.5.1-13.5.4, doi: 10.1109/IEDM.2016.7838410.

[5] Vandersypen, L.M.K., Bluhm, H., Clarke, J.S. *et al.* Interfacing spin qubits in quantum dots and donors—hot, dense, and coherent. *npj Quantum Inf* **3**, 34 (2017). https://doi.org/10.1038/s41534-017-0038-y

[6] A. Beckers, F. Jazaeri and C. Enz, "Theoretical Limit of Low Temperature Subthreshold Swing in Field-Effect Transistors," in *IEEE Electron Device Letters*, vol. 41, no. 2, pp. 276-279, Feb. 2020, doi: 10.1109/LED.2019.2963379.

[7] B. Cardoso Paz *et al*., "Performance and Low-Frequency Noise of 22-nm FDSOI Down to 4.2 K for Cryogenic Applications," in *IEEE Transactions on Electron Devices*, vol. 67, no. 11, pp. 4563-4567, Nov. 2020, doi: 10.1109/TED.2020.3021999.

[8] P. A. 'T Hart, M. Babaie, E. Charbon, A. Vladimirescu and F. Sebastiano, "Characterization and Modeling of Mismatch in Cryo-CMOS," in *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 263-273, 2020, doi: 10.1109/JEDS.2020.2976546.

[9] P. Vliex *et al*., "Bias Voltage DAC Operating at Cryogenic Temperatures for Solid-State Qubit Applications," in *IEEE Solid-State Circuits Letters*, vol. 3, pp. 218-221, 2020, doi: 10.1109/LSSC.2020.3011576.

[10] R. Otten, L. Schreckenberg, P. Vliex *et al*., "Qubit Bias using a CMOS DAC at mK Temperatures," *2022 29th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Glasgow, United Kingdom, 2022, pp. 1-4, doi: 10.1109/ICECS202256217.2022.9971043.

[11] A. A. Artanov *et al*., "Self-Heating Effect in a 65 nm MOSFET at Cryogenic Temperatures," in *IEEE Transactions on Electron Devices*, vol. 69, no. 3, pp. 900-904, March 2022, doi: 10.1109/TED.2021.3139563.