ECFA R&D electronics

DRDT 7.7 Technologies & Tools

15/3/2023 CERN

Conveners:

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Agenda

- Introducing the challenges of collaborative work at HEP 10’
  - *Kostas Kloukinas, CERN*
- Access to advanced silicon technologies for the HEP community via EUROPRACTICE 20’
  - *Paul Malisse, EUROPRACTICE IC service, IMEC IC-link, BE.*
- Access to modern EDA tools and IP block sharing in HEP community via EUROPRACTICE 20’
  - *Mark Willoughby, EUROPRACTICE design tools service, RAL, STFC, UK*
- Challenges in designing ASICs for HEP Experiments 20’
  - Adithya Pulli, CERN
- *Open Discussion* *20’*

ASIC Design Support for HEP

Foundry vendors

IP block vendors

3rd party Design Services

EDA tools

Manufacturing Services

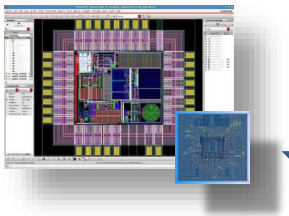
EUROPRACTICE IC SERVICE

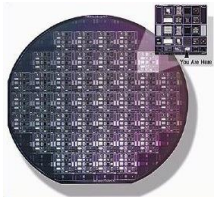
Science & Technology Facilities Council Rutherford Appleton Laboratory

CERN
common design platform
130nm, 65nm, 28nm
distribution & support

EUROPRACTICE IC SERVICE

imec
Lead Partner, MPW Service and Communications





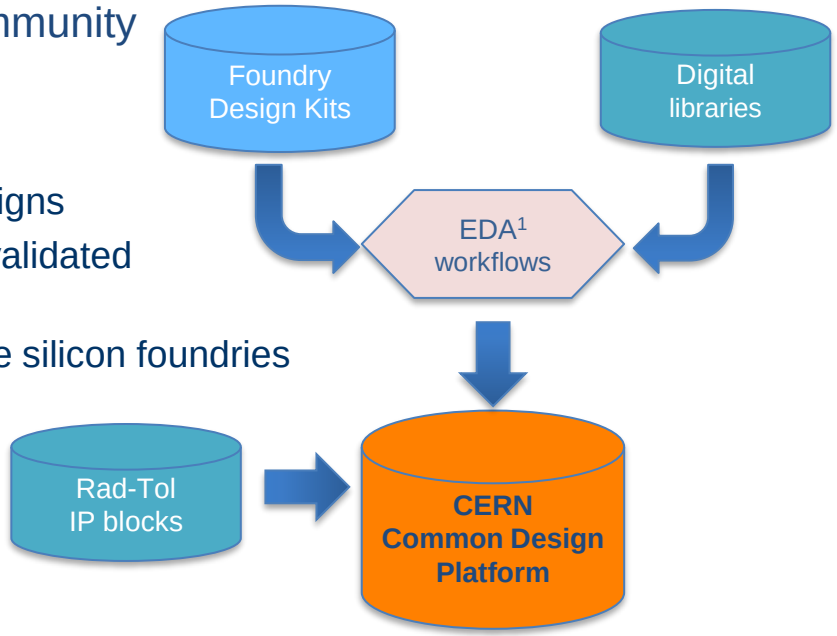
CERN & HEP design teams

asic.support@cern.ch

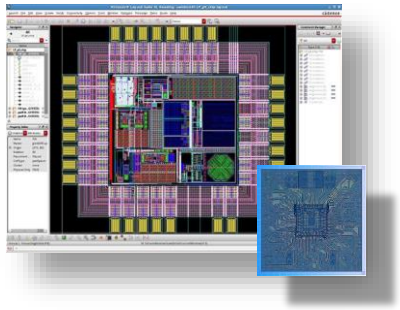
ASIC Design Platforms for HEP

- "Common ASIC design platforms" for HEP community

- Develop and Provide:
  - **Design kits** that support analog and digital designs
  - **Design Workflows** that are standardized and validated using selected EDA tools
  - **Compatible Design Workflows** across multiple silicon foundries
  - **Rad-Tol IP blocks**
  - Maintenance
  - Technical Support
  - Training

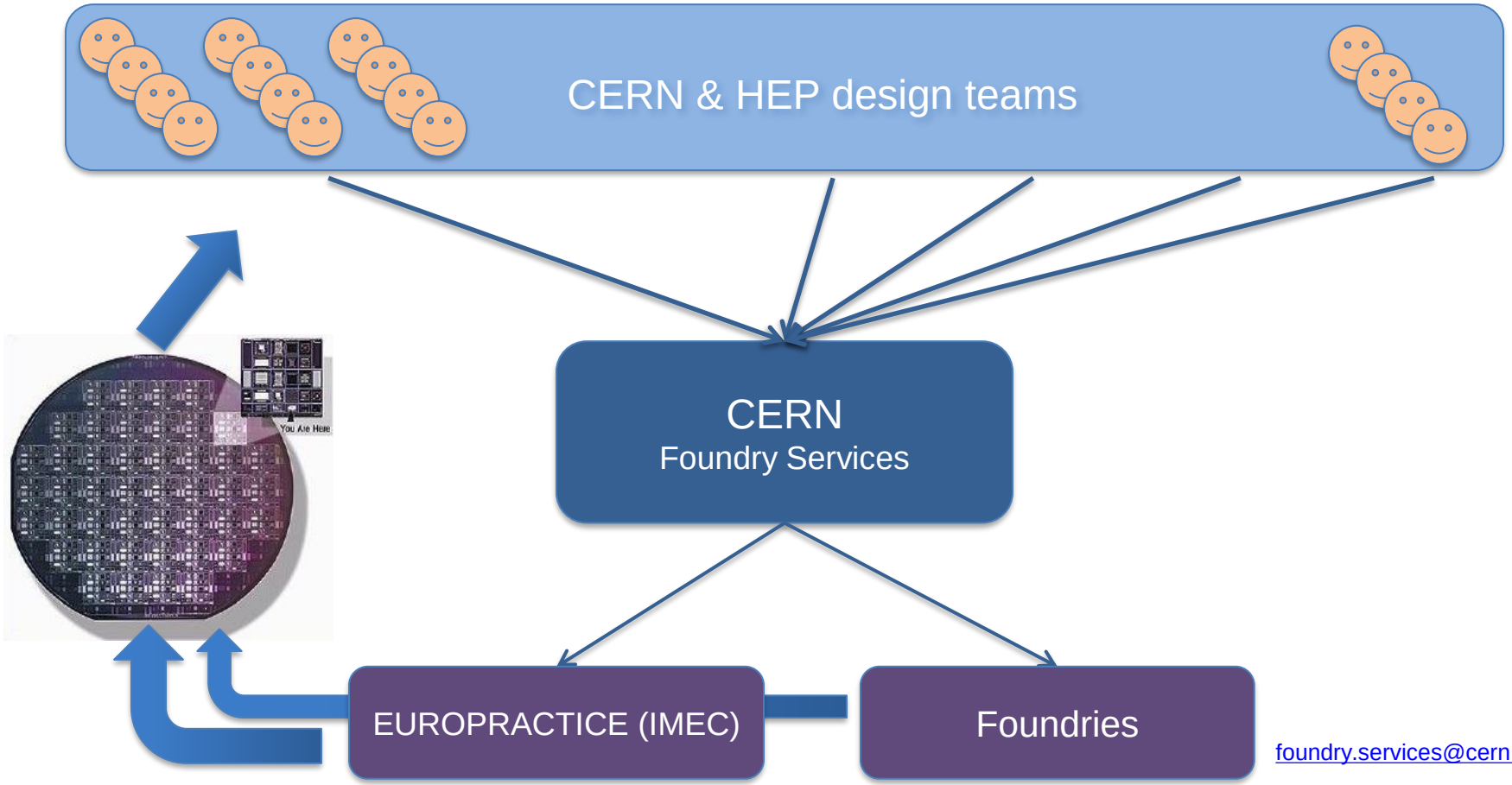


- Timeline
  - 1997 IBM 250nm
  - 2009 IBM 130nm
  - 2014 TSMC 65nm & 130nm
  - 2020 TSMC 28nm



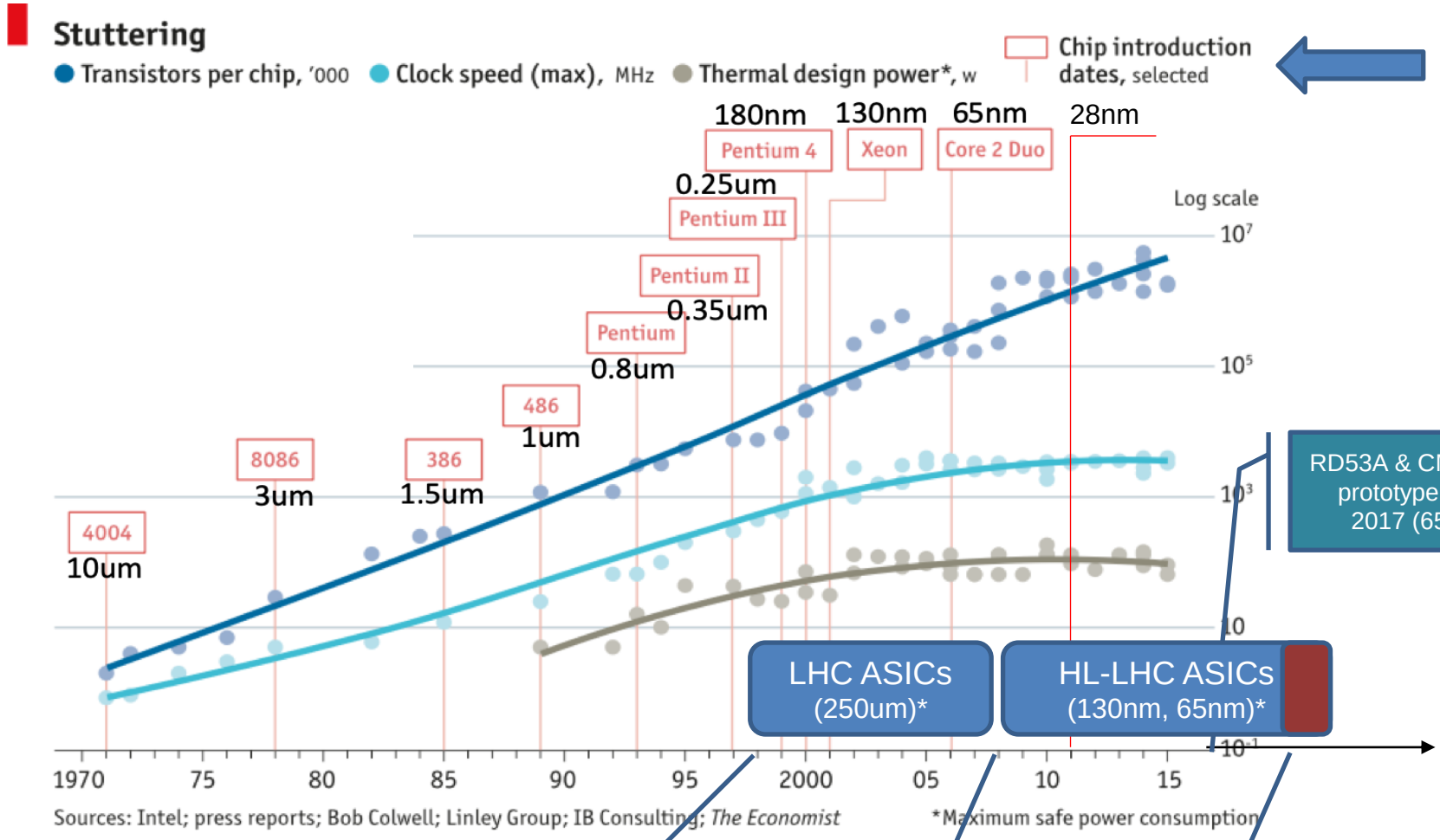
Foundry Access Services

- **Organize prototyping Multi Project Wafer runs, for sharing fabrication costs**
- **Coordinate Engineering & Production runs**



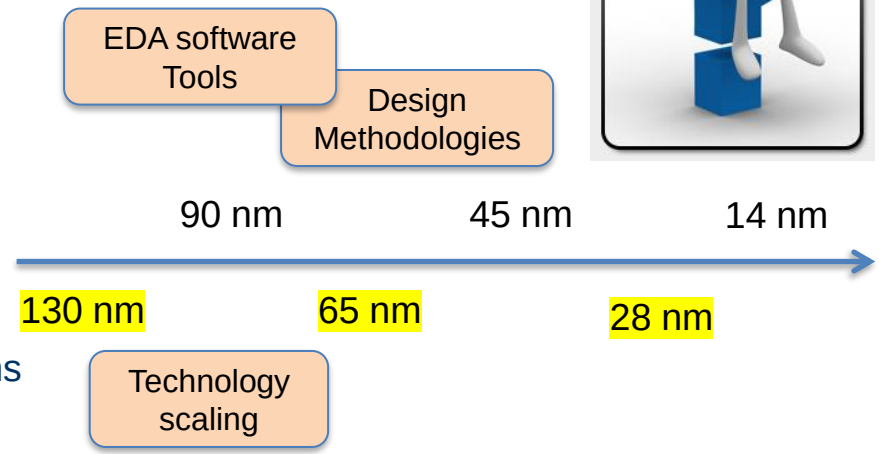
foundry.services@cern.ch

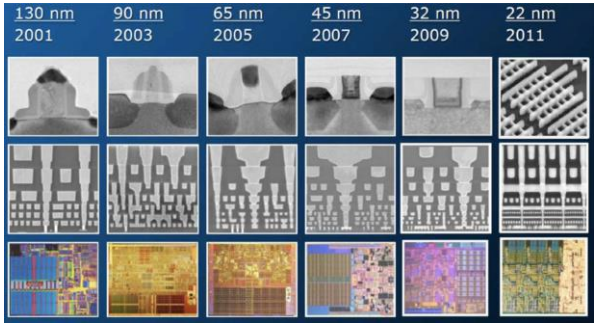
Technology evolution and HEP



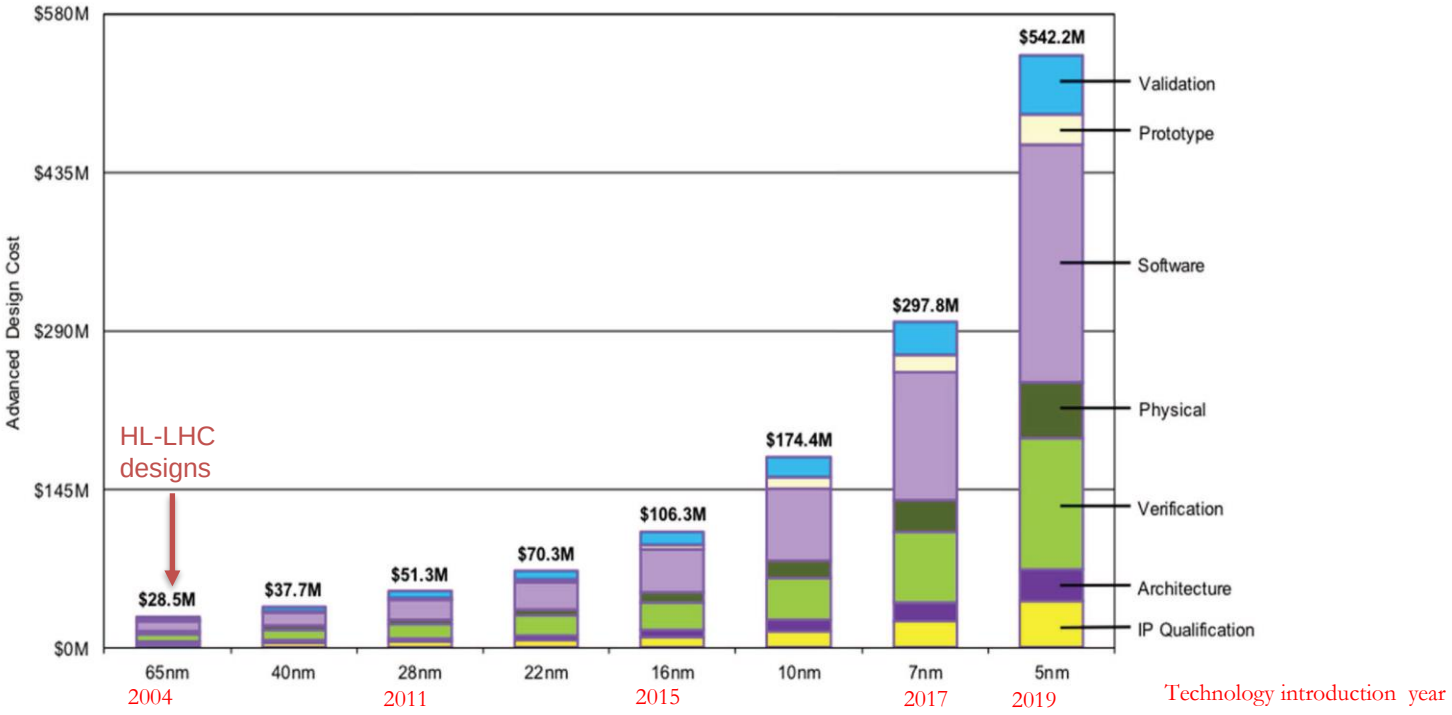
Challenges in ASIC design @ HEP

- Technology Challenges
  - Complex deep-submicron silicon manufacturing processes
  - Powerful, Flexible but highly Complex EDA Tools
- Design Challenges
  - Designs of increasing complexity and size
  - Novel designs for scientific instrumentation
  - Radiation Tolerance
- Productivity Requirements
  - Large, fragmented, multinational design teams
  - Designers with different levels of expertise
  - Work on common design projects
  - Costly technologies
  - Importance of 'first-time-right' designs !





ASIC development costs



Chip Design and Manufacturing Cost under Different Process Nodes: Data Source from IBS*

- Steep investment for node sizes <16nm. But combine strong performance with lower power consumption
- Design verification skills and effort are increasingly more important
- Cost per transistor continues to fall even at 5nm, but this is relegated to those who have large wafer volume

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Thank You

Addressing the Challenges

- Technology Challenges
  - Augment EDA Tools -> EUROPRACTICE
  - Access to Advanced technologies -> EUROPRACTICE
  - Integrate support for "More than Moore" technologies
    - 3D Interconnect & Advanced Packaging
    - SiPh
    - CMOS Imaging (monolithic sencors)
    - Specialty embedded devices
- Design Challenges
  - System Architect role
  - System Level Modeling and Simulations
  - Design Verification at System Level and component level
  - Establish & Conform to a Rad-Tol SoC infrastructure
- Productivity Requirements
  - Establish a Collaborative Work structure

Enablers for Collaborative Work

- Technical Framework
  - Comprehensive “common design platforms”
    - Foundry PDKs & Foundry IP blocks
    - Rad-Tol IP blocks and IP block repository
    - Rad-Tol SoC infrastructure
    - Design & Verification methodologies
  - Access to common EDA tools
  - Maintenance, Training & Support services

- Legal Framework
  - 3-way NDAs with Foundries permitting technology data exchange
  - Commercial Contracts with Foundries
  - EULAs of EDA tool providers permitting IP block sharing
  - IP block sharing agreements among design teams
  - Export Control regulations