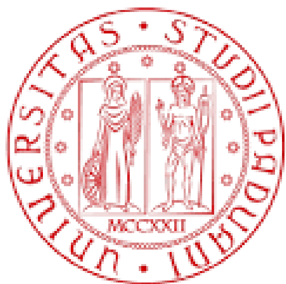
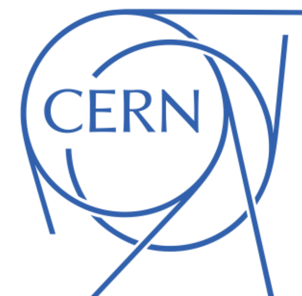
800 1222 · 2022 ANNI



Università degli Studi di Padova



DRDT7.4
TID and Challenges at Ultra-High Doses in Modern CMOS Technologies

Stefano Bonaldo

Department of Information Engineering, University of Padova, Italy

stefano.bonaldo@dei.unipd.it

RREACT lab - Reliability and Radiation Effects on Advanced CMOS Technologies

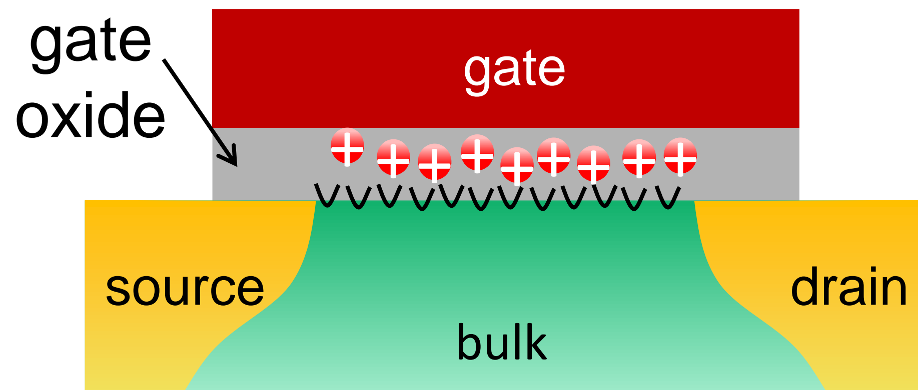
March 15th, 2022

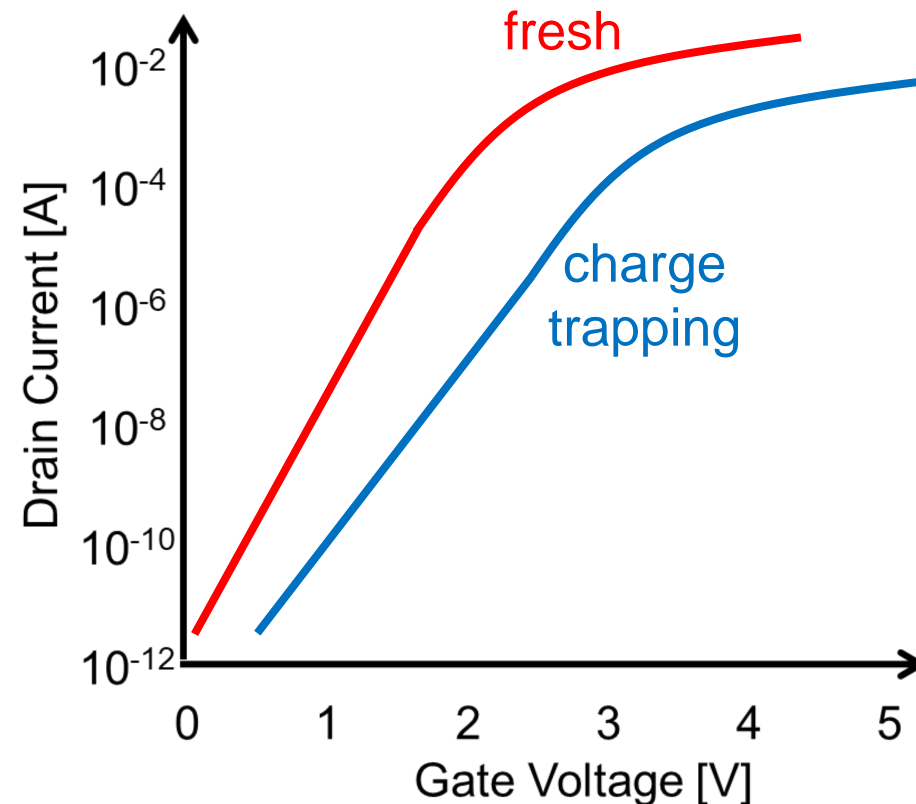
Outline

- **Evolution of TID effects in single transistors**
  I. 28 nm Si MOSFETs
  II. 16 nm Si FinFETs
  III. 16 nm InGaAs FinFETs
  IV. Gate-All-Around nano-wire Si FETs
- **Power devices: GaN HEMTs and SiC VMOSFETs**
- **Conclusions and future challenges**

Total Ionizing Dose in FETs

- TID is a **cumulative effect** affecting the **dielectric layers of transistors,** e.g. gate oxide
- Ionizing radiations may induce **build-up of trapped charge** in the dielectrics
- Trapped charge causes **parametric shifts** in electrical responses of FETs

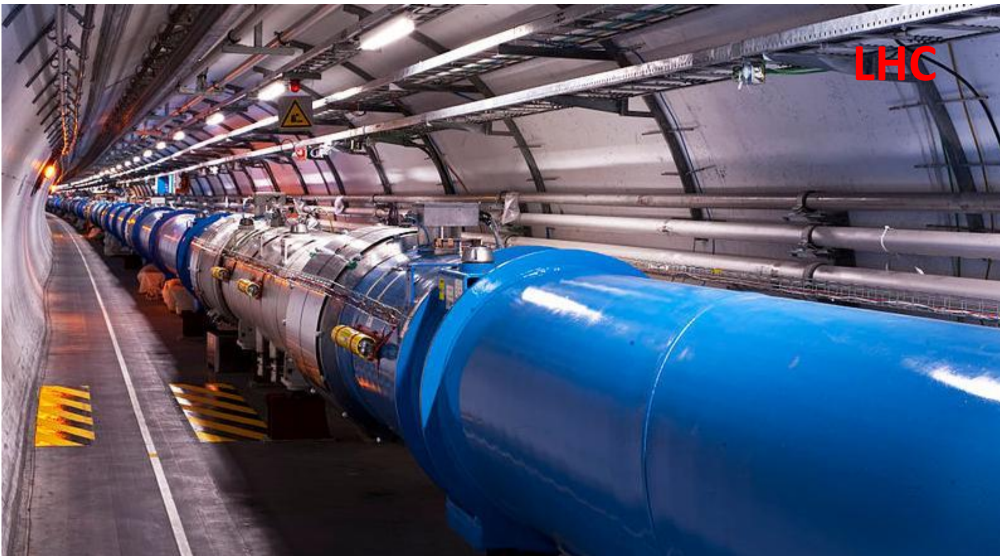




TID on electronics: new challenges

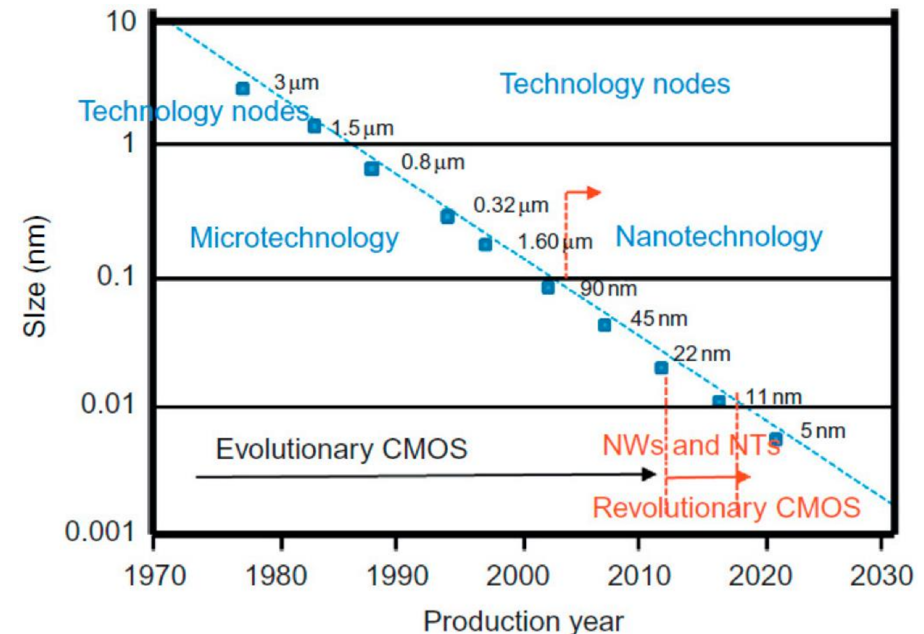
ULTRA-HIGH RADIATION LEVELS

- **Next generation particle accelerators**
- Increase of the total cumulative dose: >**1 Grad**



SCALING DOWN OF TECHNOLOGY NODES

- **High-k dielectrics**
- **New layouts**
- **New semiconductor materials**
- **Nano-scale dimensions**



Dielectrics in CMOS technologies

Several dielectrics:

1) High-k gate oxide

2) Shallow trench Isolation (STI)

Very thick low quality SiO_2 layer

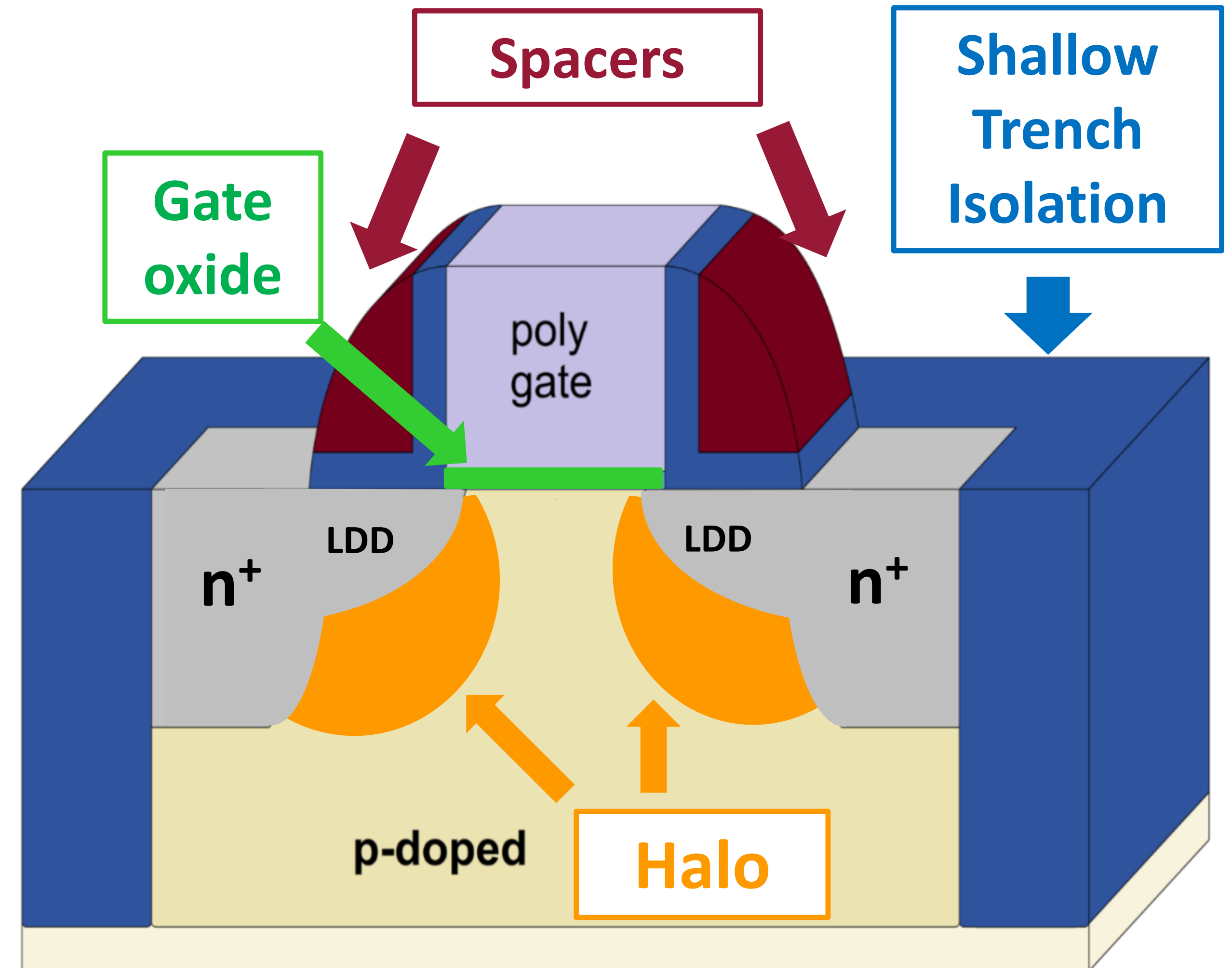
3) Spacers

Thick layer of SiO_2 and a layer of Si_3N_4 for LDD extensions

New fab processes:

4) Halo implantations

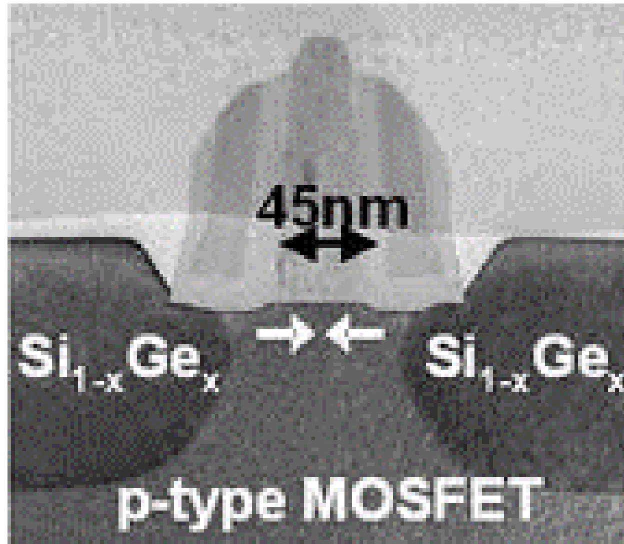
Highly doped region around S/D wells to reduce short-channel effects



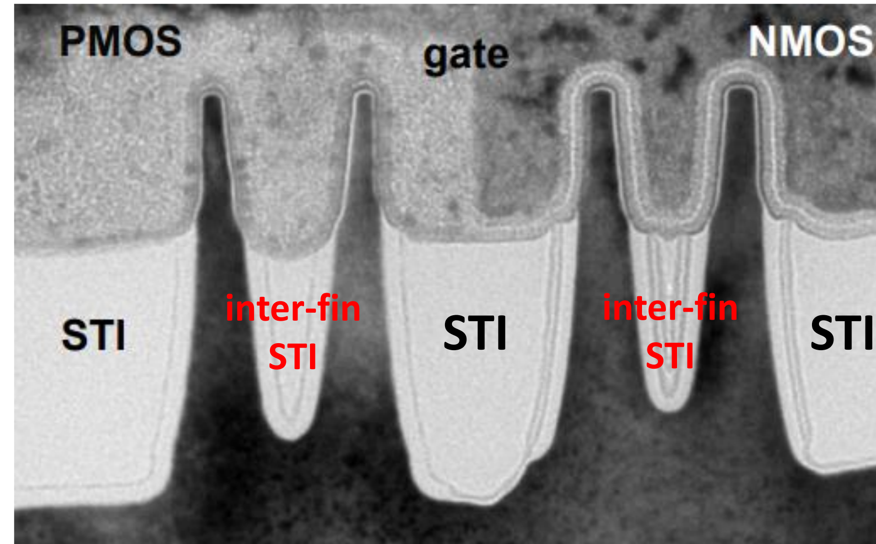
Goals

1) **Qualification of electronics** under ionizing radiation up to ultra-high doses
2) Exploring **TID effects in different modern FET technologies**
3) Correlate the macroscopic effects with the **TID microscopic mechanisms**
4) Proposing **mitigation techniques** at layout level

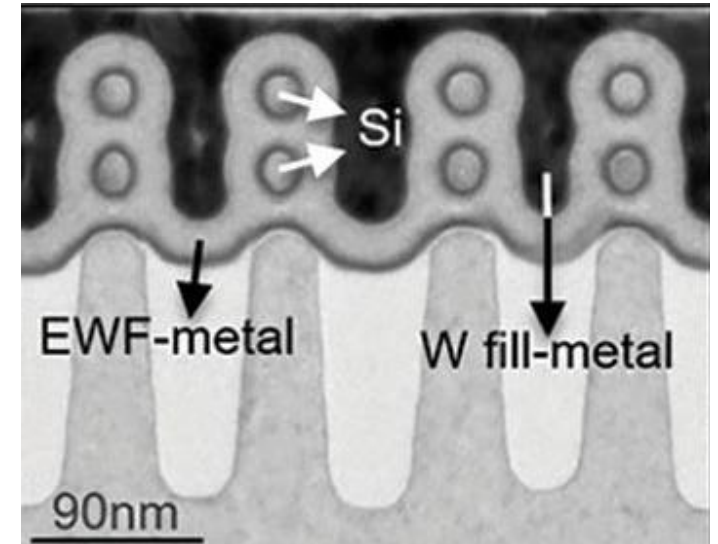
Planar FET



FinFET



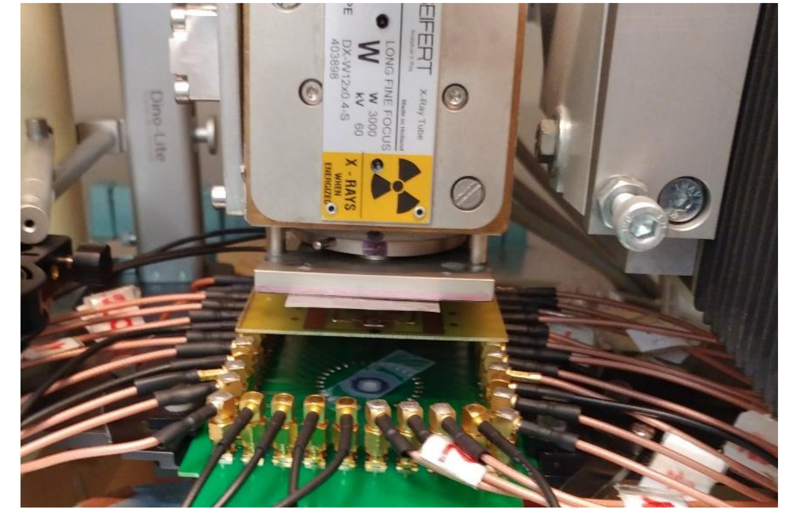
GAAFET



Test methodologies for single transistors

1. Expose the devices to ionizing radiation

- X-rays, gamma rays, protons, or other energetic particles
- X-rays up to 1 Grad: >1 week of irradiation
- Test with different transistor dimensions
- Choice of irradiation conditions (e.g., device bias, temperature)

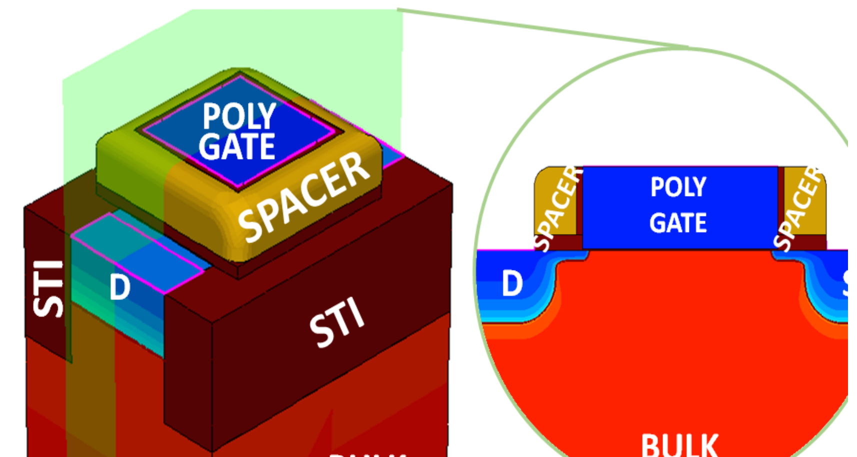


2. Experimentally characterize the electrical responses of devices after exposures

- DC measurements → evaluation of the TID sensitivity of devices
- Charge pumping → energy and space distributions of traps
- Low frequency noise → microscopic nature of defects

3. TCAD simulations and modelling

- Support tool for understanding trap location and energies
- Model the TID degradation



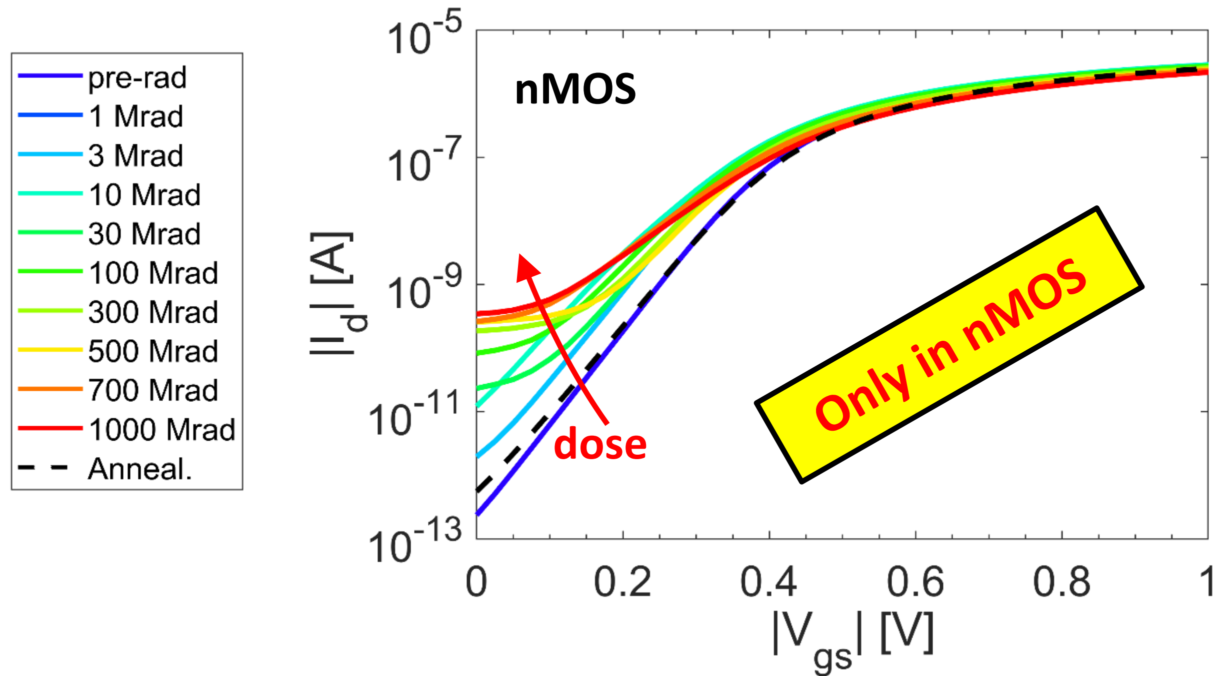
4. Find radiation hardening solutions

- Identification of the most critical parameters
- Propose changes in transistor design, fabrication processes, and trace guidelines for IC designers

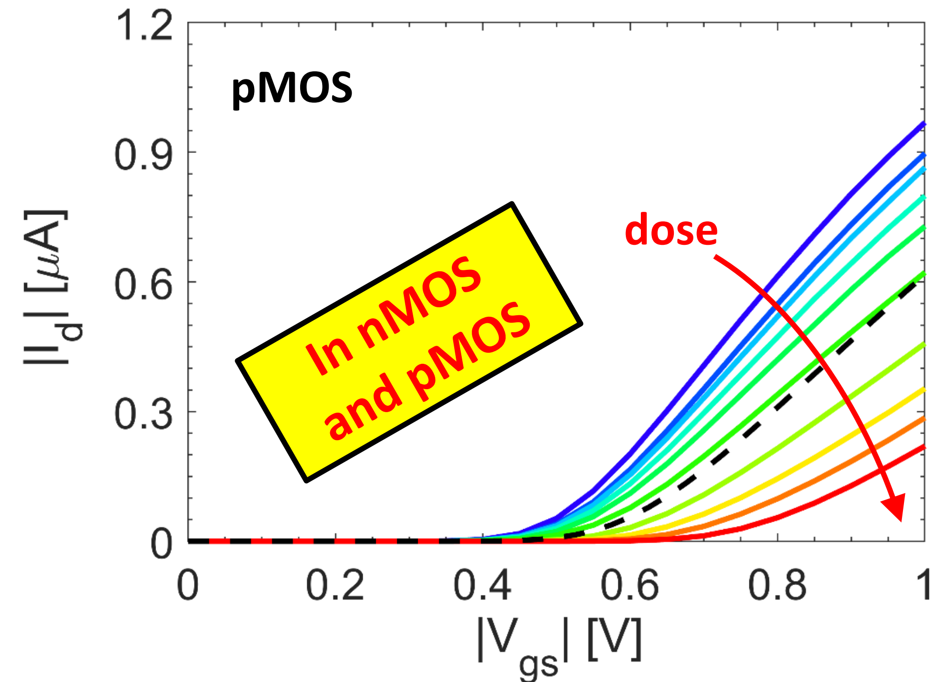
Now: 28 nm Si MOSFETs

➢ At ultra-high doses, two dominating TID effects related to **charge trapping in STI oxides**:

1) Increase of OFF-leakage current



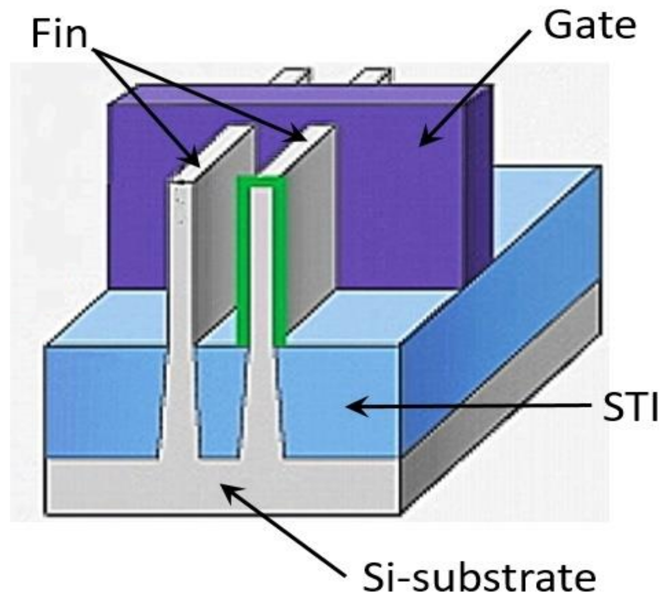
2) Loss of trasconductance (RINCE)



F. Faccio, et al., IEEE Trans. Nucl. Sci., 62(6), 2015; S. Bonaldo, et al. IEEE Trans. Nucl. Sci., 67(7), 2020

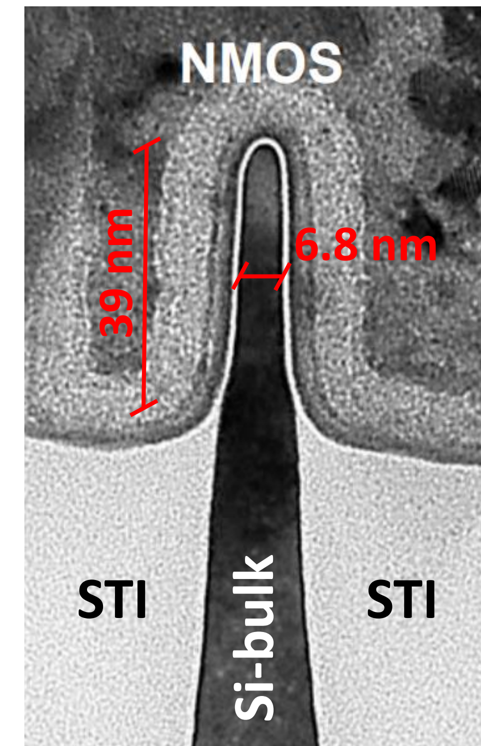
Next generation: FinFET technology

- Better gate control over the channel
- Faster switching speed
- More drive-current per footprint
- Lower switching voltage
- **No ELT solution**

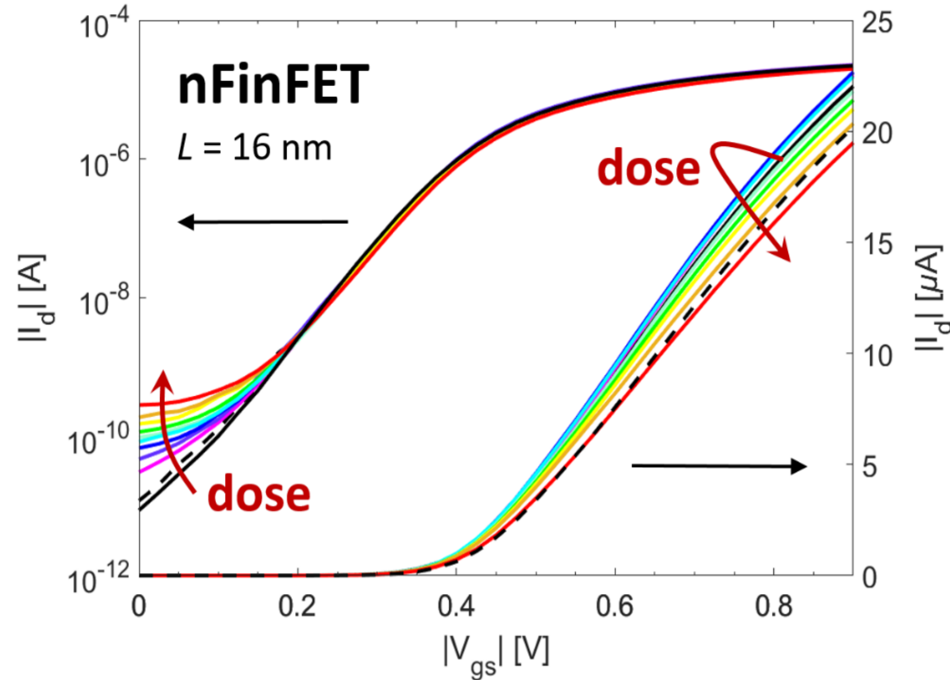


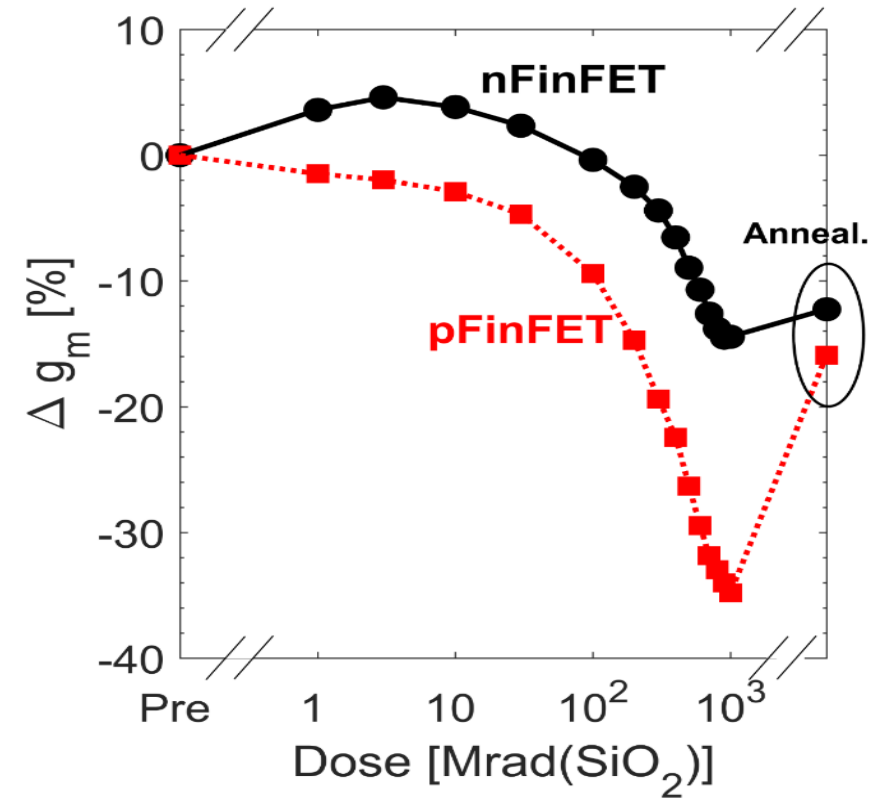
➢ Results on 16 nm bulk Si FinFET

- Manufacturer: **TSMC**
- **Tested up to 1 Grad**
- **Shallow trench Isolation (STI)**
- Designed in different combination fin/finger



TID in 16 nm Si FinFETs





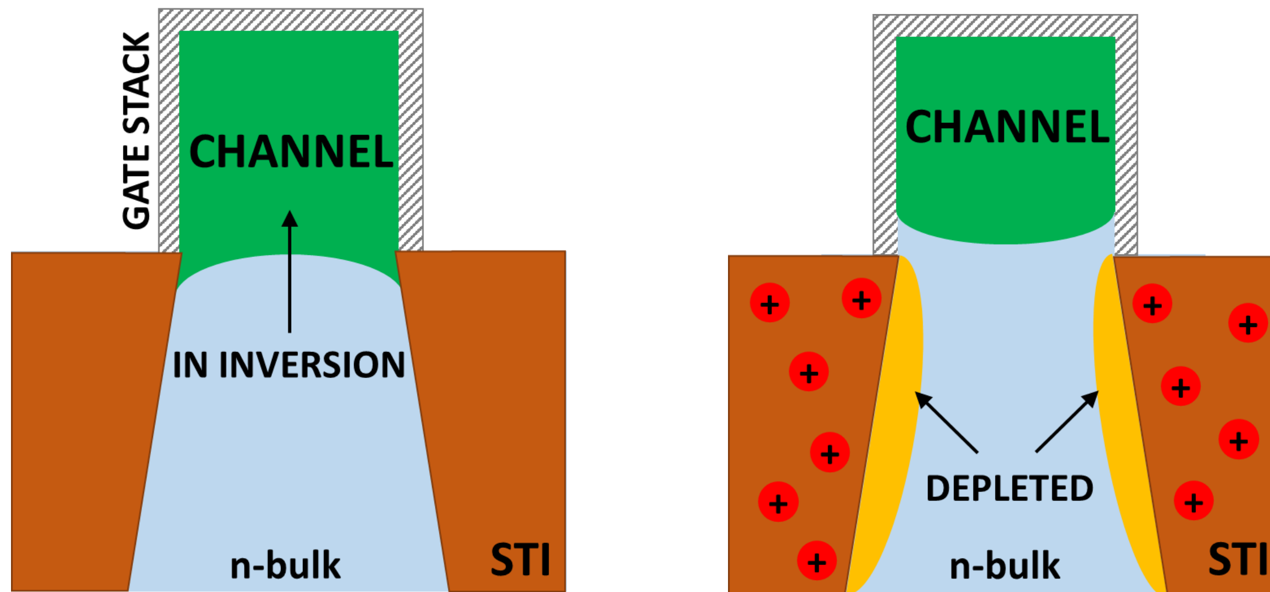
- **Modest increase of OFF-leakage current**

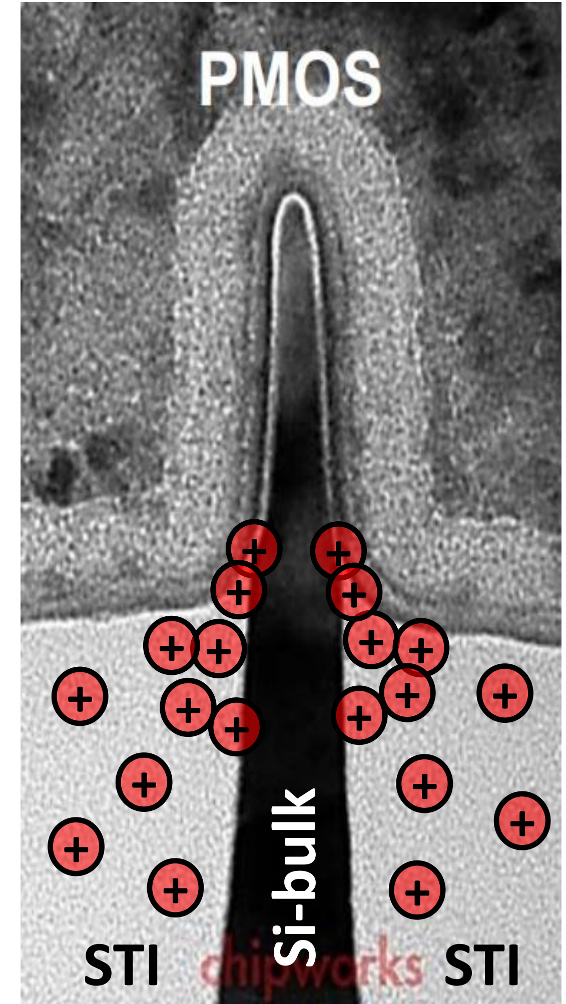
- Worst degradation in **p-channel FETs**
- Large decrease of **transconductance**

RADECS 2020 Best Student Abstracts Award: T. Ma+, S. Bonaldo+ et al., IEEE Trans. Nucl. Sci., 68(8), 2021.

16 nm Si FinFETs – the mechanisms

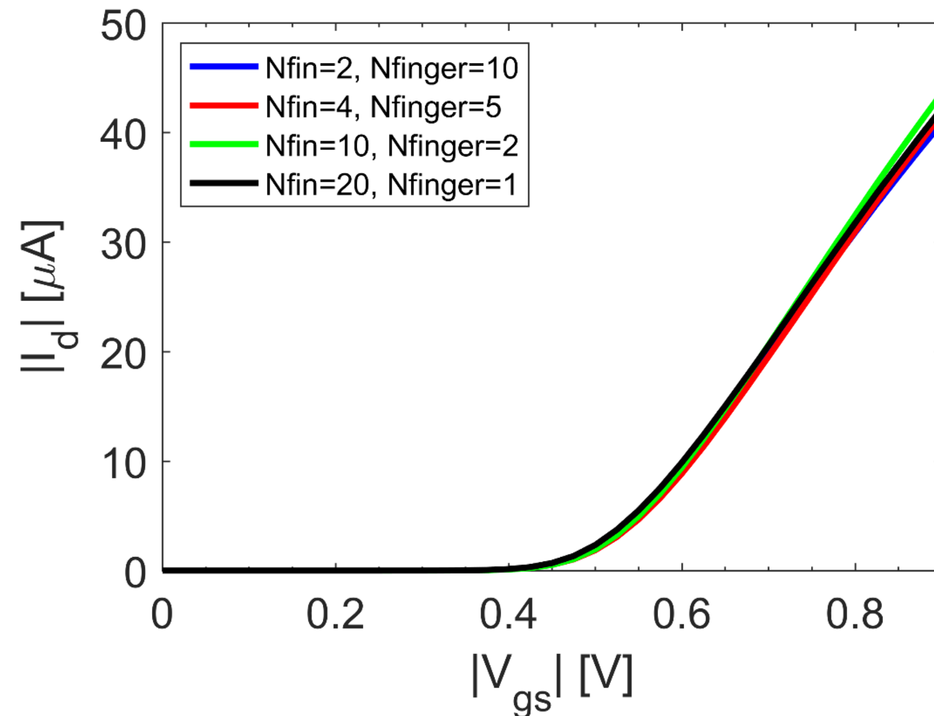
- **Similar to previous planar technologies -> STI-related effects**
- During irradiation, **hole trapping in STI** invert the lateral regions of the channel, reducing the effective channel height

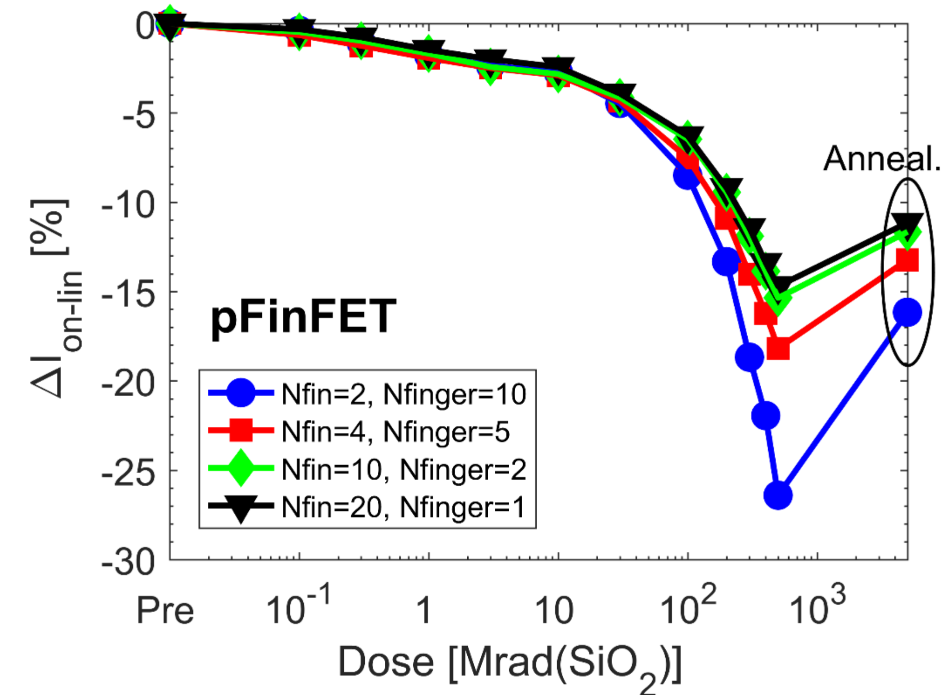




T. Ma, et al., IEEE Trans. Nucl. Sci., 68(8), Aug. 2021
S. Bonaldo et al., Nucl. Instrum. Methods Phys. Res. A, 1033(166727), 2022

16 nm FinFETs - Influence of fin and finger number





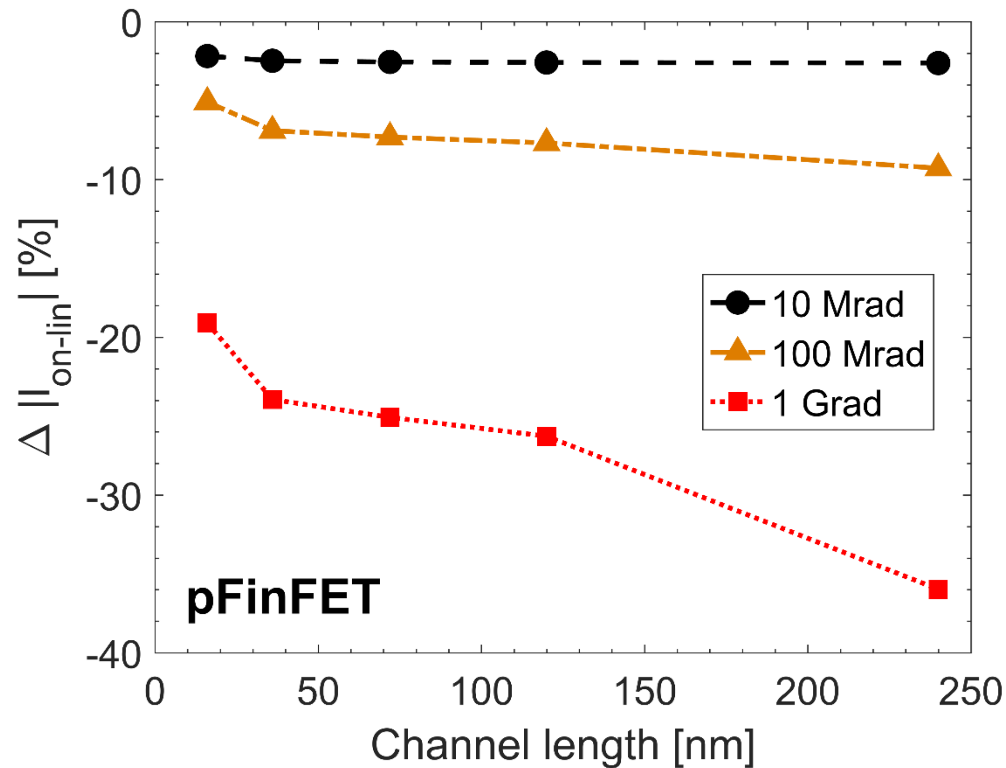
- pFinFETs with constant multiplication (20) of fins by fingers show very **similar DC performances**

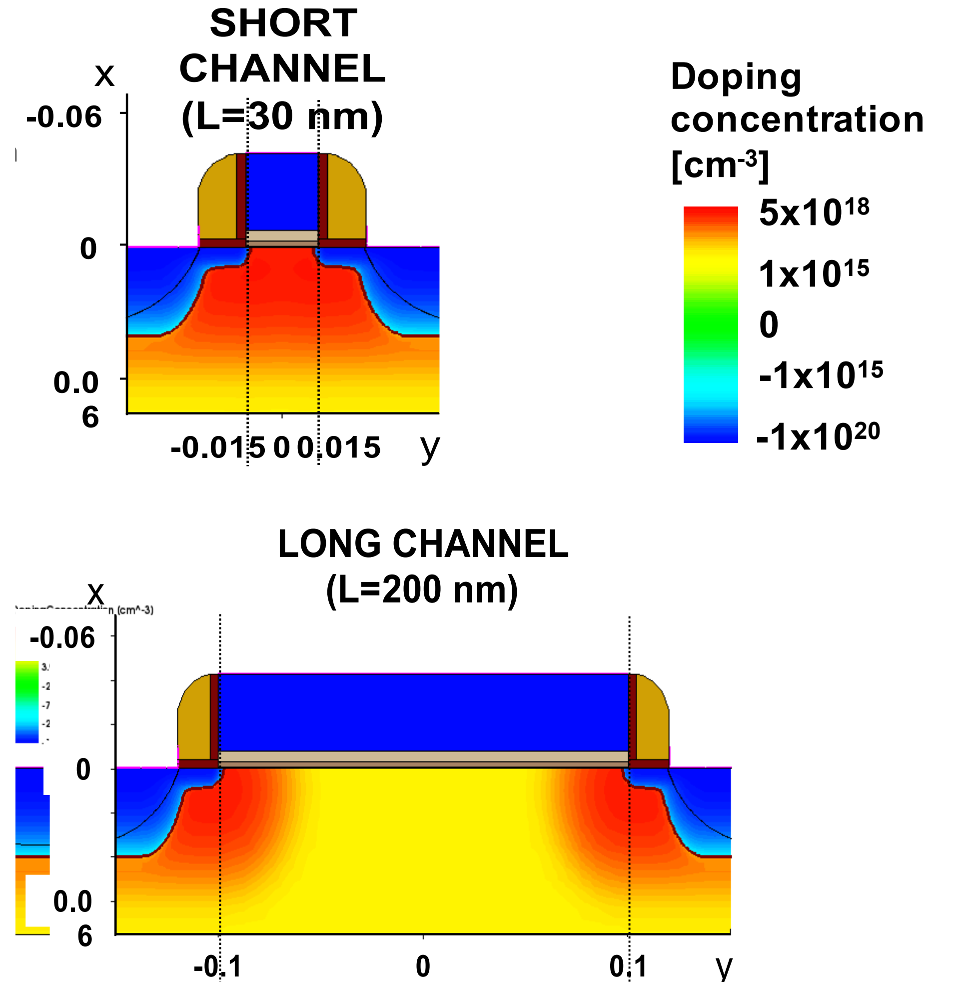
- **Highest tolerance** of transistors with the highest number of fins
- **Guidelines for IC designer** to enhance the TID tolerance

T. Ma, et al., IEEE Trans. Nucl. Sci., 68(8), Aug. 2021
S. Bonaldo et al., Nucl. Instrum. Methods Phys. Res. A, 1033(166727), 2022

Best tolerance for short transistors

- Good news: **short channel devices has the best TID tolerance**
  - The channel length dependence is due to **halo implantations**

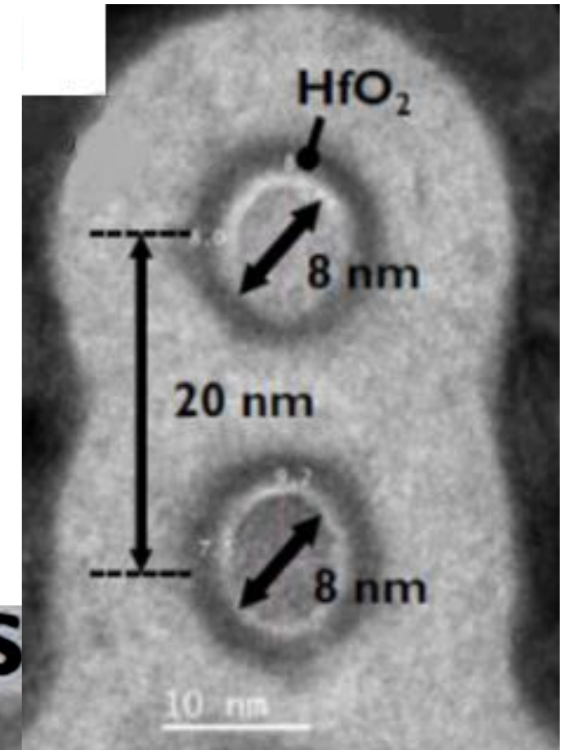


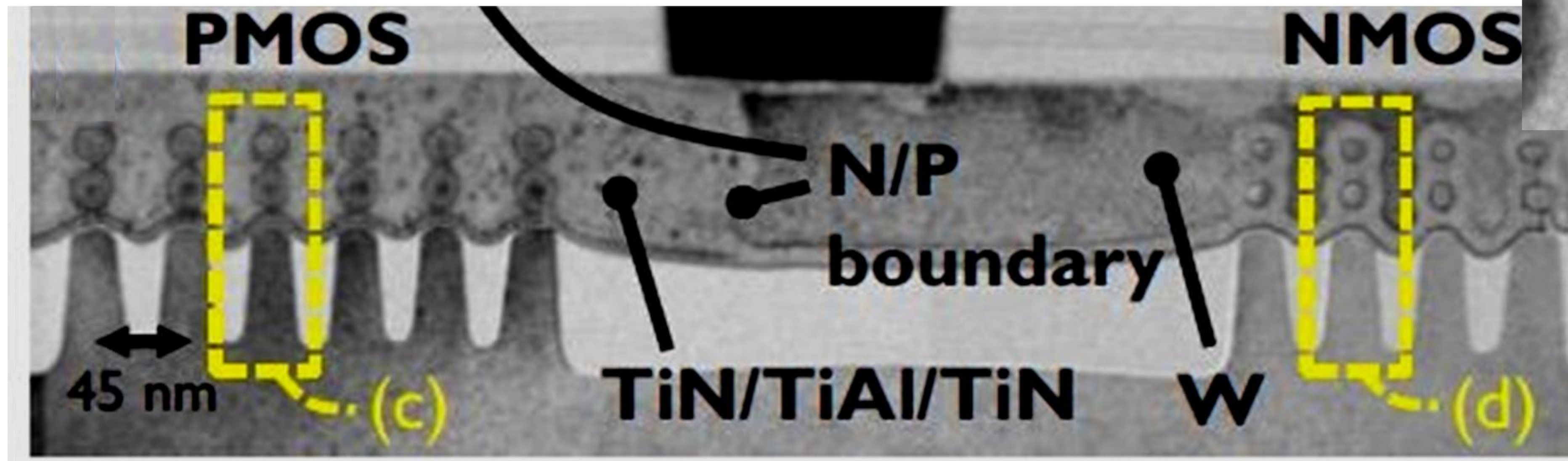


T. Ma, et al., IEEE Trans. Nucl. Sci., 68(8), Aug. 2021
S. Bonaldo et al., Nucl. Instrum. Methods Phys. Res. A, 1033(166727), 2022

Gate-All-Around Si nano-wire FETs (Imec)

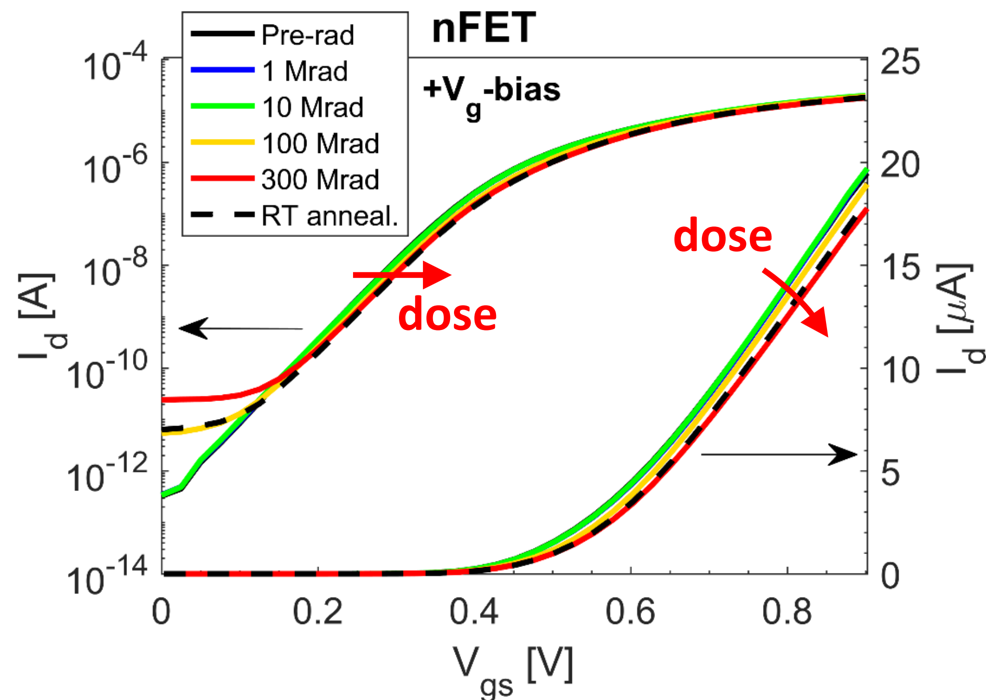
- At the **frontier of the technologies**
- Each fin contains two vertically stacked horizontal Si NWs
- **Diameter of 8 nm** and channel length **L=30 nm**
- The gate stack: **1.8 nm HfO_2** + **<1 nm SiO_2**

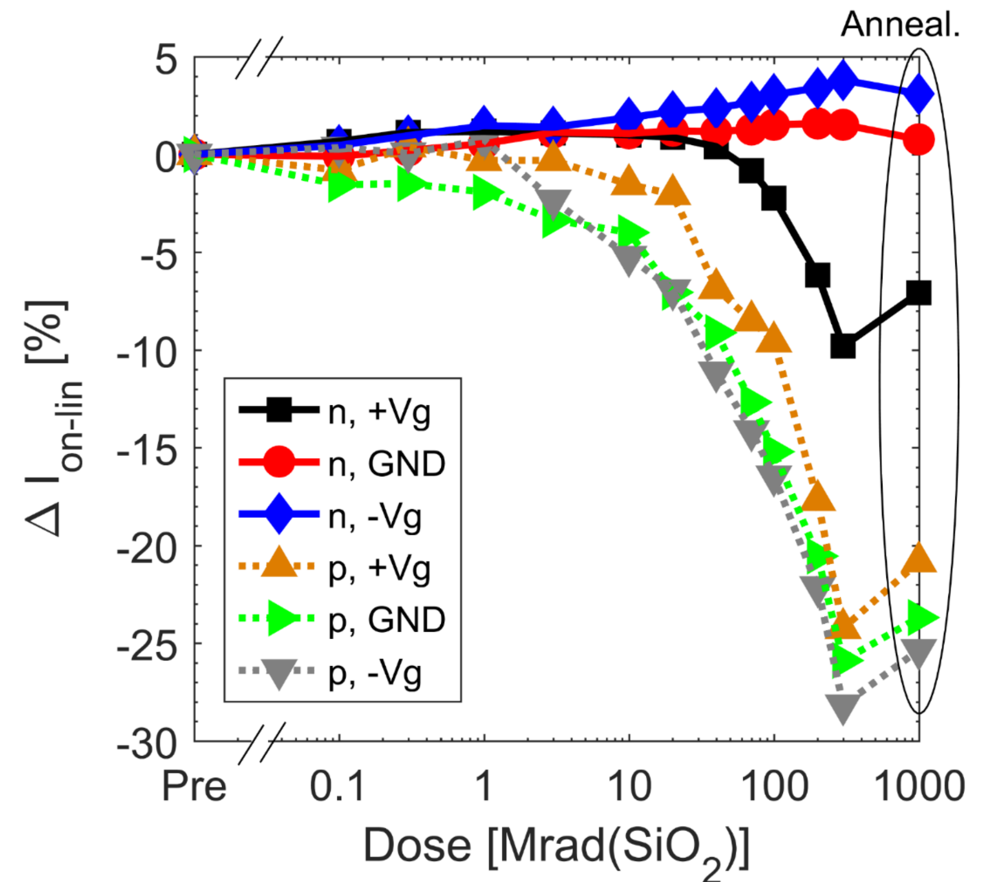




TID response of GAA FETs

- **Modest** TID effects in nFETs
- Strongly influenced by **gate bias condition**
- **More research** is required to elucidate the dominating mechanism

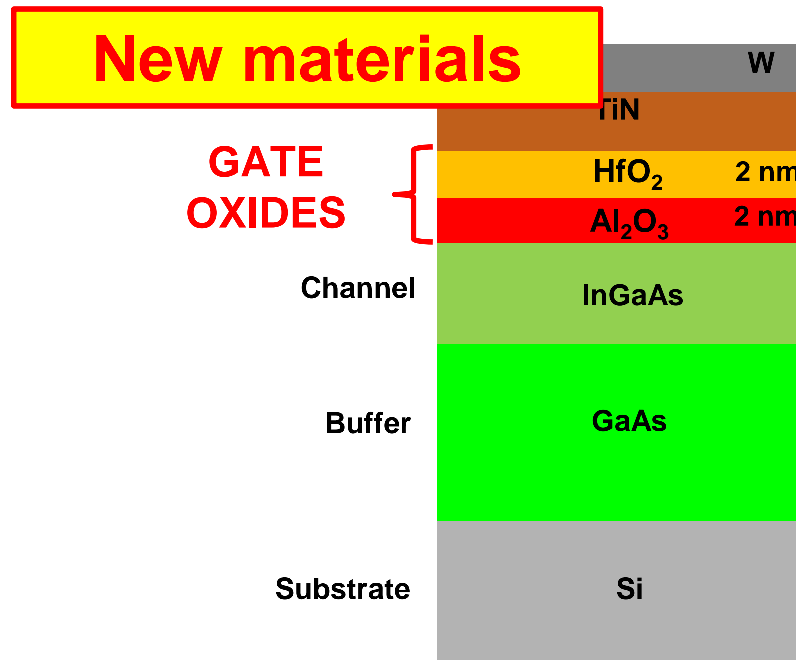


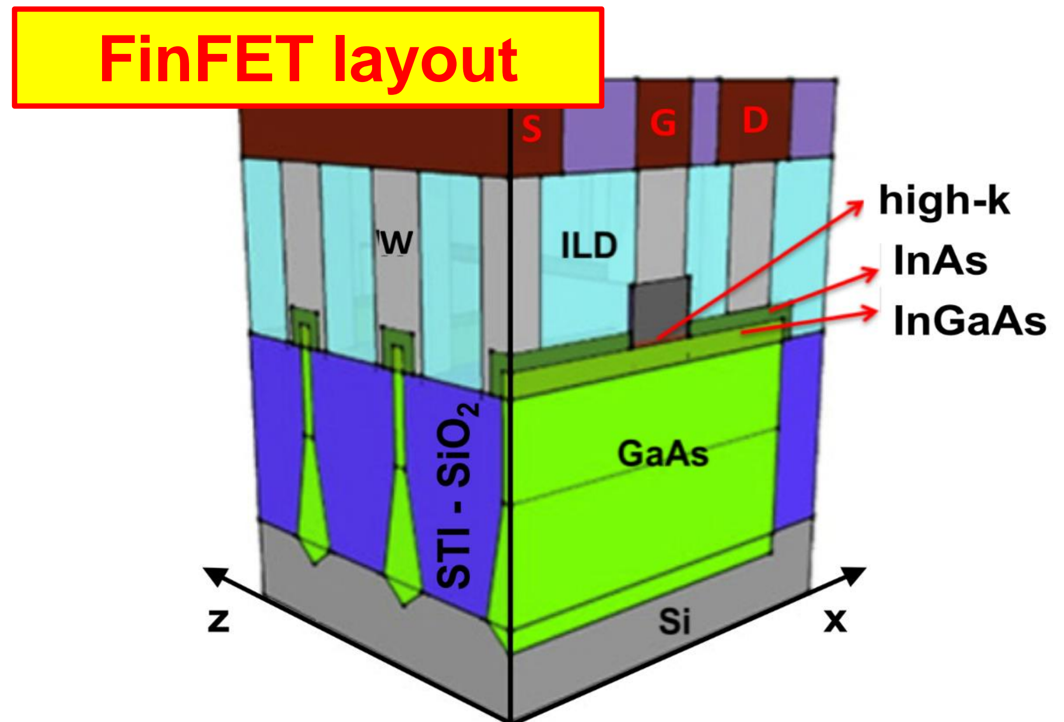


S. Bonaldo et al., IEEE Trans. Nucl. Sci., 69(7), 2022

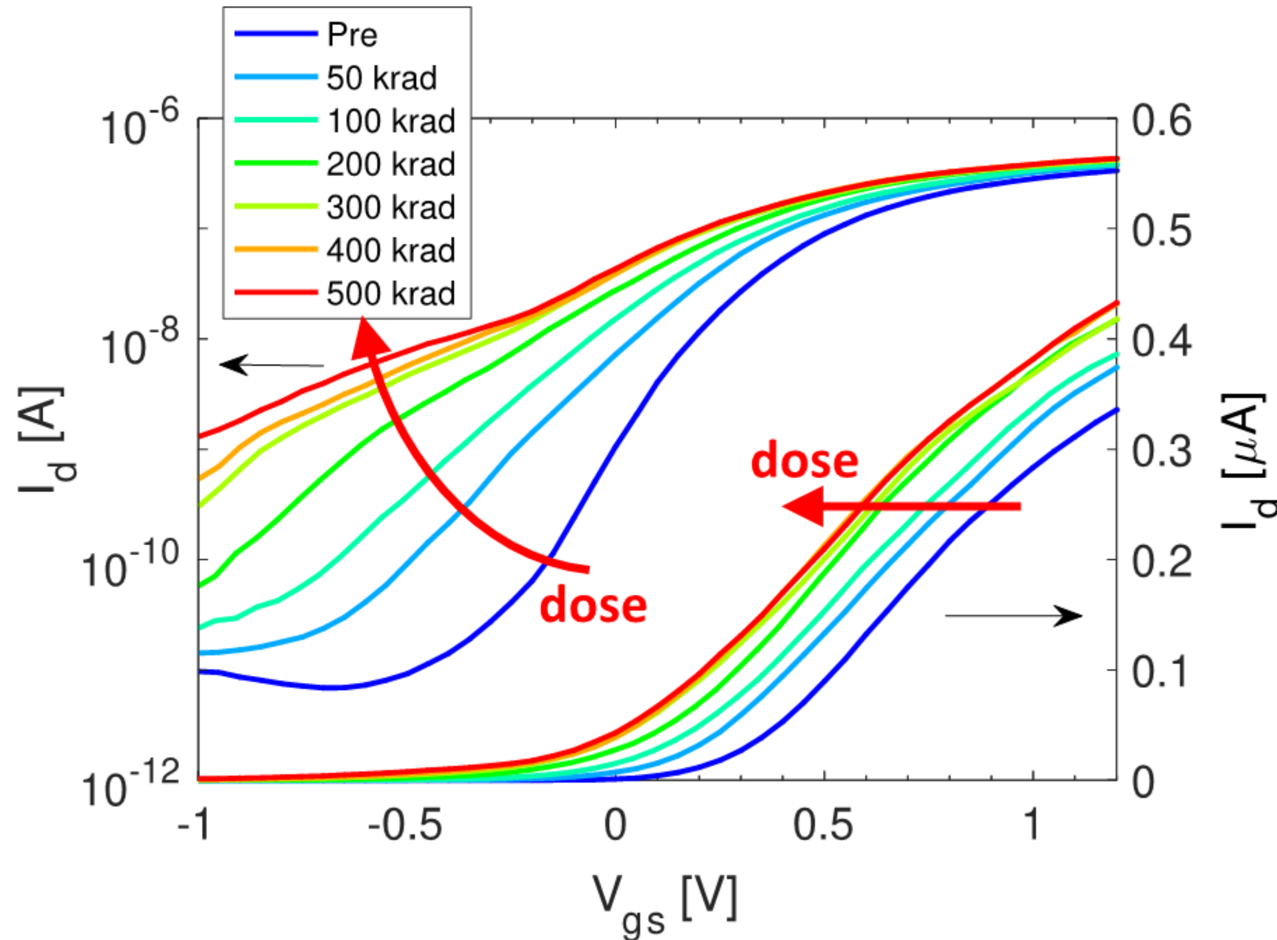
Alternative channel materials?

- Scaling limits of Si transistors → introduction of **new channel materials**
- We started exploring the TID in **16 nm InGaAs FinFETs** (only nFETs, pFETs in Ge)
  - High density of defects at the semiconductor/oxide interface





16 nm InGaAs FinFETs – TID response



I_d shifts to the left

+

Subthreshold slope increases

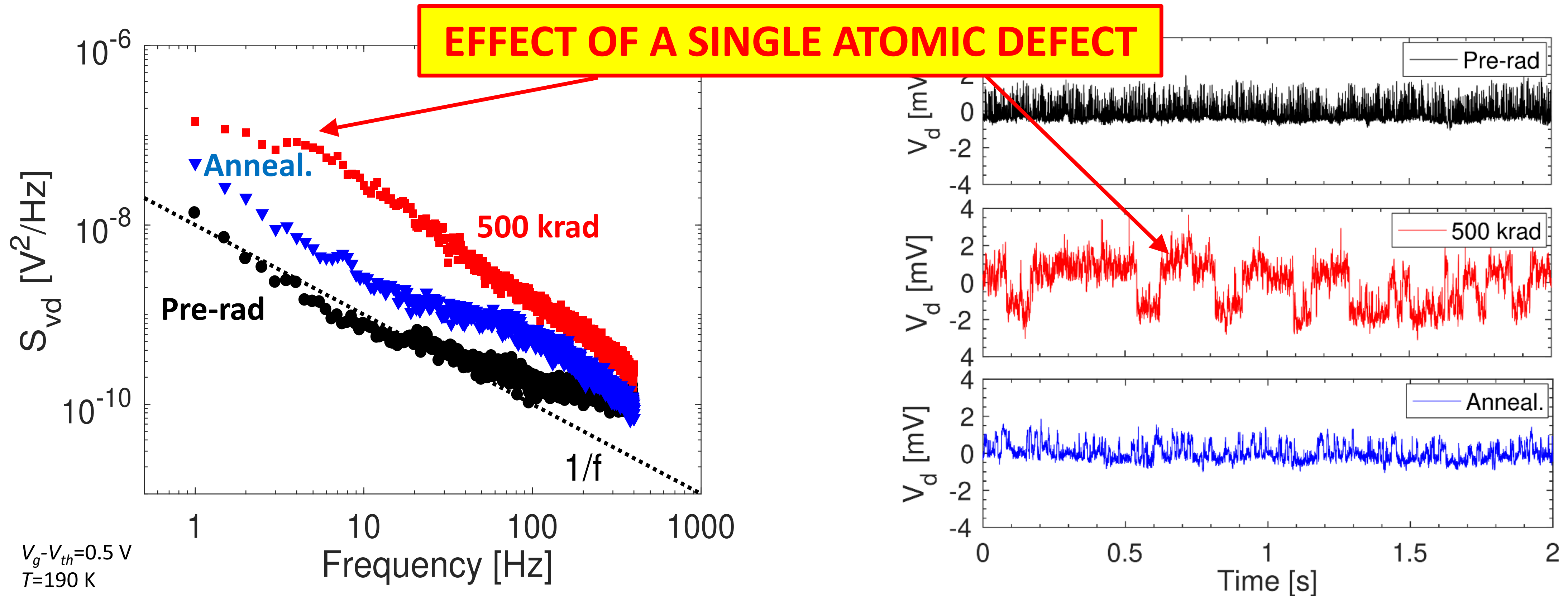
+

High noise level

High density of charge trapped in the **GATE OXIDE**

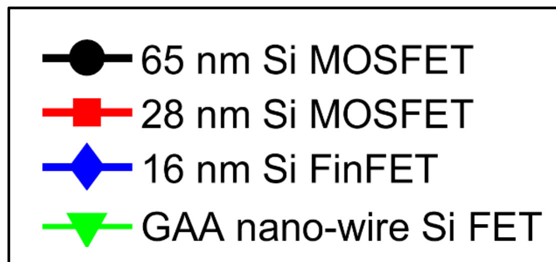
FinFETs – Effects of atomic defects

- **Low-frequency noise spectral density increases** during irradiation
  - Activation of **border traps in the gate oxides**
  - Random Telegraph Noise (RTN): electrons are trapped/detrapped in/from defect sites of the gate oxides

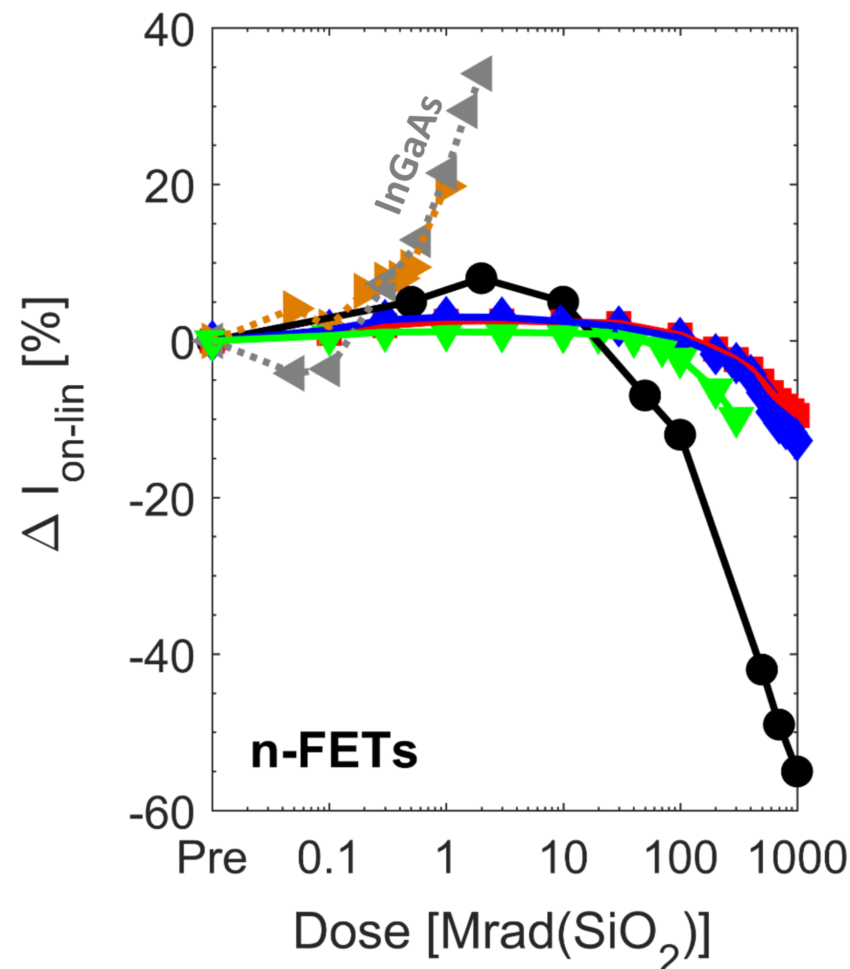


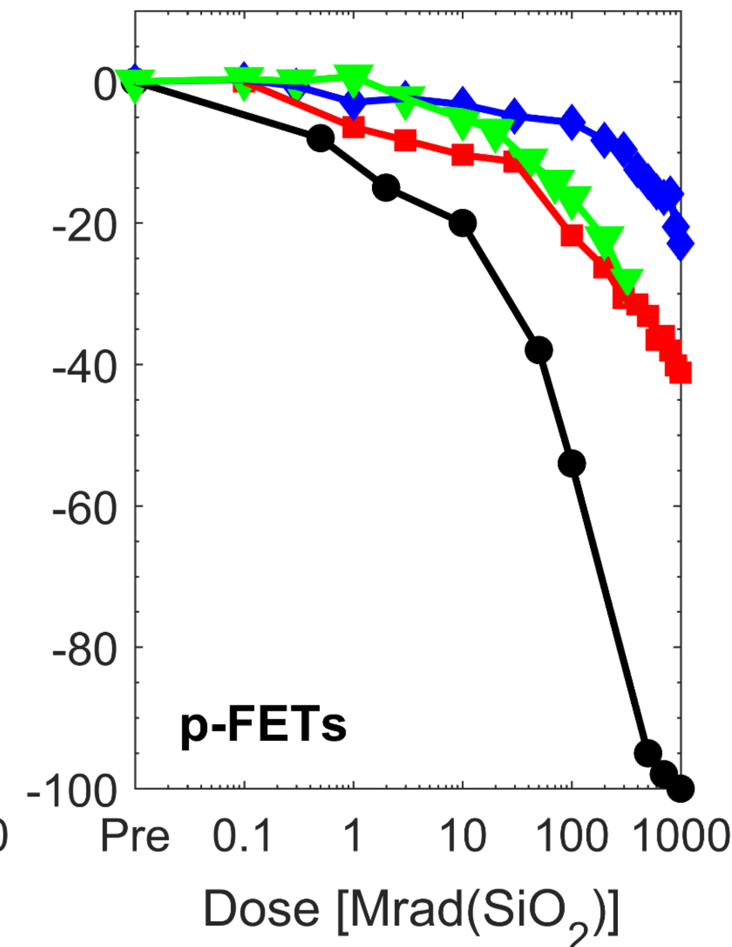
V_g-V_{th}=0.5 V
T=190 K

TID at ultra-high doses - the state of the art



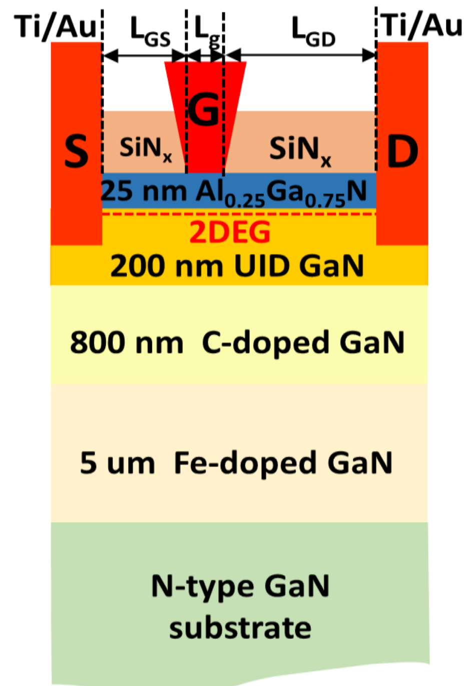
- **16 nm Si FinFETs** have the best TID tolerance
- In general, **pMOS** have the **worst TID tolerance**

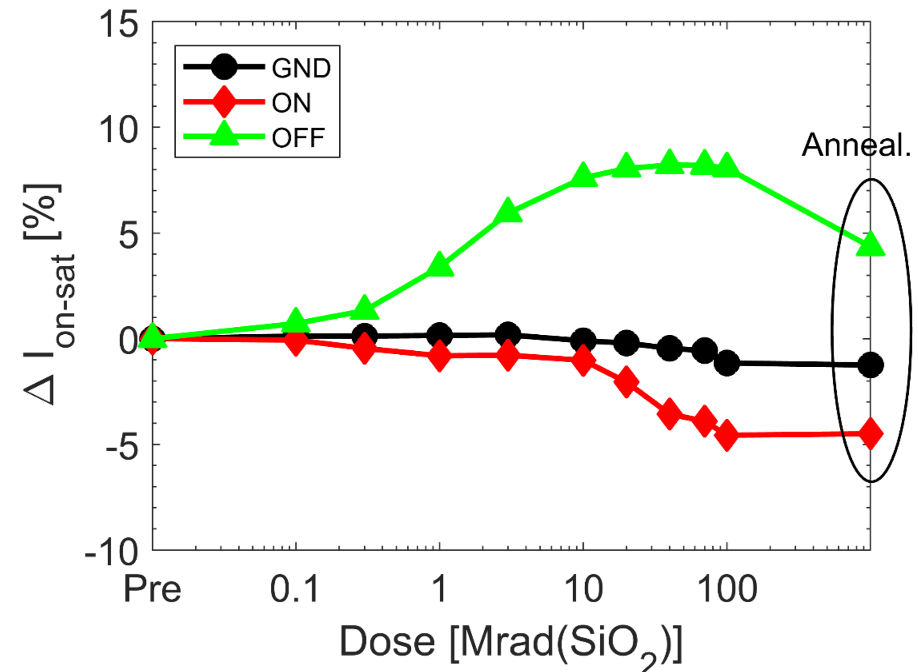




Power devices at ultra-high doses

- We have **just started** the valuation of **power devices** at ultra-high doses
- **AlGaN/GaN HEMT (Imec, < 50 V)**
  - Strong dependences with the applied bias and passivation types -> OFF condition is the worst condition
- **Vertical SiC MOSFET (> 1 kV)**
  - We got first results, stay tuned
  - Typically, very sensitive to TID due to the presence of thick gate oxide





Summary

- TID induces **charge trapping in the dielectrics,** causing parametrical shifts in the V_{th}, g_m, SS, I_{off}
- The aggressive **scaling down of the technologies** improved the TID tolerance of the gate oxide
- **New TID degradation mechanisms** are identified as new materials and layouts are used in modern fabrication processes
- In **Si FinFETs**, **charge trapping in STI** induces **g_m loss** and **modest leakage current**
  - **Best TID tolerance** on transistors designed with **low number of fin** and with **short channel**
- In **GAA FETs**, the TID tolerance is slightly worse than FinFETs -> investigation on going
- **Changing semiconductor material** may be critical for TID -> high number of defects at the semiconductor/oxide interface
- **Unpredictable trend of the TID effects with dependences on the technology node and the fabrication processes → research activities are required for the testing and qualification of modern technologies**

Future activities

- **Continue the qualification and exploration of radiation effects** in emerging technologies
    - Extend the data set of the Si FinFET technologies
- Gain knowledge about the **microscopic mechanisms,** useful for developing effective mitigation solutions
- Many open questions about:
    - **Ultra-ultra-high doses effects (>1 Grad)**
    - **Influence of dose-rate**
    - **Temperature (cryogenic and high)**
    - **Synergies between radiation and aging**
    - **Variability issues**