DRDT 7.5: Emerging Technologies

Evaluate and adapt to emerging electronics and data processing technologies

- Novel microelectronic technologies, devices, materials
  - A rolling R&D campaign is necessary to keep up with fast-moving and emerging technologies. Over the long timescales of HEP developments, one must not lose track of commercial evolution. For example, transistor structures in advanced nodes (FinFETs, Gate-all-around devices) will require thorough study of their behaviour and of the techniques for designing high performance circuits
- Silicon photonics
  - Silicon photonics is at an early stage of maturity and is new to the HEP community. A robust R&D programme is required to qualify the technology. In case of success an entire design ecosystem must be put in place to enable its coordinated use across institutes and laboratories

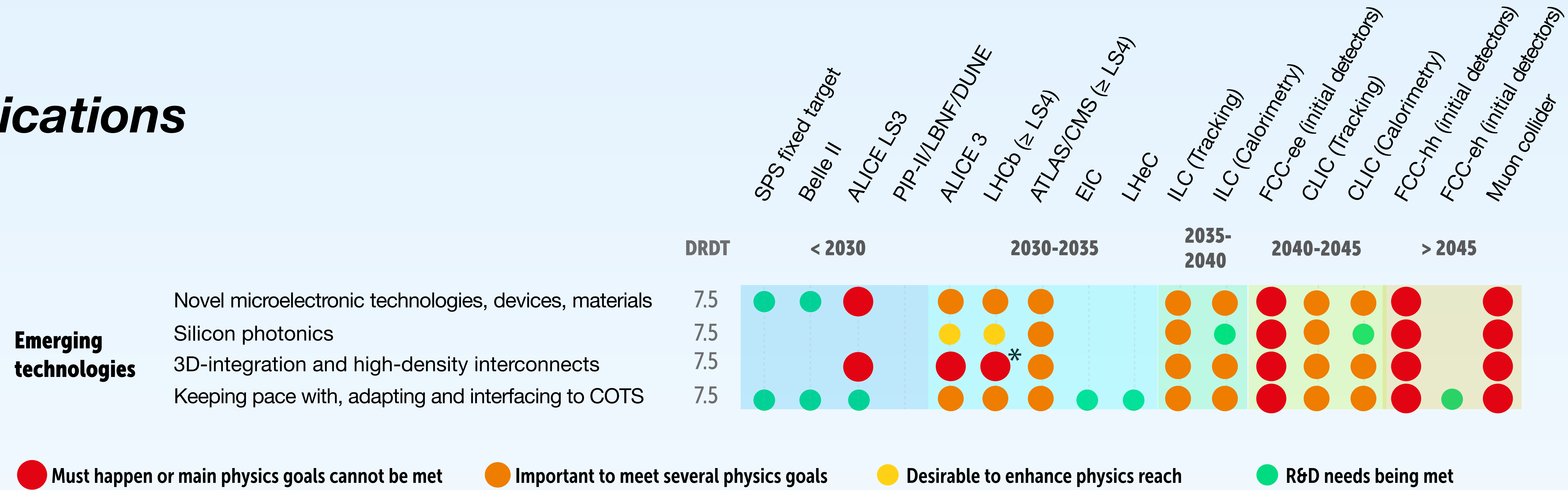
DRDT 7.5: Emerging Technologies (2)

Evaluate and adapt to emerging electronics and data processing technologies

- 3D integration and high density interconnects
  - Increasing channel density combined with enhanced functionality per pixel can only be managed with sophisticated 3D integration and interconnect technologies. 3D stacking must urgently be explored to combine analogue, digital and photonic functions. 3D integration of sensors with ASICs is critical and even more demanding. Access to reliable and affordable flip-chip processes, redistribution layers, stitching and ACF / ACP will also be important
- Keeping pace with, adapting, and interfacing with COTS
  - COTS computing (CPUs, GPGPUs, FPGAs, AI accelerators) and networking equipment increases performance at breathtaking pace. Since it is targeted mostly at cloud data centres, use in HEP requires adaptation and integration both at the hardware and software level. This is challenging work which needs to be repeated for every new generation of COTS

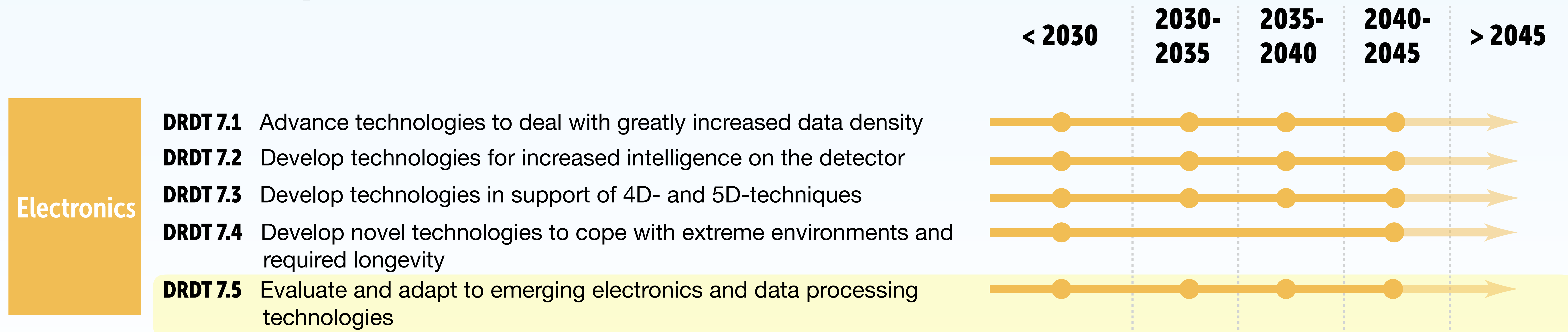
ECFA Targets

Target Applications



Source: The 2021 ECFA detector research and development roadmap

Target Dates for Completion of R&D

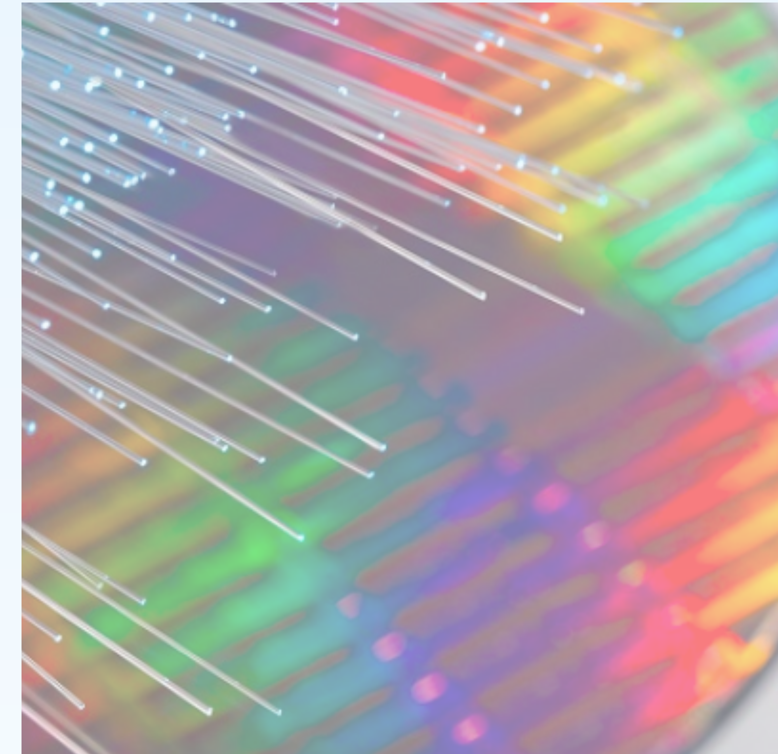


Source: Synopsis of the 2021 ECFA detector research and development roadmap

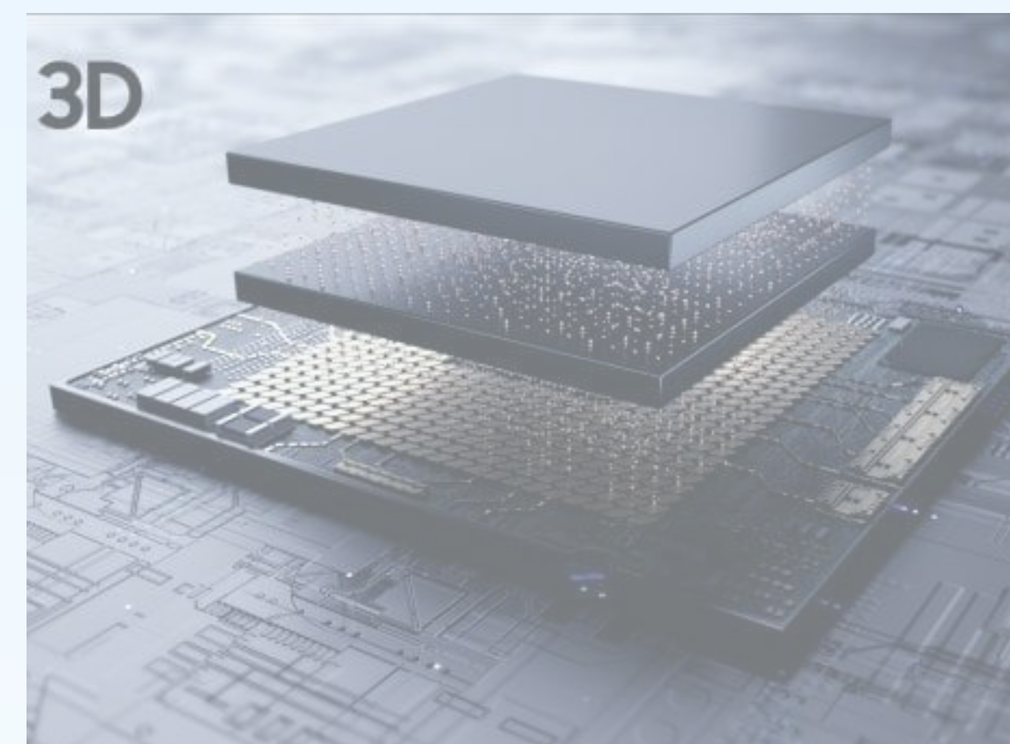
DRDT 7.5 Emerging Technologies

Novel microelectronic technologies, devices, materials

Silicon Photonics



3D integration and high density interconnects

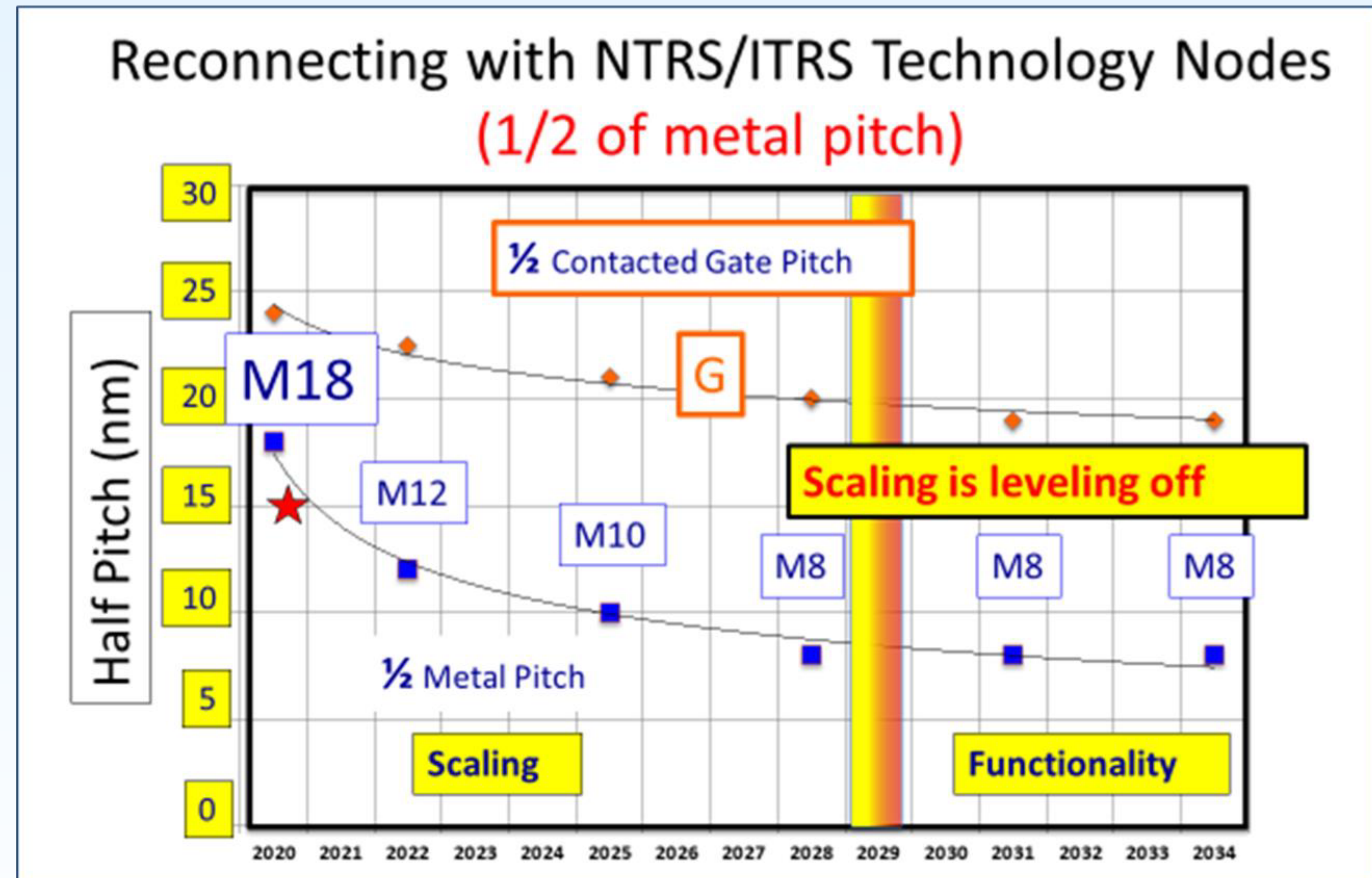


Keeping pace with, adapting, and interfacing with COTS

Novel Microelectronics

- Initially, this seems to focus on processes to be investigated for HEP applications
  - Leverage device designs from foundries
  - OR design own structures?

After: IRDS™ 2021: Executive Summary



- Clear overlap with investigation of how best to support technology access and IP sharing within the community

Staying on the wave?

ECFA
European Committee
for Future Accelerators

DRDT 7.5
Emerging Technologies

Logic/Foundry Process Roadmaps (for Volume Production)

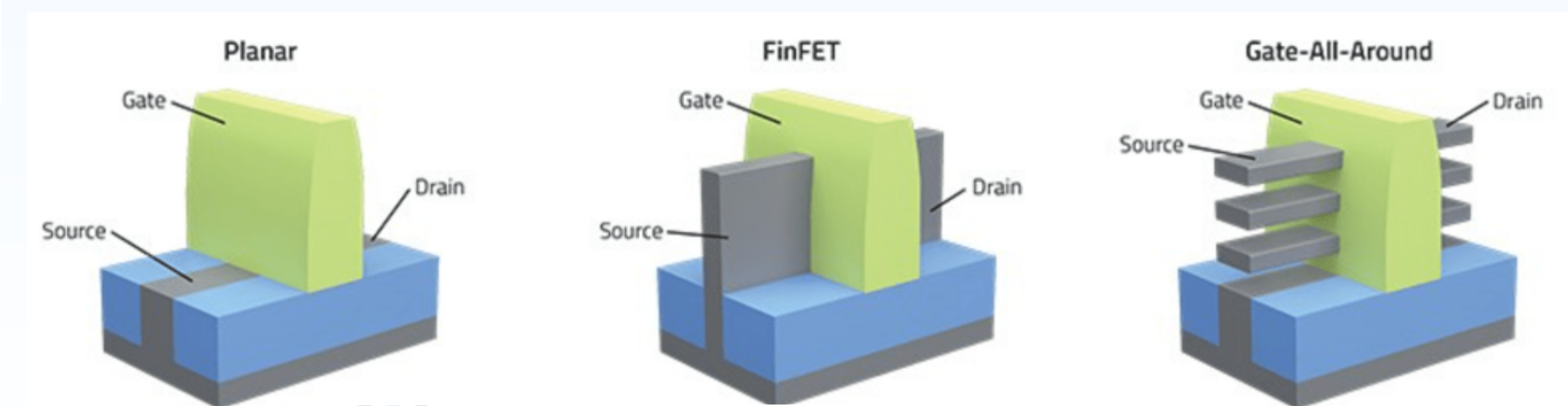
	2016	2017	2018	2019	2020	2021	2022
Intel	14nm+	10nm (limited) 14nm++		10nm	10nm+	10nm++	7nm EUV
Samsung	10nm		8nm	7nm EUV 6nm EUV	18nm FDSOI 5nm	4nm	3nm GAA
TSMC	10nm	12nm	7nm	7nm+ EUV	5nm 6nm	5nm+	4nm 3nm
GlobalFoundries			22nm FDSOI 12nm finFET		12nm FDSOI	22nm+ FDSOI 12nm+ finFET	
SMIC				14nm finFET	12nm finFET		8-10nm finFET
UMC		14nm finFET			22nm planar		

Note: What defines a process "generation" and the start of "volume" production varies from company to company, and may be influenced by marketing embelishments, so these points of transition should only be seen as very general guidelines.

Sources: Companies, conference reports and IC Insights

After: IRDS™ 2021: Executive Summary

- Most answers we got to our survey talk about FinFETs
- This is not even on the roadmap anymore…
- Are we being aggressive enough with our ambitions?
  - or would going further be dreaming?
- What about new device structures which appear at smallest features sizes?



Access to Technology

- Clear overlap with 7.7 – Paul Malisse will talk about this later today
  - https://indico.cern.ch/event/1214423/contributions/5184101/

- Processes currently shown on Europractice website:

22FDX
22 nm Fully-Depleted SOI
Access cost ~2.7x 28nm

12LP+
12 nm FinFET
Access cost ~3.8x 28nm

16nm FinFET compact
Access cost ~2.9x 28nm

7nm FinFET
No info/dates yet

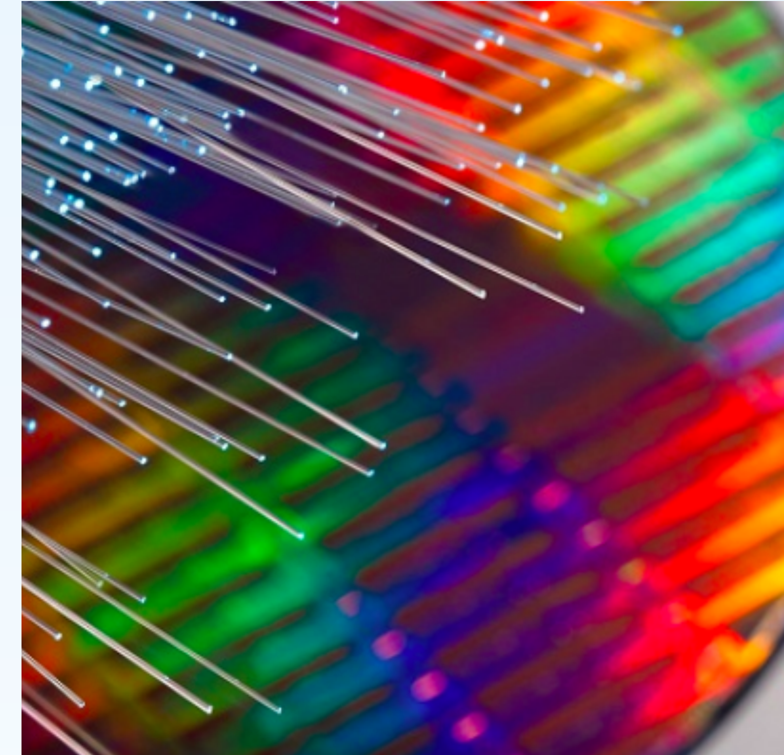
Encouraging that Europractice is looking ahead for us!

Increased cost of access obviously needs to be included in R&D budgets

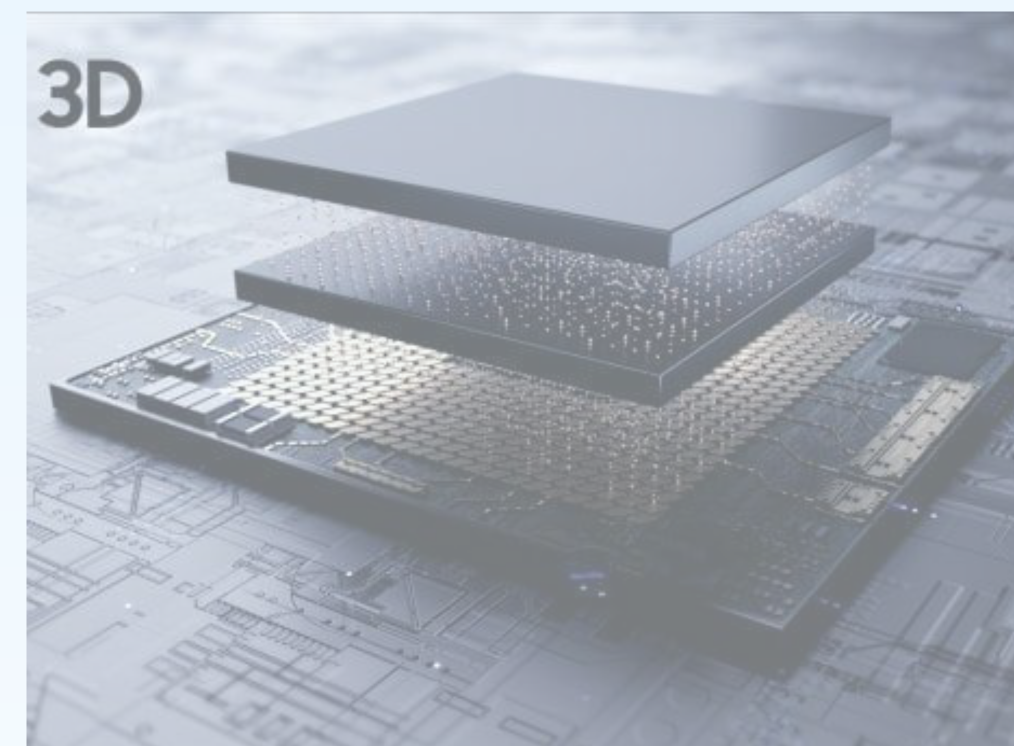
DRDT 7.5 Emerging Technologies

Novel microelectronic technologies, devices, materials

Silicon Photonics



3D integration and high density interconnects



Keeping pace with, adapting, and interfacing with COTS

Silicon Photonics

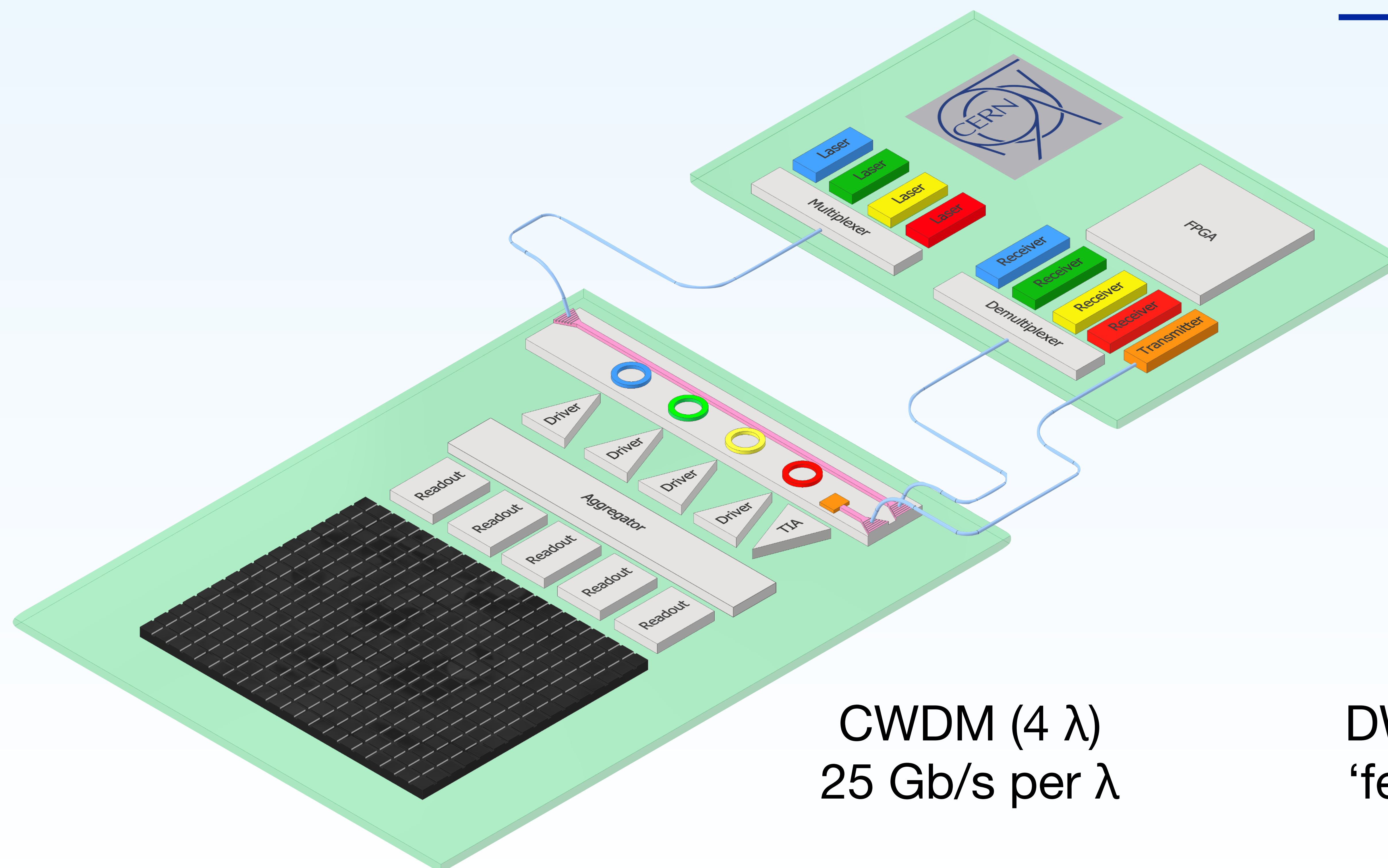
- “New” enabling technology for optical interconnects
  - Has in fact been available for purchase in commodity transceivers since ~2007 (Luxtera)
- Concept is to use CMOS-like wafer-level processing to pattern light-manipulating structures on SOI wafers
  - Processes available from at least 6 mainstream fab companies.
  - Two main families
    - Photonics only (e.g. imec/TSMC, Tower, Intel, ST)
    - Photonics + Electronics (GF, ihp)
- This technology holds many promises
  - Opportunity to design custom application-specific optical links (possibly improving radiation tolerance by design)
  - Opportunity for ultimate lowest-power links if can truly integrate electronics and photonics
  - Opportunity for similar radiation tolerance to silicon-based sensors (exceeding discrete GaAs/InP-based optoelectronics)

SiPh Technology & access

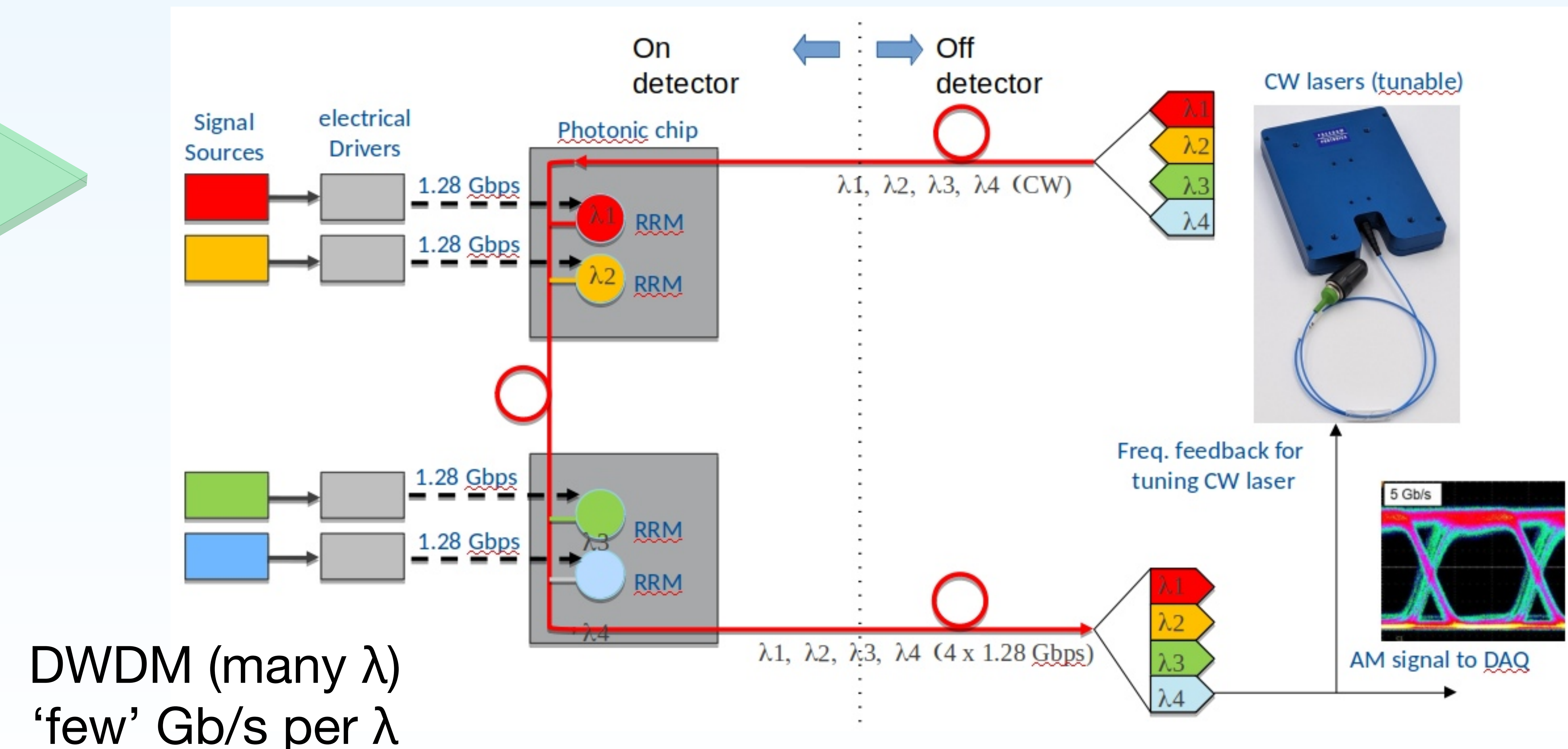
- Relatively “easy” to start designing
  - PDKs and MPW access through Europractice for
    - imec: ISiPP50G Photonics, ~12m turnaround
    - GF: 45 SPCLO Photonics & Electronics, ~6m turnaround
    - ihp: SG25H5_EPIC SiGe BiCMOS plus Si-Photonics
    - CEA-Leti: Si-310 Active and Passive Photonics platform
  - Design tools also available through Europractice
- Two flows possible
  - PDKs containing building blocks, that can be put together like a lightwave circuit with multiple functions (light I/O, couplers, modulators, …)
  - Full-custom photonic device design within the constraints of the process
- The Caveats
  - Device operation contains quite complex physics, design tools do not yet capture all effects
    - Tool support is limited when the tools come from Europractice, which is ok when there are expert users within the community – not the case for these tools
  - Full electronics-photonics co-design still somewhat in its infancy
  - New skills required, need to build a community for use in our environments

Existing efforts in HEP

- CERN
- INFN (Pisa)
- KIT
- US DoE SBIR project (SLAC, BNL, FNAL, UCSB-EE, Freedom Photonics)



CWDM (4 λ)
25 Gb/s per λ

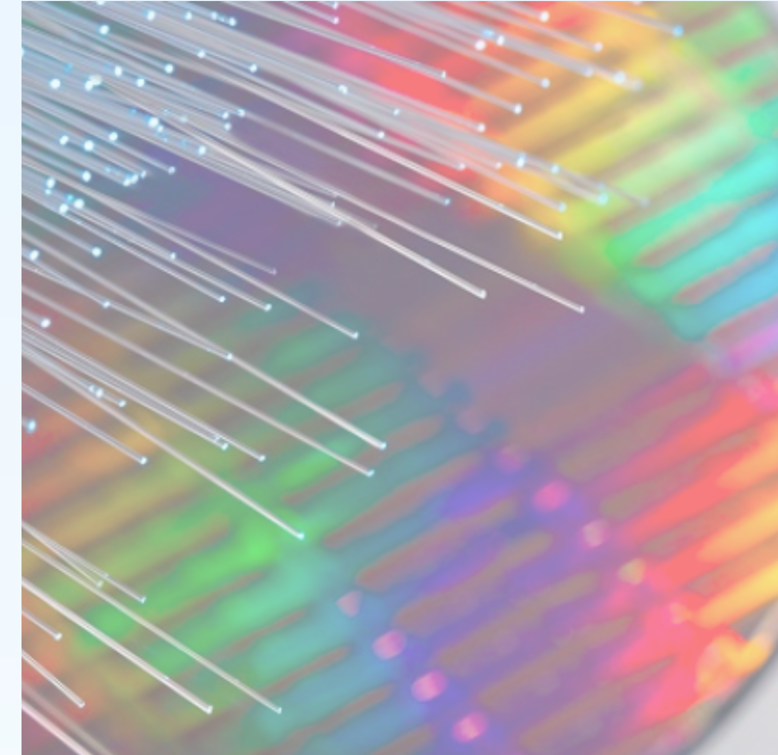


DWDM (many λ)
'few' Gb/s per λ

DRDT 7.5 Emerging Technologies

Novel microelectronic technologies, devices, materials

Silicon Photonics



3D integration and high density interconnects

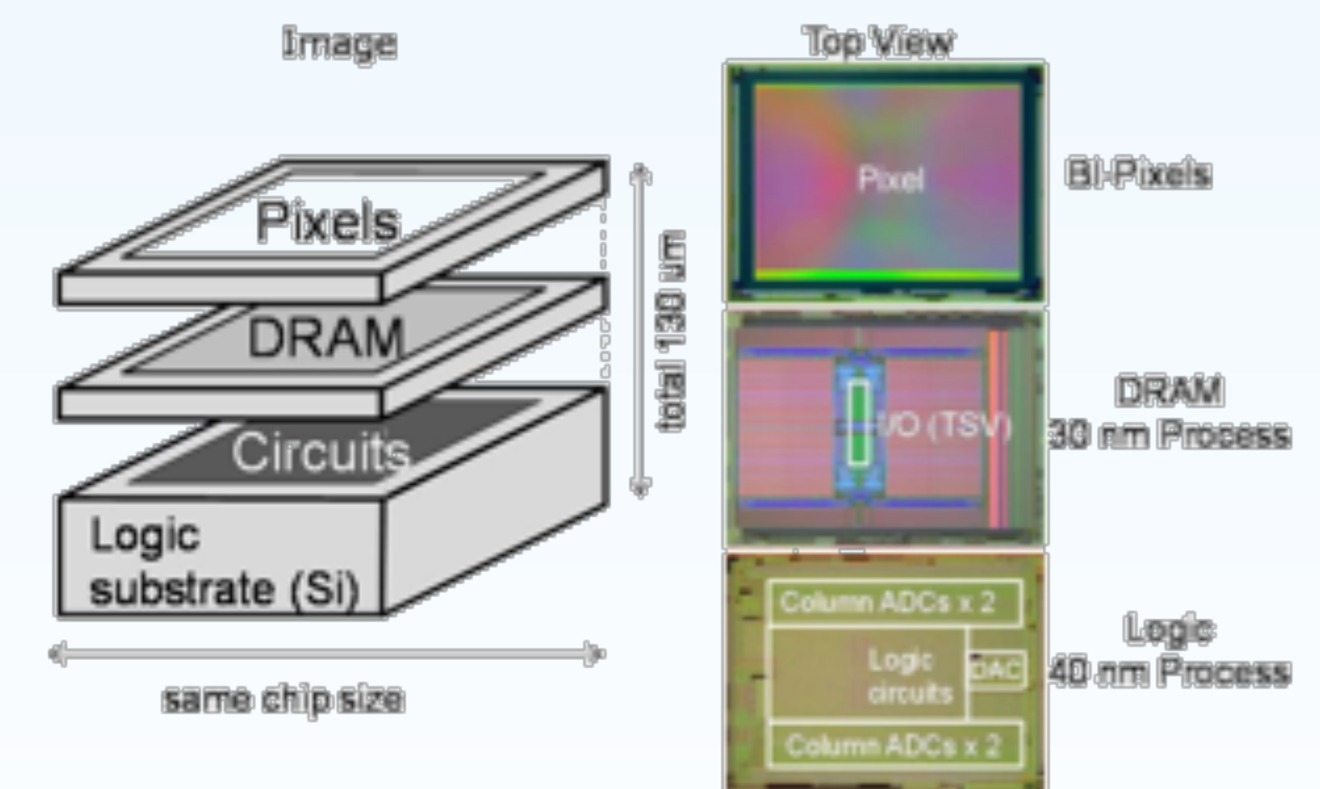
Keeping pace with, adapting, and interfacing with COTS

Towards 3D integration

- Increasing channel density combined with enhanced functionality per pixel requires sophisticated 3D integration and interconnect technologies
- Main challenges: precision timing (ToF, 4D tracking), high granularity and resolution result in increasing of data handling, processing, complexity and power
- Intelligence on detector will play an important role in data processing/reduction by ML and/or eFPGA, it requires a large and high-bandwidth memory layer tightly connected with ROIC (DRDT 7.2)

- 3-layer devices with image sensor, RAM, and logic are available thanks to high-density TSV, opening the way to event-based imaging, to AI processing and machine learning

- Development of high-speed PIC and integration with EIC is mandatory for future detectors (DRDT 7.1, 7.4, 7.5)
- Thinned down to 20-40 µm (0.02- 0.04% X0), making them mechanical flexible

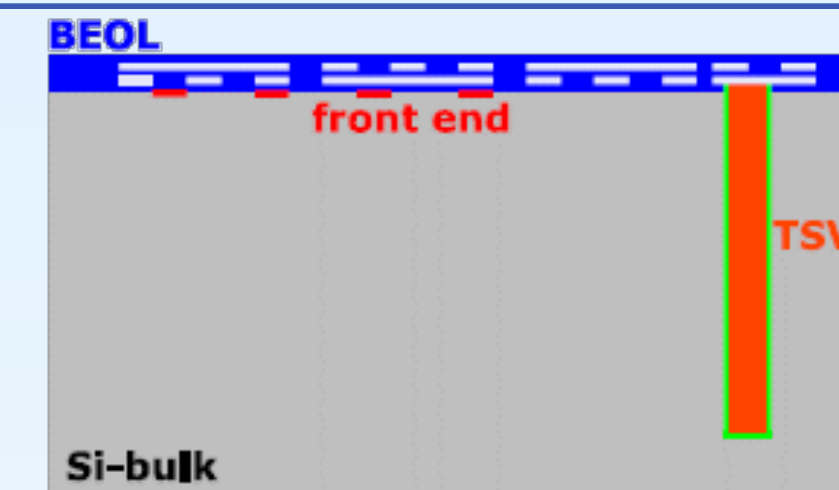


Valerio Re - ECFA Detector R&D Roadmap, April 23, 2021

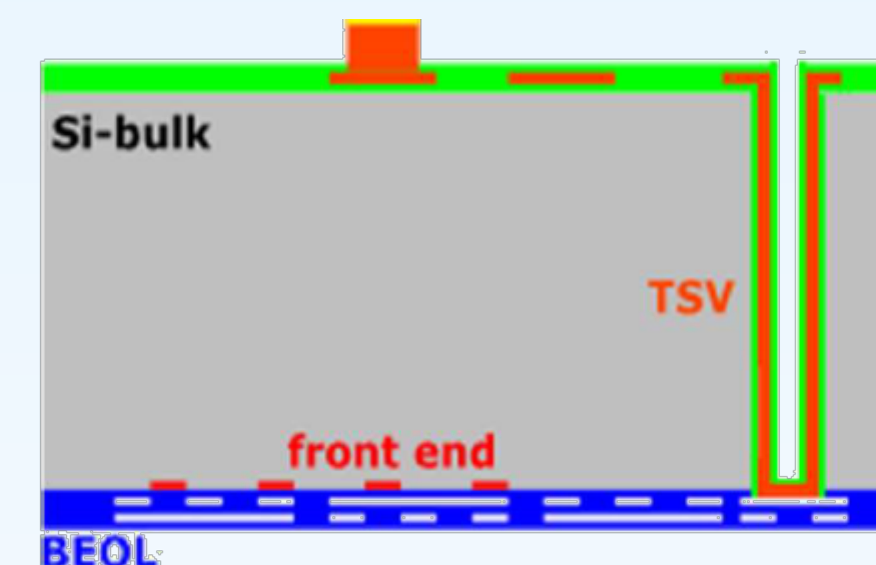
TSV Technology and RDL, back-grinding

ECFA European Committee for Future Accelerators | DRDT 7.5 Emerging Technologies

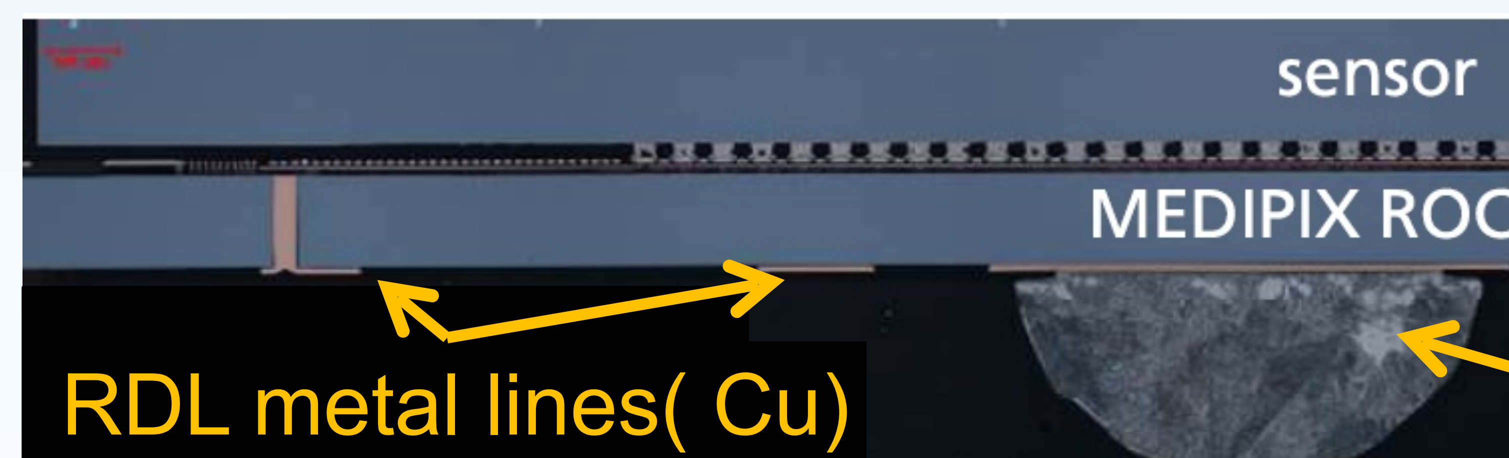
- Investigation of TSVs technologies:
  - „Via middle" enables high-density interconnections (∅ few μm)
  - TSV after the wafer is processed "via-last" enable the use of wafers from virtually any foundry for 3D integration
  - Glass Interposer with Through Glass Vias (TGV), for high-frequency applications, i.e. transceiver 4x28 Gb/s
- Investigation on Redistribution Layer (RDL) technologies:
  - Metal lines on back side
- Thinning and dicing



„Via middle" - TSV integration after FEOL and before BEOL



Back side „Via last" - TSV integration after complete wafer processing



Preliminary results of TSV Back-side – via last with RDL on Medipix/Timepix detetctors

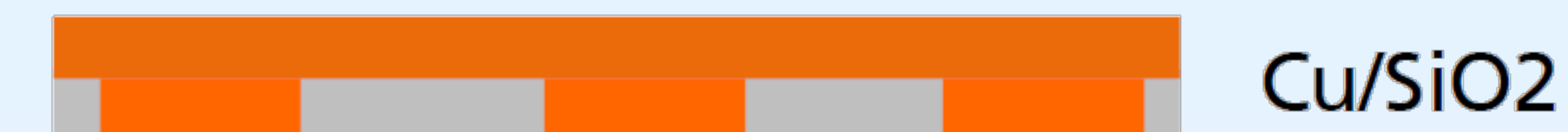
Bump bonding (BGA) between Mpx3 chip and PCB

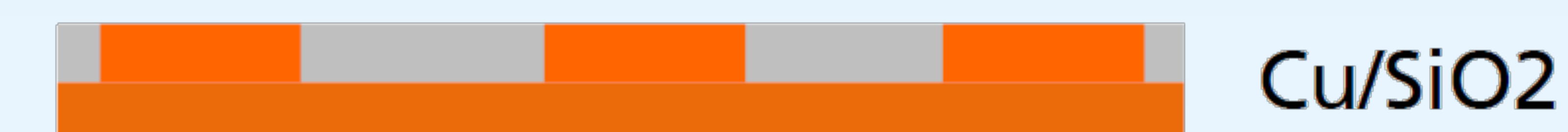
- However 3D integration exhibits some issues, which needs to be investigated, like: thermal, stresses (TSV), electro-migration

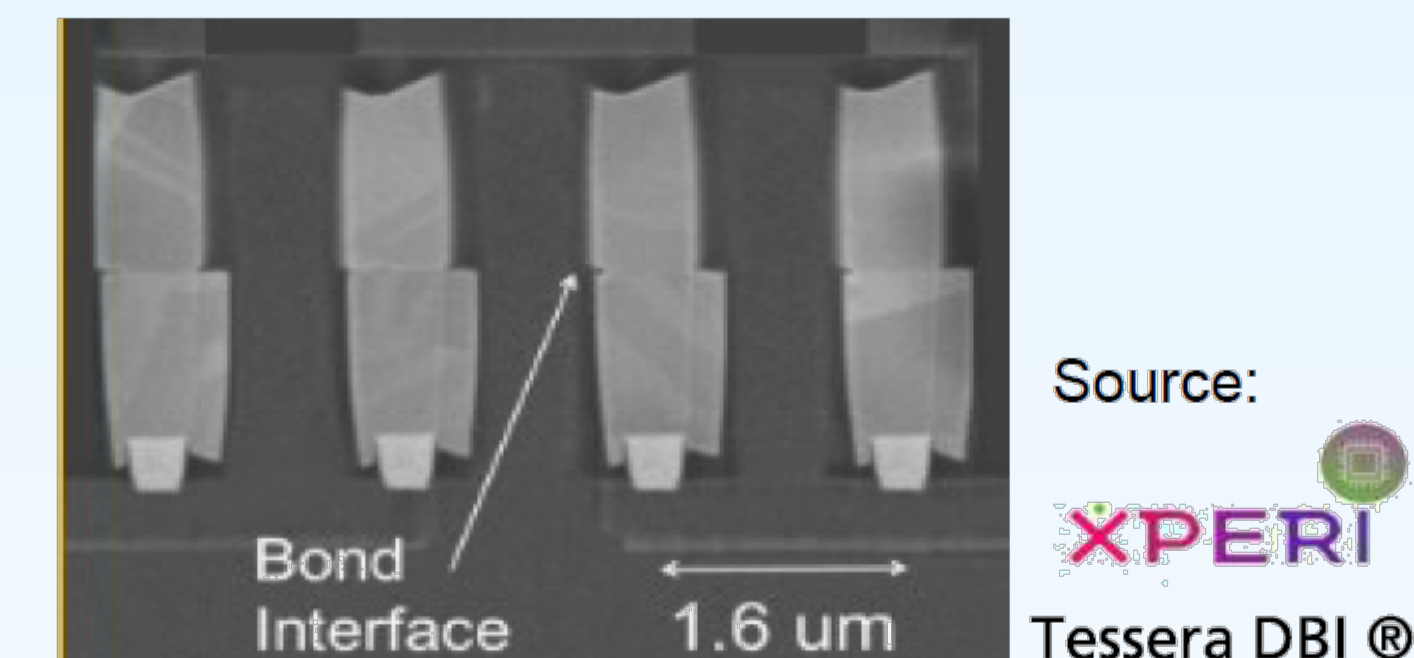
Assembly by W2W, C2W and C2C bonding

- Several bonding processes to be investigated:
- W2W and C2W bonding without solder
  - SiO_2-SiO_2 bonding: the most efficient (AC coupled sensor)
  - Hybrid Cu-SiO2 bonding
  - ACF (Anisotropic Conductive Film)

Source: Thomas Fritzsch (Fraunhofer IZM)







Source: XPERI Tessera DBI ®

- W2W and C2W bonding with “solder”
  - Solid Liquid Interface Diffusion (SLID) bump-bonding
  - Metal-Metal bonding: Cu-Cu is widely used (DC coupled sensor)
  - Gold-stud bump-bonding → for fast prototyping

Hybrid Cu-SiO2 bonding technology:

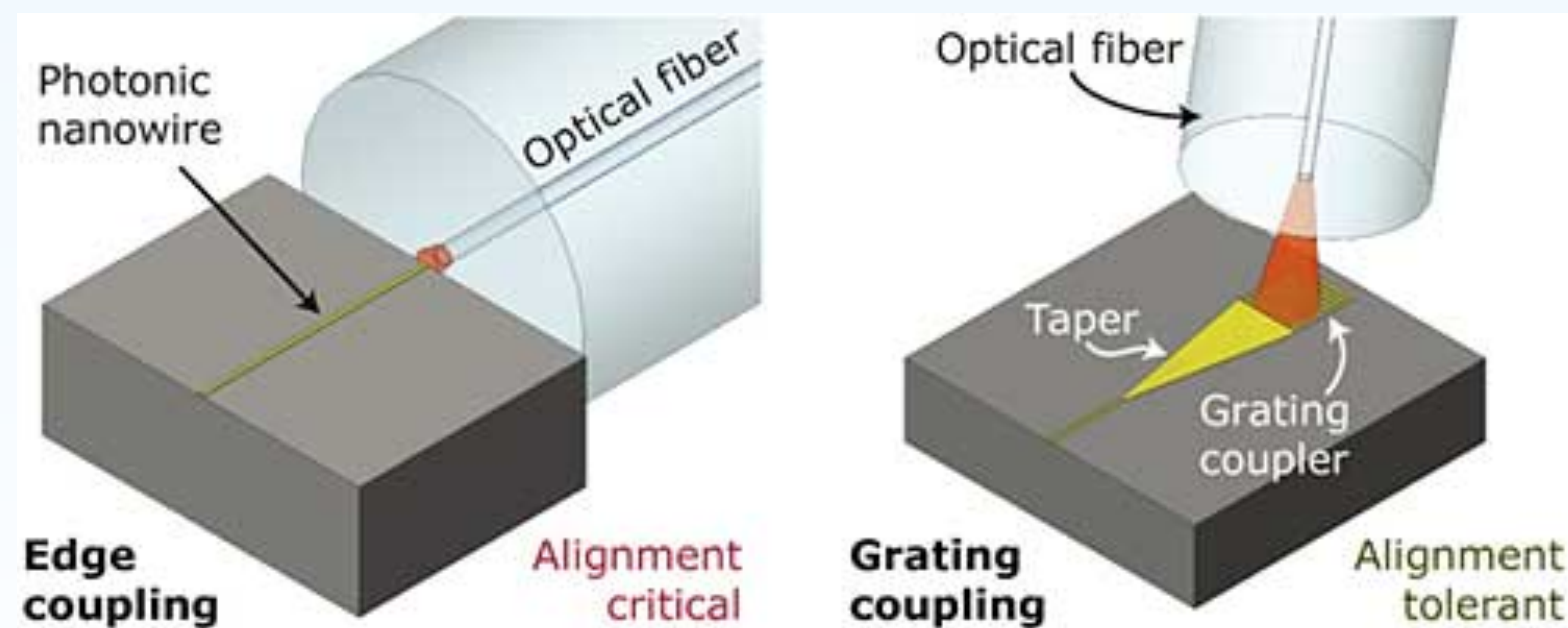
- SiO2 passivation + Cu pads
- Room temperature bond, annealing 150 – 300°C
- 3D chip stacking: memory chips, CMOS image sensors (CIS)

PIC and EIC Integration

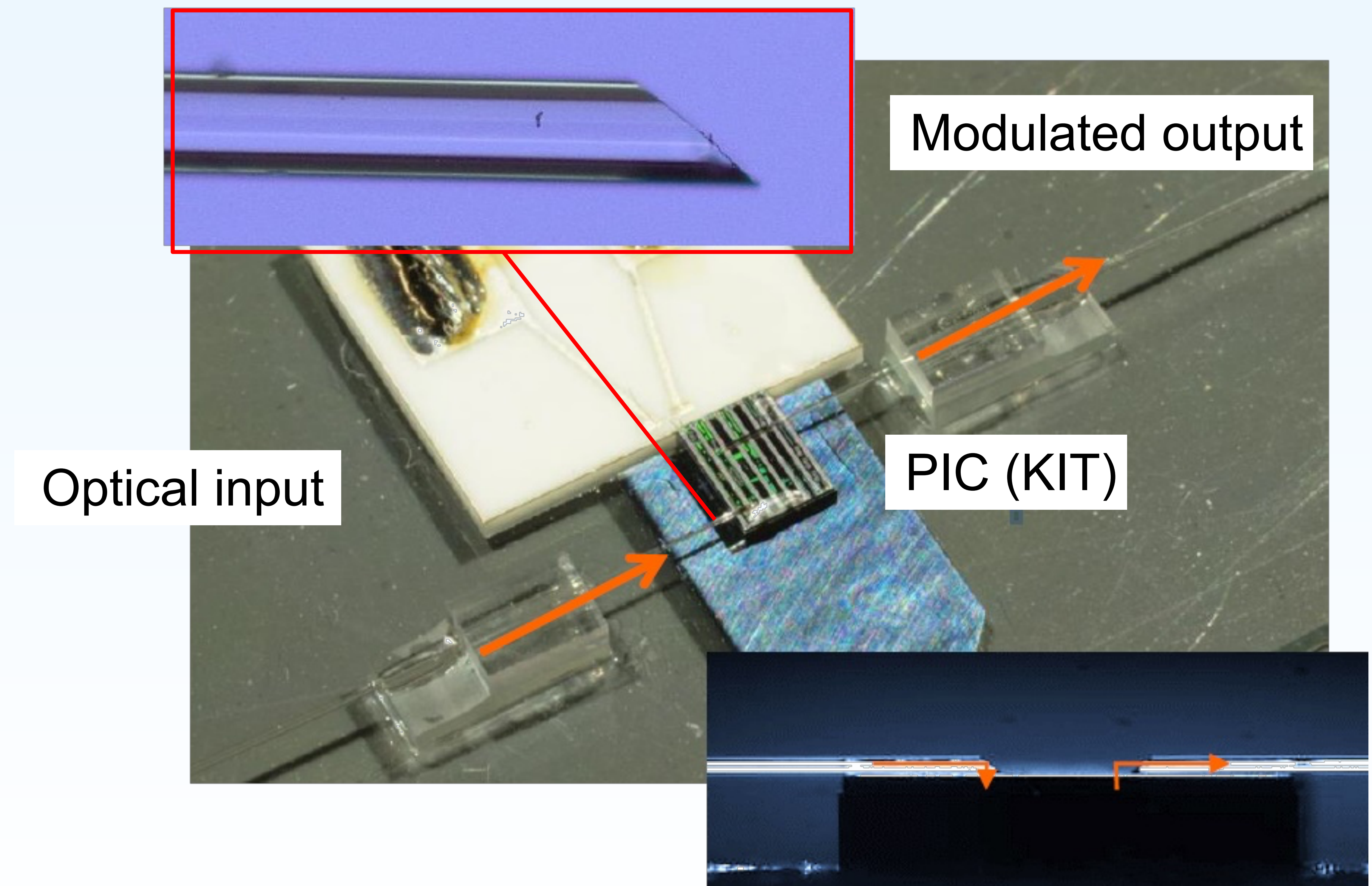
- Integration of silicon photonic chips with driver and detector
  - By flip-chip/wire-bond/TSV/TGV

→ Fabrizio slides (Prospects on new link technologies)

- Integration/coupling of optical fibers on PIC
  - Compact fiber-chip coupling
  - Low loss
  - Concept is simple, at-scale production still niche



Courtesy: Marc Schneider (KIT)



Access to 3D technologies

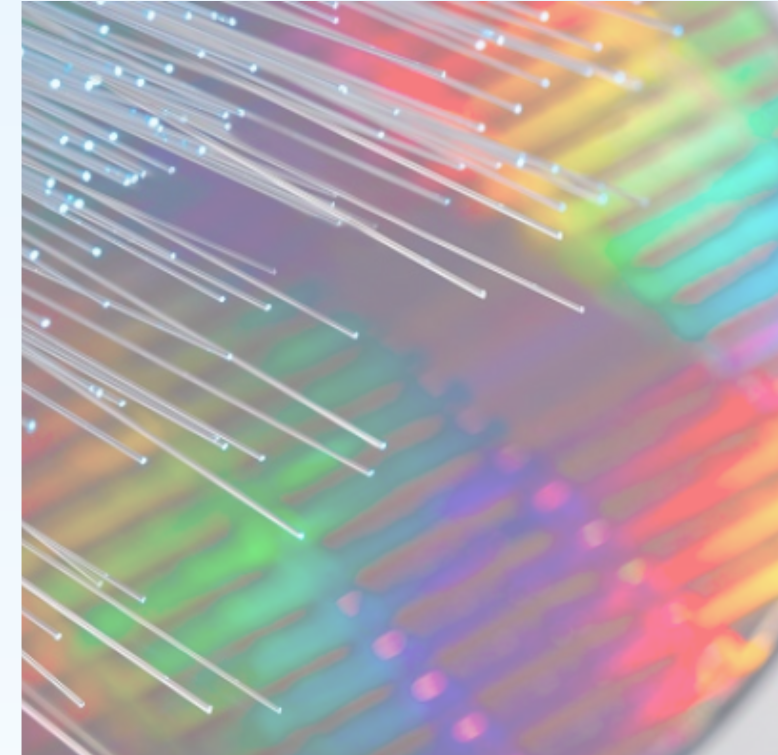
- Access via research center
  - Technology and infrastructure available at research center:
  - Enable low-cost and direct investigation on critical process
  - List of machine / infrastructure available (i.e. Femtoplacer flip-chip at KIT and DESY)
    - C2C, C2W bonding process, AC and DC coupled bonding
    - Precise integration/coupling of optical fibers on PIC
- Access via vendors / services
  - Technology like: TSVs and RDL process, W2W bonding
  - We are limited to vendors who will work with smaller customers. We need a list of vendors willing to process small numbers of high value added
- Access via silicon foundries
  - Silicon foundry with in-house monolithic 3D integration
  - Coordination/support of the process by Europractice or similar

michele.caselle@cern.ch

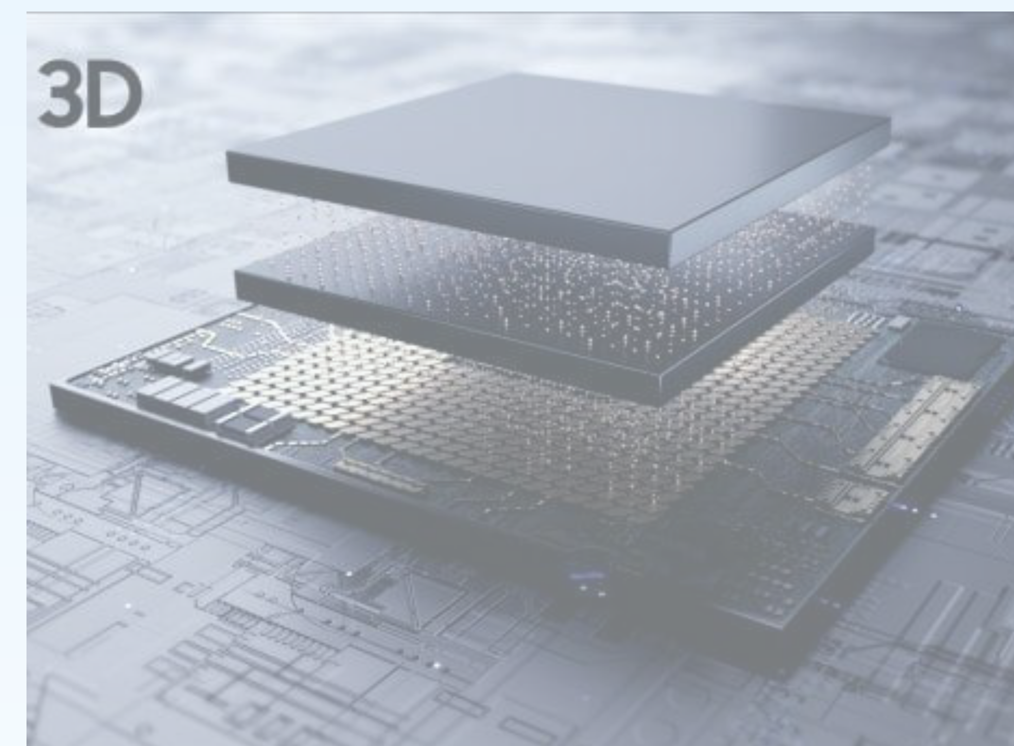
DRDT 7.5 Emerging Technologies

Novel microelectronic technologies, devices, materials

Silicon Photonics



3D integration and high density interconnects



Keeping pace with, adapting, and interfacing with COTS

Using & keeping up with COTS

ECFA European Committee for Future Accelerators | DRDT 7.5 Emerging Technologies

- Low / no radiation, no very stringent power requirements
- Full range of COTS chips/ systems available: FPGAs, GPGPUs, CPUs/SoCs, others?
- Except for SoCs and FPGAs there are usually designed with a rather specific (hardware) environment in mind →custom integration not obvious

- Strong radiation and/or strict power limitations
- Not much COTS on the horizon, excepting some chips targeting avionics / space → most likely will need some kind of ASIC
- Probably more easy and robust to stick to limited functionality and focus on efficient off-detector transport of data (--> SiPho etc..)

Whither COTS?

- COTS is driven by what everybody wants. Today this is AI, yesterday it was Mobile, tomorrow nobody knows (or please speak up! :-))
- Technologies change (or even disappear) often quickly, yet there is also inertia because of large investments: Ethernet, PCIe, x86, ARM, PC, Linux, …. It's not about what one thinks is "best", but what everybody will buy

- How well can we formulate our problems (== format out data and define our calculations) so that they can run well on the "hot" technologies. Think Machine Learning / AI.
- Data-centre COTS has a tendency to get bigger and more expensive per "piece" / "system" even if - of course!? - it gets cheaper per unit of "work": e.g. 400 G networks vs 100 G networks, AMD 9xxx CPUs (350 W+) vs CPUs from a few years ago (at most 130 W), or Nvidia GPGPUs, or also the big FPGAs ➔ technology tracking and PoCs will profit from collaborations so that we don't need to buy the same hardware n times