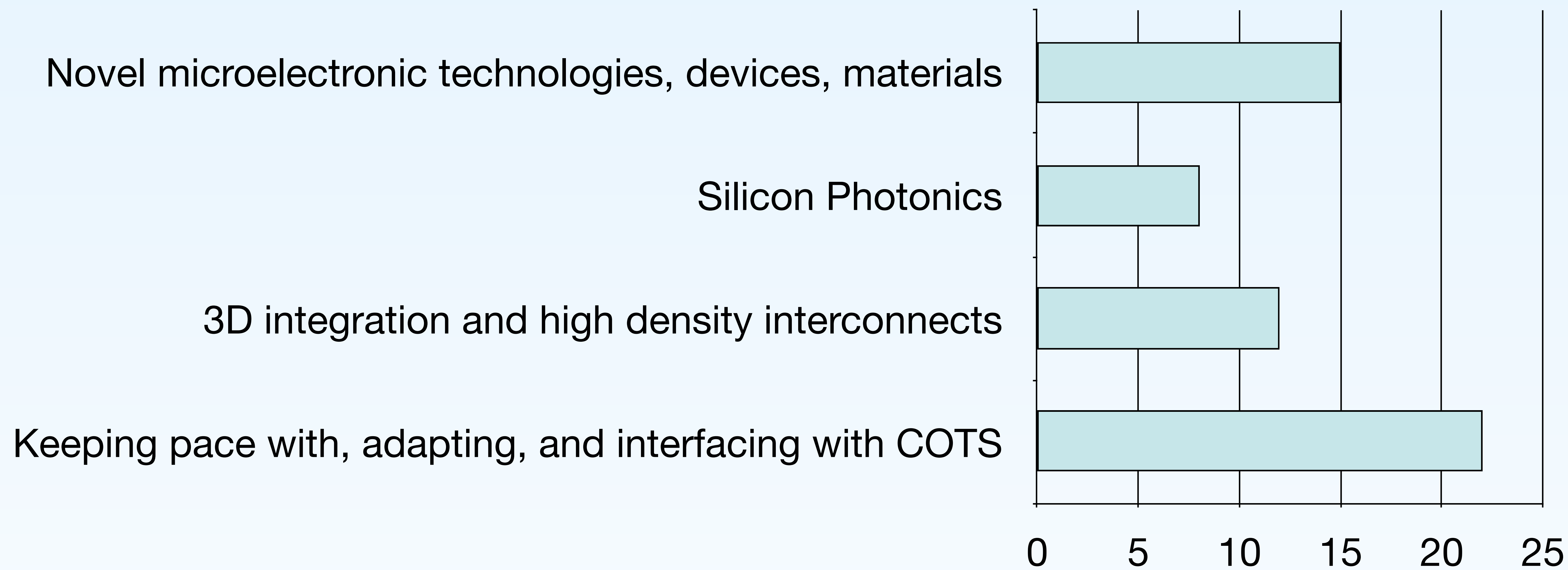
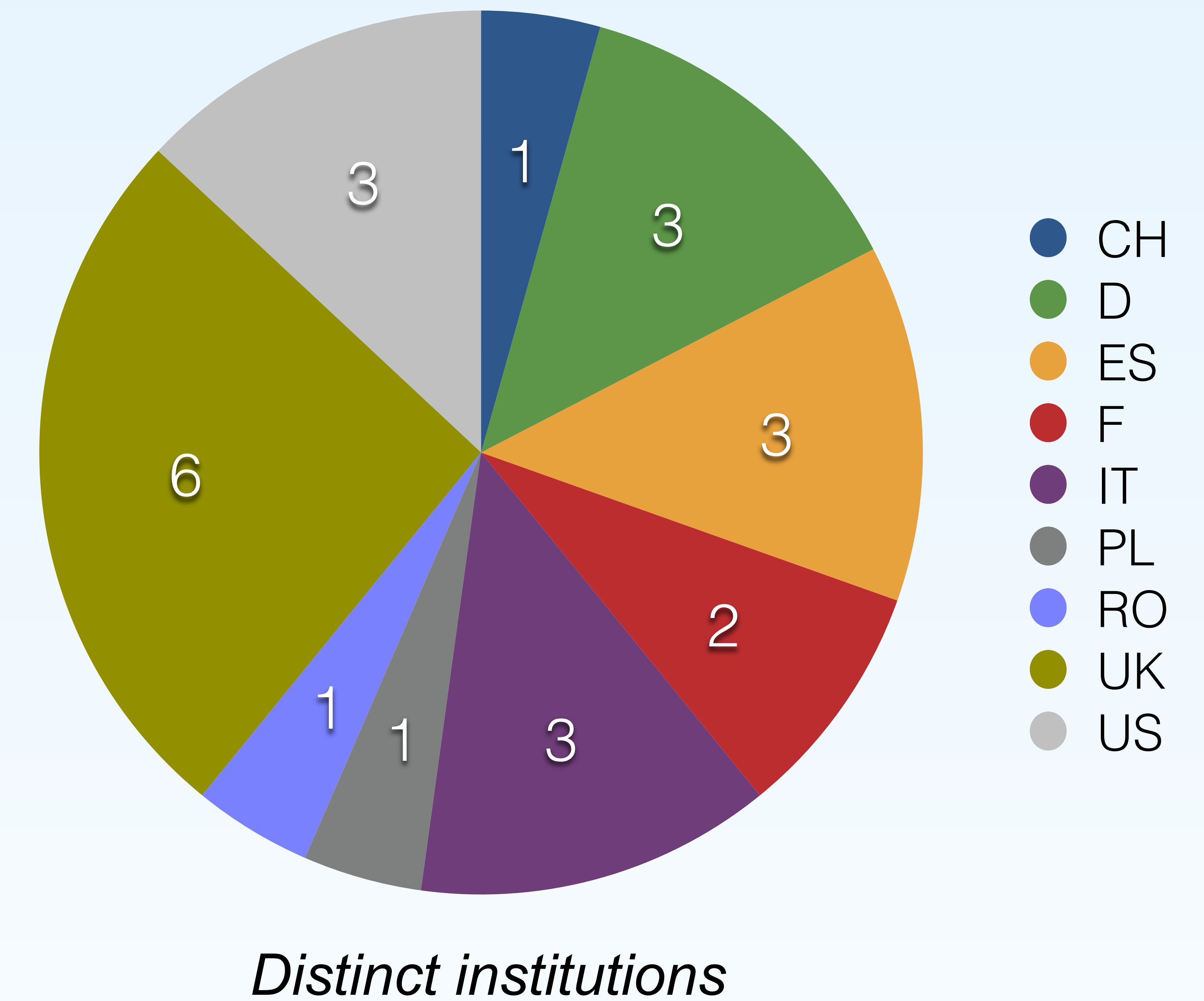
Questionnaire Responses (32 total)

Interested in working on:



Institution based in:

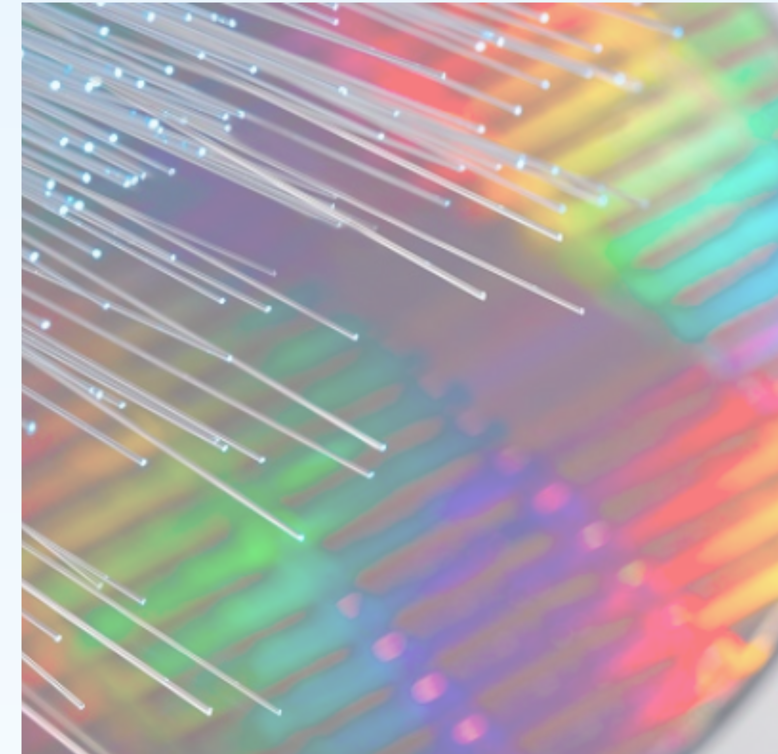


Distinct institutions

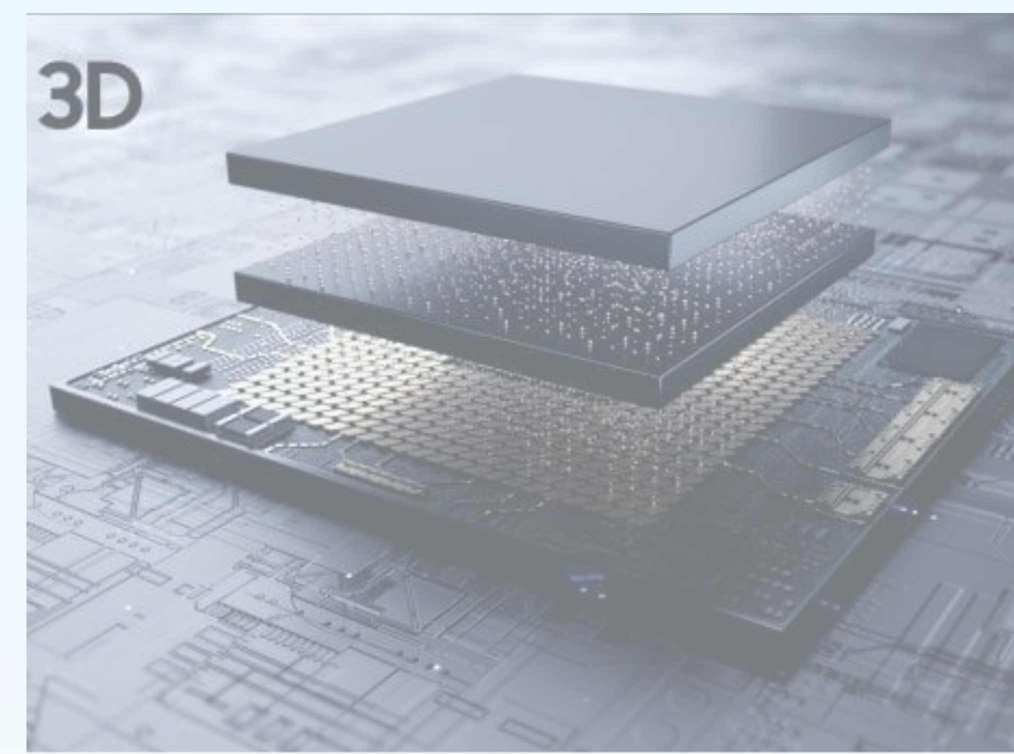
DRDT 7.5 Emerging Technologies

Novel microelectronic technologies, devices, materials

Silicon Photonics



3D integration and high density interconnects



Keeping pace with, adapting, and interfacing with COTS

Novel Technologies (1)

- Technologies of Interest
  - FinFET(16, 14, 7 nm): 7 responses
  - 22 nm FD-SOI: 1 response
  - 28 nm and below CMOS: 3 responses
  - 90 nm SiGe: 1 response
- Motivation
  - FinFET: Future dominant tech; enable high-speed links; scaling leading to power and area reduction;
  - CMOS: Development of common block for use by HEP community; follow industry trend
  - FD-SOI: Cryogenic Front-End for quantum and cryo-detectors
  - US Chips act is pushing for on-shore manufacturing
- Concerns
  - FinFET: Radiation hardness; cost; complexity; analogue performance;

Novel Technologies (2)

ECFA
European Committee
for Future Accelerators

DRDT 7.5
Emerging Technologies

- Topics of interest for research
  - Analogue performance & radiation tolerance of FinFETs (UniPavia)
  - FinFET Test Chip Design & characterisation (KIT)
  - FinFET & CMOS High-Speed Blocks CDR, Drivers, PLL, SERDES (INFN Pisa & Torino)
  - SiGe Mixed-Signal ASIC for Photosensors (UniBarcelona)
  - TPSCo 65 nm* for MAPS application (DESY)
  - Si + monolithic sensors (Liverpool)
  - High rate tests with electrons, optimizing DAQ architectures (UniMainz)
  - PDK Development (FNAL)

*Tower Partners Semiconductor Company

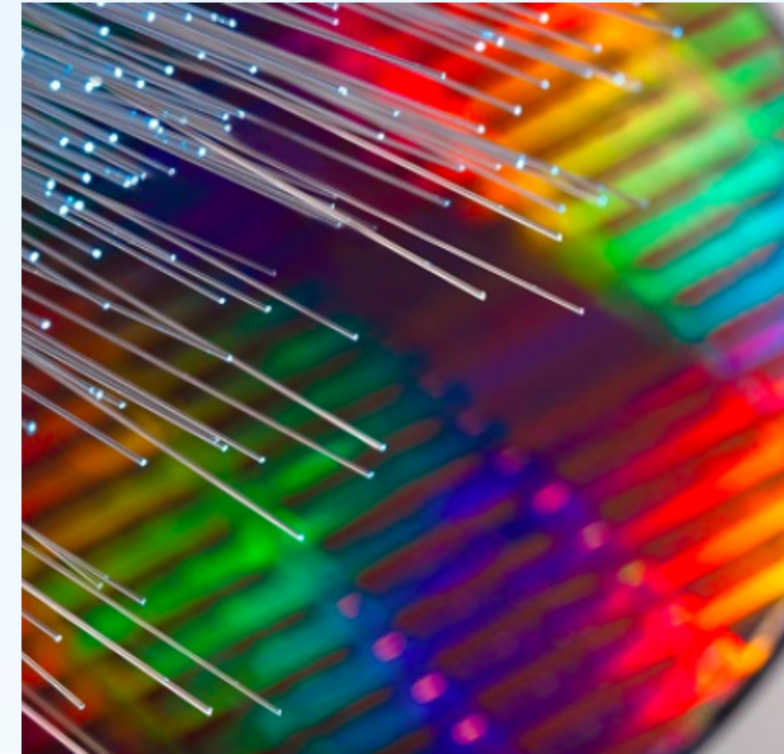
DRDT 7.5 Emerging Technologies

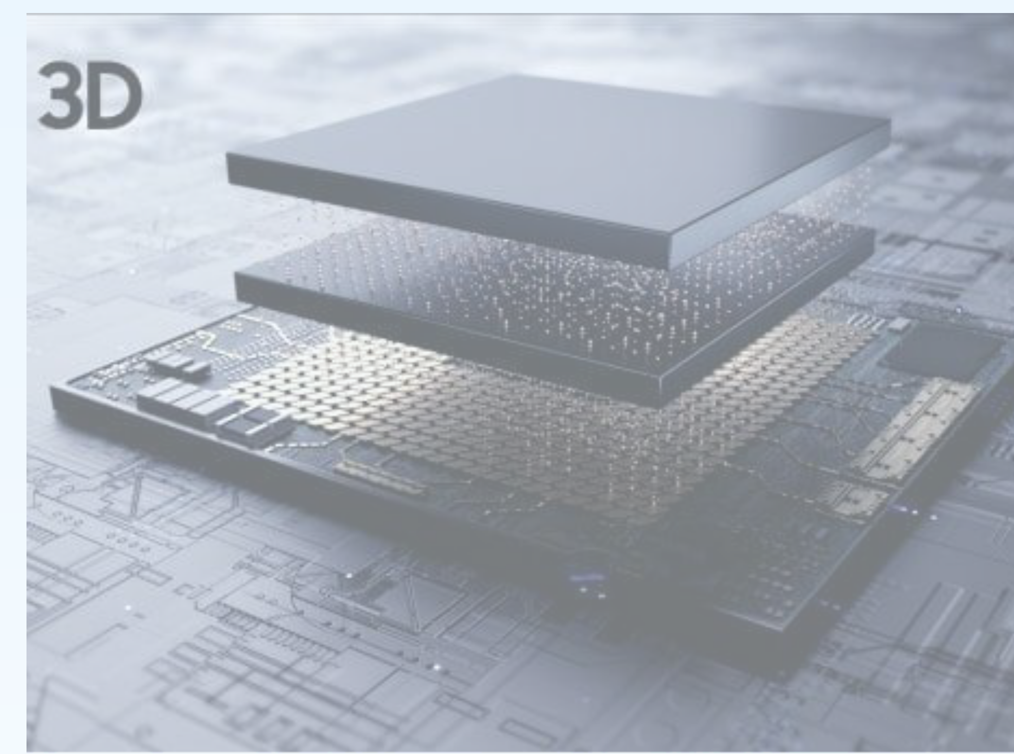
Novel microelectronic technologies, devices, materials

Silicon Photonics

3D integration and high density interconnects

Keeping pace with, adapting, and interfacing with COTS





Silicon Photonics (1)

- Research Topics
  - Environmental tolerance (radiation, temperature, vacuum): 4
  - EIC/PIC interconnection: 4
  - EIC/PIC integration (monolithic): 2
  - Fibre attach: 2
- Motivation
  - Tight front-end integration;
  - Lower power front-end;
  - Monolithic integration: single design electronic/photonic design environment; easier co-pkg
  - US Chips act is pushing for on-shore manufacturing
- Concerns
  - Monolithic integration: rad-tolerance of SOI process;

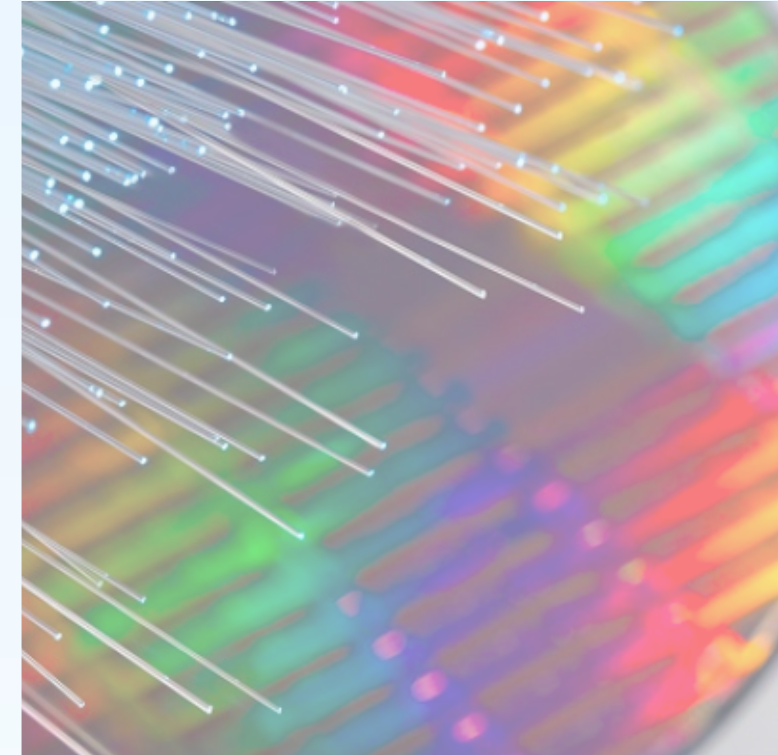
Silicon Photonics (2)

- Topics of interest for research
  - Device Design (CERN, DESY, INFN, KIT)
  - System Chip Design (CERN, DESY, INFN, KIT)
  - Packaging & Fibre Attach (CERN, KIT)
  - Driver/TIA design (CERN, FNAL)
  - FE ASIC co-packaging (Barcelona, CERN, Wuppertal)
  - Radiation tolerance (CERN, INFN)
  - System testing (CERN, INFN, KIT)

DRDT 7.5 Emerging Technologies

Novel microelectronic technologies, devices, materials

Silicon Photonics



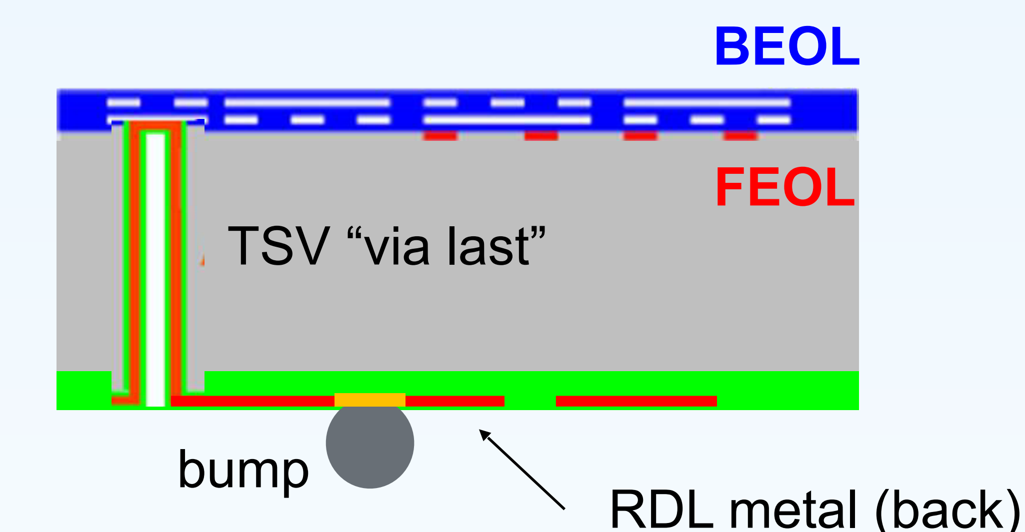
3D integration and high density interconnects

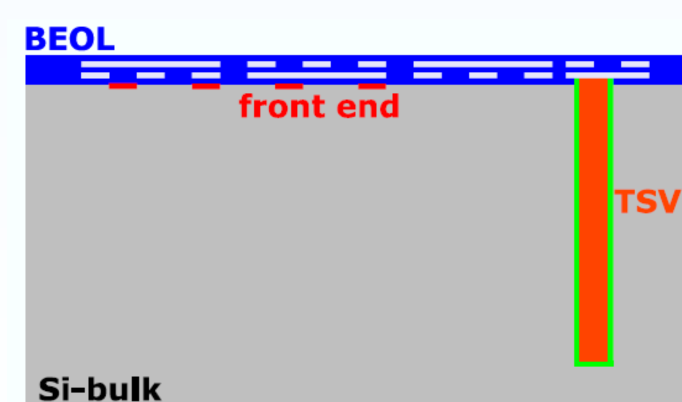
Keeping pace with, adapting, and interfacing with COTS

3D integration & high density interc. (1)

Which techniques and technologies for 3D integration should be systematically studied?

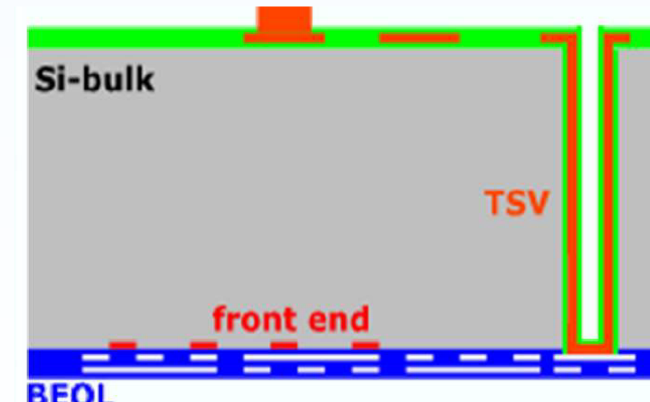
- High density TSVs (TSV "via middle“ and back side TSV ”via last”): *5 responses*
- Through Glass Vias (TGV), which employs a glass interposer for 3D integration: *1 responses*
- Redistribution layer (RDL) process: *2 responses*
- 3D IC technologies, direct wafer bonding: *3 responses*
- Anisotropic Conductive Films ACF and ACP (paste) bonding: *2 responses*
- Integration of silicon photonic chips and ASICs: *3 responses*
- PCB/flex hybrid integration based on new materials: *1 responses*
- Power consumption and heat, combination of different signals: *1 responses*





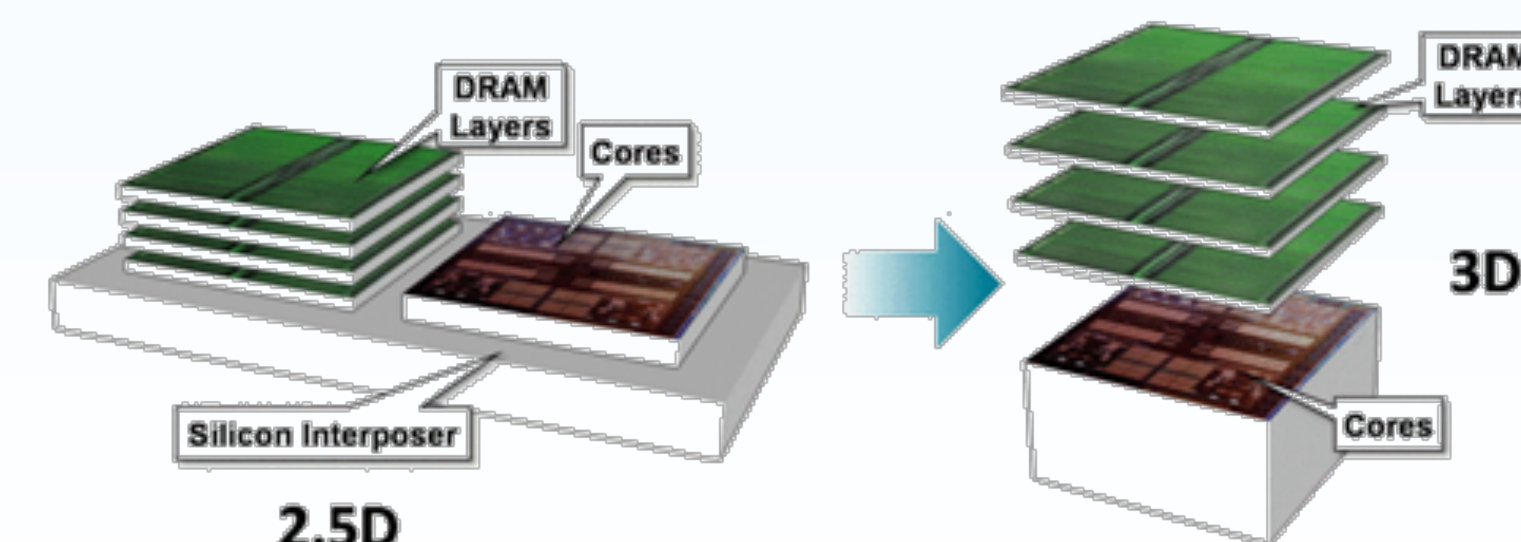
TSV “Via middle”

TSV integration after FEOL and before BEOL



TSV “Via last

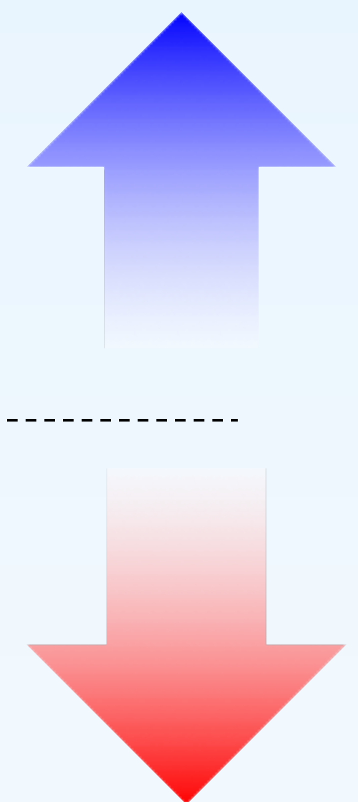
TSV integration after complete wafer processing



3D integration & high density interc. (2)

Which facilities / procedures do you need to have access to, to be able to use 3D integration in future projects?

- Precision placing, flip chip bonder machines: *4 responses*
- Wire bonding machine, fiber alignment machine, RF or EMC equipment / facilities: *3 responses*

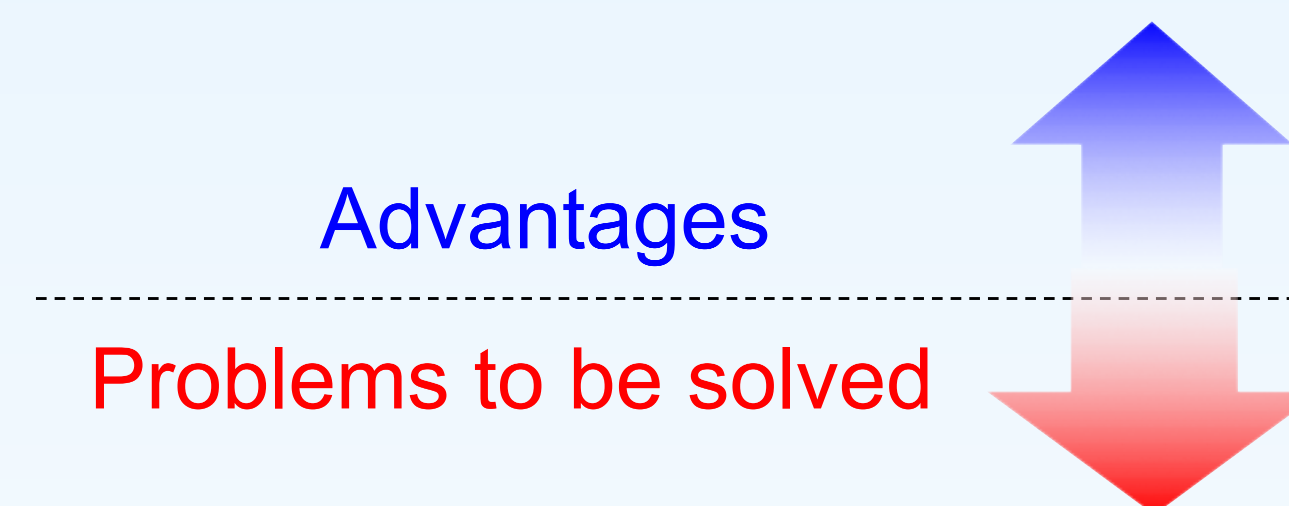


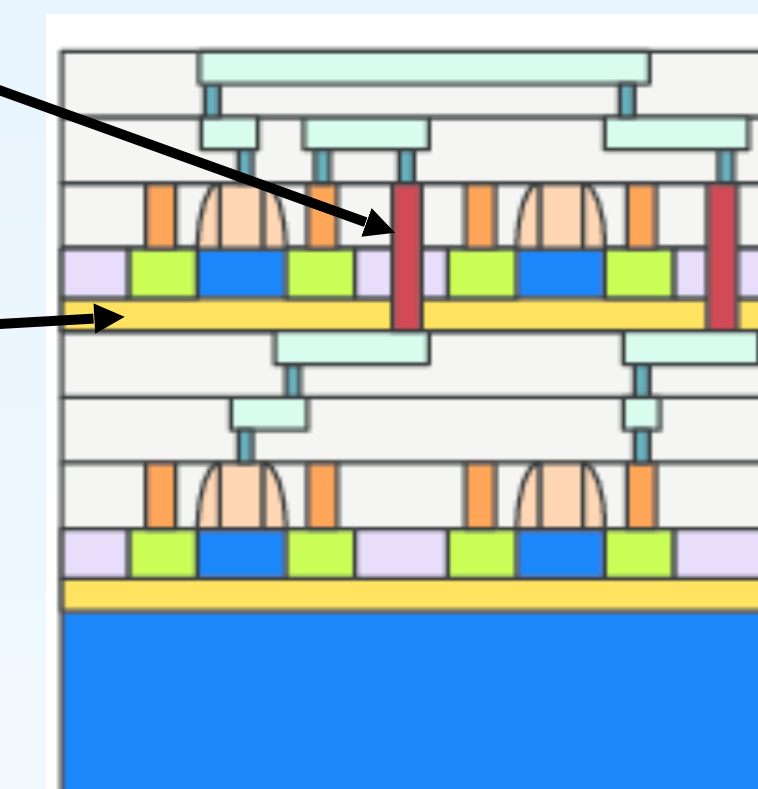
- TSV, RDL, W2W bonding are complex process that often involves many companies:
  - FBK and IZM
  - Nhanced and IMEC *3 responses*
- Establish a link with a silicon foundry with in-house 3D technology: *1 responses*
- Access to reliable and affordable wafer bonding processes: *1 responses*
- A coordination of the process by an entity such as Europractice or similar will also be most useful. This also concerns SiP solutions and advanced packaging

3D integration & high density interc. (3)

Which problems must be solved to 3D-combine sensors and analogue/digital components in a single stack (monolithic 3D integration) ?

- Make easier the access and standardization: *2 answers*
- Reliability & compact cooling concept: *1 answers*





- Besides 3D processing, for 3D microelectronics it is essential to have access to the proper simulation and verification tools: *1 answers*
- Yield, powering, heat dissipation and noise/crosstalk issues: *3 answers*
- The use of high resistivity wafers in the stack, that might not be default in commercial 3D stacks: *1 answers*
- TSVs and a via-first or via-middle process; planarity of sensor and IC wafers: *1 answers*
- 12" sensor wafers necessary for direct W2W bonding between sensor and readout layers: *1 answers*

3D integration & high density interc. (4)

Are you (and/or is your group) interested in investigating 3D integration and high density interconnects?

- CERN
- KIT and DESY
- FNAL
- UniBarcelona
- ITTAINOVA (Instituto Tecnologico de Aragon)

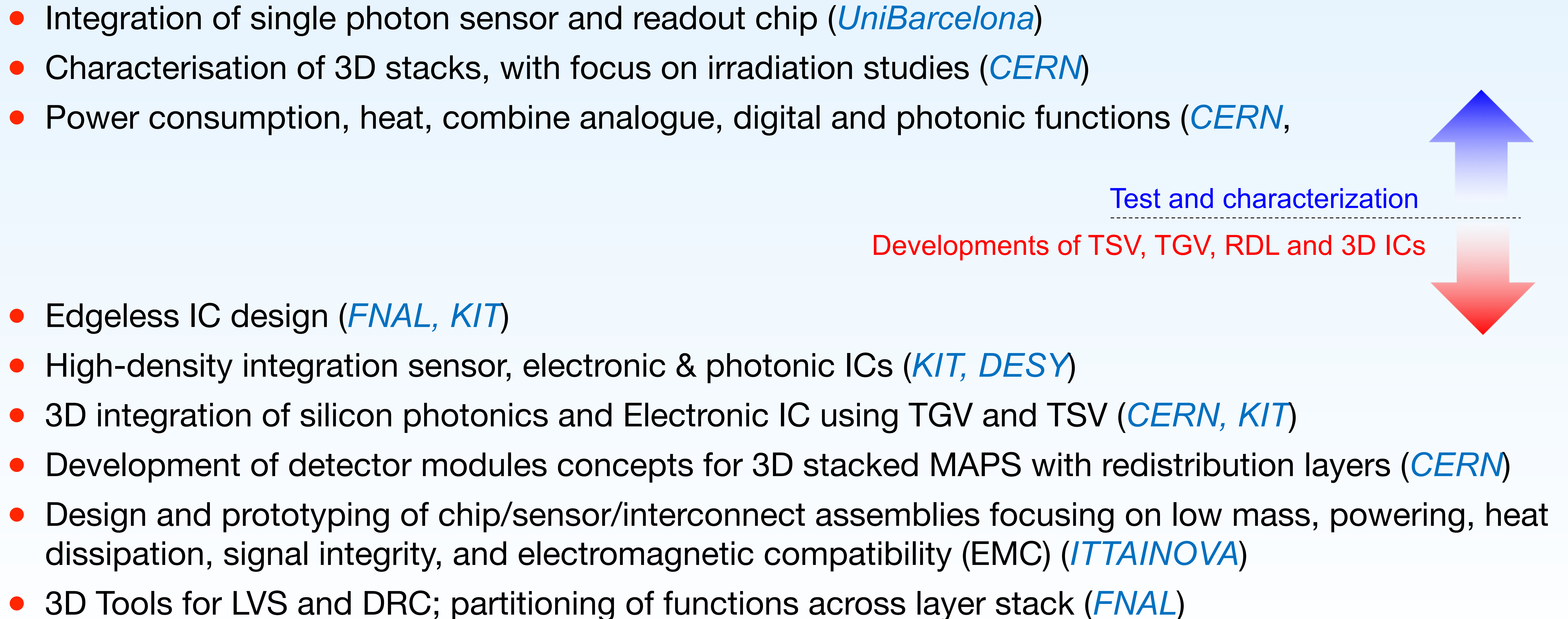
3D integration & high density interc. (5)

ECFA
European Committee for Future Accelerators

DRDT 7.5
Emerging Technologies

Please describe the topics you (and/or your group) would like to participate in?

- Integration of single photon sensor and readout chip (*UniBarcelona*)
- Characterisation of 3D stacks, with focus on irradiation studies (*CERN*)
- Power consumption, heat, combine analogue, digital and photonic functions (*CERN*,

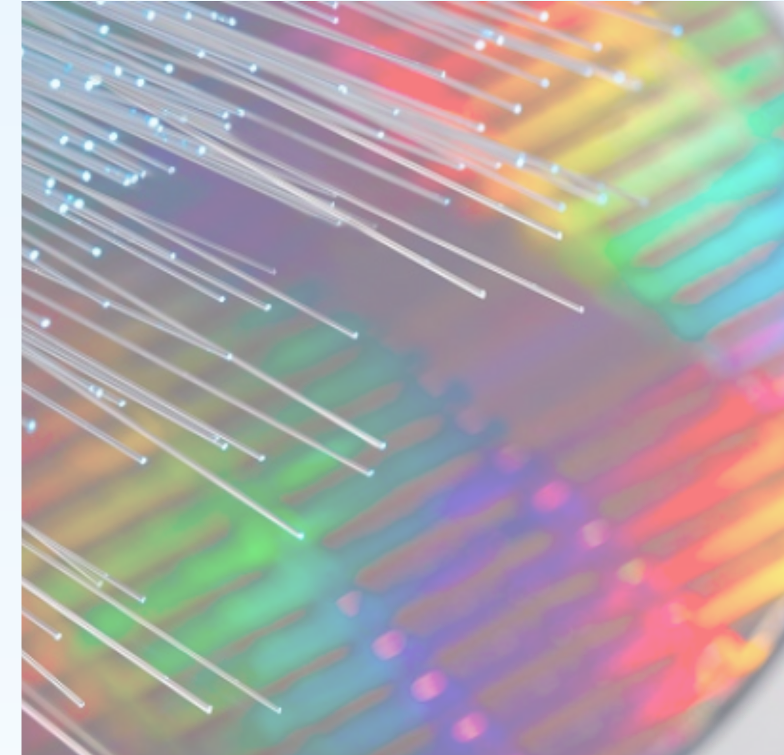


- Edgeless IC design (*FNAL, KIT*)
- High-density integration sensor, electronic & photonic ICs (*KIT, DESY*)
- 3D integration of silicon photonics and Electronic IC using TGV and TSV (*CERN, KIT*)
- Development of detector modules concepts for 3D stacked MAPS with redistribution layers (*CERN*)
- Design and prototyping of chip/sensor/interconnect assemblies focusing on low mass, powering, heat dissipation, signal integrity, and electromagnetic compatibility (EMC) (*ITTAINOVA*)
- 3D Tools for LVS and DRC; partitioning of functions across layer stack (*FNAL*)

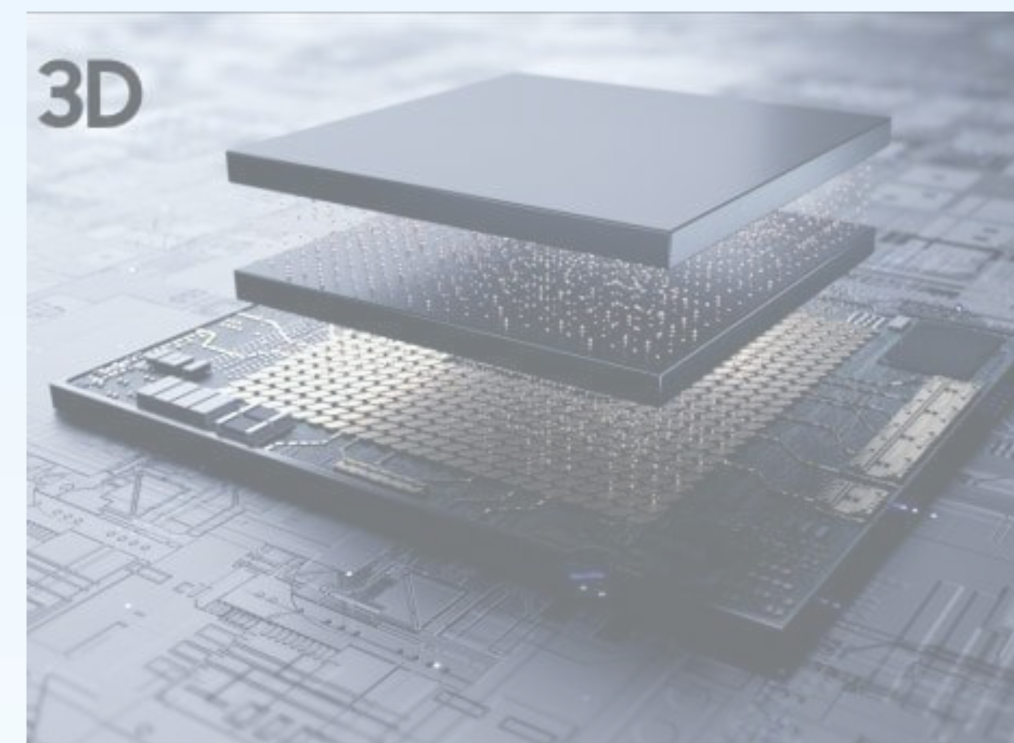
DRDT 7.5 Emerging Technologies

Novel microelectronic technologies, devices, materials

Silicon Photonics

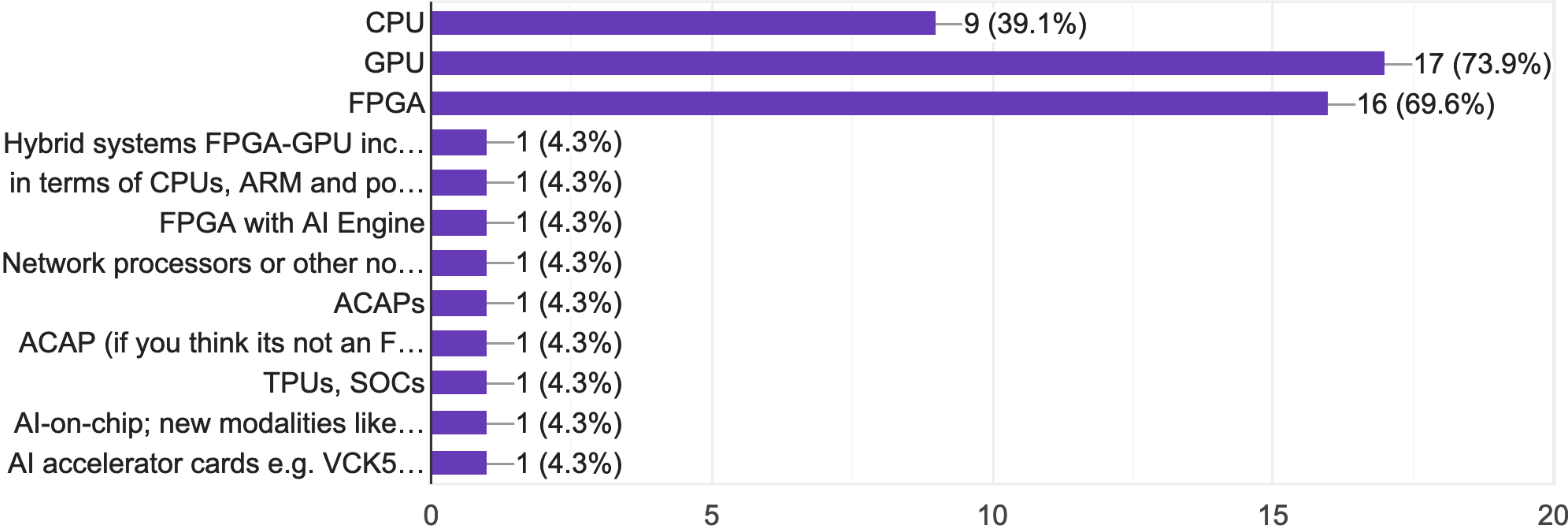


3D integration and high density interconnects



Keeping pace with, adapting, and interfacing with COTS

Keeping pace with, adapting, and interfacing with COTS



jan.troska@cern.ch

What should be studied to find the most efficient (in terms of cost and/or power) technology?

- TCO based on end-to-end physics and computational needs of concrete workflows
- HLS (e.g. SYCL) for complex algos on FPGAs, integration with classical HDL
- ML/AI inference for tracks and clusters
- Power consumption, latency
- How to build disaggregated systems with easily scalable amount of various processing elements
- Find optimal mix of technologies at each stage. FPGA on- or near- detector for localised processing (clusters, calorimeter objects) and GPU for global off-detector seems like the cost-effective mix now

jan.troska@cern.ch

Where do you see the main software challenges?

- Effectively exploiting specialised silicon (e.g. TensorCores on GPUs but this is a widespread phenomenon). Specialised languages?
- C++ less fashionable than 20 years ago
- Long-term maintenance of heterogeneous code in an environment which combined high staff turnover, a funding model which makes talent retention difficult, and difficulties in recruiting already-skilled talent (i.e. typical developers start as untrained students and leave once trained).
- Getting reliable data out of AI systems
- Reception path of fast streaming systems - drivers, efficient software for data storage
- Good benchmarks / decision criteria to decide between technologies (TCO)
- Get simulation code(s) efficiently running on a maximum variety of compute technologies (GPU, various CPUs)

jan.troska@cern.ch

Which device types (FPGA, SoC, Processor) will form the basis for future off-detector electronics?

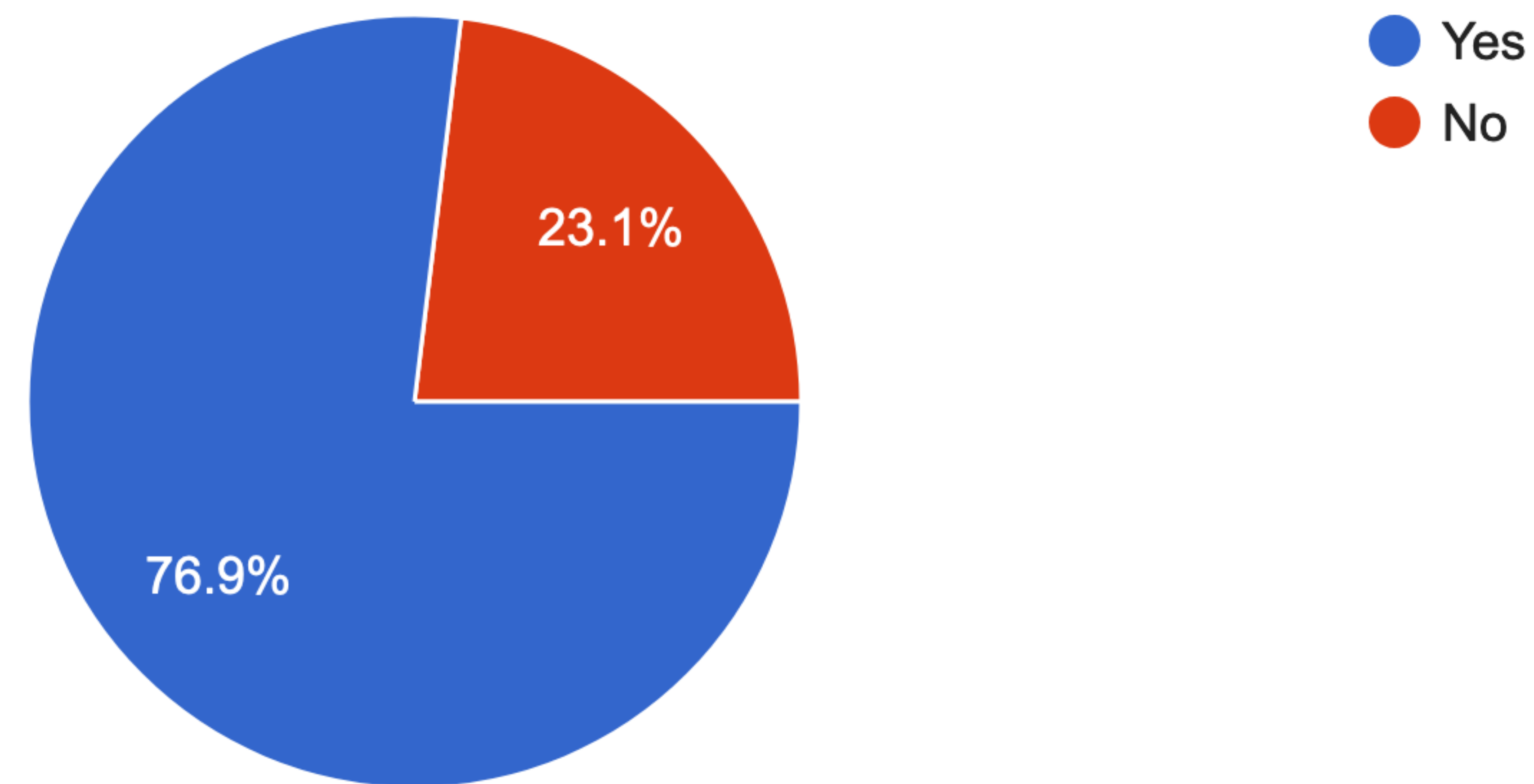
- Split evenly between FPGA and GPGPU or a combination of both
- FPGAs most often paired with SoC
- FPGA is in particular thought to be needed to terminate custom front-end protocols

jan.troska@cern.ch

Interest in futher research & collaboration

Are you (and/or is your group) interested in investigating COTS components for compute acceleration, detector readout and/or trigger system?

26 responses



jan.troska@cern.ch

Research topics (20 answers!)

- Cross-architecture / heterogeneous framework
- Tracking on FPGAs with and w/o HLS
- ML/AI for tracking / triggering / on FPGAs and/or GPUs
- FPGAs for networking (Ethernet)
- Networking protocols for DAQ / readout Ethernet (70%), InfiniBand (30%),
- VL+ to Ethernet translator (PCIe based), Ethernet from the front-end (asymmetric)

jan.troska@cern.ch

Keeping pace with COTS

ECFA
European Committee for Future Accelerators

DRDT 7.5
Emerging Technologies

- Survey highlights changing trends: CPU distant second to FPGA + GPU
  - SoC mentioned more than once as well. Would be interesting to understand use cases better

- Granularity issue: ‘On detector, Off detector and Near detector’
  - Survey answers don’t capture this, requirements and costs are very different in each location
  - Could imagine that off-detector technologies are less constrained beyond **total cost of ownership -** mentioned by several respondents.
  - This could be a metric to follow for emerging off-detector technologies: Think eg: ‘HEPSPEC/ HEPSCORE for DAQ’

- Adapting to emerging technologies means there has to be a mechanism to access them, availability of people to learn new tools, and/or availability of cross-architecture tools.
  - HLS + SYCL were noted as a trend to follow closely.