Progress of Silicon Tracker for the CEPC

Yiming Li
on behalf of the CEPC Silicon Tracker Group

IAS Program on High Energy Physics (HEP 2023)
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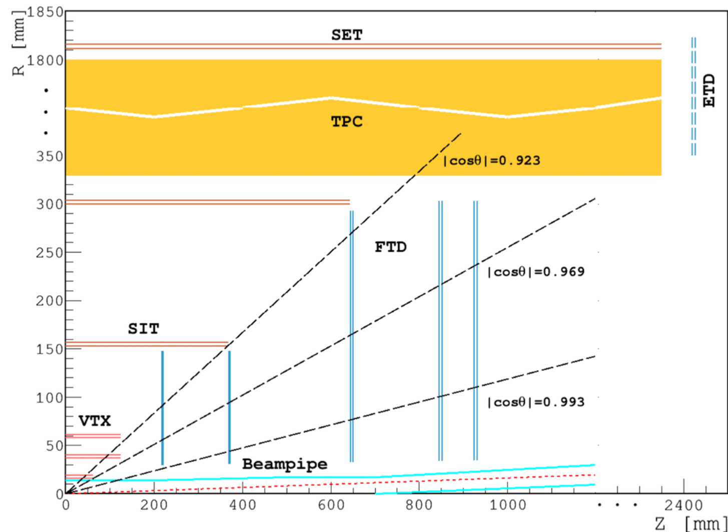
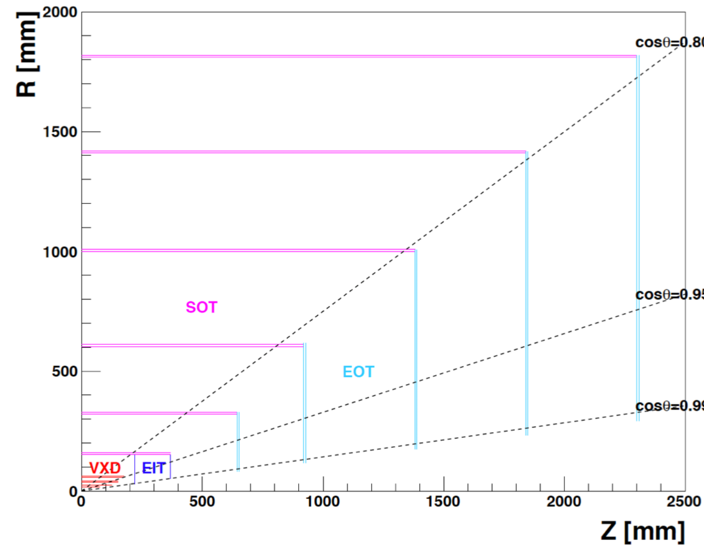
Introduction

- CEPC requires a high-resolution and low-material tracking system
- Large area of silicon!
  - > 70 m^2 for baseline design: Silicon + TPC
  - ~ 140 m^2 for Full Silicon Tracker
- CMOS is the promising technology for cost effectiveness and performance



Baseline design



Full Silicon Tracker

$$\sigma_{1/p_T} = a \oplus \frac{b}{p \sin^{3/2}\theta} \quad [\mathrm{GeV}^{-1}]$$

$a \sim 2 \times 10^{-5}\ \mathrm{GeV}^{-1}$

$b \sim 1 \times 10^{-3}$

CMOS Tracker Collaborators

- Australia
  - University of Adelaide
- China
  - Harbin Institute of Technology
  - Hunan University
  - Institute of High Energy Physics, CAS
  - Northwestern Polytechnical University
  - Shandong University
  - T. D. Lee Institute – Shanghai Jiao Tong University
  - University of Science and Technology of China
  - University of South China
  - Zhejiang University
- Germany
  - Karlsruhe Institute für Technologie
- Italy
  - INFN Sezione di Milano, Università degli Studi di Milano e Università degli Studi dell' Insubria
  - INFN Sezione die Pisa e Università di Pisa
  - INFN Sezione di Torino e Università degli Studi di Torino
- UK
  - Lancaster University
  - Queen Mary University of London
  - STFC – Daresbury Laboratory
  - STFC – Rutherford Appleton Laboratory
  - University of Bristol
  - University of Edinburg
  - University of Liverpool
  - University of Oxford
  - University of Sheffield
  - University of Warwick

HVCMOS sensors

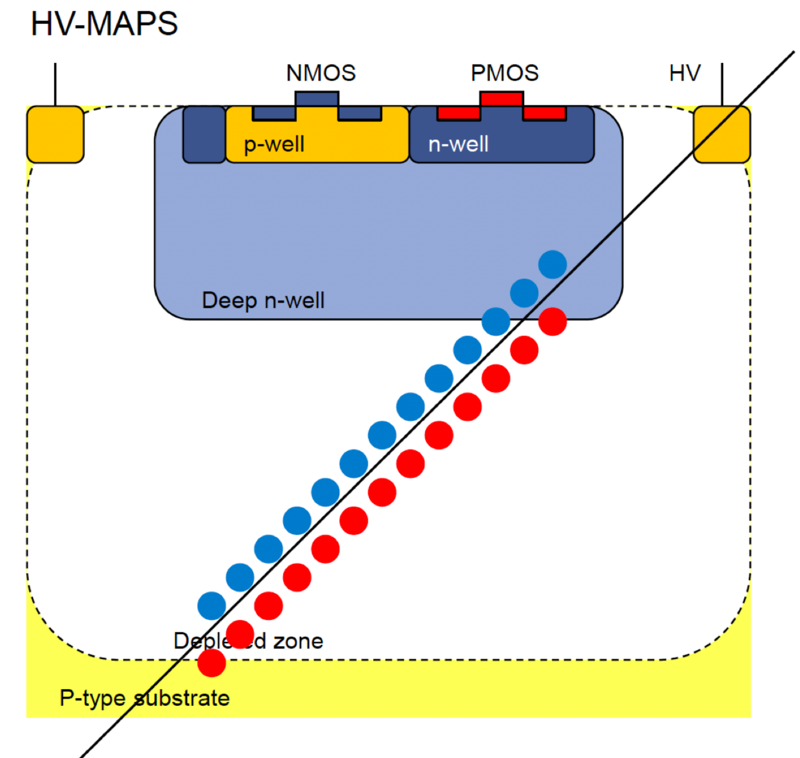
- HVCMOS sensors features large charge collection electrode encapsulating pixel electronics

- Achieving HV bias (> 50 V) without process modification

=> Cost-effective solution for large area detectors

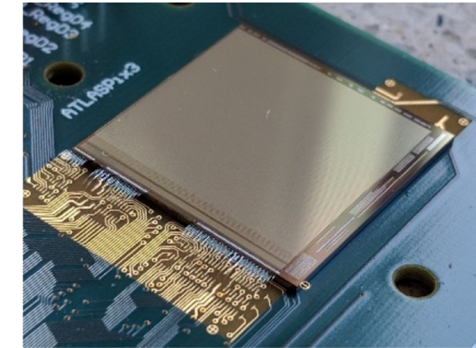
- Intrinsic radiation hardness
  - Verified by radiation tests up to 10^{15} n_{eq}/cm^2

- Large capacitance due to the large electrode
  - Causing increased noise and power consumption



A sensor candidate: ATLASPix3

- ATLASPix3 features
  - TSI 180nm HV process on 200 Ωcm substrate
  - Pixel size 50 × 150 μm^2
  - 132 columns × 372 rows (20.2 × 21 mm^2 chip)
  - Each pixel has 7-bit TOT + 10-bit timestamp
  - Continuous / triggered readout with 8b10b / 64b66b coding
  - Power consumption ~160 mW/cm^2.



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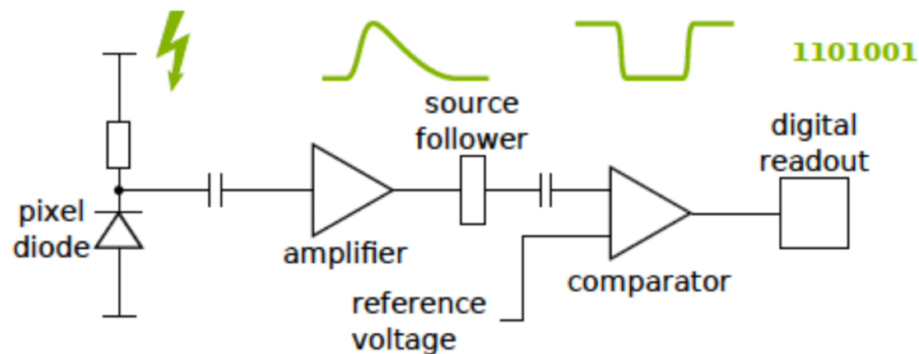
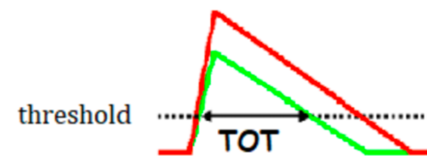
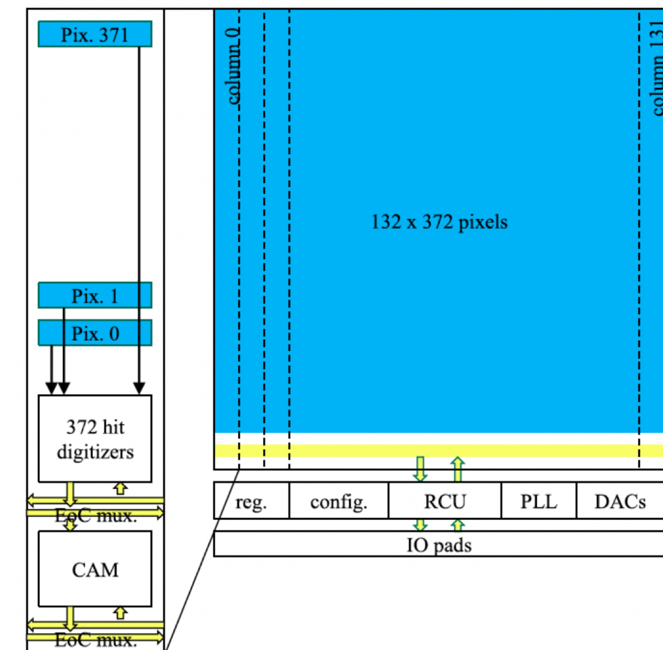


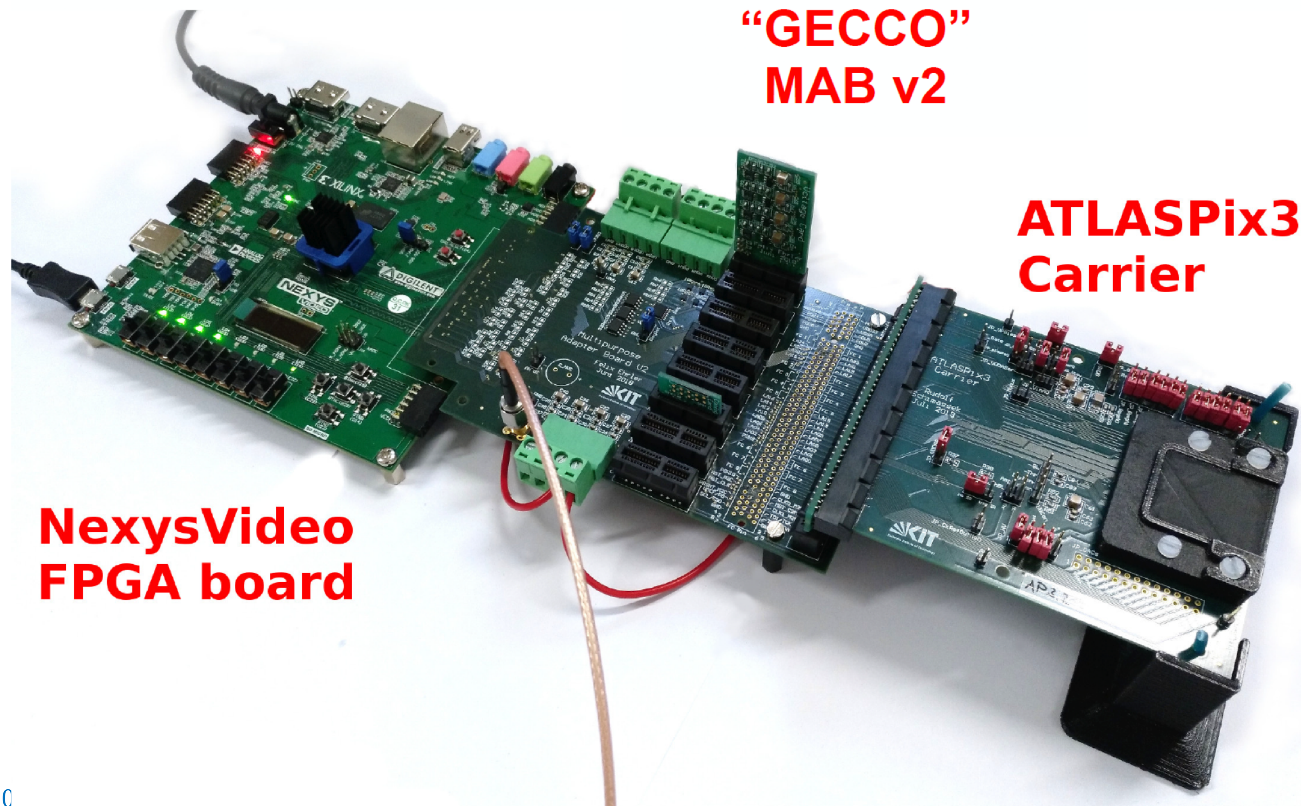


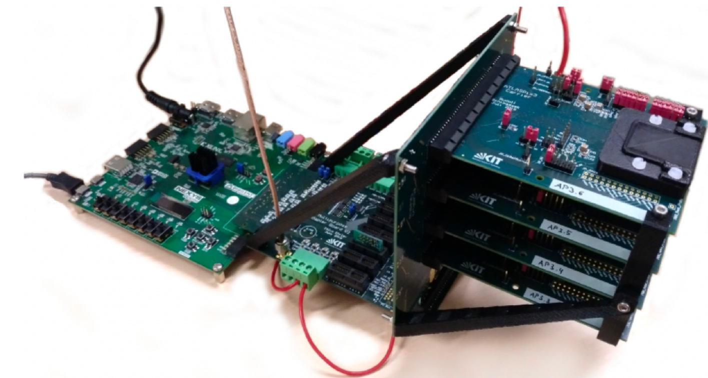
Time-Over-Threshold:
proxy of signal amplitude



Readout system

- GEneric Configuration and COntrol System
  - Versatile system for different applications designed at KIT
  - LFP-FMC connection to Nexys FPGA, PCIe x16 to DUT, allows extensive tests
  - Configurations: Single-board; Telescope; Quad



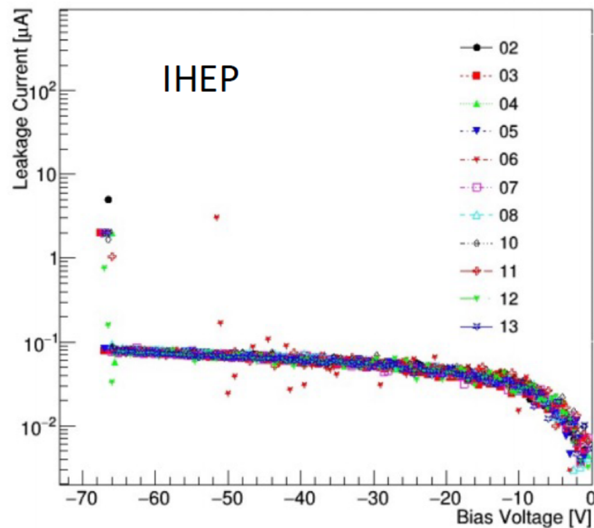


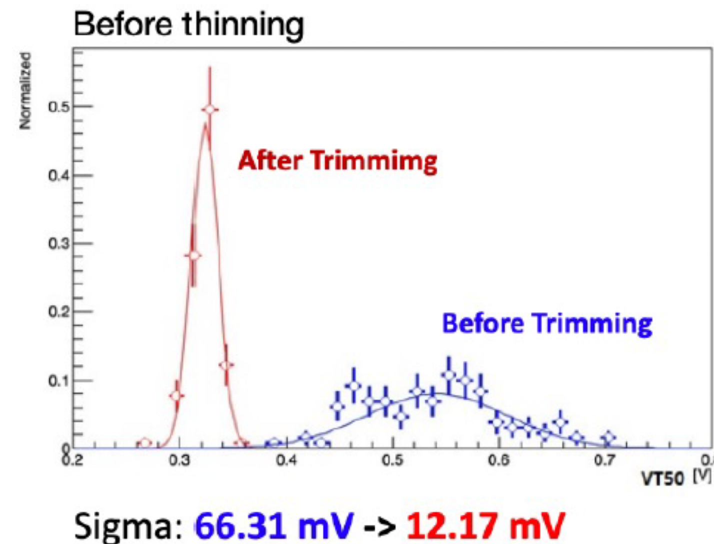
Telescope

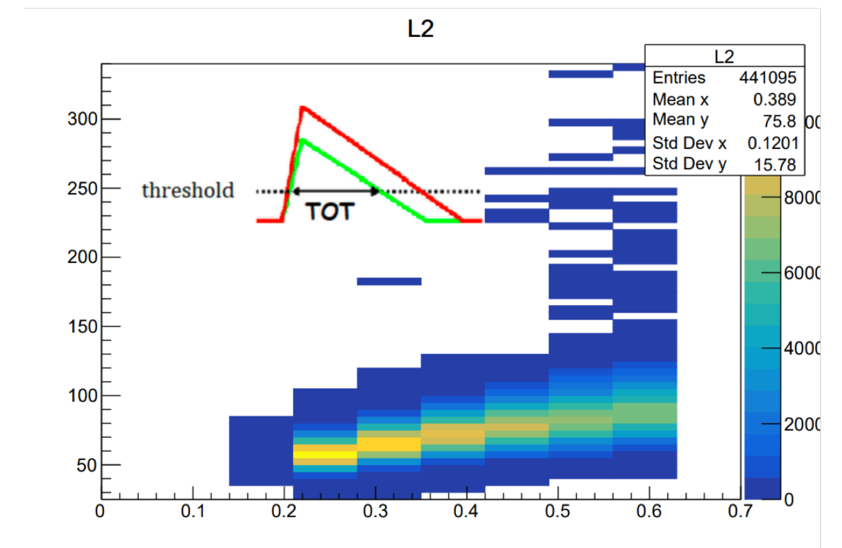
Single-board

ATLASPix3 tests

- IV scan confirms sensor electrical characteristics: breakdown up to 60V
- The 3-bit TDAC in pixel allows tuning threshold for each pixel to gain homogenous response across sensor array (Trimming)
- ToT: a measure of deposited energy; calibration needed due to non-linearity





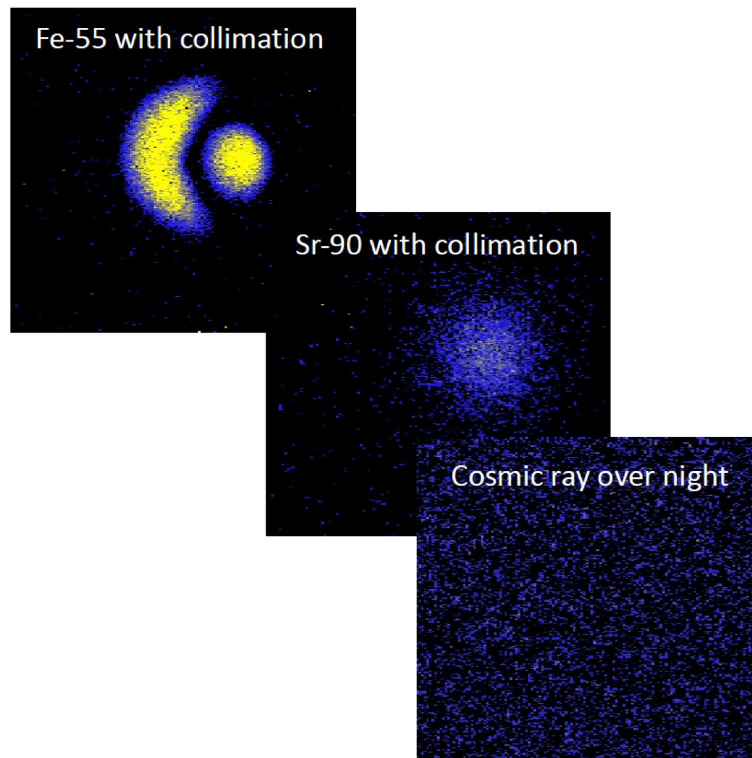


Noise ~60 e-
For threshold ~1700 e-

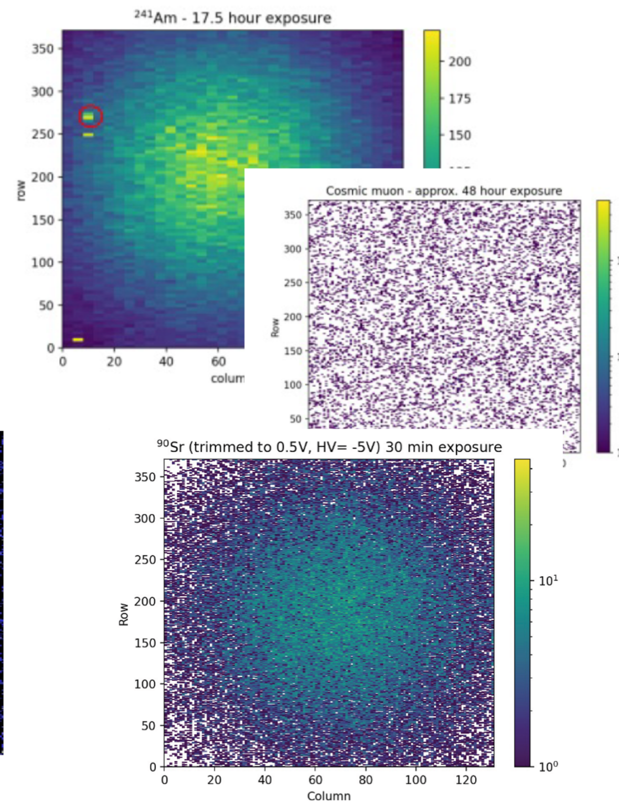
ATLASPix3 tests with radioactive sources

- ATLASPix3 responses to cosmic ray or various radioactive sources are observed at different sites

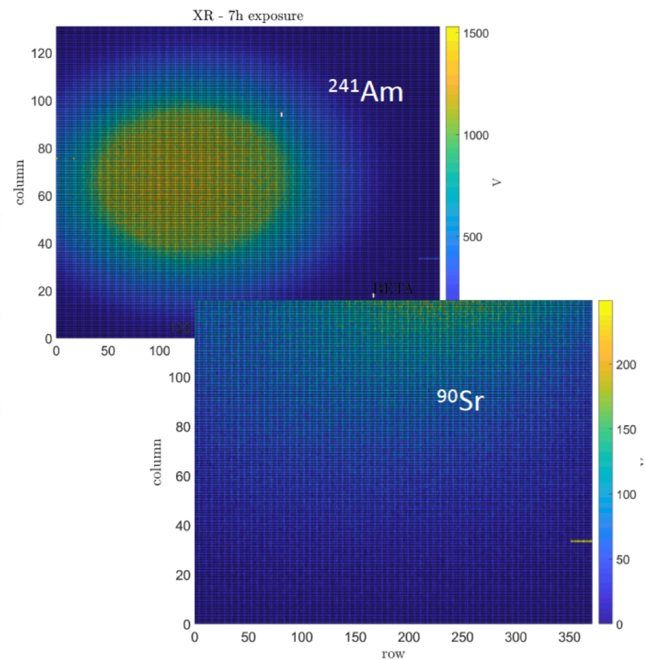
IHEP



Edinburgh/Bristol/Lancaster

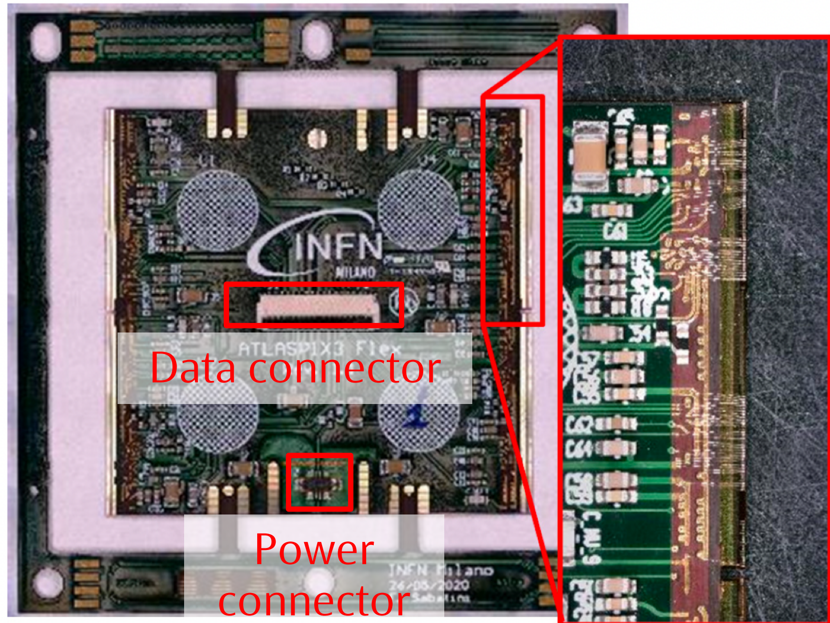


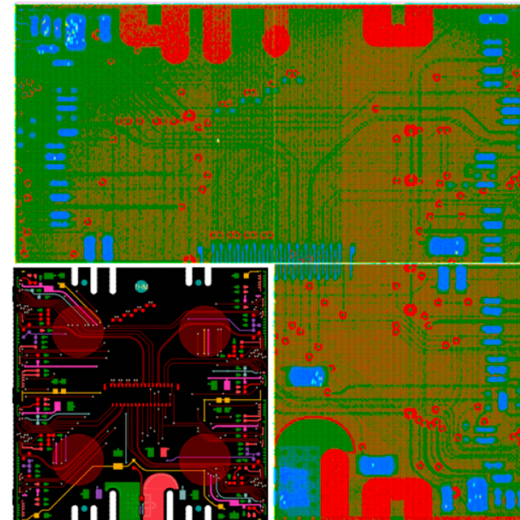
Milano



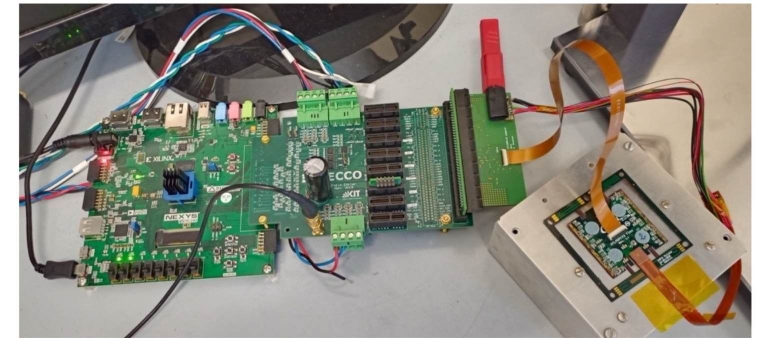
Quad module

- Readout unit based on 4 ATLASPix3 chips with common power and data readout
- Flex designed, assembled and tested by INFN Milan
  - Shared service by common power connections and configuration lines
- Readout using GECCO system with dedicated adapter card and data flex





X-ray scan
5 min with 15k-34k hits/s

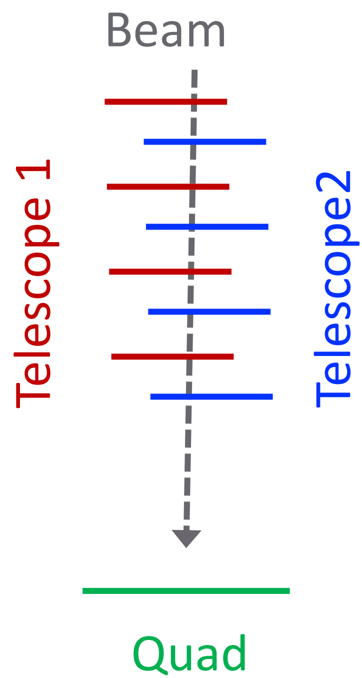


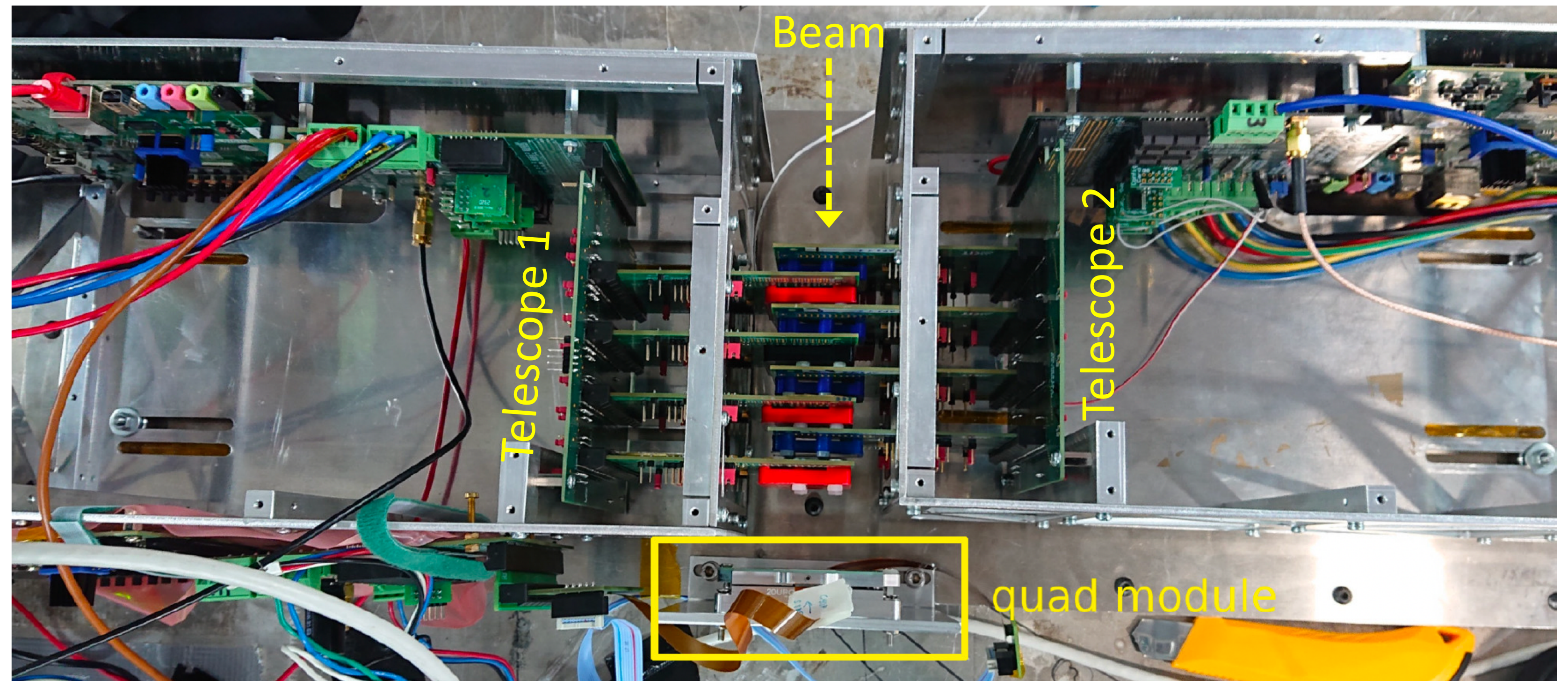
Test setup with GECCO

Beam test

- Testbeam at DESY in April 2022 using electron beam up to 6 GeV
  - Two standalone telescope systems in interleaved configuration
  - Each equipped with 4 chips
  - Quad module located downstream

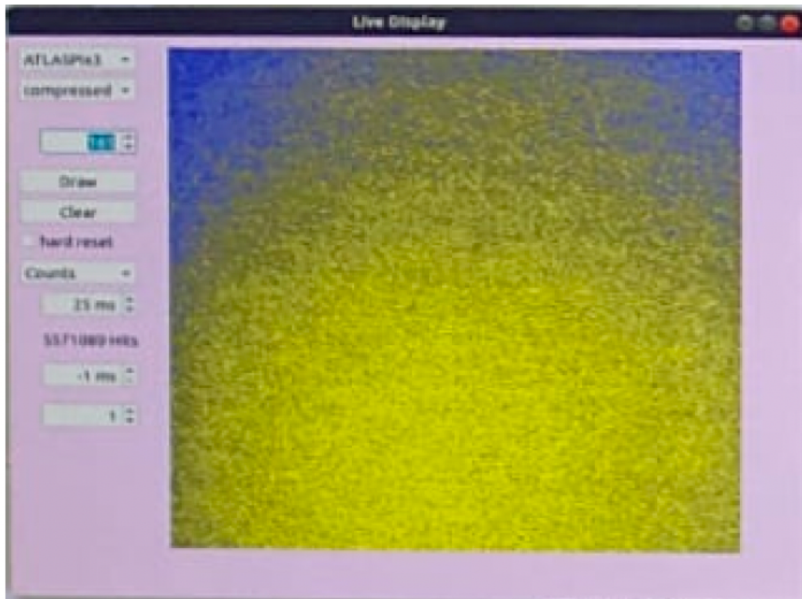
L.Meng @ VERTEX2022
R. Zanzottera, E. Hutchinson @Pixel2022



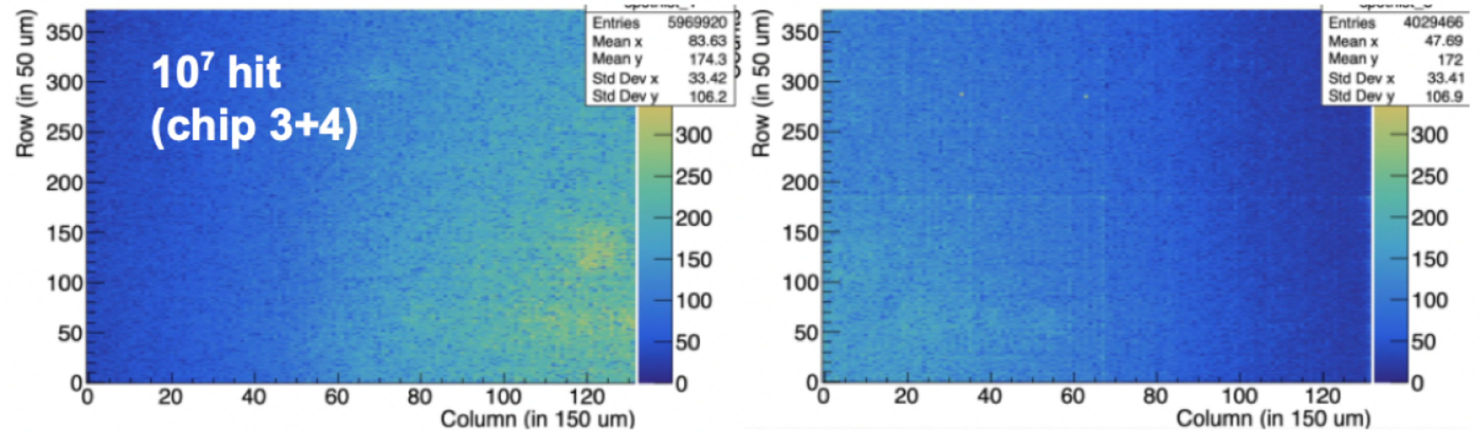


Hitmap

- Both telescopes and the quad response to the beam



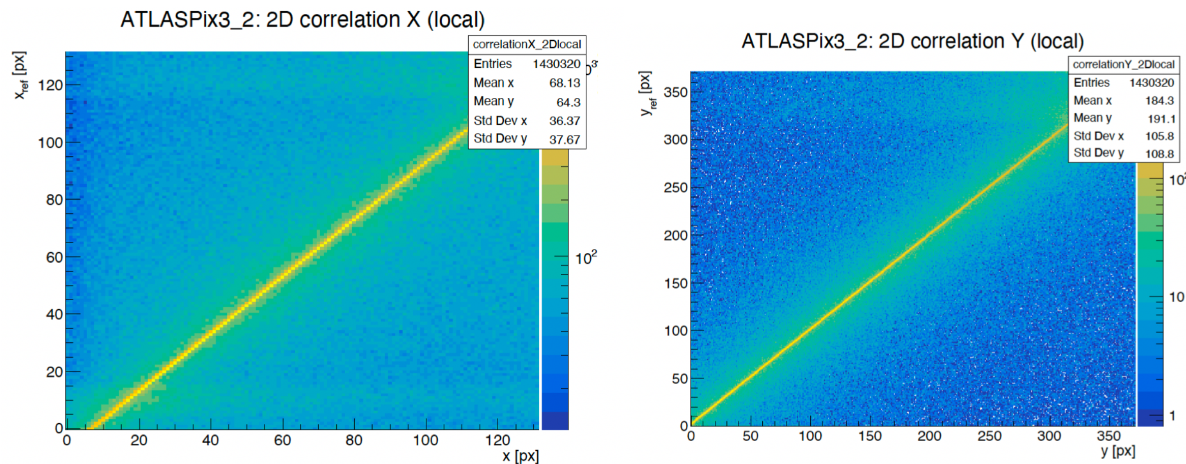
Event display of all layers



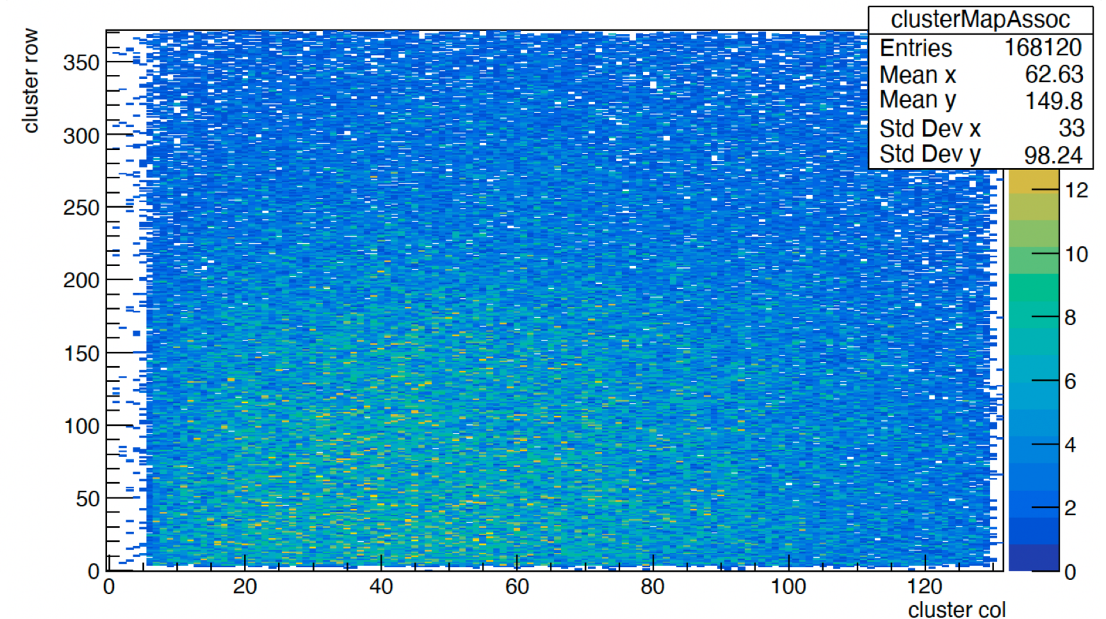
Hitmap for two chips in the quad

Track reconstruction

- Track reconstruction using Corryvreckan
- Use 3 telescope layers (L1, L2, L4) for track iterative alignment and L3 as DUT
- Preliminary results from one telescope using a long run at 6 GeV, bias at 50 V



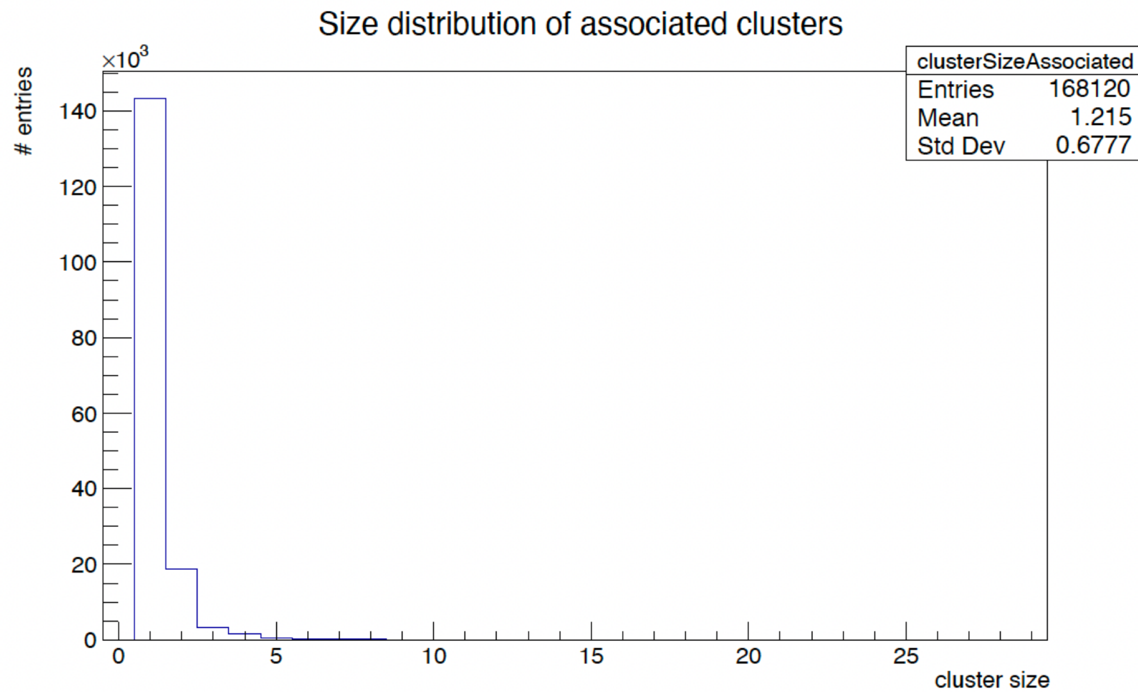
Correlation of L2 with respect to L1 in X and Y

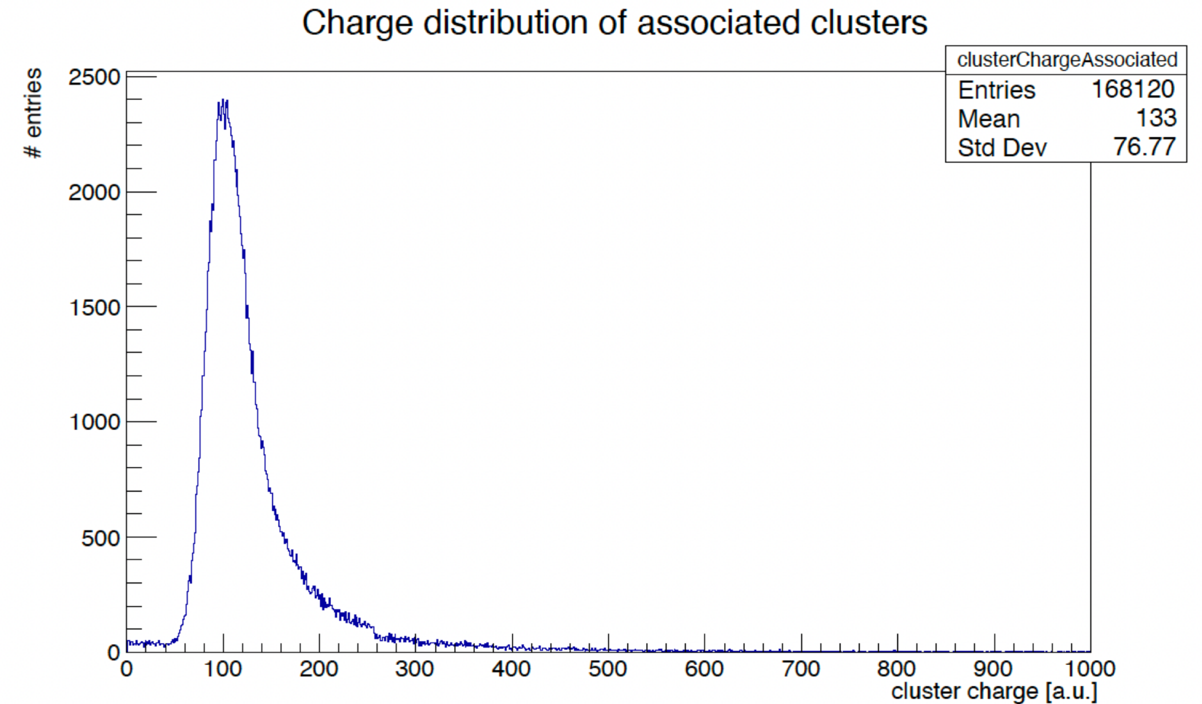


Map of associated clusters in DUT plane

Cluster size and charge

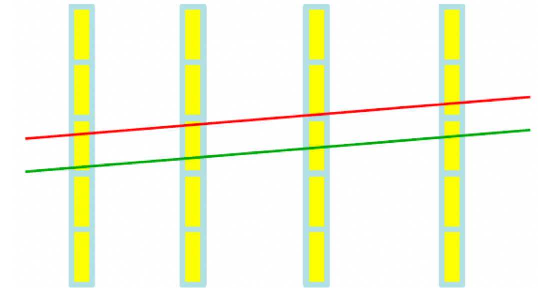
- Dominated by single-pixel cluster – expected given the pixel size
- Charge of clusters associated with tracks follow Landau distribution

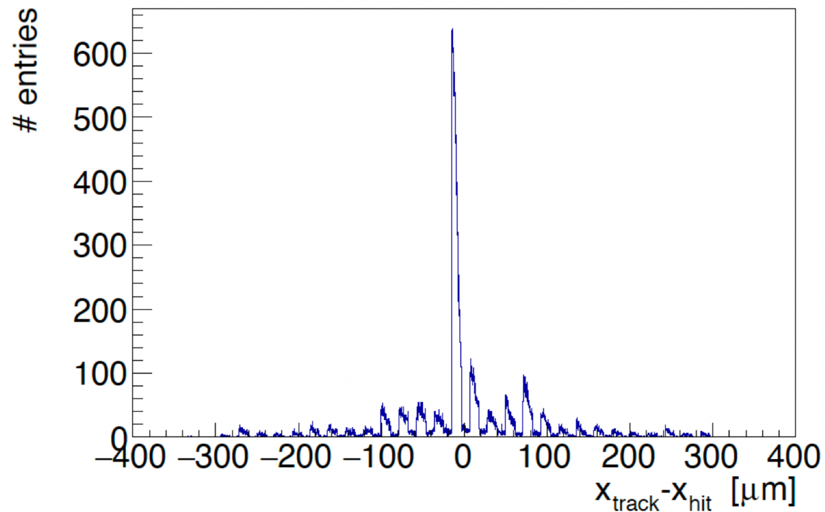


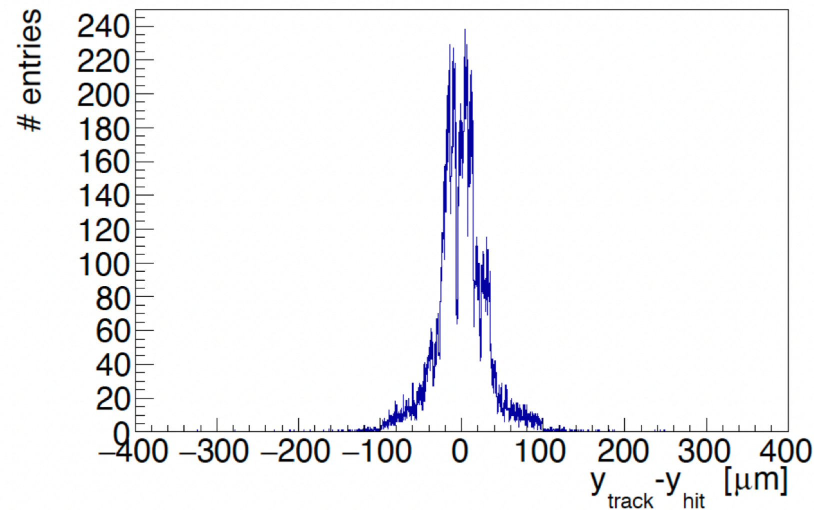


Residuals

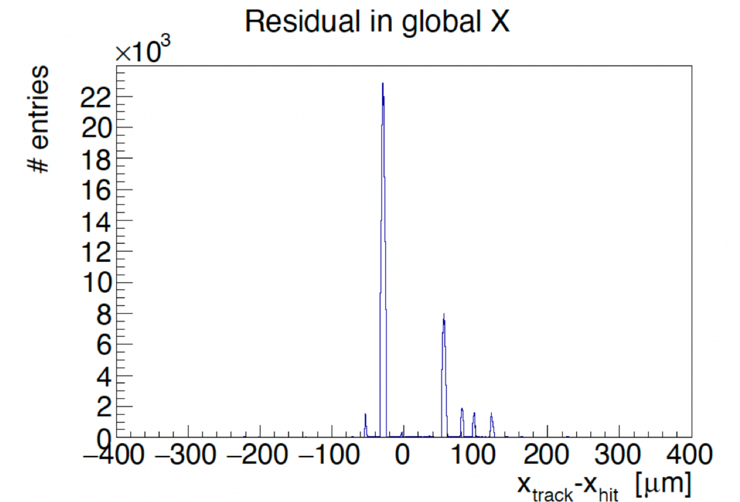
- Peaks in residual distributions (defined as $x_{track} - x_{hit}$ in DUT)
- Due to large pixel size and single-pixel clusters in telescope planes
- Verified by AllPix^2 simulation







Simulation:

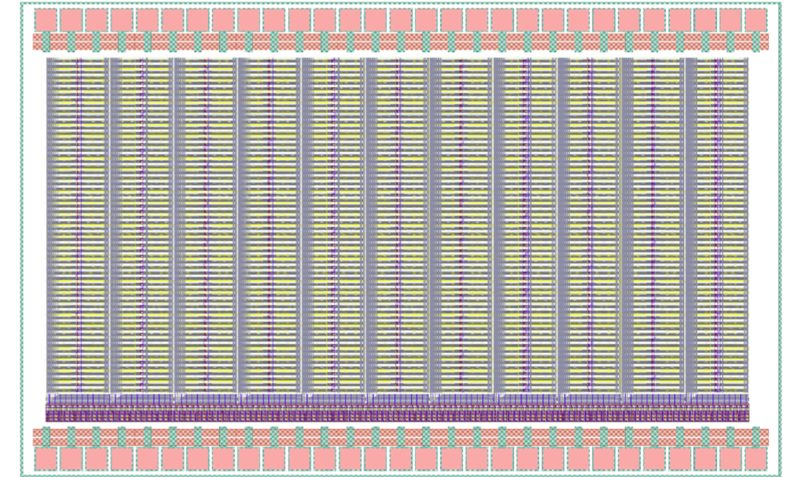


Sensor development

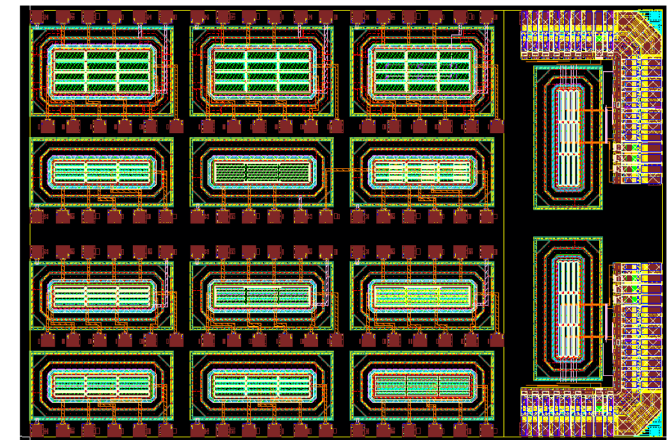
- ATLASPix was developed with TSI 180nm HV process, new sensor development for CEPC should be pursued
  - Smaller pitch, lower power consumption, lower noise ⋯
- CEPCPix
  - Smaller pixel size in $r\phi$: 50 μm → 25 μm
  - Low-power amplifiers and comparators
  - Daisy chain of readout reduces number of data links in case of low occupancy
  - Submitted in 2022 together with LHCb

Sensor development

- Attempts to explore alternative foundries
- HLMC 55nm HV CMOS process
  - Seeking MPW opportunity
  - Caveat: not supporting high-resistivity wafer
- SMIC 55nm CMOS processes
  - Possible to use high-resistance wafer
  - MPW submitted with Low-Leakage process in Oct 2022 with simple design of passive diodes and a few amplifiers
  - Seeking MPW opportunity using HV process and high resistance
- ARCADIA: 110nm CMOS at LFoundry
  - Main demonstrator ARCADIA-MD1 tested; MD2 submitted



Test matrix for HLMC MPW (KIT)



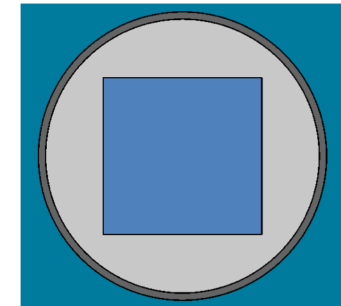
Floorplan for SMIC LL MPW (IHEP, HNU, ZJU)

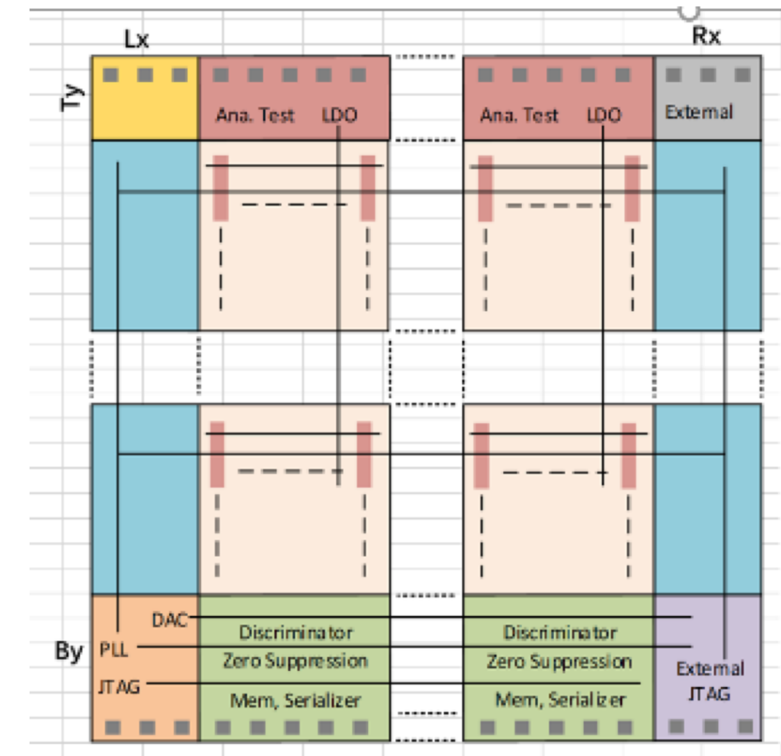
Sensor development

- Development of wafer scale CMOS pixel sensor (SDU, IHEP, HIT, DLMU)

- XFAB 350nm CIS process with stitching technique and high-resistivity wafer

- First design finished and to be submitted in Feb 2023
  - Wafer-scale sensor: ~ 11 × 11 cm^2
  - Pixel matrix: 644 × 3600
    - 92 rows × 600 columns per reticle
  - Full function integrated:
    - Analogue pixel matrix
    - Column-level discriminator
    - On-chip zero-suppression
    - Other periphery blocks: Bias DAC/Buffers/I2C/PLL/LVDS/LDO⋯

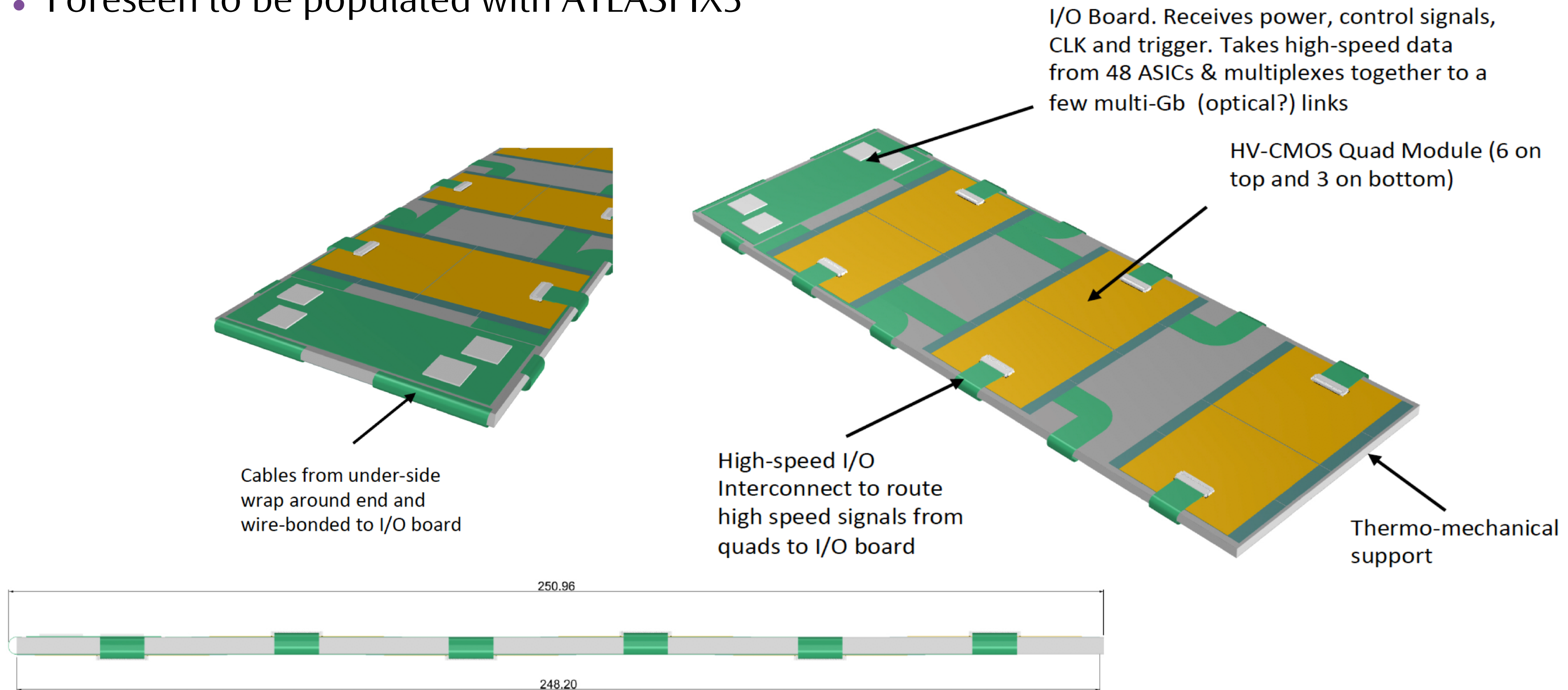




Floorplan of the first wafer-scale sensor

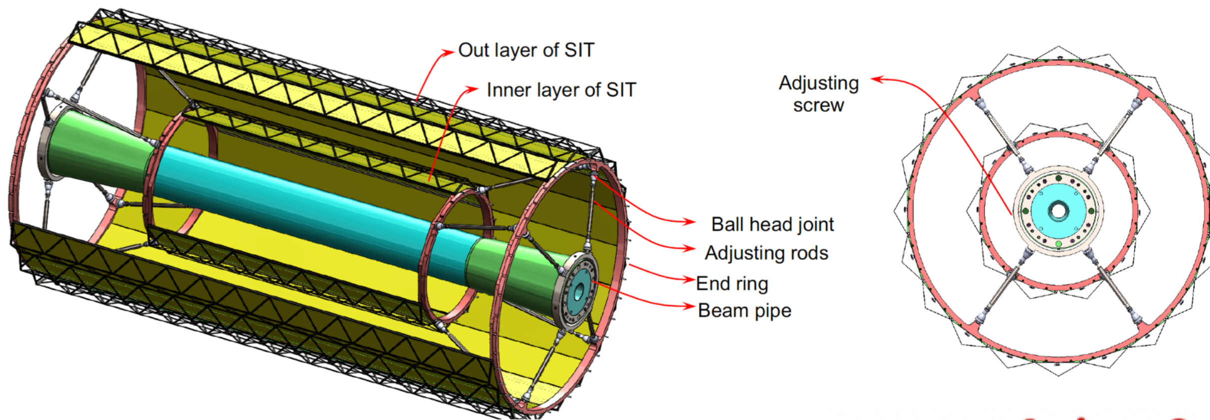
From quad to stave demonstrator

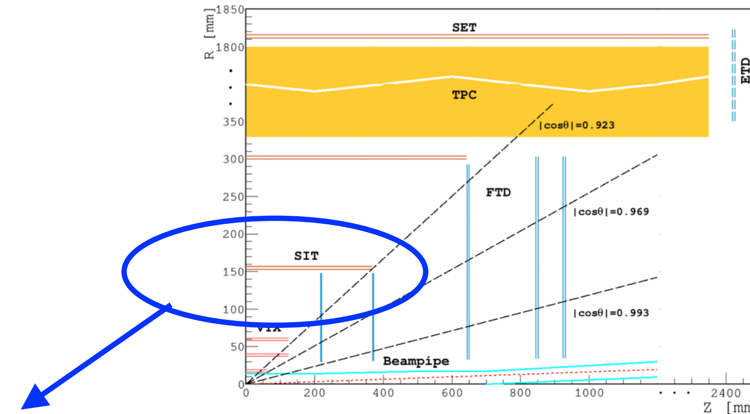
- A stavelet demonstrator with 12 quad modules under development
  - Aggregation of data + optical conversion at end-of-stave; serial powering
  - Foreseen to be populated with ATLASPIX3



Mechanical design

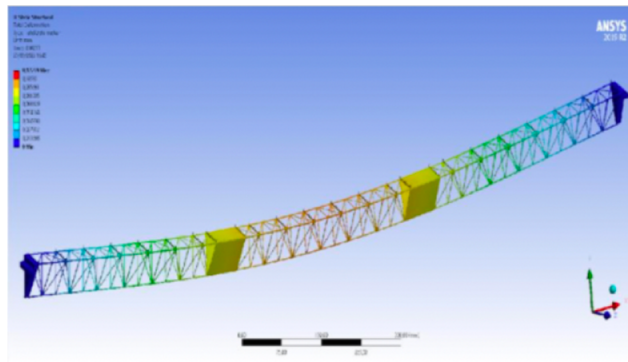
- Design target: 0.65% X_0 for stave + modules
- CDR baseline design: 2 SIT layers
  - Stave concept: truss structure with cold plate





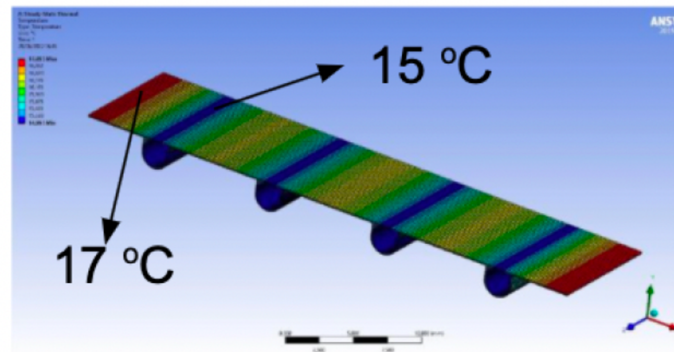
Similar to staves of ALICE Outer Barrel (0.8% X_0)

R. Zanzottera, @Pixel2022

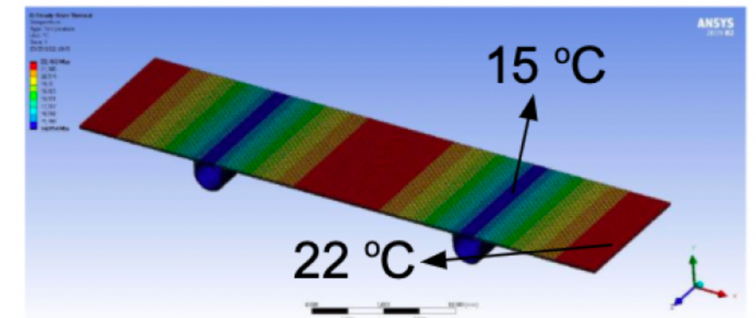


Simulation of truss rigidity

4 pipes 0.4% X_0



2 pipes 0.3% X_0



Thermal simulation for 2 vs. 4 cooling pipes

Summary

- CMOS-based silicon tracker is a promising solution for CEPC

- Development and prototyping have been progressing mostly using ATLASPix3 sensors
  - The first beam test with ATLASPix3 telescope performed at DESY
  - R&D on HVCMOS pursued at various foundries
  - Stavelet demonstrator and mechanical design in progress

- Your participation is welcome