CMS HCAL upgrade and its electronics

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for the CMS HCAL collaboration

PH/ESE group seminar
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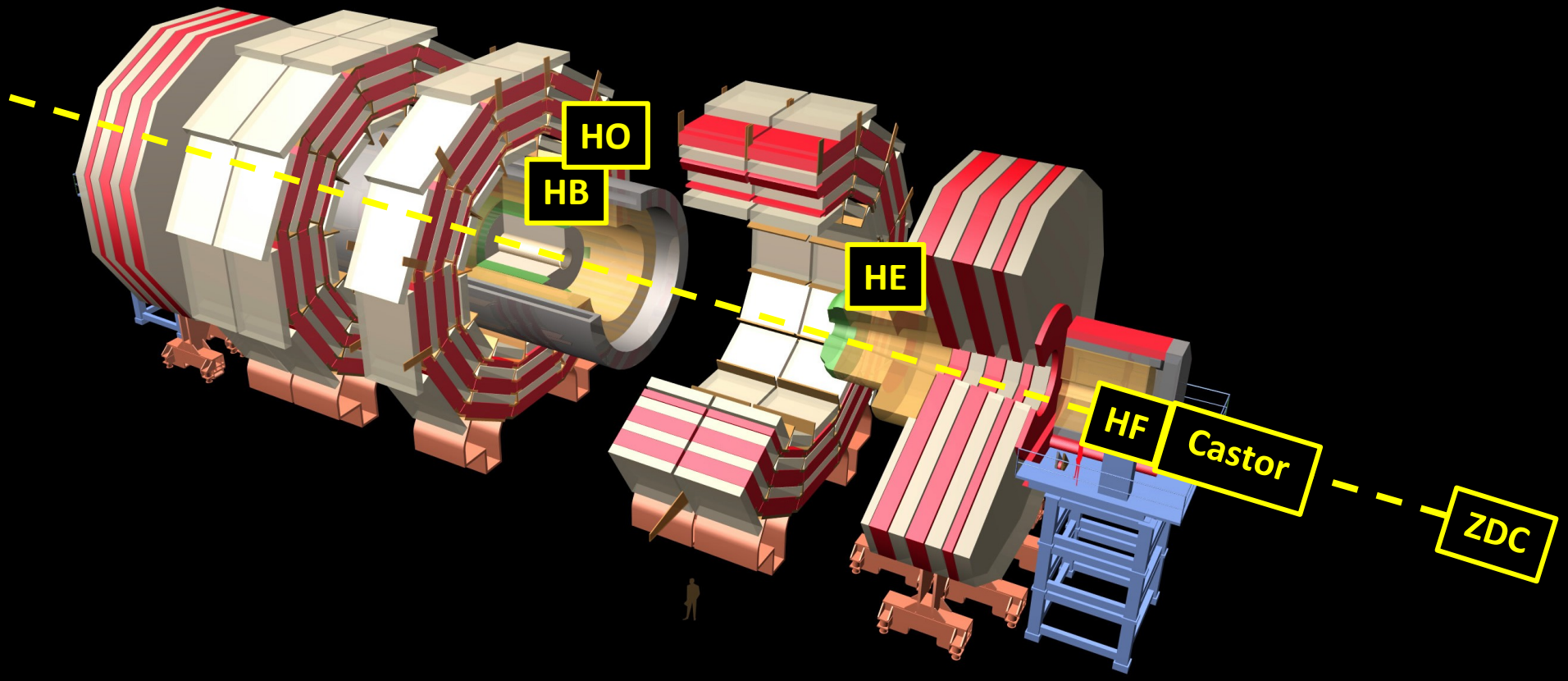
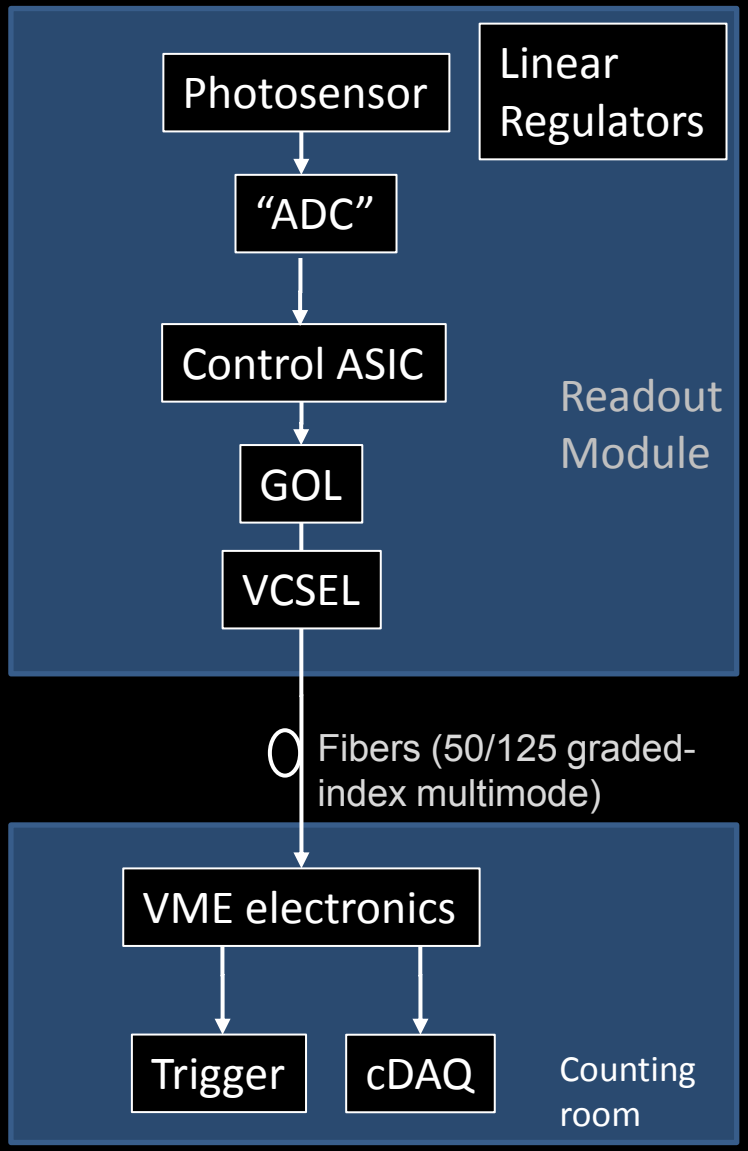
Existing CMS “HCAL”

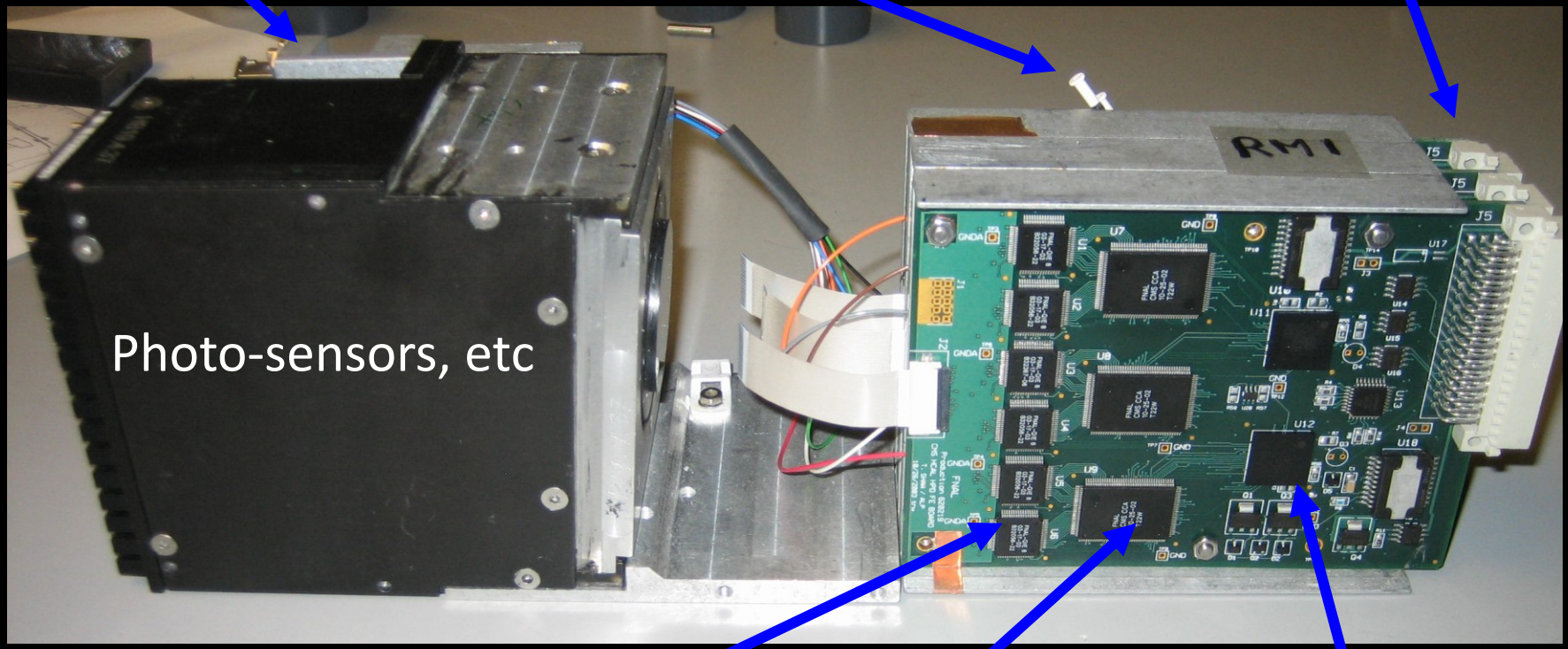


- Electronics built in year ~2004
- ~6000 channels from Hybrid photo-diodes (HPDs), on HB, HE and HO
- ~3000 channels from Photo-Multipliers Tubes (PMTs), on HF, Castor and ZDC
- Measure the energy deposition with a dynamic range ratio = 10000.
  In HF the range is (1 fC; 10000 fC) with a noise RMS < 0.5 fC.
- Full readout every 25 ns
- Generate trigger data in the counting room, keeping the time-alignment

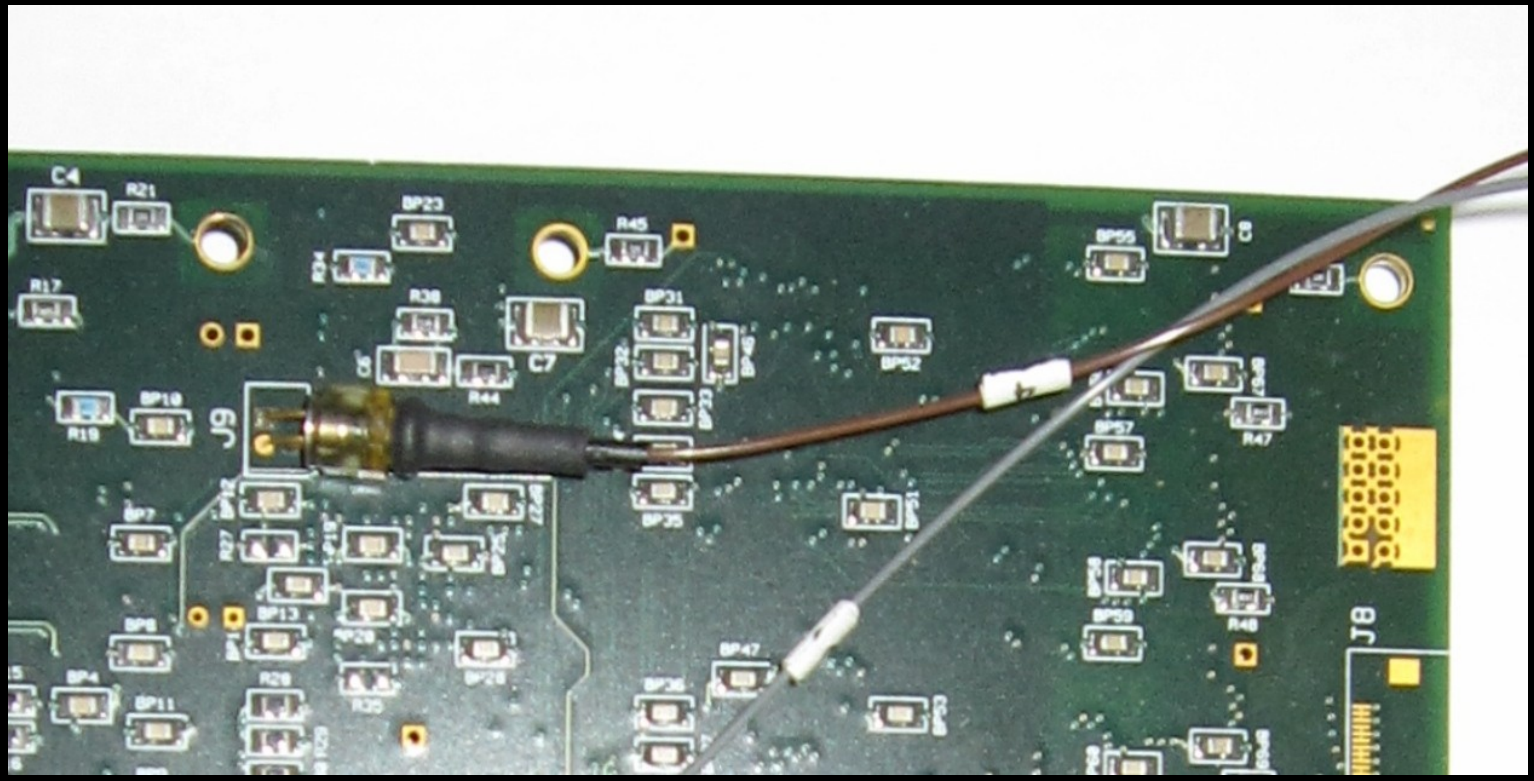
Data-path in the present HCAL



Existing Readout Module (RM)



Rear-side of a readout card: connection of individual fibers



A heat shrinking tube holds the fiber in place → limited volume.
No major problems has been observed in the existing readout electronics.

Upgrade: Motivations

Physics: not covered in this presentation.

Problems of the existing system:

- Obsolescence of electronics built in 2004
- HPD: discharge; ion-feedback → burst noise
- PMT: hit on the glass window; hit on fibers (input of PMTs) → burst noise
- Occasional problems in the control path

Improvements:

- Replace HPDs with SiPMs
- Replace PMTs with multi-anode, “thin-glass” PMTs
- Separate readout of anodes of PMT
- HB, HE have 16 depths, processed together → separate readout
- Extend the dynamic range of the analog-to-digital conversion
- Add TDC capabilities, in order to separate burst noise from physics signal
- Faster, more reliable control path

Upgrade: Overview

Requirements:

- support new photo-sensors
- increase the dynamic range by a factor of 10
- increase the number of channels by a factor of 3 or 4
- add timing information (TDC)

Installation and commissioning of Front-End electronics:

- HB and HE: during a long shutdown after 2015
- HF: during a ~3 months technical stop

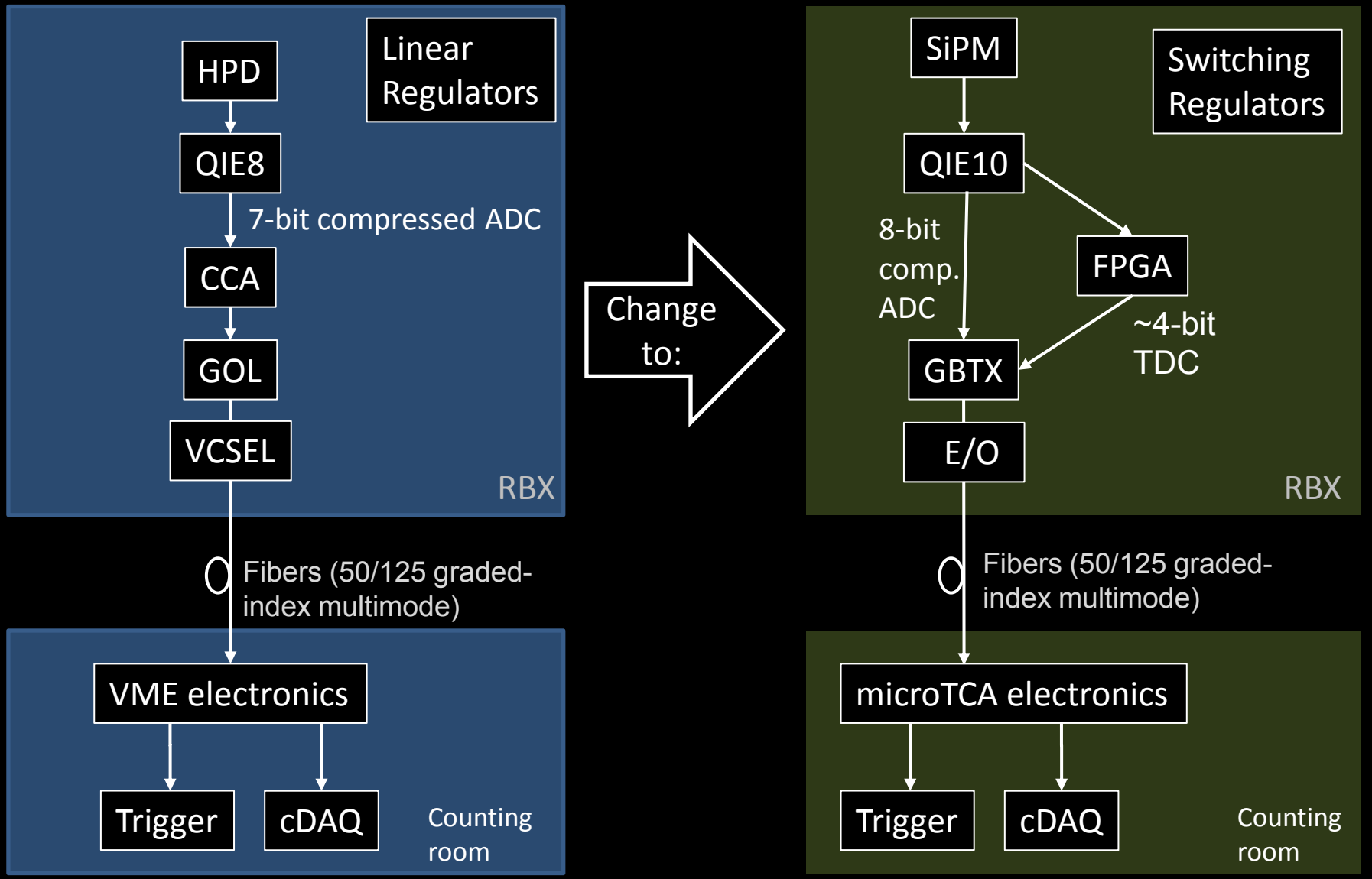
Environment:

- Total radiation dose = 10 krad = 100 Gy
- Neutron fluence = $10^{13}/cm^2$
- Charged hadron fluence = $2 \times 10^{10}/cm^2$
- Magnetic field = 4 Tesla on HB, HE. Lower field for the other partitions.

Infrastructure: very limited possibilities to change power cables, optical fibers, cooling pipes, on-detector mini-crates ("Readout Boxes" a.k.a. RBX).

Disclaimer : funding for the full project has not been approved yet (so far funding is allocated on a yearly basis).

HB HE data-path:
Existing vs Upgraded



References to the Upgrade work

PH/ESE group development: first integration tests are satisfying

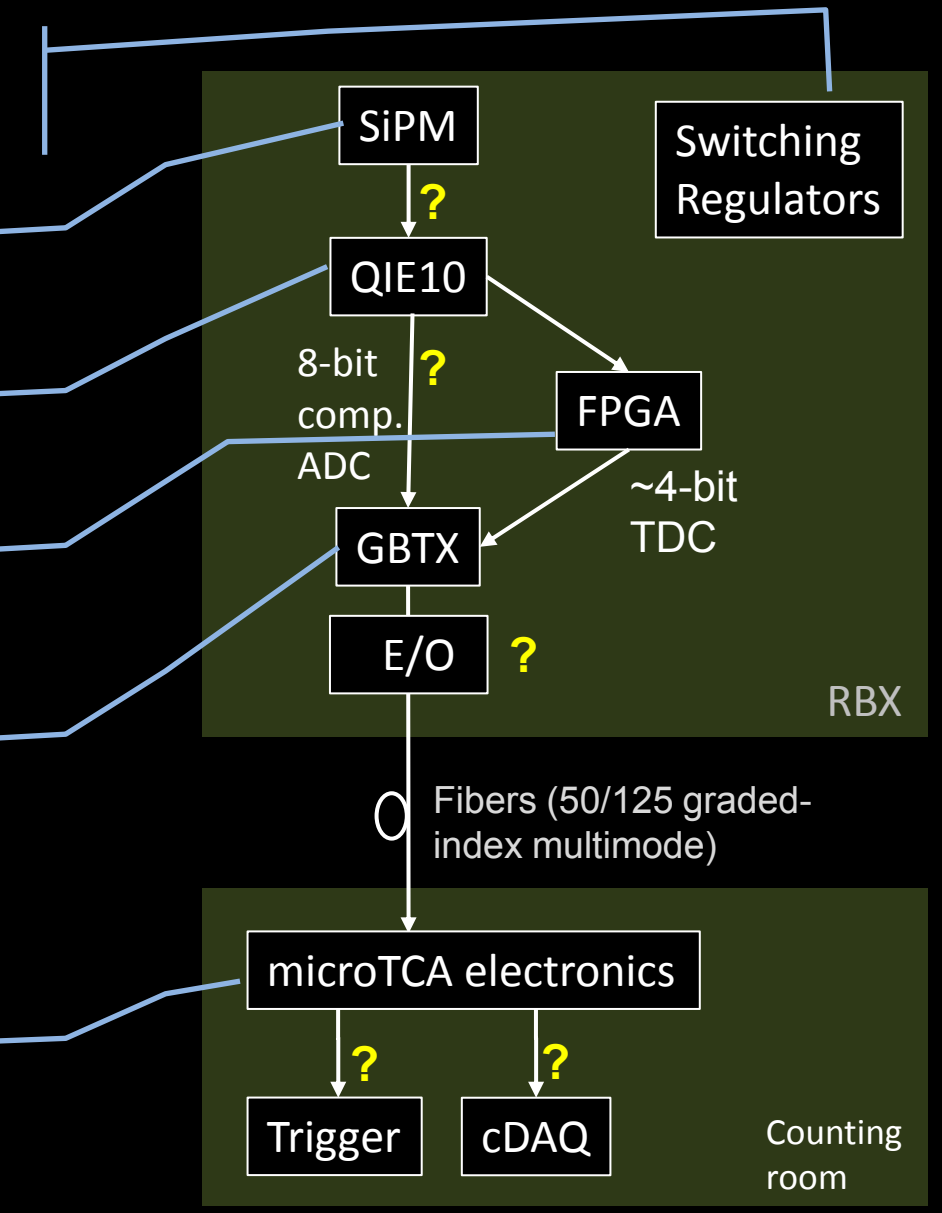
CMS HCAL R&D:
http://indico.cern.ch/conferenceOtherViews.py?view=standard&confId=113796

CMS HCAL R&D: See next slides

FPGA Rad-tol interest group

PH/ESE group development

CMS HCAL R&D: See next slides



Digitizing photosensor charge pulses

THE PROBLEM:

- digitizing photosensor charge pulses
- over wide dynamic range (≈15 bits)
- with negligible quantization error
- at frequency > 40 MHz (high rate for this kind of problems)

THE SOLUTION:

- Controlled input impedance over the entire dynamic range
- Integrate input charge on multiple scaled ranges simultaneously
- Select one appropriate range for any given input amplitude
- Digitize the integrator output on that range
- Read out the digitized result (“mantissa”) and the range code (“exponent”)
- Pipeline all operations to eliminate dead-time
- Scaling ratios between ranges must be constant to allow slope/offset calibration

→ QIE = Charge Integrator and Encoder.

An ASIC which digitizes a wide dynamic range into a floating point format.
Designer: Tom Zimmermann (Fermilab).
Various versions have been used in Tevatron, in neutrino experiments, in CMS HCAL.
The next version is considered for the upgrade of CMS HCAL and ATLAS TileCal.

QIE10proto2 chip

AMS 0.35u SiGe BiCMOS process.
Submitted to MOSIS on 8/30/10. Tests almost completed.

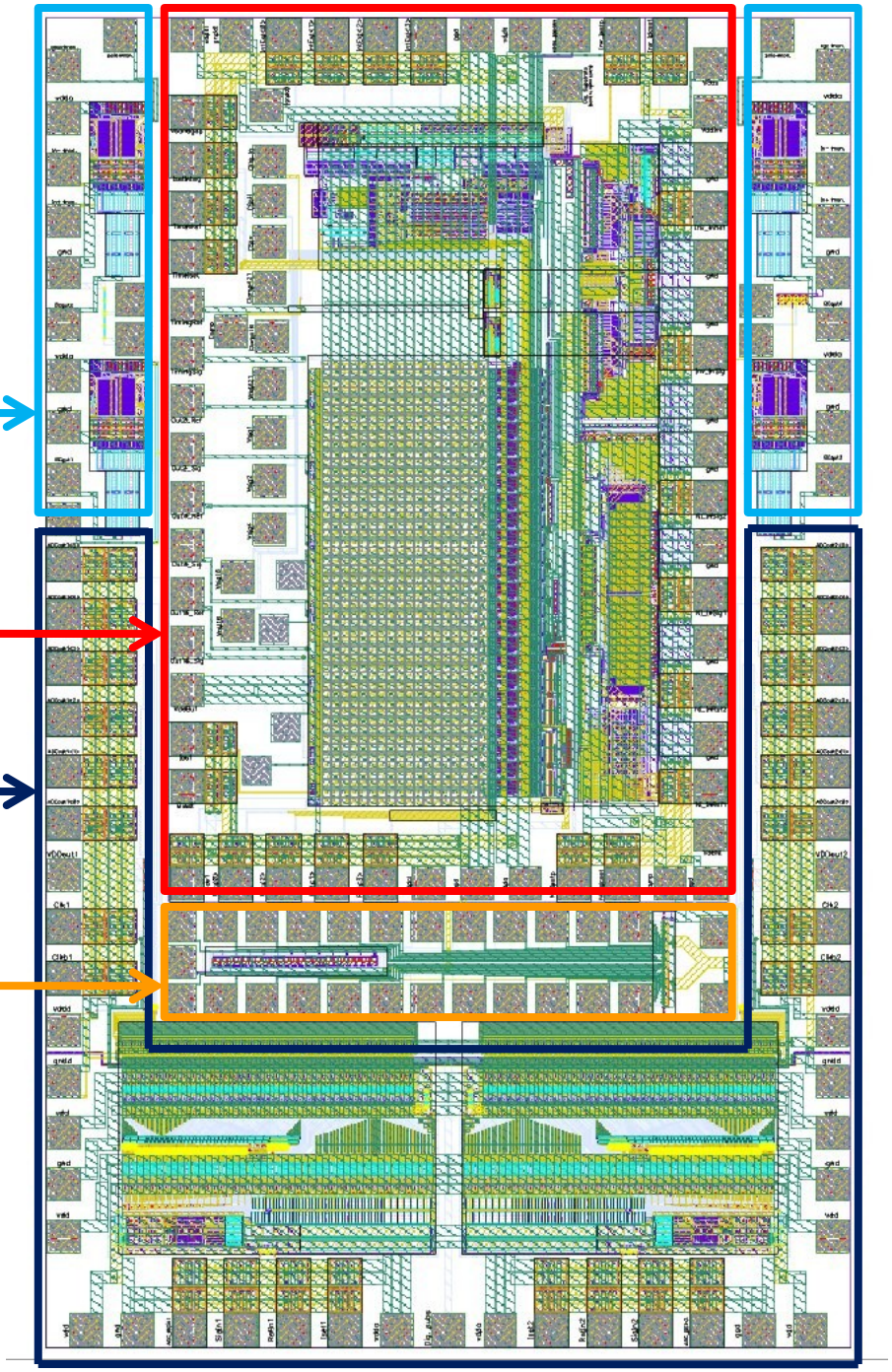
Several chips in one:

Bandgap circuits
(2 flavors: previous design + revised design)
(Bandgap on first prototype oscillated)

FrontEnd Version2
(First version had some matching problems)
Version 2 incorporates a "timing" amplifier

6-bit nonlinear FADC
New design.(2 ADCs are on this chip, identical but mirrored)

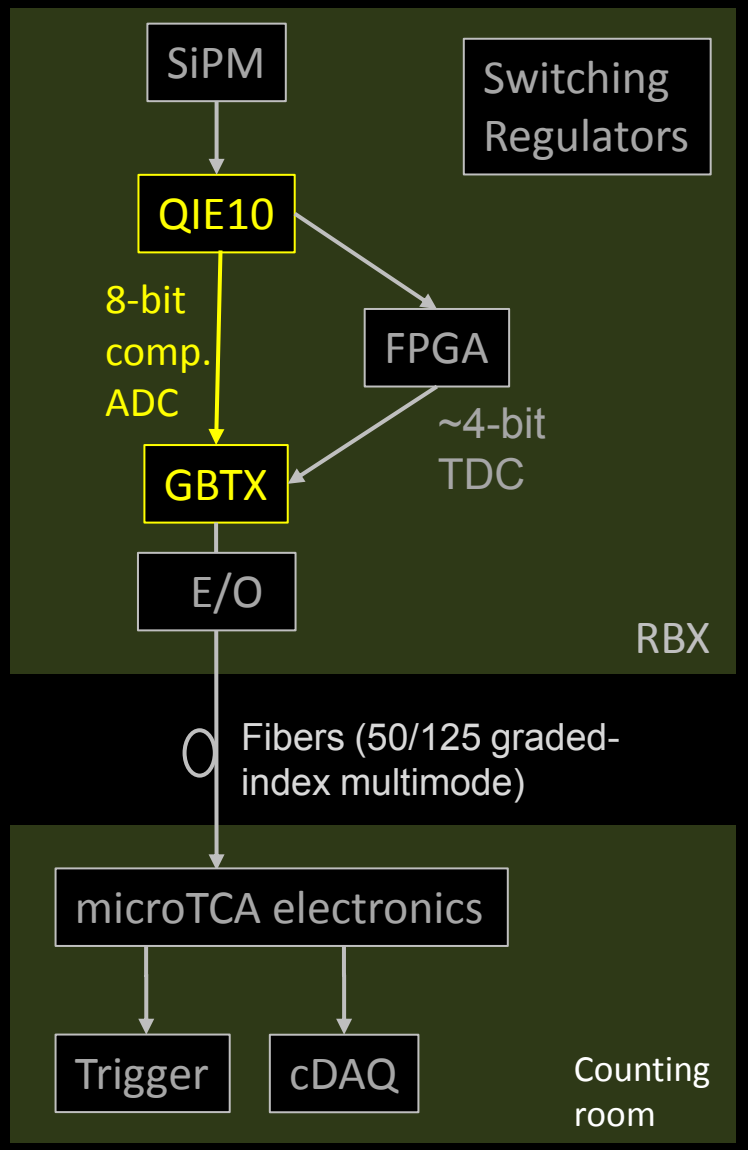
Matching circuits
(NMOS and NPN)



QIE10 prototypes and issues

- migration to AMS 0.35μm SiGe BiCMOS process 
- irradiation tests 
- input impedance matched to new photosensors 
- greater dynamic range → 100000:1 
- encoded output, 8 ADC bits at 40MHz
- serialized output data 
- bit, word and channel alignment
- output (“signal-over-threshold”) for the TDC
- 4 identical circuits on a single chip (increase channel density)

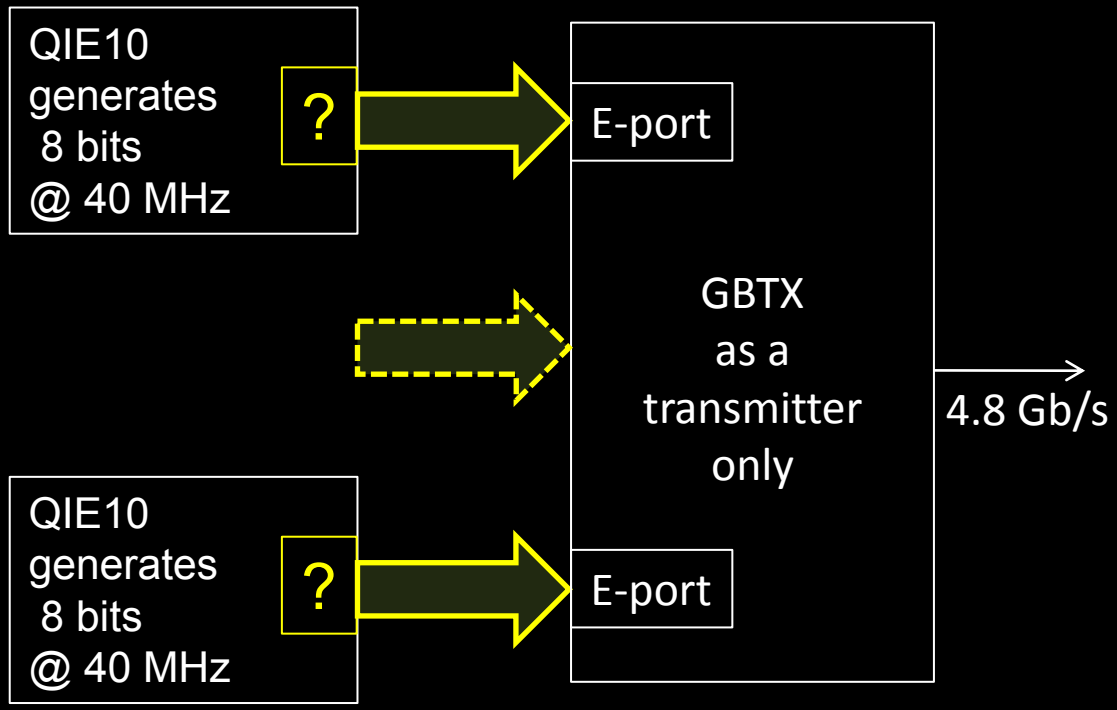
Data-path : QIE10 → GBTX



Readout issues: QIE10 → GBTX

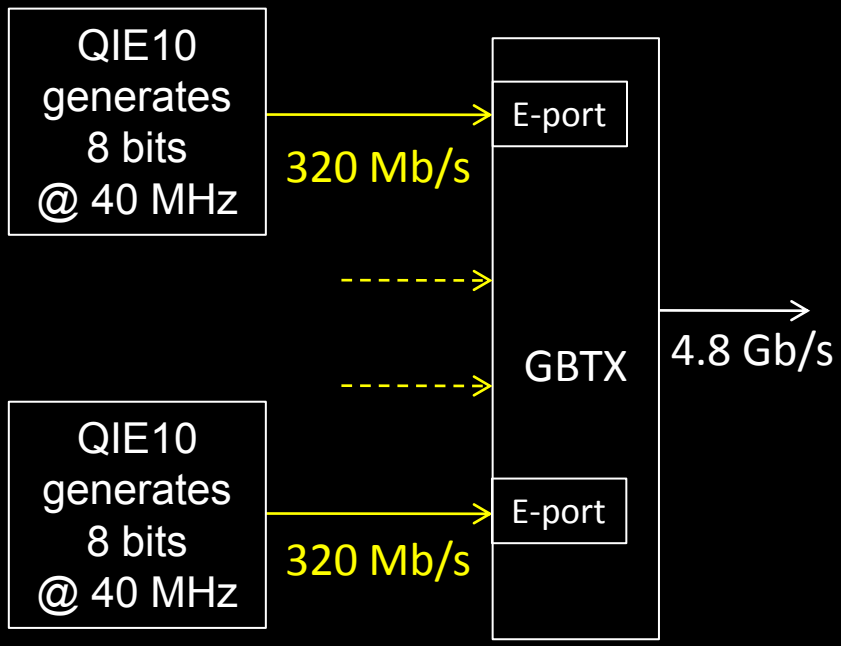
Requirements:

- **stable latency, preferably across power cycles**
- **high density of channels, 8 QIE10 circuits per GBTX**
- **ability to tune the sampling clock of the QIE10 ADC**



QIE10 → GBTX: High density of channels

QIE10 generates 320 Mb/s of payload data.
We'd like to send them to the GBTX using its E-ports in 320Mb/s mode.
Advantages: reduce power consumption, require fewer connections on the PCB).
Disadvantage: no room for encoding or framing.



Three problems:

1. sampling phase at the GBTX input.
2. identify the boundaries of the 8-bit words.
3. channel-to-channel alignment.

Ideas:

1. avoid long string of zeroes in the payload (forbid "0000 0000" and "1111 1111")
2. inject known data patterns (during orbit gaps? During timing-calibration runs?)
3. align words and channels off-detector

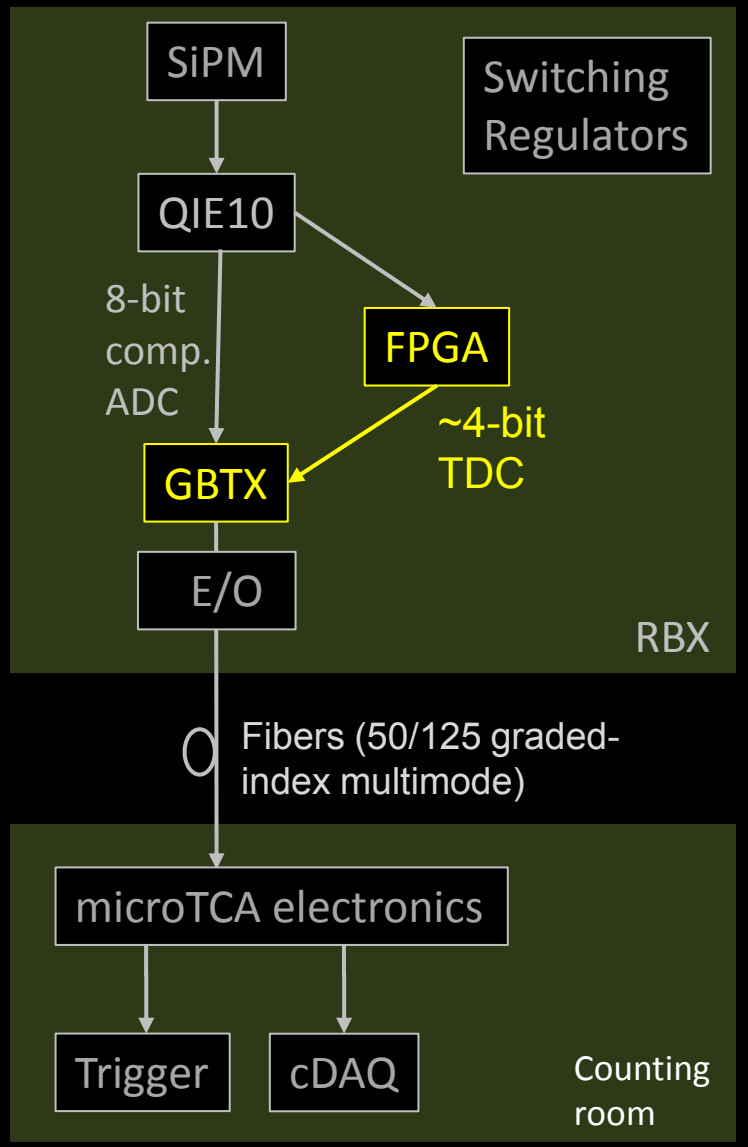
QIE10 → GBTX : Sampling clock tuning and E-link

GBTX provides clocks with controlled phase → use them for sampling.
What clocking scheme for the serializer in the QIE10 output ?
Ideas:

1) Follow the GBTX guidelines, use E-Link clock → then we have two clock domains (Sampling clock and E-Link clock). Options:
   - a FIFO between the two clock domains → latency ?
   - a forbidden phase between the two clock domains

2) Ignore the E-port guidelines, use the 40MHz sampling clock also for transmission: need a frequency multiplier in the QIE10; need to use the “dynamic phase adjustment” feature of GBTX, which needs transitions on the data line.

Data-path : TDC FPGA → GBTX

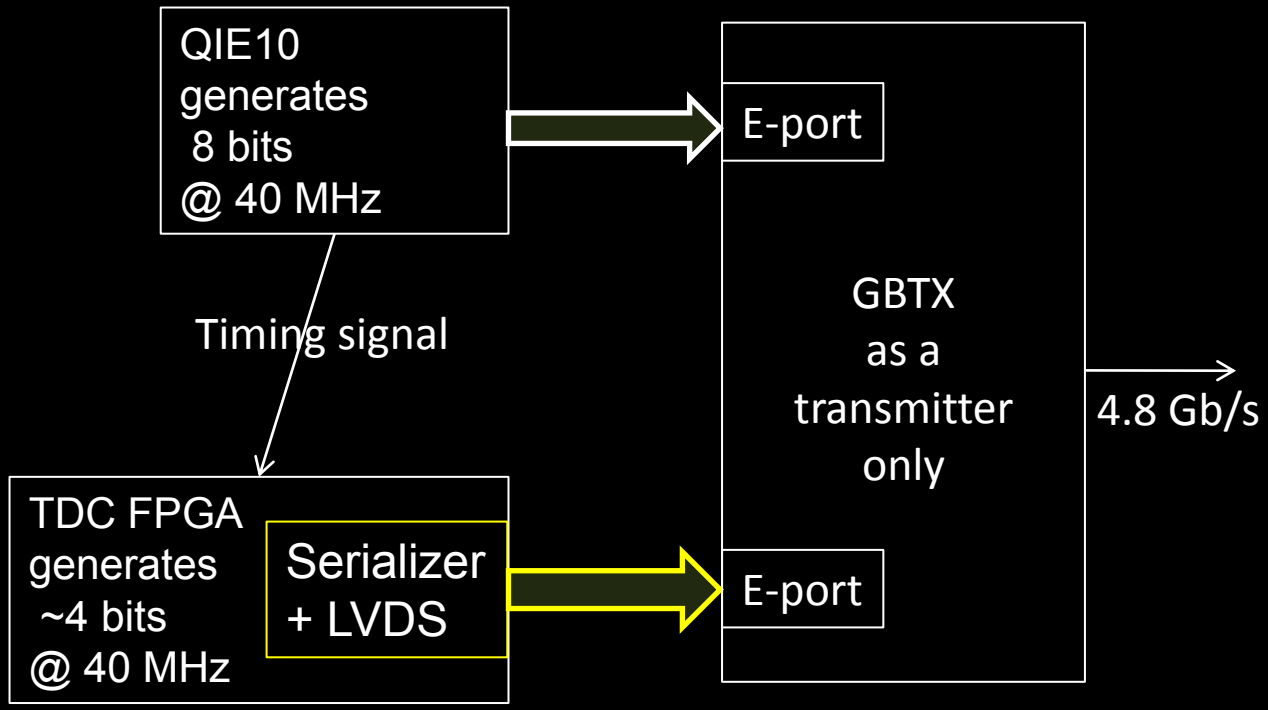


TDC FPGA → GBTX

Issues:

- **stable latency, preferably across power cycles**
- **electrical levels**
- **keep synchronization with QIE10 data**

  → work on this problem after the QIE10 output scheme.

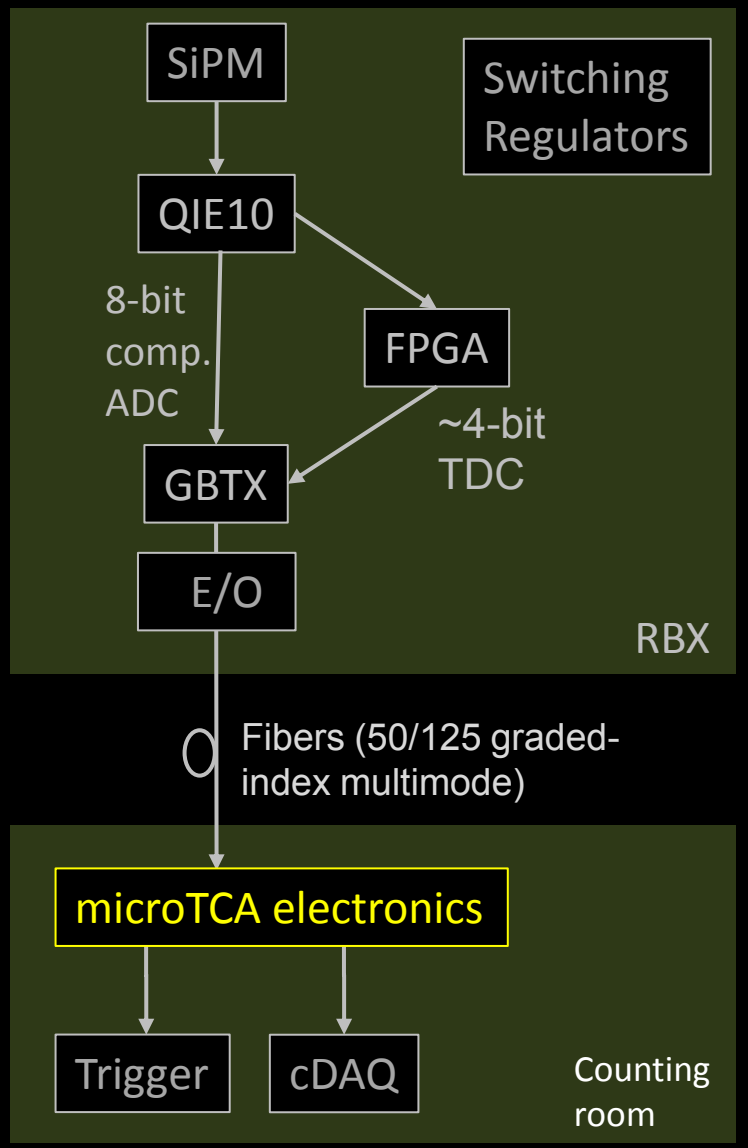


TDC FPGA: Radiation

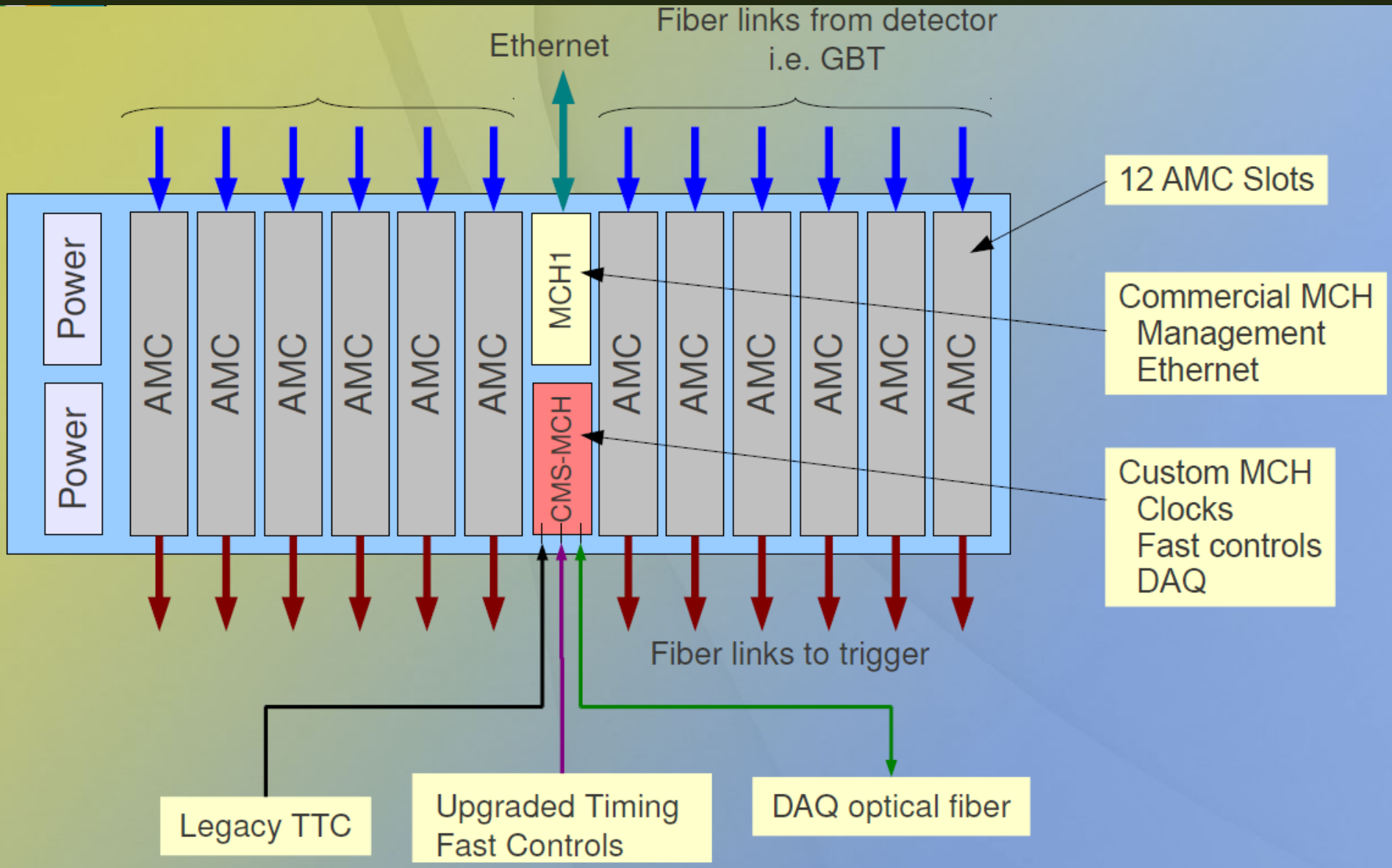
The best FPGA candidates are Actel ProASIC3L or ProASIC3E (flash-based).

- **TID**: various tests show a tolerance between 300 and 900 Gy → OK.
- **SEL**: ProASIC3x not sensitive to SEL (as explained by Federico Faccio on the FPGA-radtol interest group).
- **SEU on configuration**: immune.
- **SEU on logic**: TMR mitigation with automatic tools (http://www.actel.com/documents/SynplifyRH_AN.pdf).
- **SEGR**: Single Event Gate Rupture, it can happen if the FPGA is reprogrammed while exposed to radiation. The solution is to reprogram the FPGA only when there is no beam or other source of radiation.
- **SET**: Presently there is no easy solution. We may have to accept it and mitigate it at system level. It can appear in the logic and in the FPGA configuration.

Data-path: Counting room



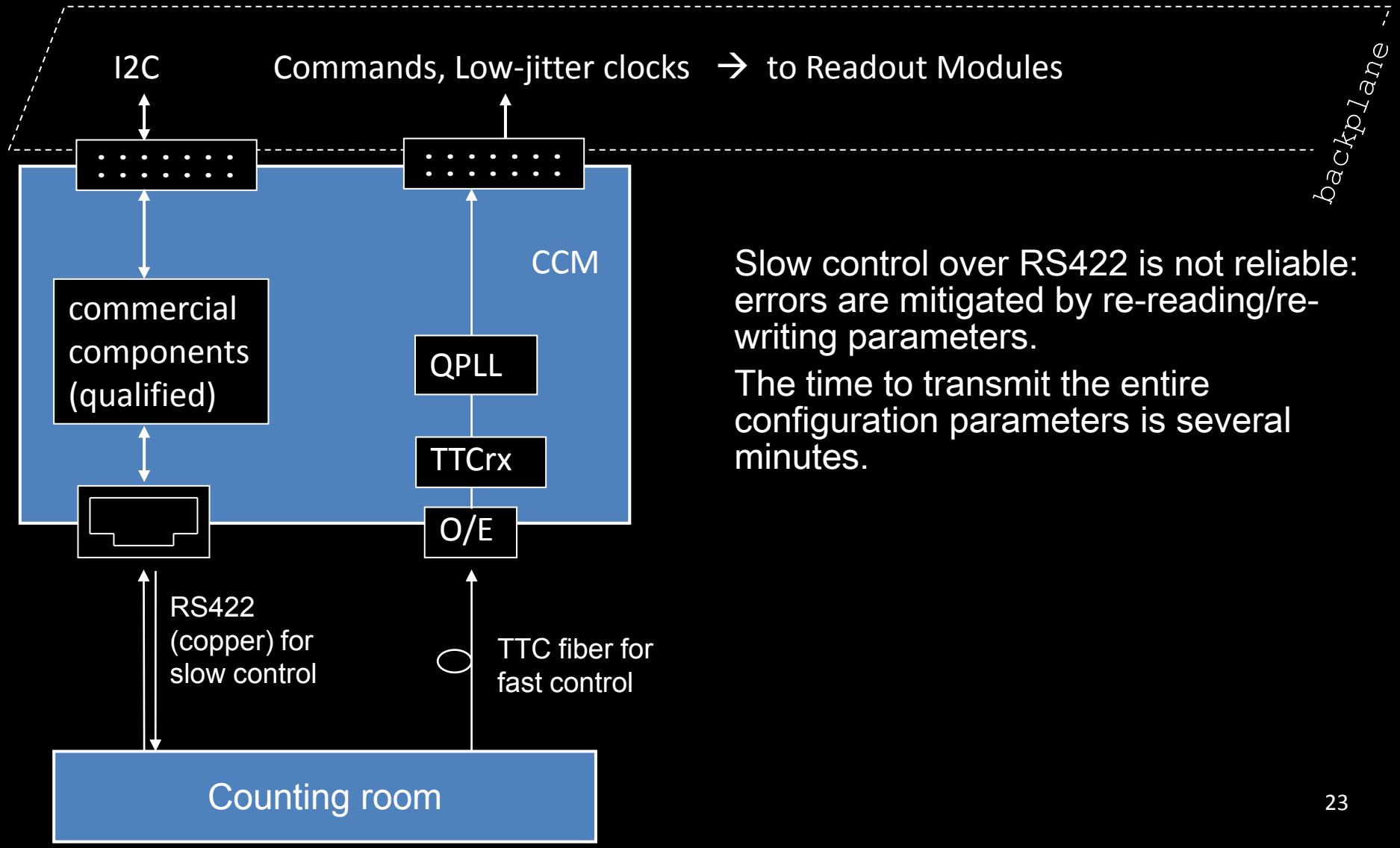
Counting room: CMS uTCA readout crate



Effort to standardize part of uTCA hardware and software in CMS (other systems welcome)

Control system

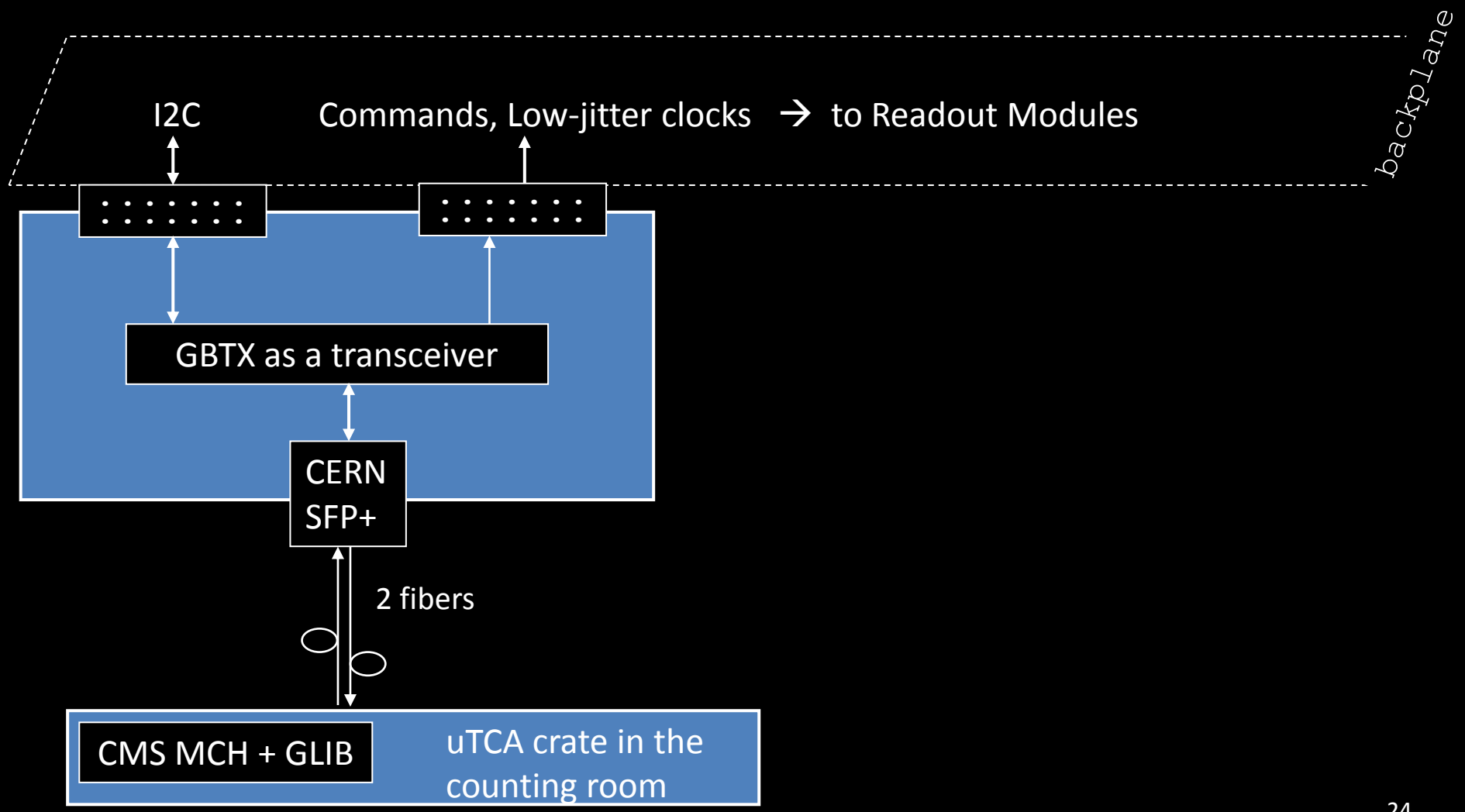
Existing CCM (Clock and Control Module)



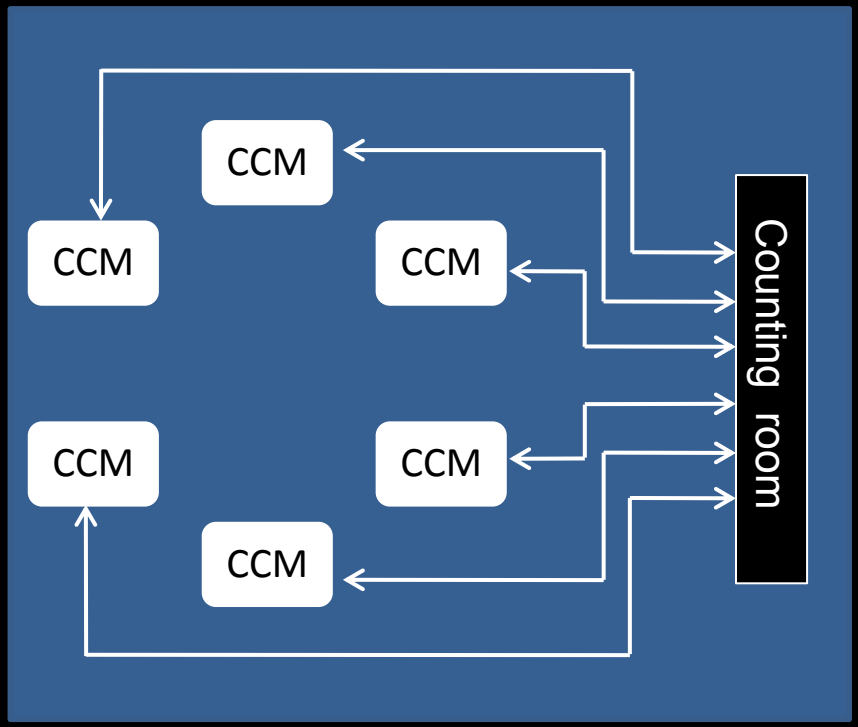
Slow control over RS422 is not reliable: errors are mitigated by re-reading/re-writing parameters.

The time to transmit the entire configuration parameters is several minutes.

New CCM: add the GBT…



Existing CCM: architecture and weaknesses

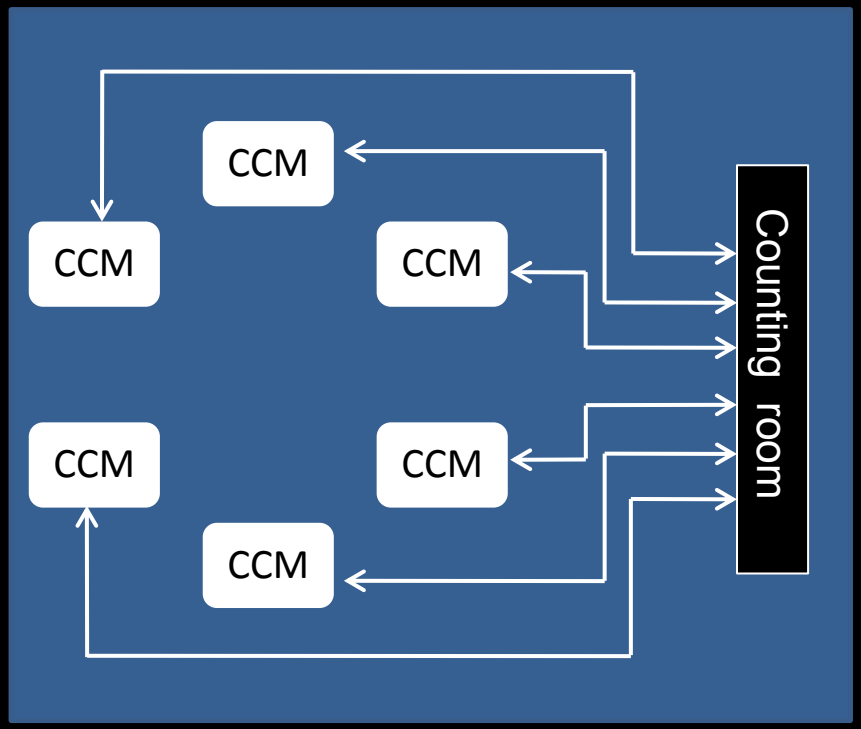


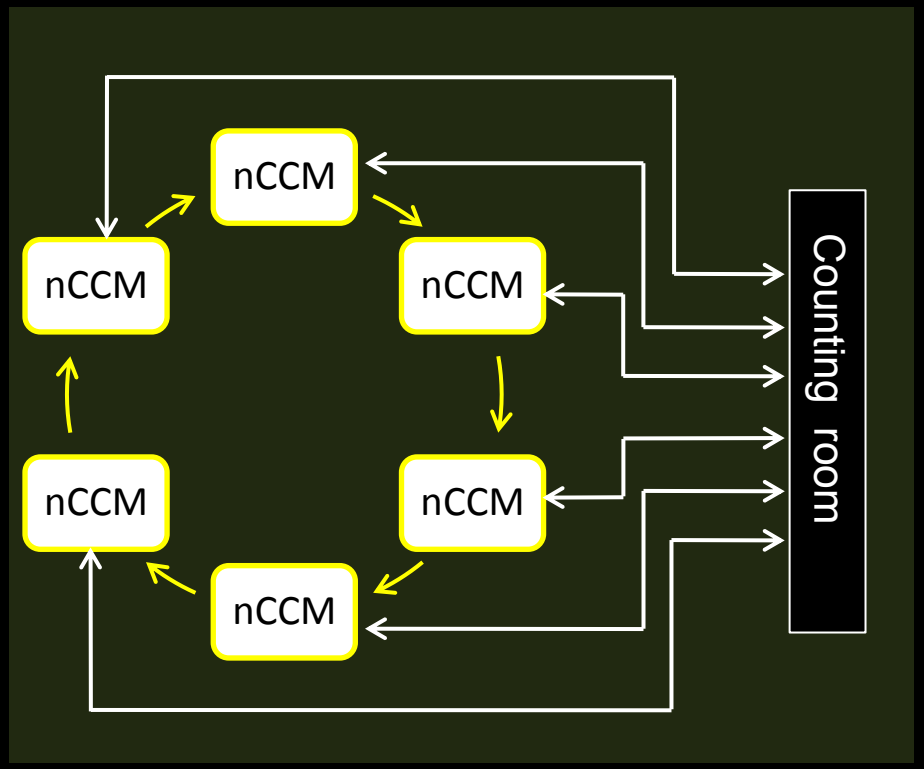
In the existing system, a CCM controls 72 data channels (≈ 1% of the total).

The point-to-point links to the counting room are an important **single point of failure**.

If a control link or part of a CCM breaks, we would loose control on 1% of the data channels. This is considered not acceptable.

New CCM: architecture with redundancy





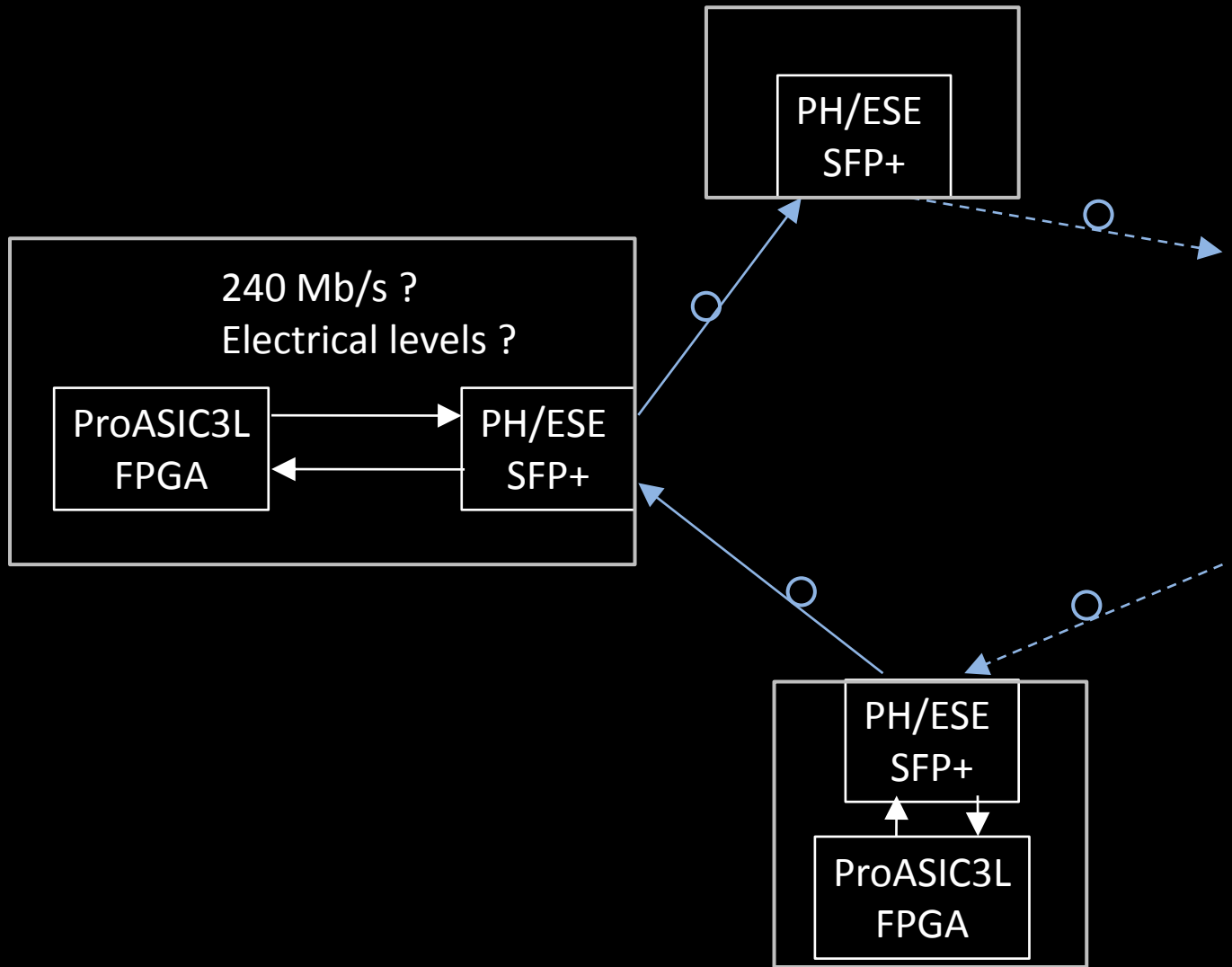
New redundant control path: ~2-meter links from a new CCM to a new CCM.

These links will create a ring of CCM's and can provide the clock and a few essential commands, in case the main control link fails.

Implementation with ProASIC3L **FPGA** and PH/ESE SFP+ ? Electrical interface ?

Line rate ~240 Mbps. Need to define a line coding (looking at 5b6b and FF-LYNX).

Implementation of the new CCM redundant link

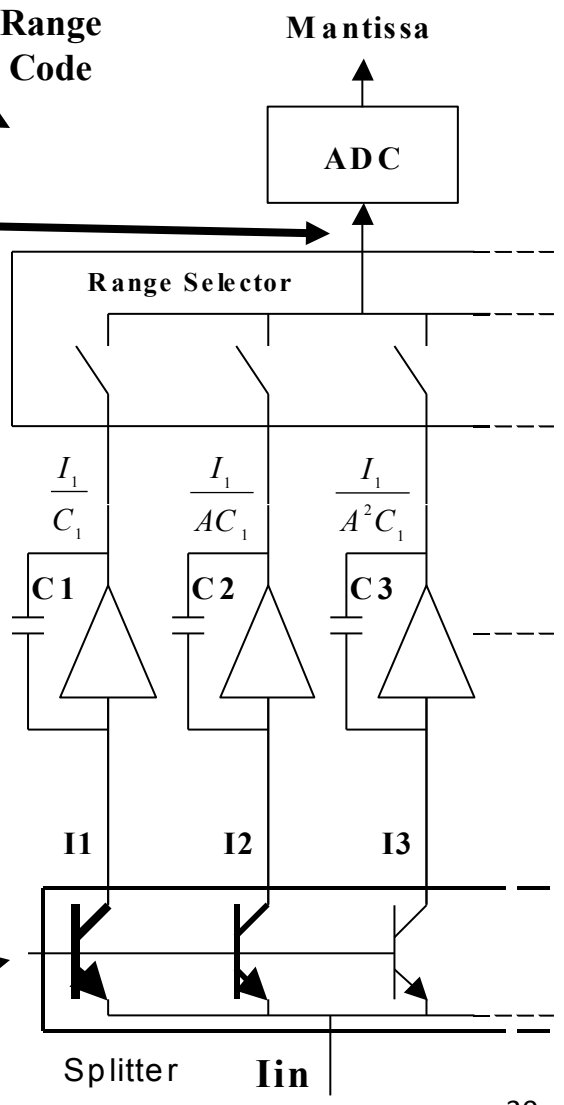


QUESTIONS ?

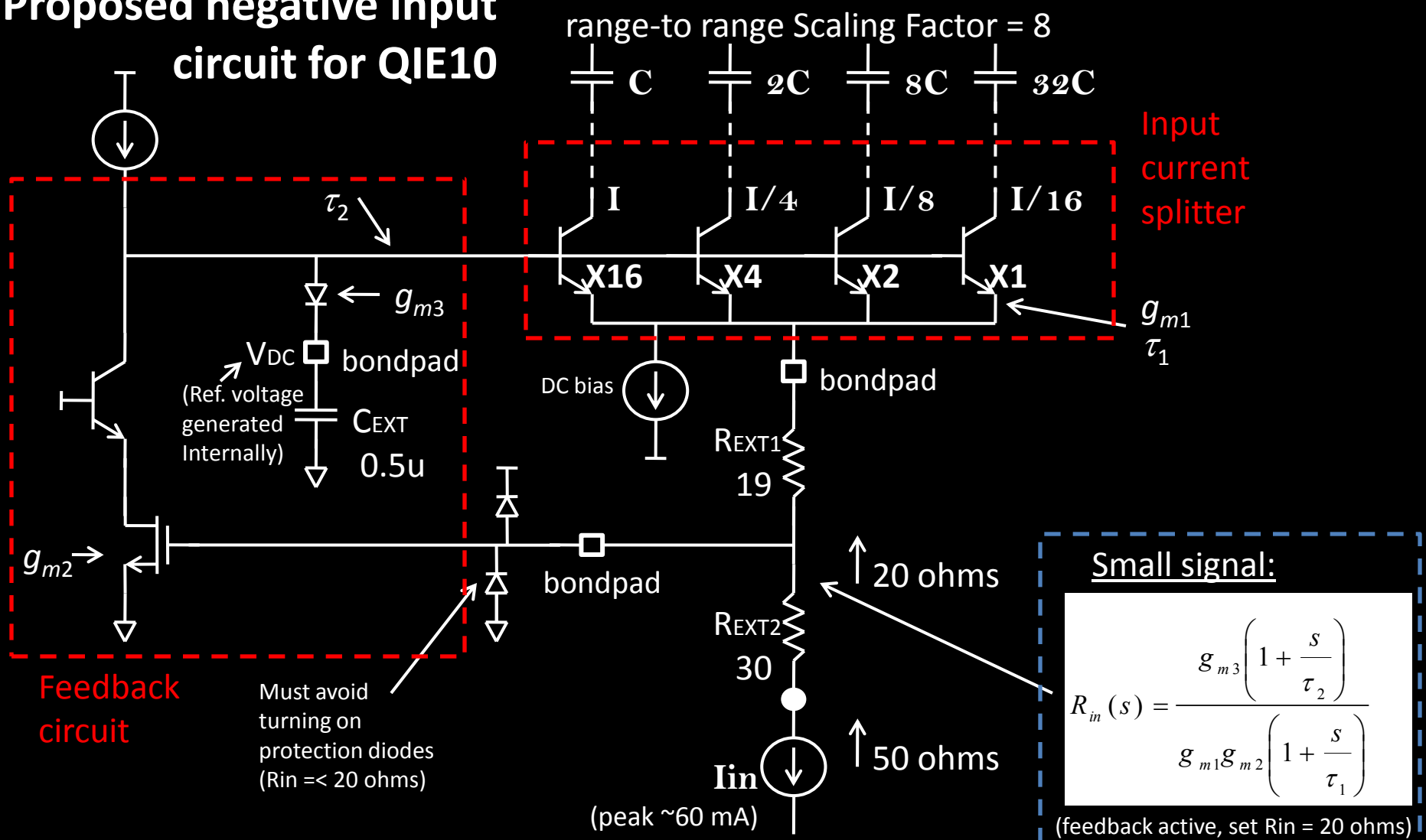
Backup slides

The QIE Concept (simplified)

- 5) The range code forms the exponent.
- 4) For a given input charge, one appropriate range output is selected and digitized by an ADC, forming the mantissa.
- 3) Splitter ratios and integration C ratios are chosen to achieve range-to-range scaling of the transfer gain (I/C) by factor ***A***.
- 2) Each splitter range output feeds a charge integrator. The current fractions are integrated simultaneously on all ranges.
- 1) Input current pulses are divided into weighted fractions by a current splitter



Proposed negative input circuit for QIE10



Small signal:

$$R_{in}(s) = \frac{g_{m3}\left(1 + \frac{s}{\tau_2}\right)}{g_{m1}g_{m2}\left(1 + \frac{s}{\tau_1}\right)}$$

(feedback active, set Rin = 20 ohms)

Large signal:

Rin ~ 20 ohms

(feedback circuit inactive)

Nice properties of this BiCMOS circuit:

- Small bipolar transistors give good g_m, good speed (>100 MHz).
- Split ratios are constant over wide range with a bipolar splitter
- As Iin increases, g_{m1} increases but g_{m3} decreases, so that Rin ~ constant! Arrange VDC for Rin = 20.
- Rin looks resistive to > 1GHz!

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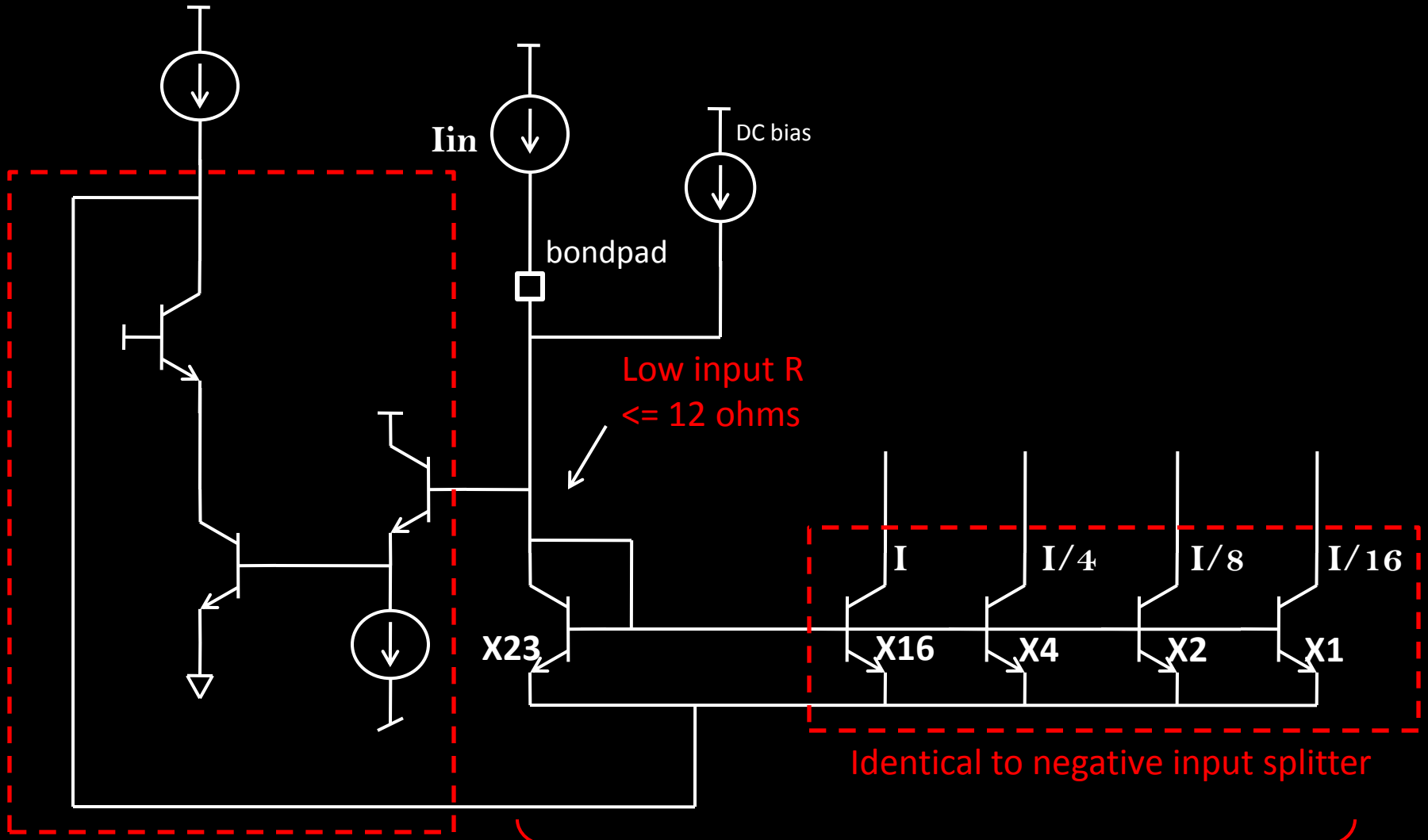
Proposed positive input circuit for CMS QIE10

(Invert and split the signal current)



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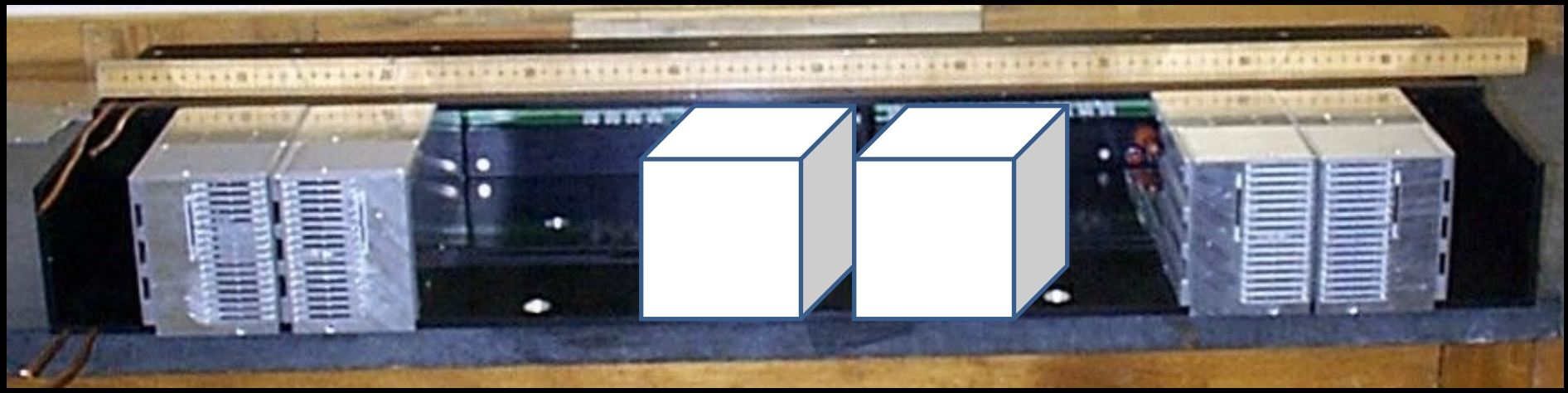
Existing On-Detector Electronics: Readout box ↔ 20° of HCAL



Readout Module | Readout Module | Clock and Control Module | Calibration Module | Readout Module | Readout Module

Infrastructure

The cooling system is designed to remove 200 W per Readout Box. The existing Readout Boxes dissipate “only” 90 W. The goal for the upgraded Readout Boxes is to dissipate < 200W (with ~4x increase in data) .

→ switching regulators will play a key role

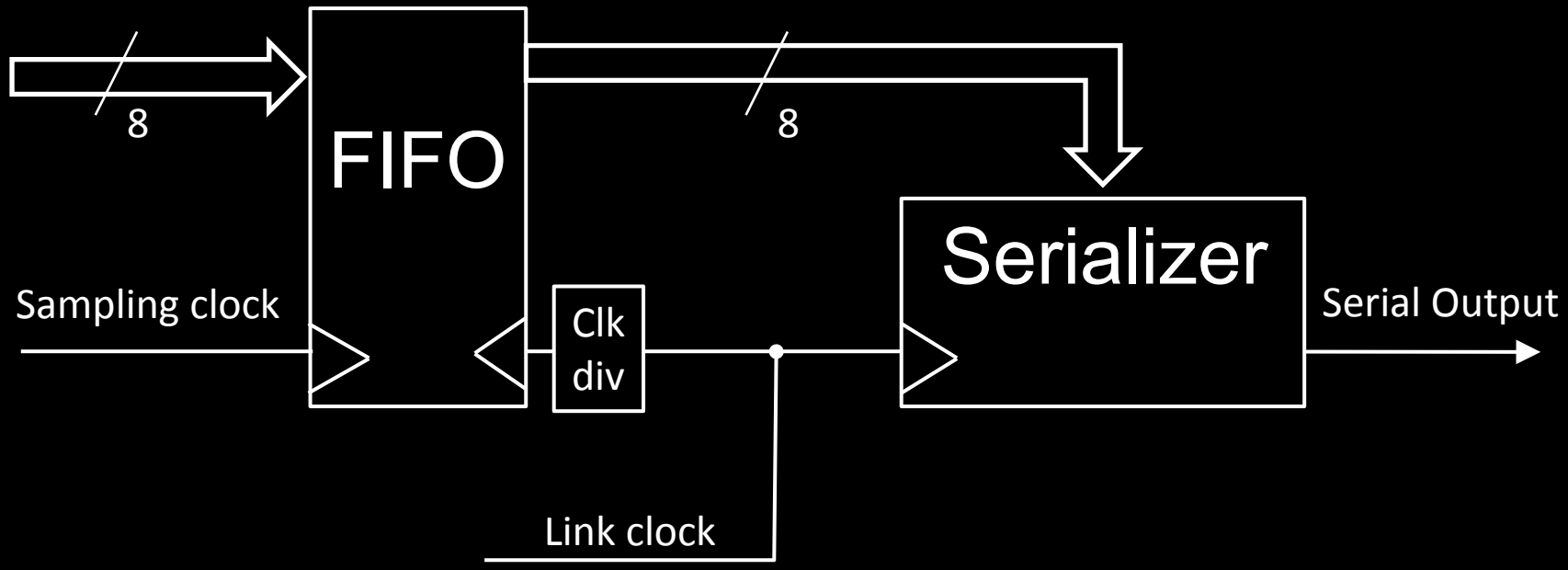
Very difficult to lay more cables to the detector. The upgrade plans do not assume to change the cabling.
This limits the bandwidth to send TDC bits to about half of the channels
→ FPGA reprogrammability can play a role to decide where and how to do TDC.

The existing power supplies from CAEN are not compatible with the upgraded system

→ need to specify and purchase new power supplies.

→ we have an estimate compatible with our budget

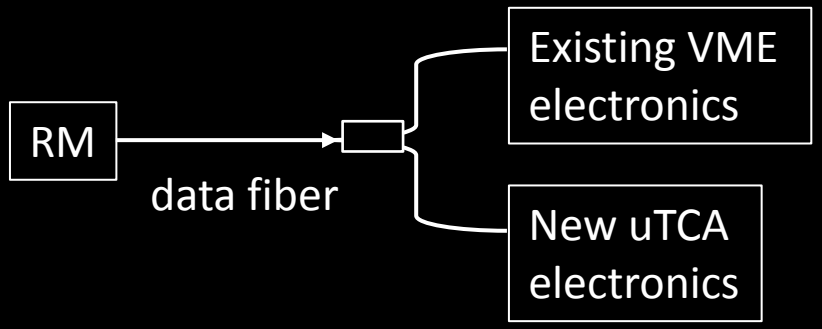
A possible scheme for QIE10 output: Sampling clock, E-Link clock and FIFO



Appropriate control logic receives QIE_Reset and controls the FIFO.
A FIFO built with flip-flops could be sufficient.

HB HE draft installation plans

- 2013 shutdown: install optical splitters on a few data fibers: one side goes to the existing VME electronics (preserve existing functions), the other side of the splitter go to new uTCA electronics
- Commission the new uTCA electronics “parasitically”
- Iterate over the whole HCAL ?



- In this way the Counting-room electronics could be upgraded gradually

2014: production of front-end cards
2015: test of cards, assembly of the modules
2016: Burn-in tests of modules
→ **Ready for c**omplete installation in mid-2016