>50Gs/s CMOS ADC, DAC and DSP

- ADC/DAC/DSP applications

- Design tradeoffs
- Single-chip challenges
- CMOS ADC
- CMOS DAC
- Digital noise coupling
- Package and PCB design

- ADC/DAC standard products and test chips
- Future roadmap

>50Gs/s ADC/DAC/DSP applications

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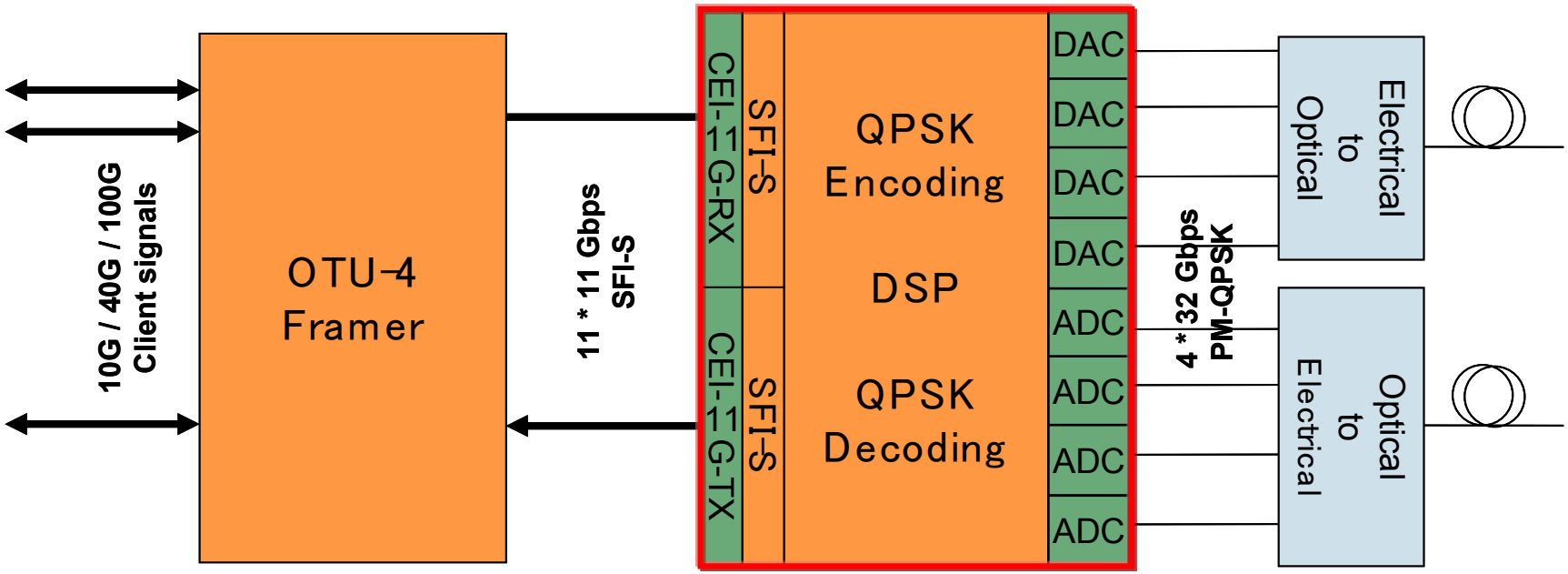
- 56Gs/s ADC developed for long-haul optical transport
  - Coherent receivers for 100G systems (CMOS ADC + massive DSP)
- 55-65Gs/s DAC designed for same market
  - Coherent transceivers for 100G systems (ADC + DAC + bigger DSP)
- These are custom ASICs with DSP IP from customers
- Availability of macros has triggered interest in other areas
  - Ultrafast signal acquisition and generation
  - Test & measurement, radar, radio telescope, particle accelerators...
- Standard products needed for fragmented markets

Example ADC/DAC/DSP application – 100G



- Coherent transceiver for 100G long-haul optical transport
  - 4ch 55-65Gs/s 8b RX ADC
  - 4ch 55-65Gs/s 8b TX DAC
  - DSP for RX and TX processing
  - SFI-S interfaces to framer/FEC

What is driving ADC/DAC/DSP design?

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- Power consumption
  - System power/thermal budget per channel in many applications
- Cost
  - Especially for future higher volume systems
  - Mass-production capable solution -- cost down as volumes go up
- Single-chip CMOS is the “holy grail”
  - Foundation of the semiconductor industry
  - Continuous process development driven by digital
  - Inherently low-cost in high volumes (“high” is ***not*** 10k pieces/year!)
  - Higher functional integration is simple

Why not use multi-chip module (MCM)?

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- SiGe can make ADC/DAC design easier
  - But power consumption is higher than CMOS, especially with scaling
- "Can use same ADC/DAC with multiple DSP chips"
  - Since custom DSP is needed anyway, ADC/DAC can easily be added
- Interconnect problem between ADC/DAC and DSP
  - 4ch ADC/DAC ➔ 4Tb/s between chips
  - Silicon interposer MCM makes this technically possible
    - Still has power penalty even with low-power transmission – OK for FPGA ☺
- Barrier to cost reduction
  - Inherently more expensive and lower yield
  - Difficult to leverage into higher-volume or cost-sensitive applications

Single-chip CMOS ADC/DAC/DSP

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- The good...
  - Device speed and power (including ADC/DAC) continually improving
  - No multi-terabit chip-to-chip interconnect needed
  - Integration of more functions/channels is “free”
  - Can add arbitrarily complex calibration at little cost
  - High yield and low cost (in high volume)
- the bad...
  - Very challenging ADC/DAC design in CMOS
  - Decreasing supply voltages and increasing device mismatch
- and the ugly ☹
  - Integrating ultra-low jitter ADC/DAC with massive DSP on same die

So what's so difficult?

- Power, efficiency, thermal design (chip/package/PCB)
  - ~70W OIF target for 100G transponder ➔ <50W for transceiver
- ADC/DAC design
  - ~60Gs/s in CMOS is "challenging" – but see later...☺
  - Large mismatch and noise for small low-power low-voltage transistors
- DSP
  - ~50TOPS needed for 100G soft-FEC TX and RX processing
  - Massively parallel interconnect problem -- bus widths 4kb or more
- Noise isolation
  - ~100fs ADC/DAC jitter on same die as ~100A DSP current peaks
- Signal integrity
  - Good S11 and bandwidth from PCB through package/chip to ADC/DAC

ADC / DAC design for high-speed systems

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- Many common design issues for ADC and DAC
  - Very high sampling rates, wide bandwidth, low noise
  - Low-jitter clock generation and distribution
  - Interconnect can be more difficult than circuit design
  - Low voltage design with poorly matched small transistors
- Use parallel lower-speed circuits with precise MUX/DEMUX
  - More power efficient in CMOS (similar reason to DSP)
  - High integration levels are no obstacle (hundreds of internal ADC/DAC)
- Take advantage of the strengths of CMOS
  - If it moves, calibrate it ☺
  - Move calibration into digital – an extra million gates is “free”...

CMOS ADC design issues

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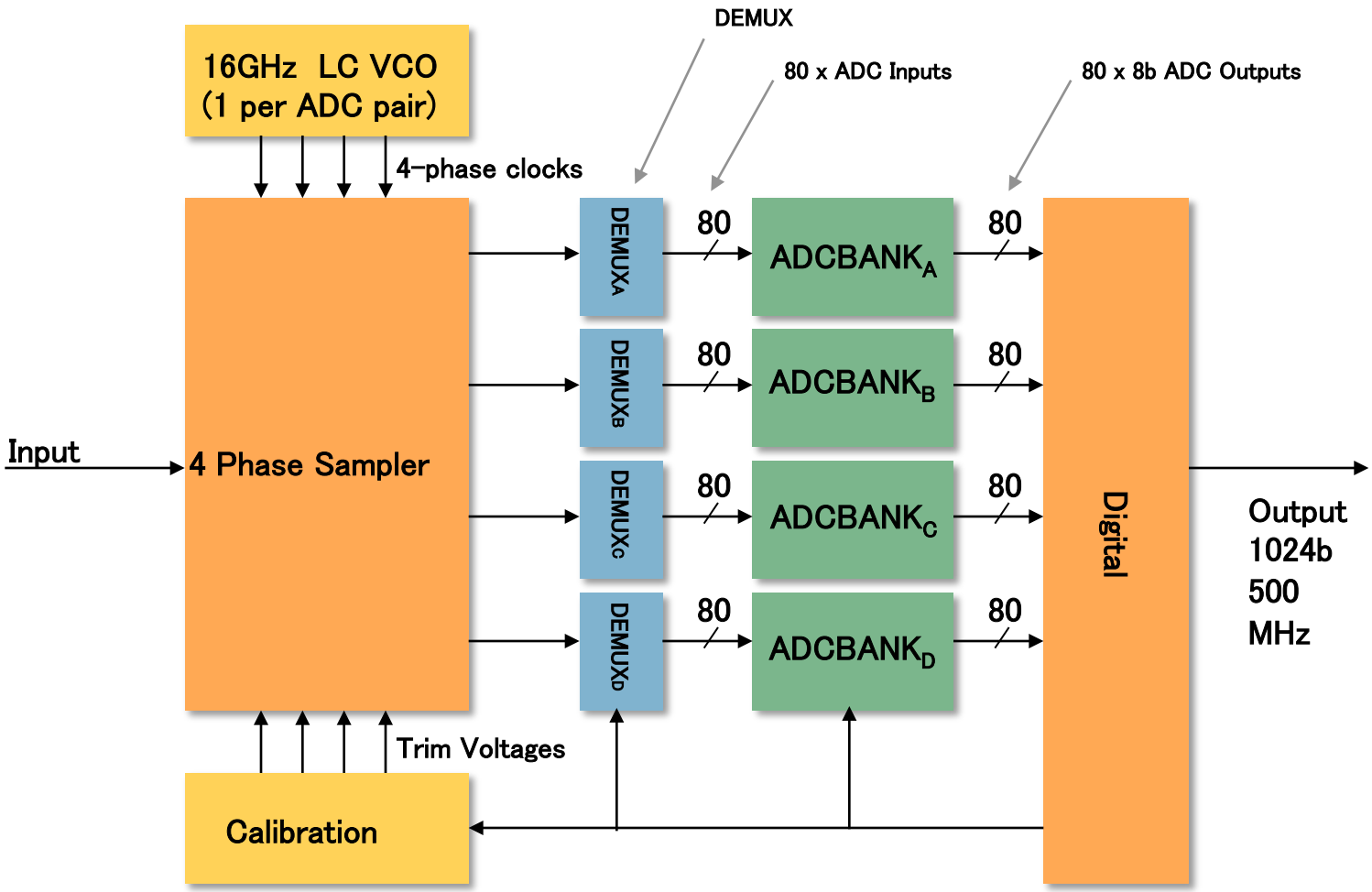
- Front-end sampler is the most difficult problem
  - Effective sampling pulse width <20ps
- Time interleaving is pretty much essential
  - Allows roadmap to >100Gs/s when required
- How to get accurate matching of multiple paths?
  - Gain, offset, time mismatch ~100fs
  - Need to measure/calibrate in background – how?
- How to get low noise/power and good input matching?
  - Input buffer adds noise/distortion and consumes power
  - Low noise + low voltage ➔ bigger sampling capacitors and switches
    - But need small input capacitance to preserve S11 and/or keep power down
- Conventional circuits cannot do all this simultaneously
  - Some new technique is needed...

CHAIS 64Gs/s CMOS ADC

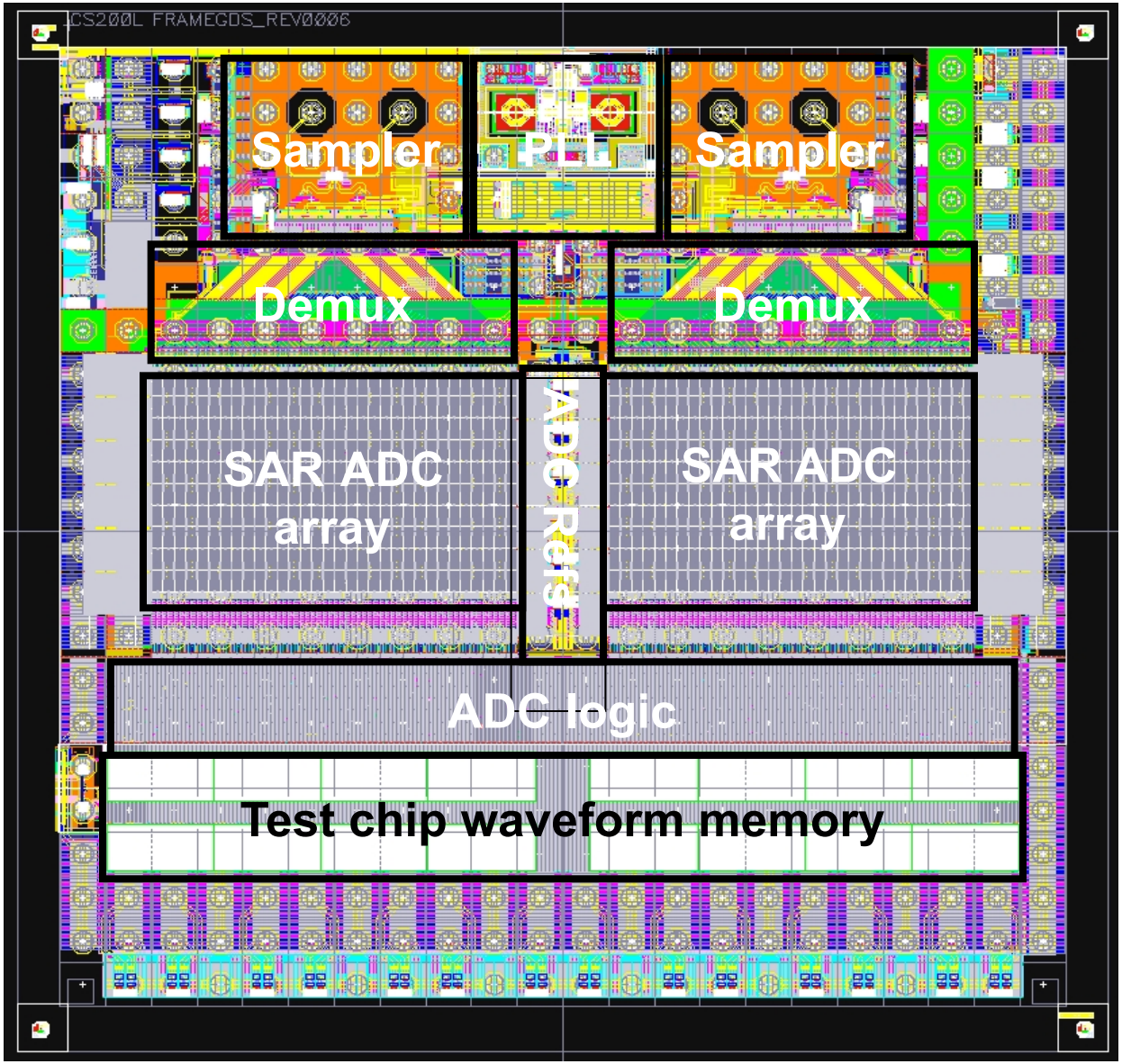
CHArge-mode Interleaved Sampler (CHAIS)



ADC circuit blocks

- Sampler/demux using charge-mode signal processing
  - No large voltage swings or gain errors
- 4-way sampling front end
  - Uses 4-phase 16GHz clocks from low-noise LC VCO
  - 50ohm resistive input
- 4-to-320 way demultiplexer
  - “Lossless” steering of charge packets from sampler to ADC array
- 320 8-bit 200Ms/s SAR ADCs
  - Large (~200fF) input capacitors for low noise/good matching
  - Optimised for area and power efficiency, not maximum speed
- Digital background calibration of all analogue circuits
  - For mismatches in offset, gain and time delay (skew)

Dual ADC layout (4x4mm test chip)



Measured ADC performance

- 55-65Gs/s with 8 bit resolution
  - Lower noise floor allows digital EQ/AGC after ADC
- >18GHz bandwidth
  - Closely controlled, can be extended to >20GHz using digital EQ
- Low noise and distortion
  - Small-signal: noise floor <-40dBFS
  - Large signal: THD <-40dBc for 20GHz full-scale input
  - ENOB >5.7 for signals like 100G OFE output (PAR=9dB)
- ENOB flat with input frequency
  - <0.2ENOB variation from 1GHz to 20GHz input signal
  - Total sampling clock jitter ~100fs rms
- Power consumption ~1.5W/ch in 40nm (~6W for RX macro)
  - Scales with process better than typical digital circuits

ADC calibration

- Interleaved paths need accurate delay/gain/offset matching
  - 100fs inter-sample skew generates -40dBc distortion for 16GHz input
- Clock and signal mismatches get worse as process shrinks
  - Smaller gates (for higher speed/lower power) have worse matching
- Can't take ADC offline to calibrate *(excuse me while I turn the Internet off…)*

- How to measure and correct these errors during operation?
  - Measurement accuracy problem *(Quis custodiet ipsos custodes?)*
  - Algorithm complexity (FFTs at these rates for calibration not desirable)

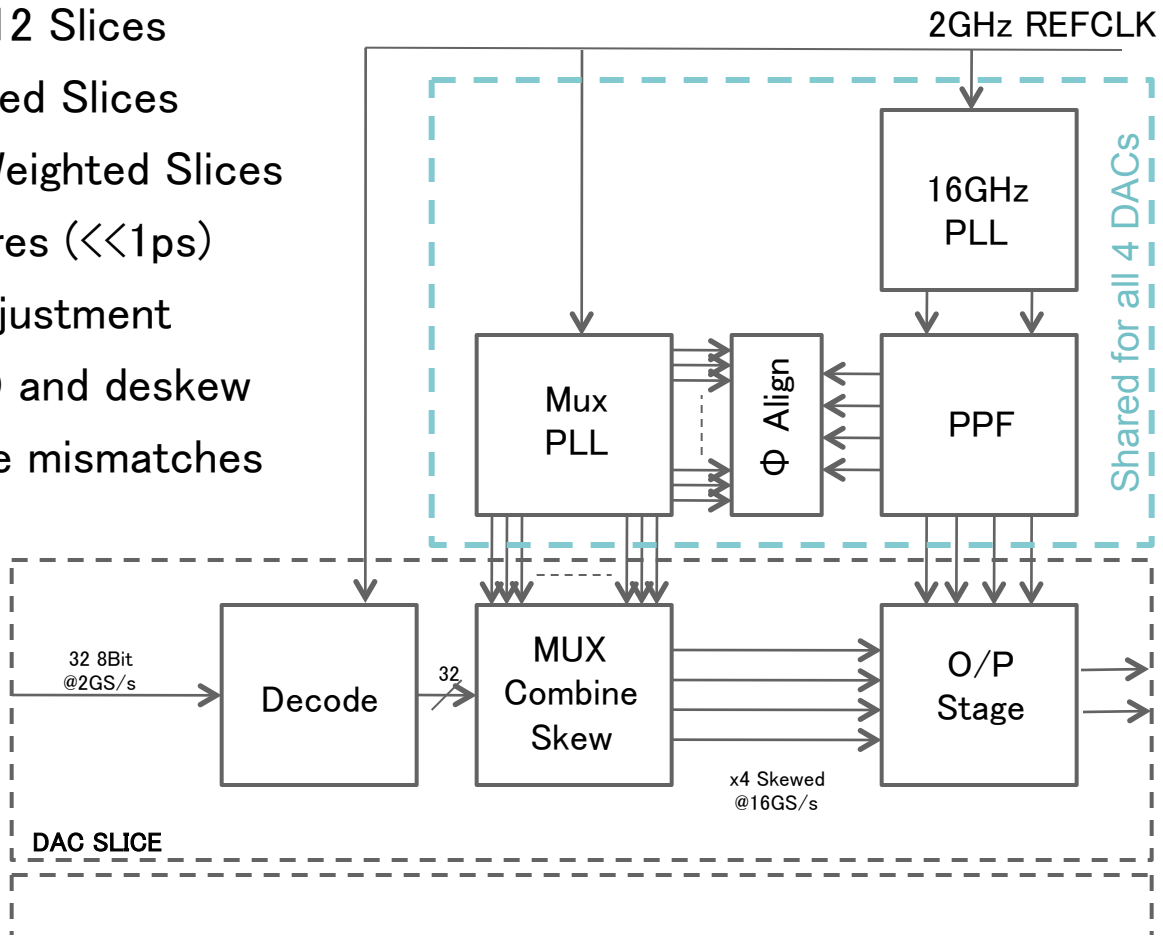
- CHAIS architecture calibrated by simple output data analysis
  - Average errors calculated digitally in background during operation
  - Analogue trim coefficients calculated to drive trim DACs (>400)

CMOS DAC design issues

- Many similarities to CHAIS ADC
- Current-mode output stage with interleaved switches
  - Segmented MSBs + binary weighted LSBs, matched delays
- Same clock requirements (actually, same circuits...)
  - 4-phase clocks from 16GHz LC VCO
  - Common clock wires to all output stages ➔no source of mismatch
- Similar matching requirements but many fewer contributors
  - Calibrate out switch Vth mismatches (delay, offset) using DACs
  - Calibrate out current source mismatches (gain) using DACs
  - Calibration at startup gives stable results
- Getting good output matching (S11) is difficult
  - DAC output capacitance (inc. ESD protection) can’t be seen at pad

64GS/s CMOS DAC – “Leia”

- PLL, PPF, Mux PLL, Phase aligner derived from ADC
- DAC circuits derived from 14b 12Gs/s DAC
- 4 DAC cores in macro, common PLL clocks (same wires)
- Each DAC core contains 12 Slices
  - 3 MSB → 7 Segmented Slices
  - 5 LSB → 5 Binary Weighted Slices
- “Zero-skew” between cores (<<1ps)
  - No analogue delay adjustment
  - FIR filter used for EQ and deskew
- Calibration of output stage mismatches



Simulated DAC performance

- 55-65Gs/s with 8 bit resolution
  - Low noise floor allows digital EQ (pre-emphasis) before DAC
  - 2 samples per symbol allows digital skew/waveform shaping in FIR filter
- >15GHz bandwidth
  - Closely controlled, can be extended to >20GHz using digital EQ
- 1.2Vpp differential full-scale output signal
  - ~600mVpp usable after pre-emphasis -- depending on amount!
- Low noise and distortion
  - THD <1% for 20GHz full-scale output
  - Noise floor < -40dBFS
- Power consumption ~0.75W/ch in 40nm
  - ~3W for 4-channel TX macro
  - Scales with process better than typical digital circuits

Processing -- on-chip DSP vs. FPGA

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- FPGA gives “unlimited” flexibility and upgradeability – but...
  - Limitations with I/O bandwidth even in next-generation FPGAs
  - One ADC/DAC needs 40-48ch 11Gb/s SERDES channels
    - Or 16ch 32Gb/s SERDES in future
  - FPGA power is high, memory capacity/bandwidth is relatively low
    - May not be able to process data even if it can be got onto chip
  - High cost for multichannel applications

- On-chip DSP/memory is much more efficient
  - ASIC power is typically 5x -10x lower than FPGA in same process
  - No need to get massive bandwidth data on/off chip
    - May still need external memory (DDRx? GDDRx?) for very big record lengths
  - Much lower unit cost per channel (10x or less) -- once you have chip...
  - Very large NRE investment needed ($5M-$20M including design)

Noise coupling – round up the usual suspects…

- Reduce aggressor (DSP logic) noise generation
  - Use intentional clock skew within each block and between blocks
    - Reduces peak current and spreads out in time ➔ >10x lower di/dt
  - On-chip (~300nF) and low-inductance (~4pH) in-package decoupling
    - Even with this can expect >100mVpp supply ripple (see later…)
- Increase victim (ADC/DAC analogue) immunity
  - Fewest possible noise/jitter sensitive circuits, all fully differential
  - Lots of on-chip (~100nF) and low-inductance in-package decoupling
    - For 100fs jitter and delay sensitivity of 1ns/V, need 100uV of supply noise
- Improve victim-aggressor isolation
  - Build “nested walls” of isolation with most sensitive circuits in the middle
    - 100mV digital noise + 100uV analogue noise ➔ 60dB isolation
    - Wideband noise coupling (DC to many GHz) not narrowband like RF – tricky…
- Result : <1dB measured SNR degradation due to digital noise

Package and PCB design

- 1mm pitch FCBGA, >1000 pins, ~20 internal layers
  - Test chips use 100G production package to ensure same performance
  - Low-loss high-TCE LTCC (12ppm/C) for improved second-level reliability
- Multiple power/ground regions and shields for noise isolation
- Ultra-low-inductance internal decoupling for supplies and bias/ reference
  - Multiple VDD/VSS planes connect chip to multi-terminal decouplers
  - Noise dealt with inside package ➔ simplifies customer PCB design
- Coaxial via and waveguide structures, <1dB loss at 20GHz
  - Ground planes removed above signal balls to reduce capacitance
  - Increased layer spacing (wider tracks) to reduce losses
- Optimized launch to G-S-G coplanar waveguide on PCB
  - Balls next to signals removed to reduce parasitic, PCB grounds cut back
  - PCB uses Megtron 6 (very low loss, lead-free multilayer compatible)

Chip-to-package transition : S11 < -20dB to ~100GHz

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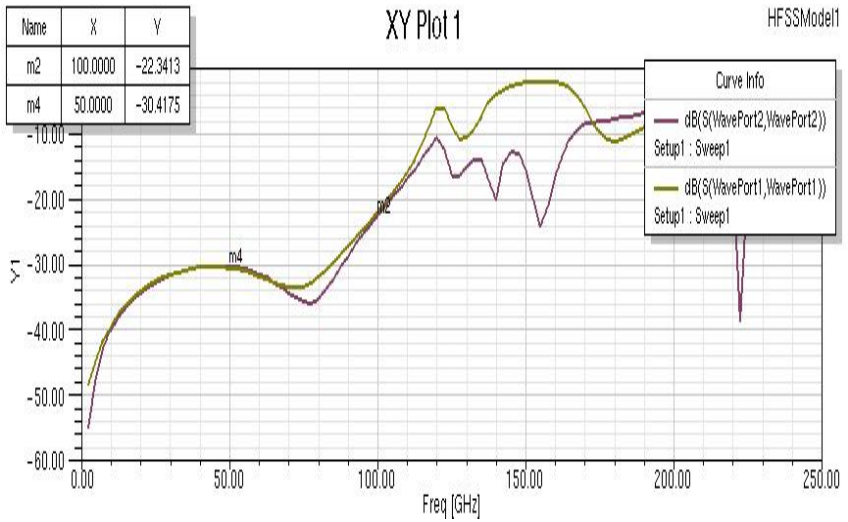
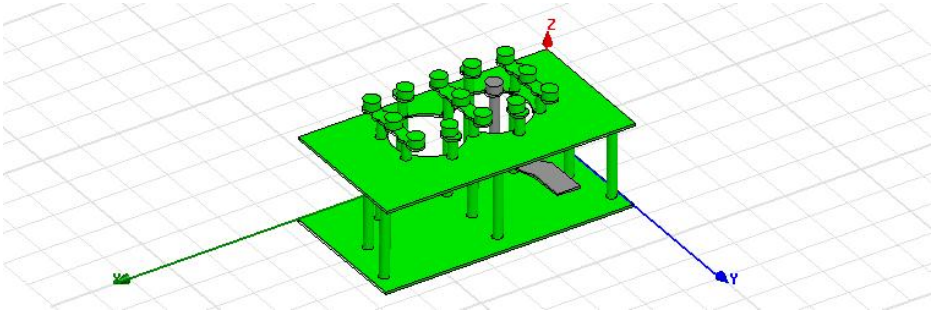
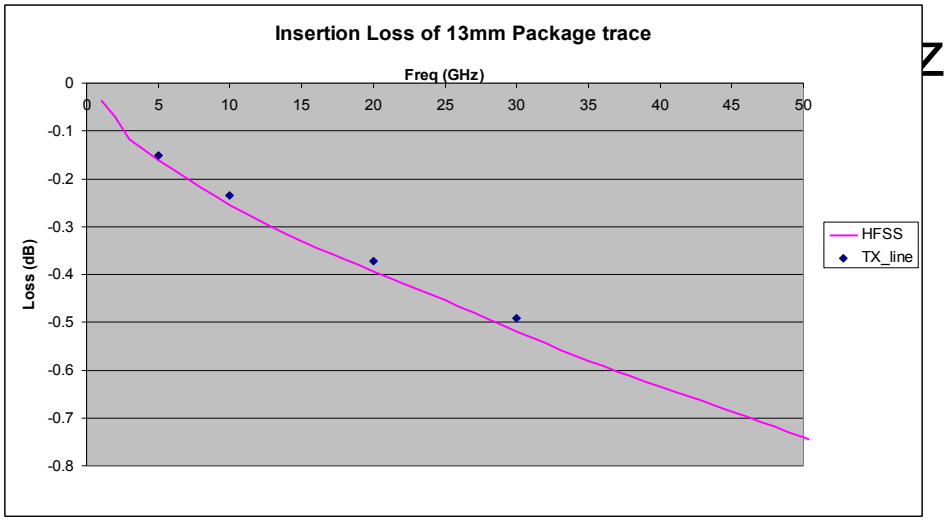
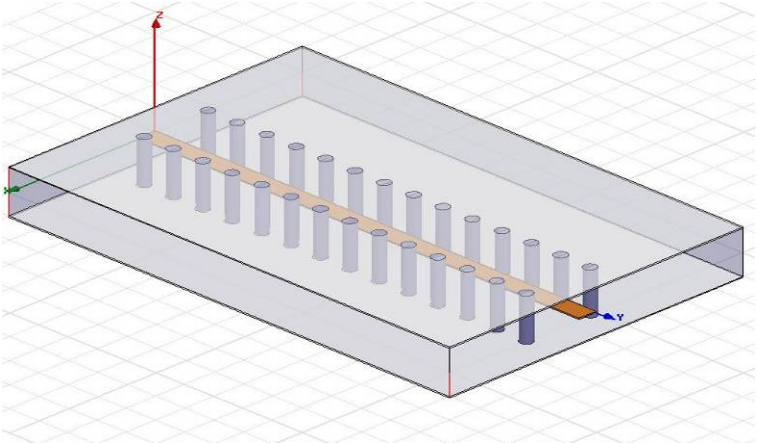
ADC Bump-Pkg Transition









Package-to-PCB transition : S11 < -20dB to ~50GHz

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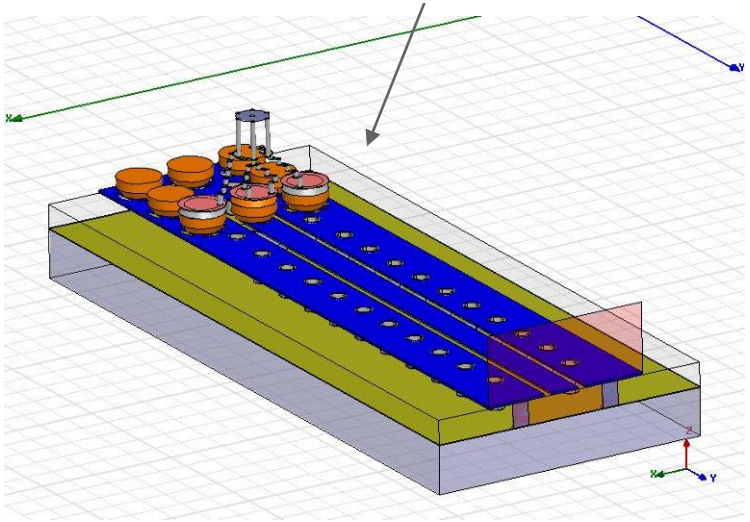
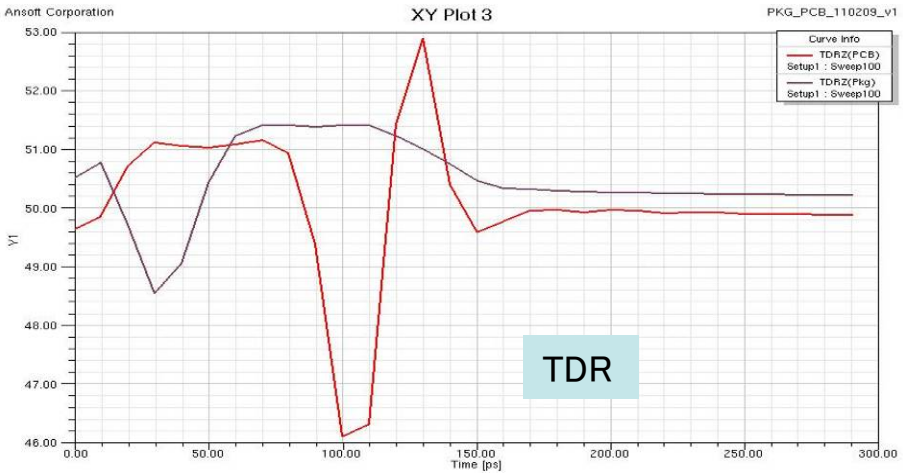
ADC Pkg-PCB Transition

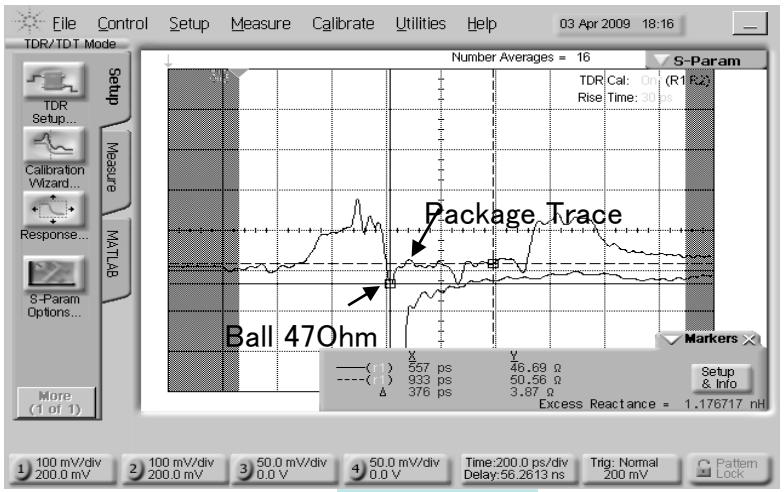
S11

HFSS sim model



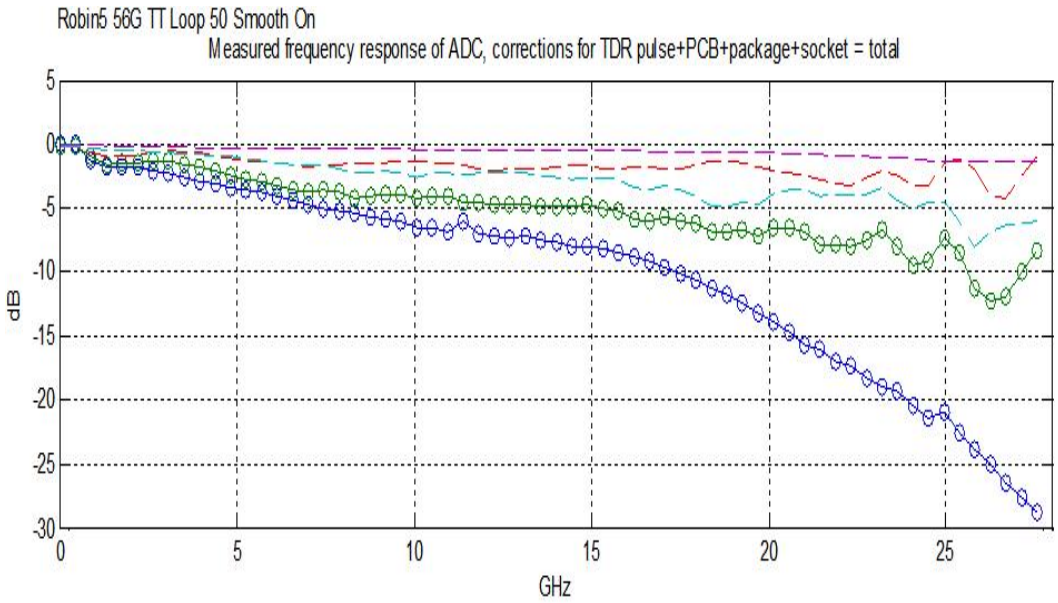


TDR

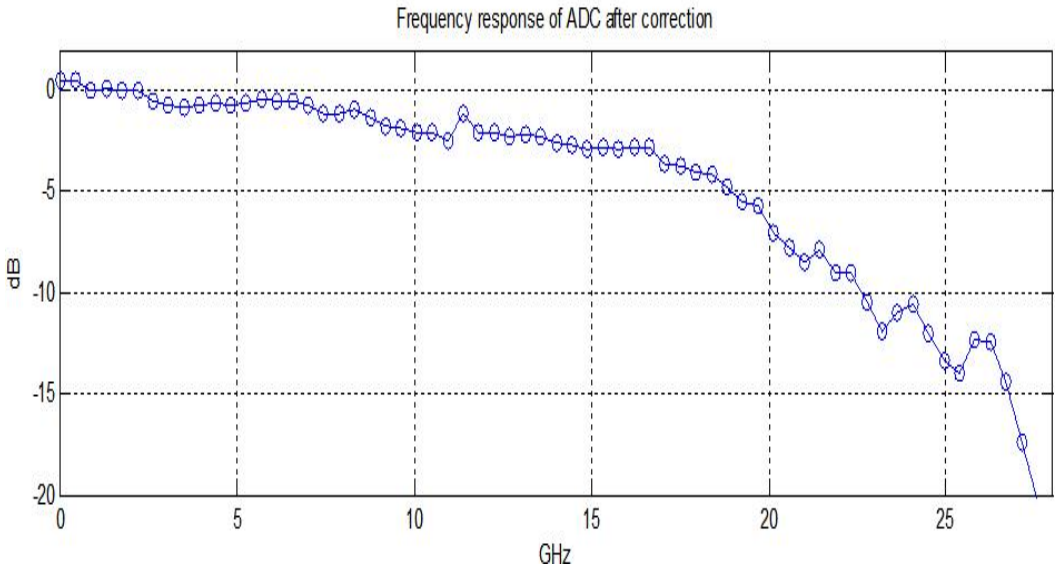


Measurement

Frequency Response (test setup and 56Gs/s ADC)

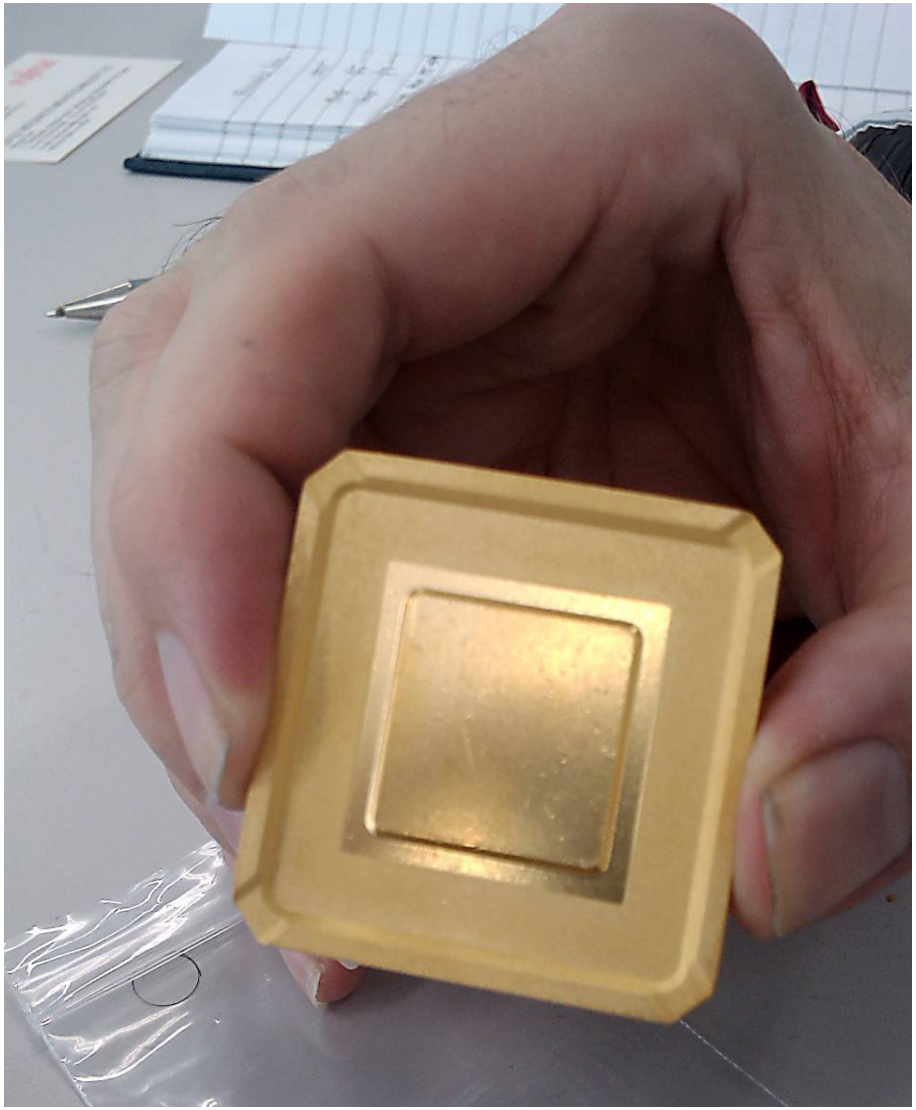


- Frequency response of test setup
  - TDR step (measured)
  - Batboard PCB (measured)
    - ENIG not Ag finish (Ni is lossy!)
  - Socket (estimated -1dB @ 20 GHz)
- Test setup loss bigger than ADC loss!



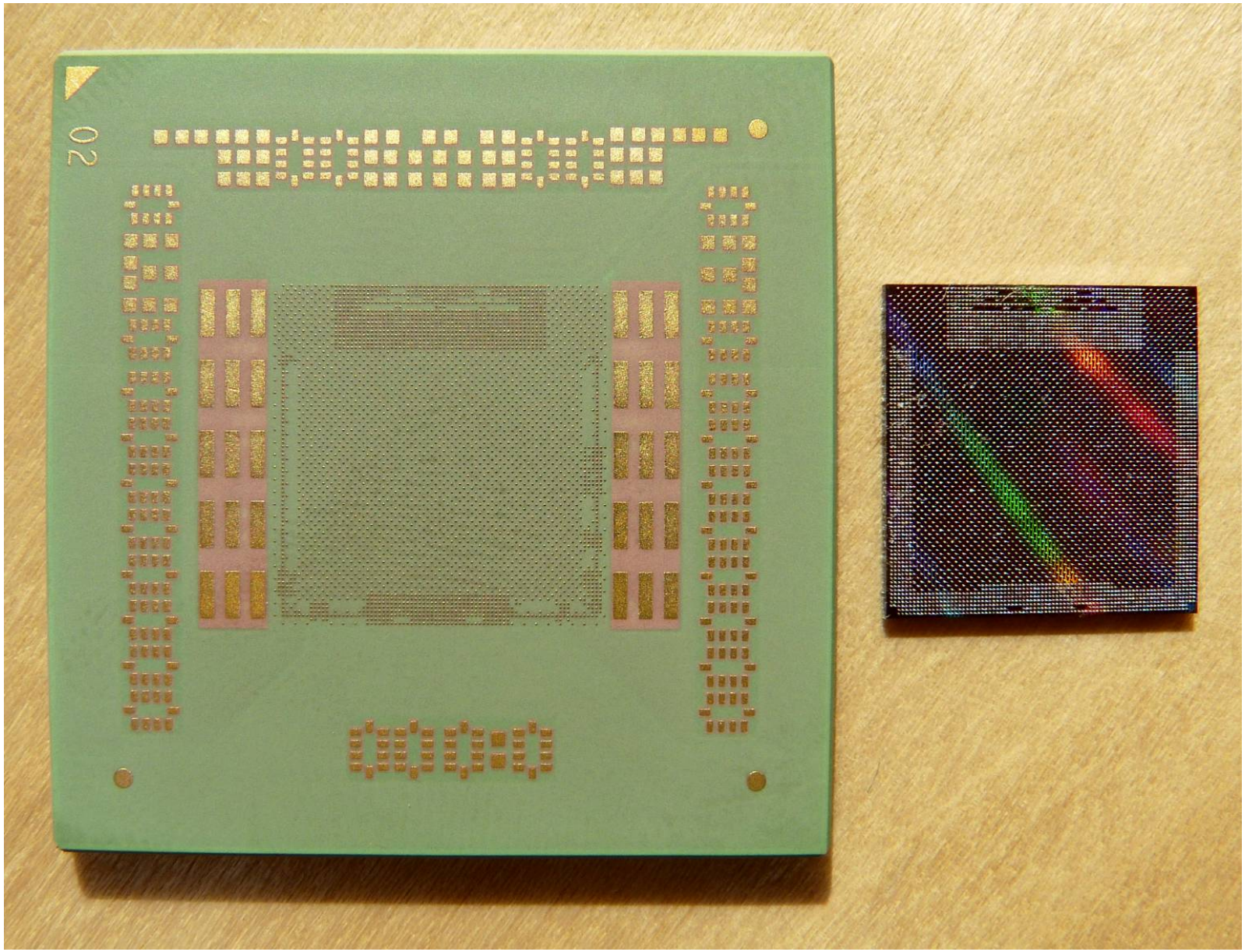
- Corrected ADC frequency response
  - accurate measurements are not easy ☹
- ADC -3dB bandwidth 16GHz
  - close to simulation and specification

A “gold-plated” package solution…



- Advanced package technology originally developed for server CPU
  - It’s nice to have in-house packaging ☺
- High-reliability Hi-TCE LTCC package
  - >2000 thermal cycles
- In-Ag TIM and gold-plated AlSiC lid
  - Very strong reliable chip-lid bond
  - All-metal path for heat transfer
- Very low thermal resistance
  - Theta-jc <0.2C/W (JEDEC)
- Package structure and design changed for better noise isolation

Example 100G chip and HiTCE LTCC substrate



ADC and DAC standard products / test chips

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- 56 Gs/s 65nm 4-ch ADC standard product “Blackbird”
  - Targeted at test and measurement applications
    - On-chip RAM, digital processing, 11Gb/s SERDES outputs
  - Available in 2011/2012 for design-in to systems
    - Also available as commercial digitiser board/module through industry partner
- 55-65Gs/s 40nm 4-ch DAC test chip “Leia”
  - Targeted at 100G/400G optical transport (also test/measurement etc.)
    - On-chip RAM (v1), digital processing +11Gb/s SERDES inputs (v2/v3)
  - Samples available for prototyping in 2012
- 110-130Gs/s 28nm ADC/DAC test chips in development
  - Exact configuration not fixed yet, depends on customer feedback
    - On-chip RAM (v1), digital processing + 30Gb/s SERDES I/O (v2/v3?)
  - Samples available for prototyping in 2013

“Blackbird” -- high speed ADC standard product

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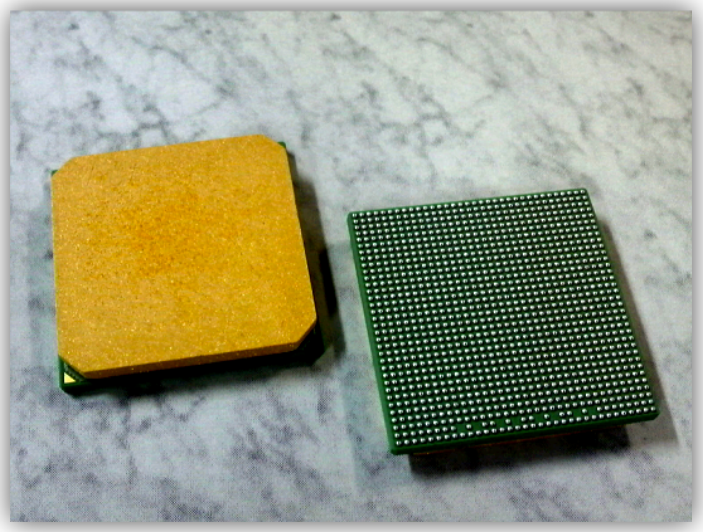
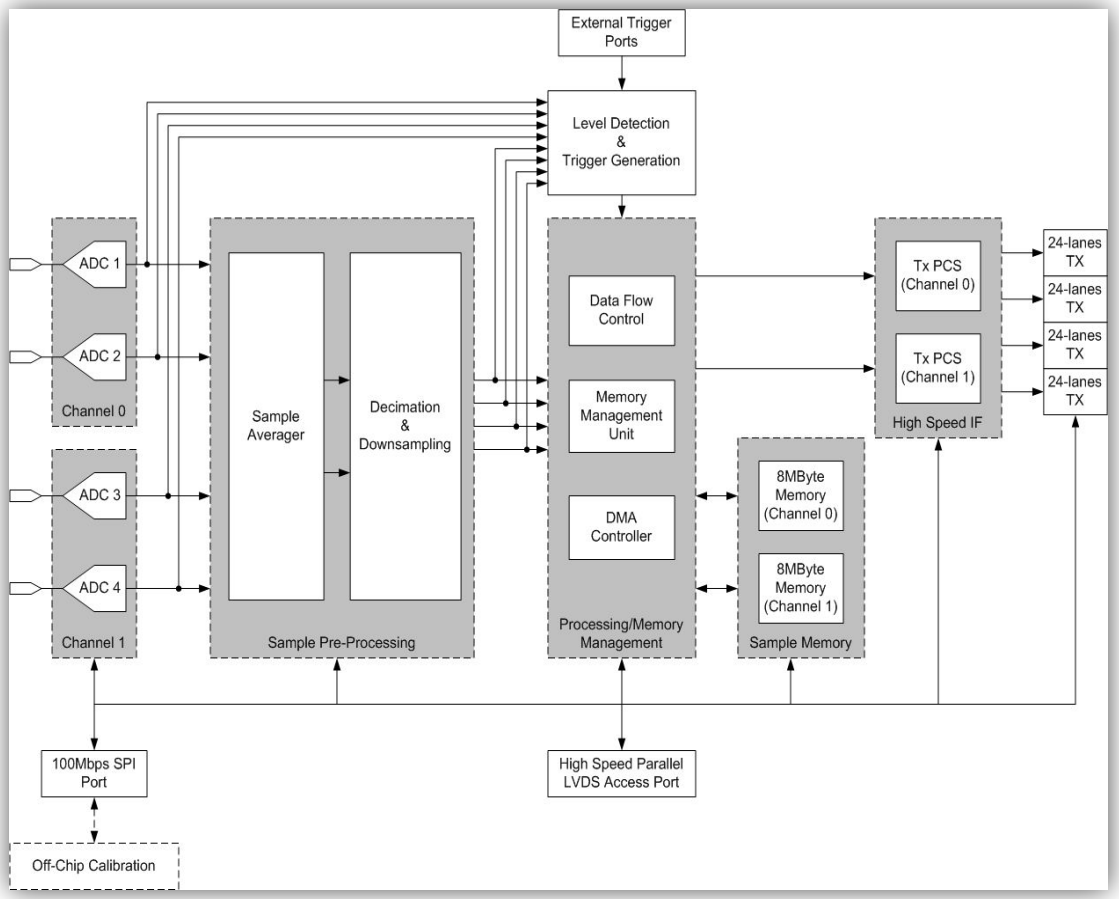
- Fujitsu CHAIS ADC macro made 100G coherent transmission and many other high speed solutions feasible for the first time
- Following on from this:
  - 40nm 65GS/s ADC macro provides more speed and 40% less power consumption
  - 65nm 56GS/s ADC macro is turning into standard product in FCBGA packaging
- ADC standard product “Blackbird”
  - Includes both offline and online data streaming
  - Many features useful for different systems
- Available in 2012
- Future roadmap to 110-130Gs/s in 2014 (est.)



Blackbird block diagram



Power estimation

- Total device power around 45w
- Power in ADC, memory, TX
  - 4 ADCs at full rate ~ 9w
  - Memory around 6w
  - 1.5w for every 12 channel (1 clock, 1 de-skew, 10 data) TX macro
  - clocking, decoding, routing and additional logics

Blackbird – Features (1/2)

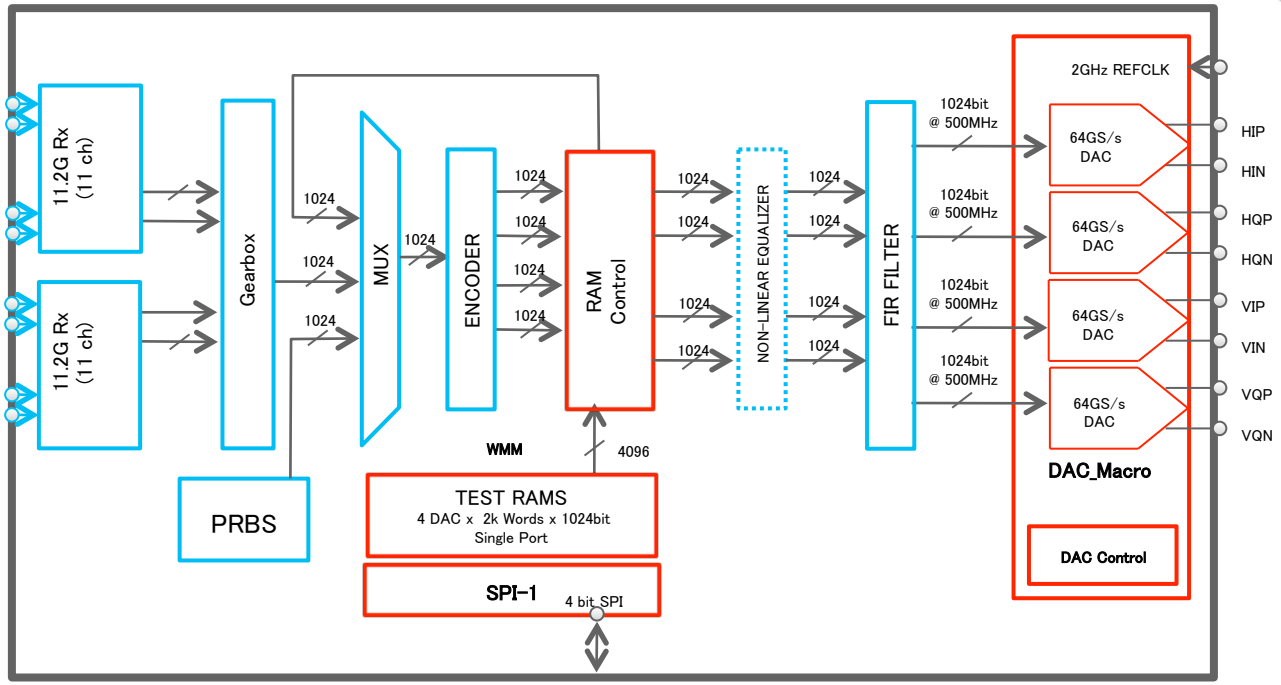
- 4 x 56GSa/s ADCs with independent input channels,
  - supporting 56GSa/s (full rate)
  - 28GSa/s (half rate) sampling mode
- 16MB (128Mbit) of high density SRAM for on-chip (configurable 8M per ADC or 16M for single ADC)
- Full rate online streaming for 2 ADCs (half-rate for 4 ADCs)
  - 4 x 24 lanes of CEI-11G compatible Transmit interface (10.3Gbps - 11.2Gbps)
  - Source synchronous interface with differential clock and sync per 10 data lanes
- Sample averaging improves overall system SNR up to 6dB
- Sample rate reduction
  - 39-tap programmable symmetrical FIR filter for each ADC channel
  - Decimation by 2 (28GS/s)
  - Down sampling factor 2 to 128 by dropping samples

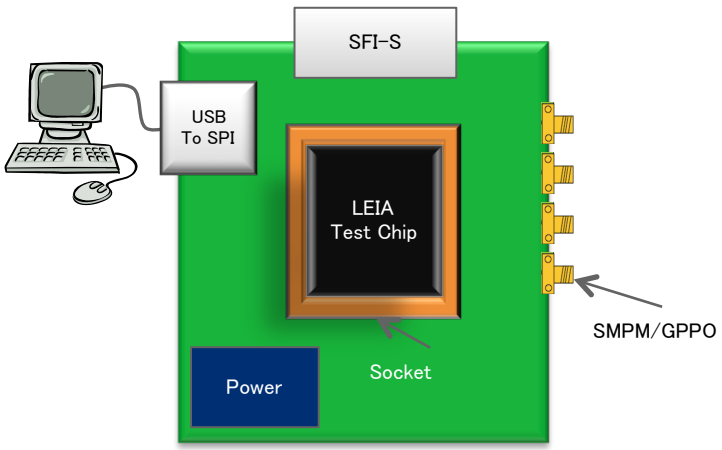
Blackbird – Features (2/2)

- Level detection and triggering
  - Triggering using 2 ADCs or 8 bi-directional trigger signals for external triggers
  - Glitch / Threshold / hysteresis trigger (improved triggering in noisy environment)
  - Pre and post trigger sample storage with user programmable record size for storage of multiple events
- Physical coding sub layer (PCS)
  - 64b/66b encoding and scrambling (allows static data)
  - Link training for startup / alignment
  - Ensures valid data transfer to FPGA or ASIC through high speed serial links
  - Power saving mode available for unused serial lanes
- Optional FEC (Forward Error Correction) for BER improvement (<1e-15)
- Device configuration and programming
  - SPI or high speed LVDS parallel port (437Mbps)

LEIA 55-65Gs/s DAC Test Chip

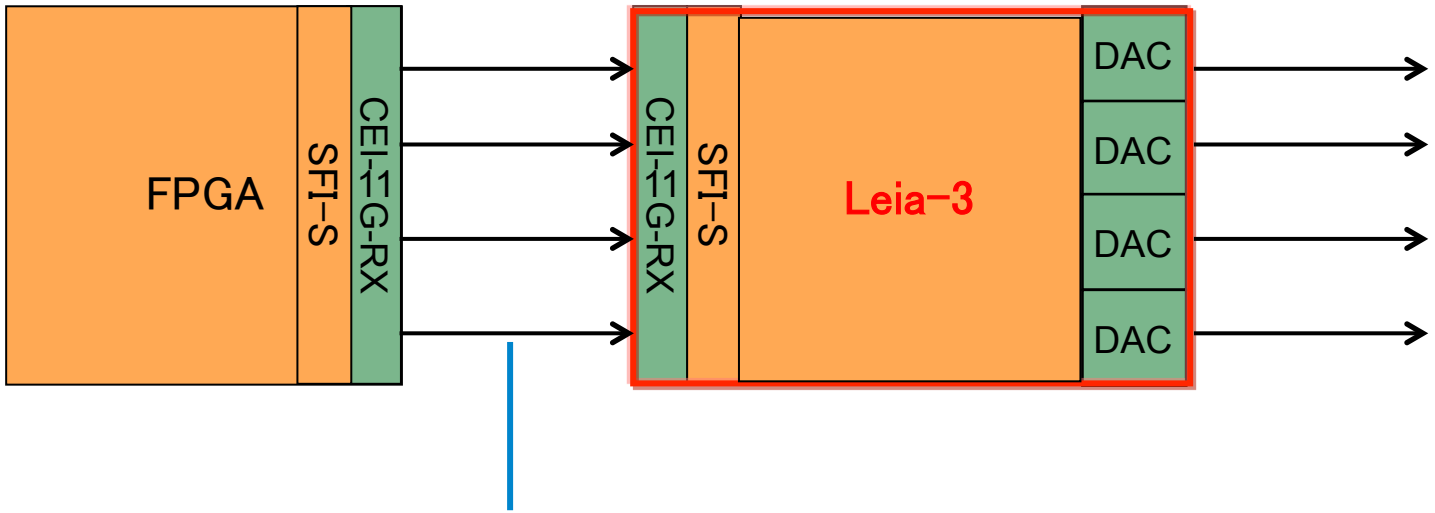
- Leia1 Test chip drives DAC macro from Waveform memory
  - No need for FPGA
  - Memory for 256K 8-bit samples
  - Available September 2011
- Leia2 Test chip drives DAC macro from Waveform memory, high speed IO or both
  - Input real-time data
  - Drive one DAC at full rate
  - 2 DACs at half-rate
  - 4 DACs at quarter-rate





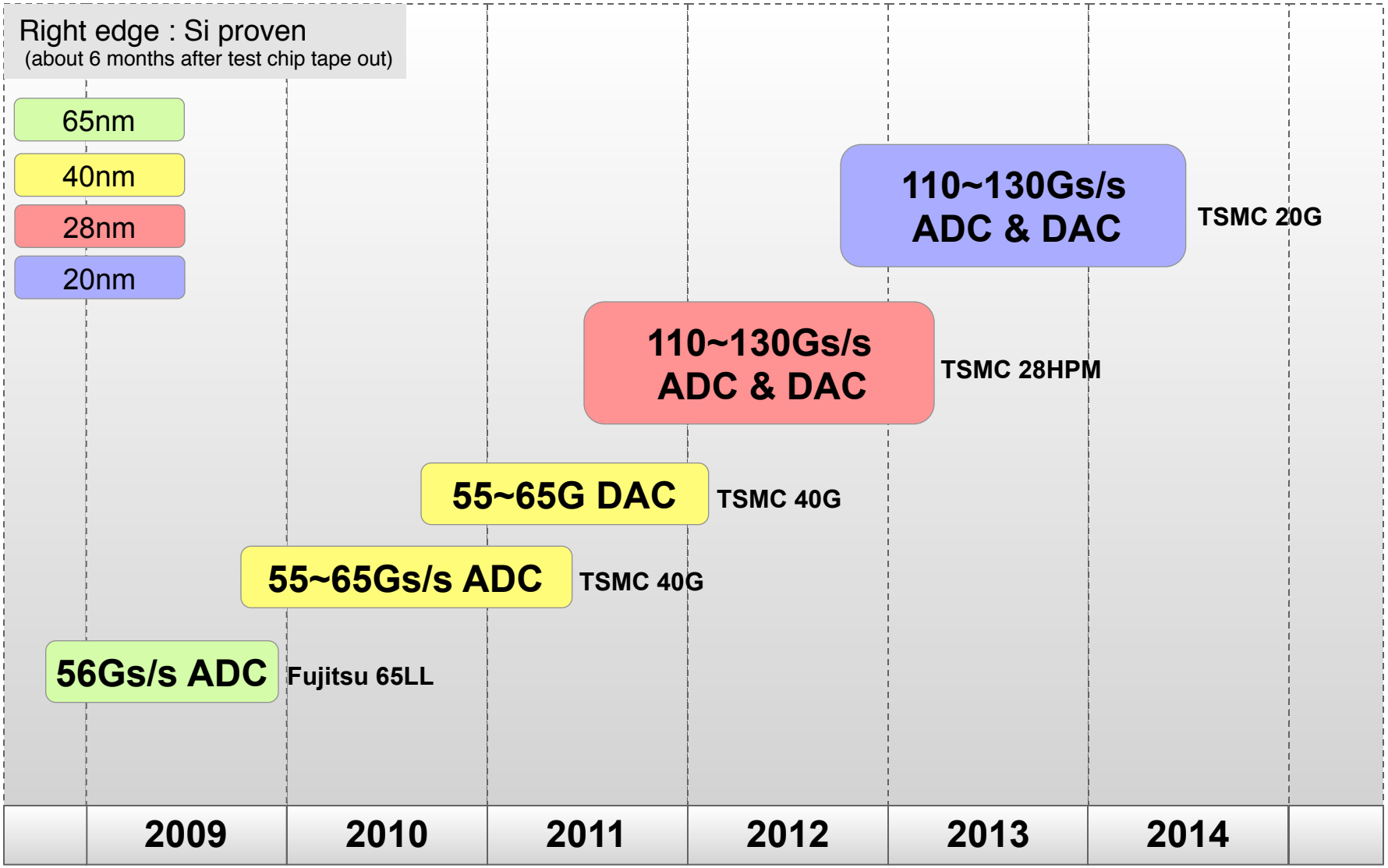
- LEIA-DK will drive 4 DAC Channels
- USB interface to PC
- Driven using intuitive GUI
- SMPM/GPPO outputs
- Choice of board with socket or solder mounted test chip
- Mains powered
- Available September 2011

LEIA 55-65Gsps Arbitrary Waveform Generator



1, 2 or 4 SerDes-macro
10, 20 or 40 data lanes at up to 12.8Gbps each
offering up to 512Gbps data feed to Leia3
Leia3 output = 1ch * 64Gsps
(or 2ch * 32Gs/s or 4ch * 16Gs/s with FIR on-chip interpolation)

CHAIS ADC/DAC Roadmap



What are the limits for CMOS ADCs?

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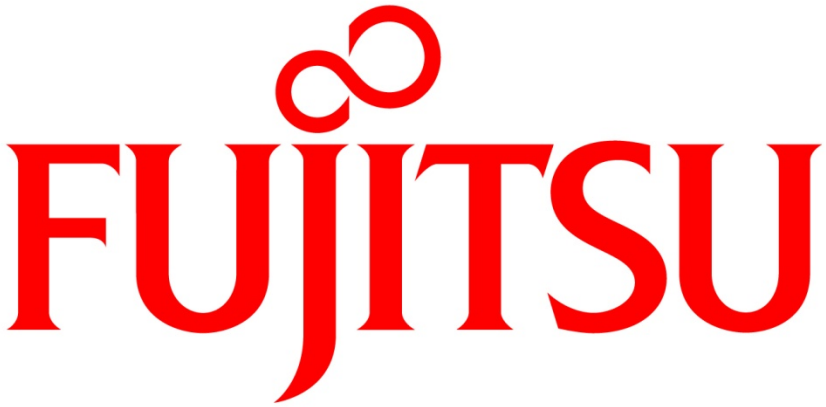
- How close can ADCs get to theoretical speed/noise limits?
  - 130Gs/s already on roadmap for 28nm CMOS
    - Circuits portable to 20nm, 15nm, … (speed increases each time)
  - Higher ENOB achievable with circuit refinements
    - How many ENOB are really useful given front-end dynamic range?
- What limits bandwidth?
  - Sampler BW is not close to fundamental performance limit of transistor
    - ESD protection – a “conventional” ASIC needs *some* ESD immunity ☺
- How about sampling clock jitter?
  - Not a limit right now (~50fs rms), really only set by VCO power
  - Should be OK even for higher BW and more ENOB
- ADC performance is not the main limiting factor
  - For many applications, getting access to the technology is the real issue



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