R&D Research Lines at IGFAE/USC

Instrumentation for the future of particle, nuclear and astroparticle physics and medical applications in Spain

Barcelona March 2023

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IGFAE/USC

Outline

- Solid State Detectors (DRD3)
- Electronics and Data Processing (DRD7)
- Particle identification and Photon detectors (DRD4)
- Infrastructure
- Research Team
- Summary

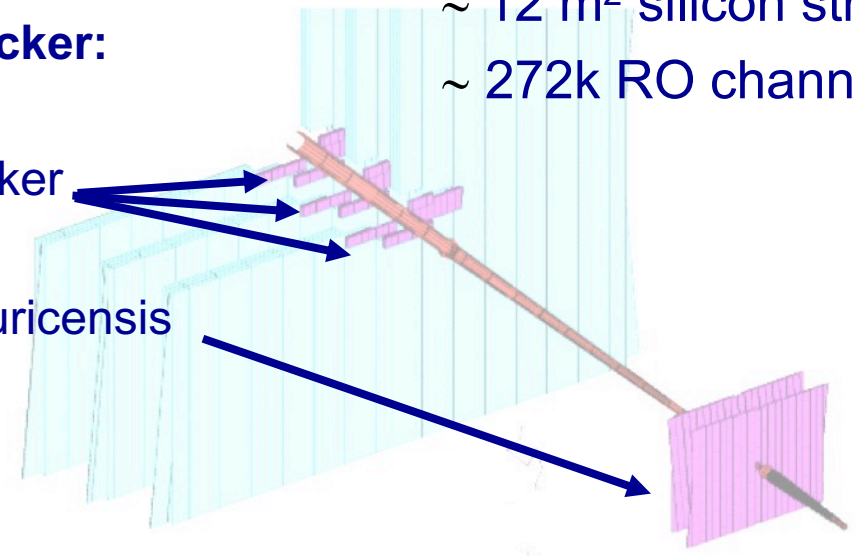
Solid State Detectors (DRD3): Expertise I

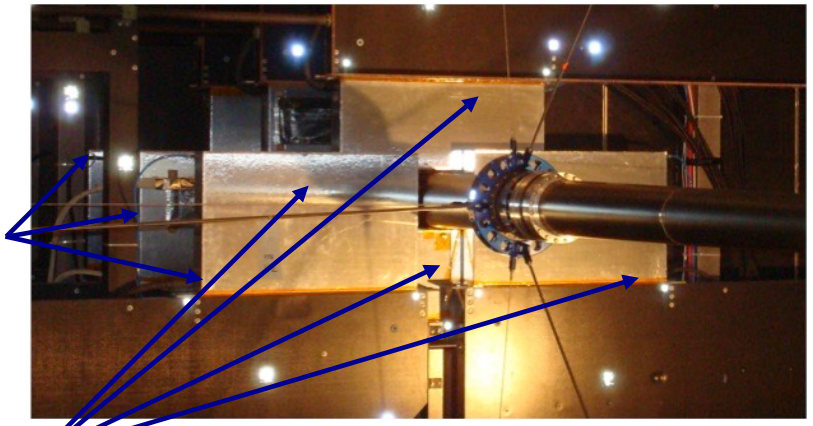
- **Construction, assembly and installation of LHCb Inner Tracker:**
  - Bonding and Burn-in of LHCb Inner Tracker (IT) detector modules
  - Control Electronics of Silicon Tracker (TT+ IT)
  - IT Faraday cages design and production
  - Silicon Tracker Low and High Voltage systems
  - Silicon Tracker ECS (PVSS, WinCC)
- **Operation, coordination and maintenance of Silicon Tracker, during LHCb experiment data taking (2008-2018):**
  - Project Leader ST (2011-2014)
  - Deputy Project Leader (2009-2010, 2015-2017)

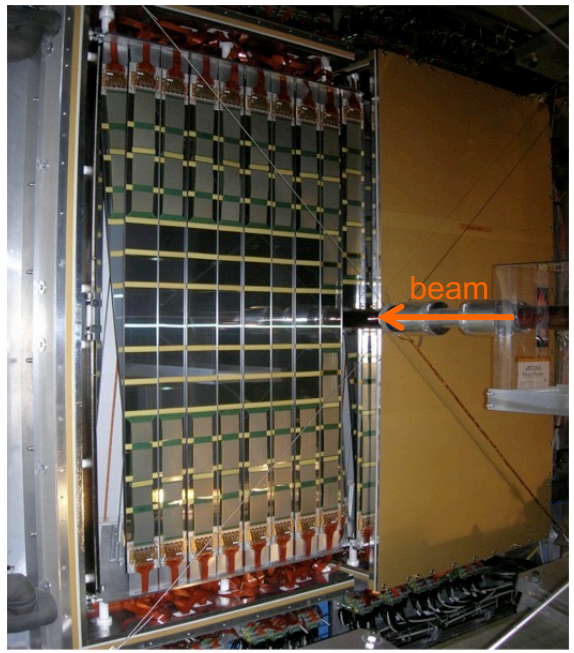
Silicon Tracker:

~ 12 m^2 silicon strips

~ 272k RO channels

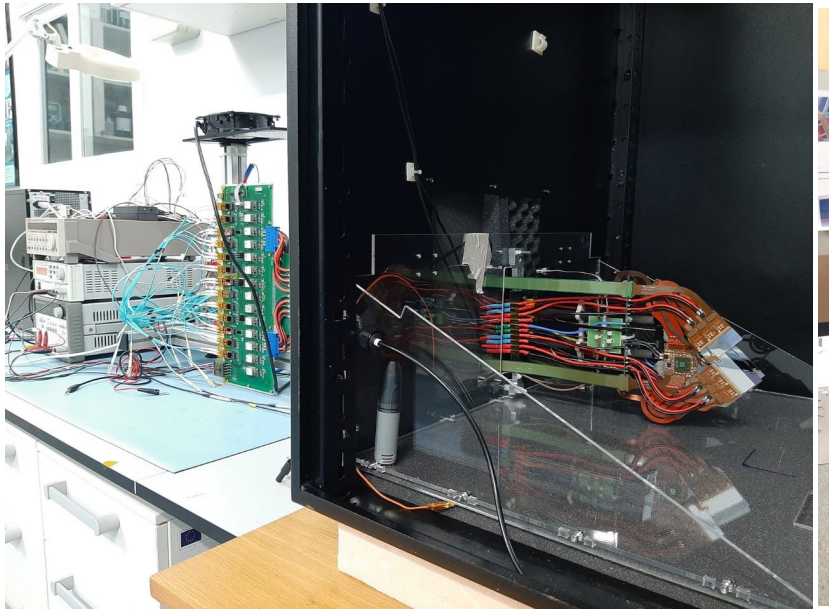


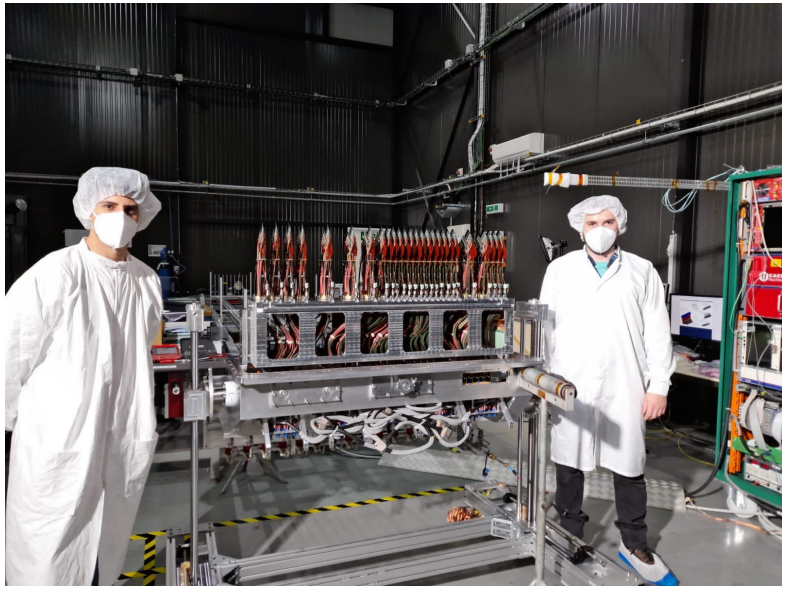


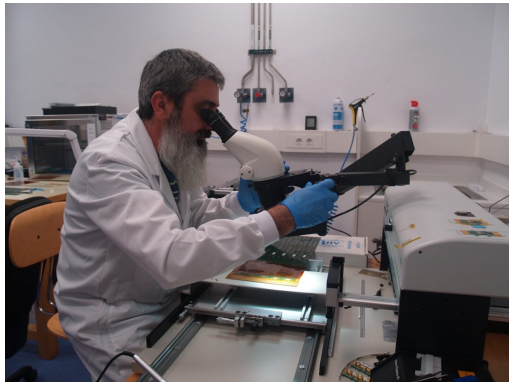


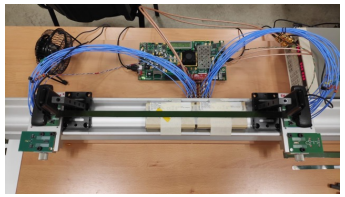
Solid State Detectors (DRD3): Expertise II

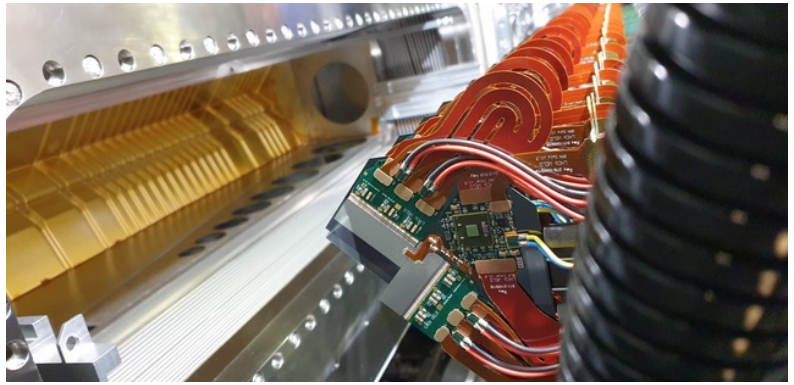
- **Design, construction and installation of LHCb Upgraded VELO:**
  - R&D sensors, FEE and BEE (2008 – 2018)
  - VeloPix ASIC verification (SEE, TID, funcionalities)
  - VELO readout system developments:
    - DAQ, Control and Synch firmware
  - VELO detector Design, Construction and QA:
    - 320 High-speed data links (D,C,QA)
    - 190 High Voltage tapes (C,QA)
    - 52 Vacuum Feedthrough and Optical Power Boards (C,QA)
  - Validation of a complete VELO slice
  - VELO installation
  - VELO commissioning and calibration
- **Project Coordination:**
  - VELO Commissioning coordinator (2023-)
  - VELO FE/ECS/SOL_40 coordinator (2023-)
  - VELO electronics and DAQ coordinator (2018-)
  - Deputy project leader VELO Pixel Module-0 WP (2012-2014)
  - Project leader VELO micro-strip project (2010-2012)









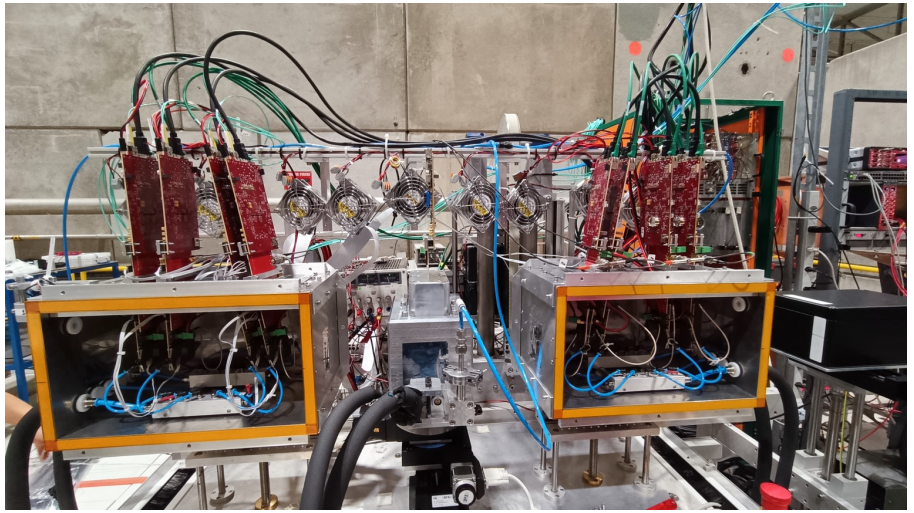


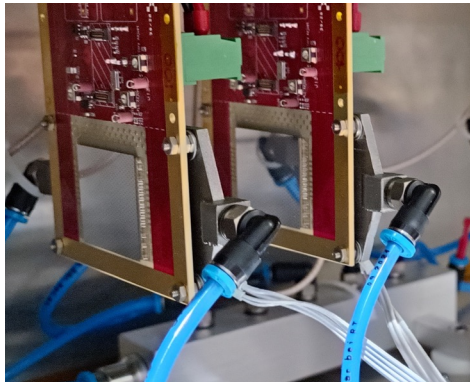
Solid State Detectors (DRD3): Future

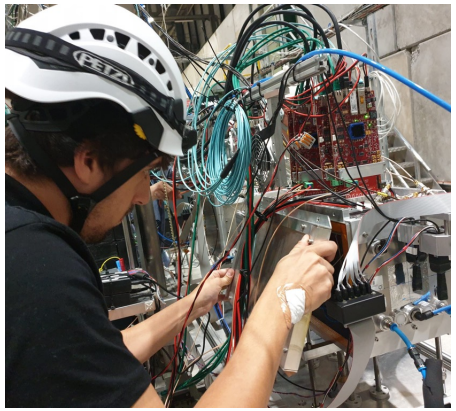
- **Vertexing at HL-LHC (4D-tracking)**
- **Requirements:**
  - High spatial resolution (small pixel size)
  - Ultrafast timing (O(10) ps)
  - Low material budget
  - Radiation hardness
- **<u>Interests</u> in improvements for**
  - Sensors (3D, iLGAD , thin planar…)
    - Production at CNM (thin planar TimePix4 finished, iLGAD April 2023)
  - ASIC, Front-End and DAQ
    - First tests with TimePix4 (65nm)
    - Following tests with PicoPix (28nm)

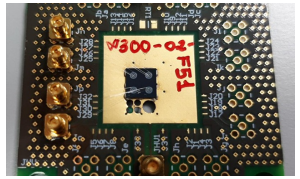
Solid State Detectors (DRD3): Present

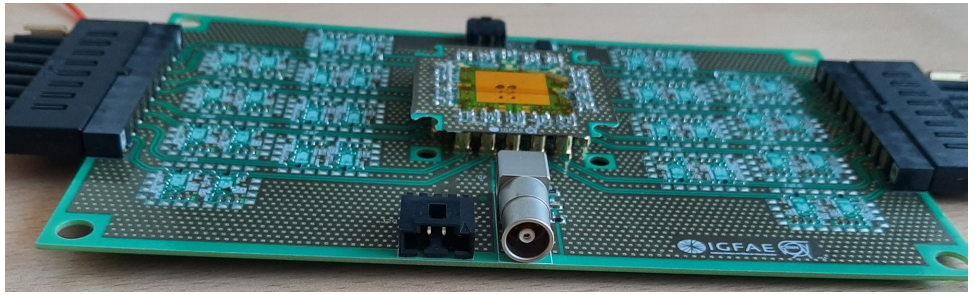
- **2022 CERN Test beams campaigns** (Sensors May-June, TimePix4 beam telescope July, October)*
- **Multichannel timing board****:
  - 16 Channel RB with first and second stage amplifiers integrated
  - 15 mm x 15 mm central opening
  - Use of miniaturized coaxial connectors. High life cycle
  - First and second stage SiGe Transistor
  - Sensor board
    - Quick sensor test around
    - Simplified probing and reduce sensor damage
    - Low material budget and easy alignment











- **AIDAinnova — H2020-INFRAINNOV-2019-2020 (GA : 101004761) (2021-2025)**
- **Collaboration and synergies with: IFCA, CNM, IFIC, IFAE**

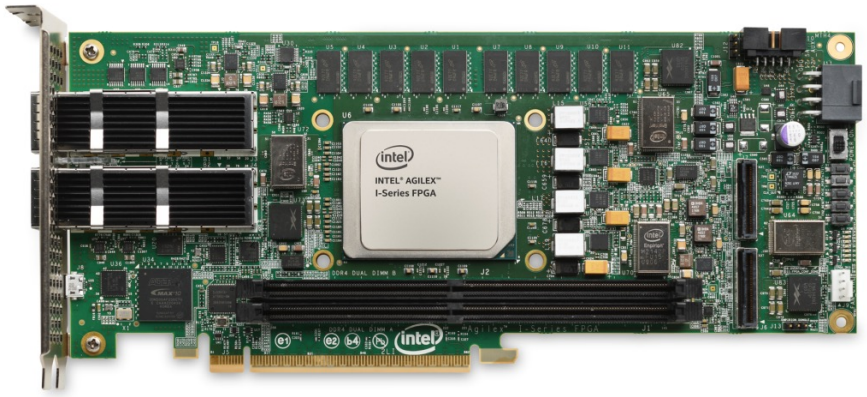
(*) E. Rodríguez. Trento Workshop 2023

(**) E. Lemos. Trento Workshop 2023

Electronics and Data Processing (DRD7): Future

Based on the experience in electronics, ASIC verification and FPGA design for the VELO and Silicon Tracker in the past we are interested in:

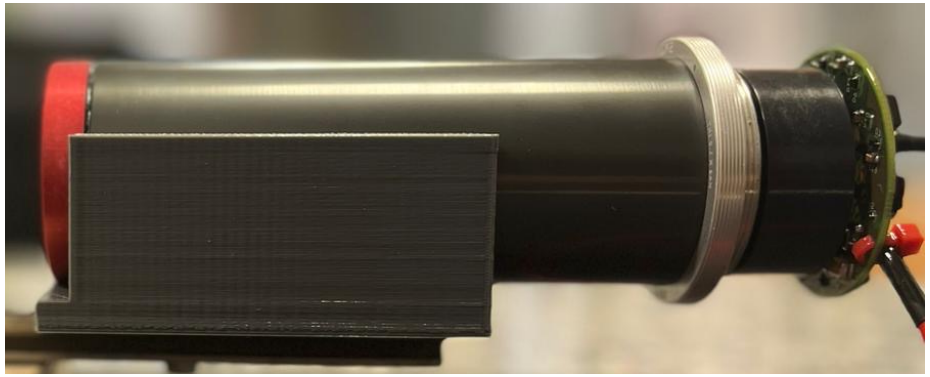
- **Detector electronics for 4D-tracking**
  - Back-End readout and control electronics
  - Front-end electronics integration
- **ASICs for 4D-tracking:**
  - PicoPix DAQ FPGA design
    - Using new CERN 26Gb/s link (DART28)
  - Development of ASIC emulation platform based on FPGAs
    - Devoted to study new ASIC digital architectures beyond PicoPix (VeloPix 2)
  - Digital ASIC design



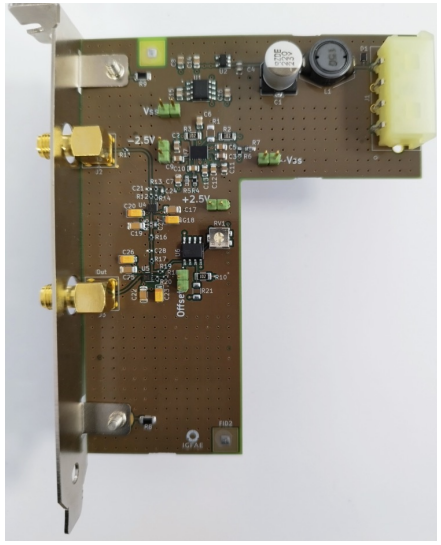
FPGA used for PicoPix DAQ and emulation platform

Coaxial prompt-gamma ray monitoring for proton therapy in vivo range verification (Collaboration with IFIC)

- IGFAE contribution:
  - Detector and DAQ design
    - PMT active voltage divider design for running at 10Mcps without degradation
    - Accelerator interface board
    - Detector signal conditioning board
  - Detector modelling and iterative simulation
    - Crucial for precise range verification



Photodetector coupled to the active voltage divider designed at IGFAE



Detector signal conditioning board

Accelerator interface board

Infrastructures

Existing:

- Silicon Laboratory (Electrical tests, laser, radioactive sources, tests in vacuum, cold tests of irradiated sensors)
- Clean room (Wire bonding machine Delvotec MS17, Pull tester, Metrology)
- SMD Laboratory *(PCB design and assembly, BGA Rework)*
- Readout and DAQ laboratory (36 GHz scope, TDR 15 GHz, …)

Planned:

- New Laser facility: TPA-TCT for silicon sensors.

In construction:

- Metrology Laboratory
- Machining Workshop

Research Team

2 Senior staff:
A. Gallas, P. Vázquez.

2 PhD Engineers:
E. Lemos, A. Fernández.

2 Technicians:
A. Pazos, E. Pérez.

2 PhD students:
E. Rodríguez, I. García.

Summary

- Broad experience in silicon tracking and vertexing detectors at the LHC:
  - Sensor design and characterization
  - Readout electronics: ASIC, Front-End and Back End Electronics
- Interests in :
  - Solid State Detectors (DRD3)
  - Electronics and Data Processing (DRD7)
  - Particle identification and Photon detectors (DRD4)
- Goals:
  - 4D tracking in future colliders
  - ASIC digital design and emulation
  - Applications outside HEP: Medical Physics…

Backup Slides

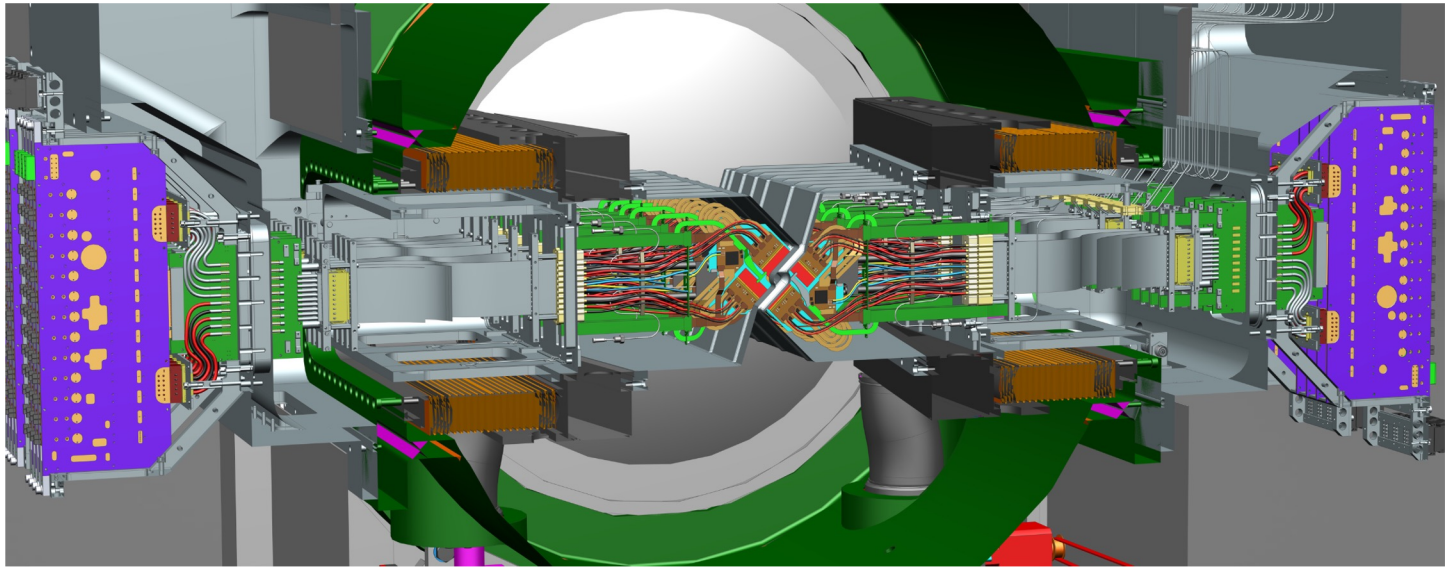
Research Team

	DRD3	DRD7	DRD4
A. Gallas	50 %	30%	20 %
P. Vázquez	30%	20%	50%
E. Lemos	40%	50%	10%
A. Fernández	10%	60%	30%
A. Pazos	40%	20%	40%
E. Pérez	40%	20%	40%
E. Rodríguez	80%	20%	
I. García	20%		80%

Instrumentation: LHCb VELO Upgrade I

- **Primary tracking and vertexing detector** surrounding the collision region
  - In high vacuum (separated from the LHC vacuum by a RF foil)
- **Pixel** technology (formerly r/ϕ silicon microstrip)
  - **More robust track reconstruction performance**
  - Better resolution
  - **Closer to beam (8.1mm to 5.1mm). Two retractable halves**.
- **Faster readout (1MHz to 40MHz)**
- New ASIC VeloPix, based on TimePix family
- New micro-channel evaporative CO_2 cooling
- Some figures:
  - 52 modules, 624 VeloPix ASICs
  - Detector active area 0.12 m^2
  - **~41 M pixels** (**55x55 μm^2**)
  - HV tolerance of 1000V
  - **Trigger-less readout ~2.9 Tb/s**
  - Highly non-uniform radiation (4MGy)

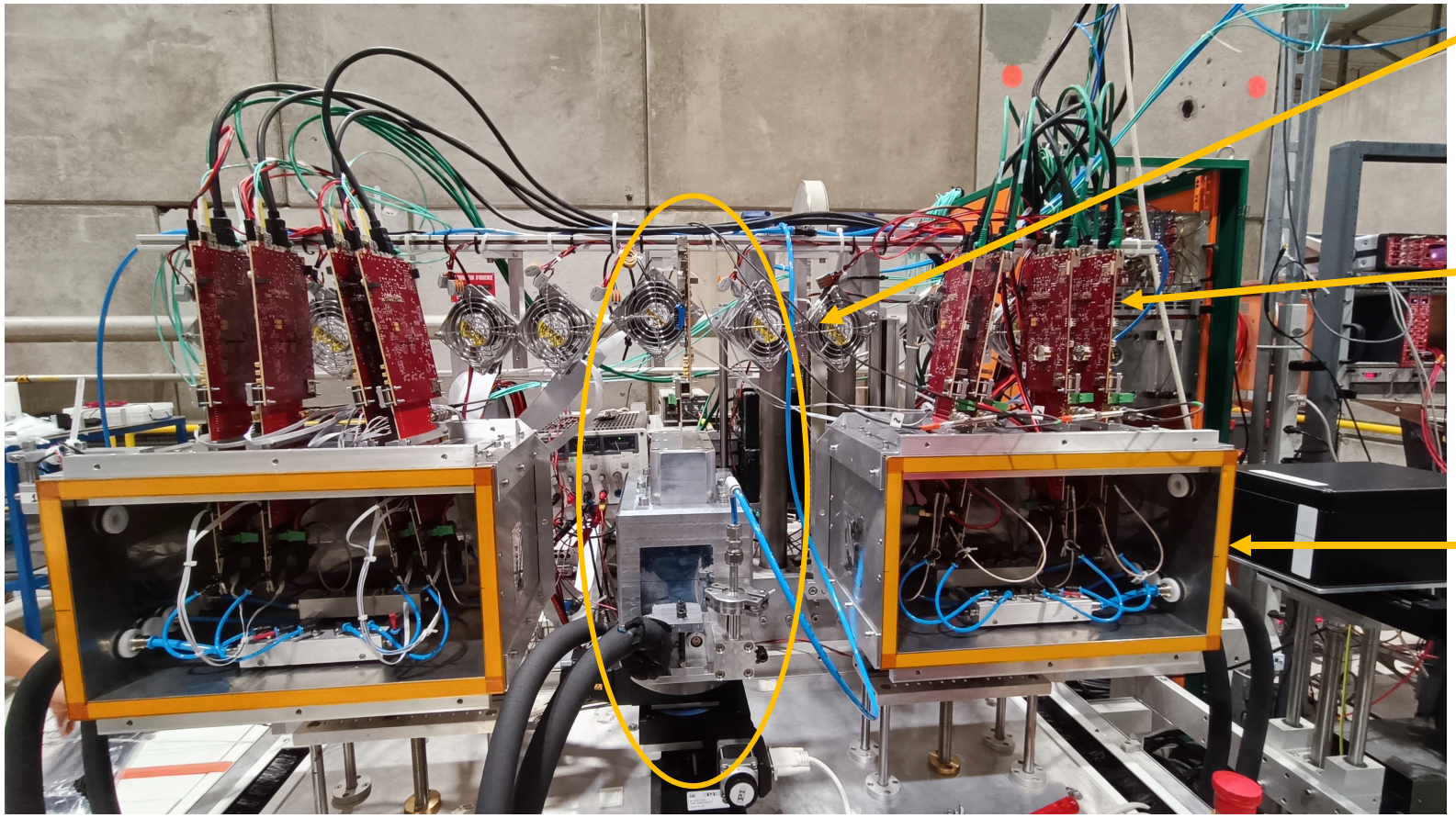
Feature	Old VELO	upgraded VELO
Sensors	R & Φ silicon strips, semicircular	Pixel sensors, L shape geometry
Maximum fluence	4.3×10^{14} 1 MeV neq cm^{-2}	8×10^{15} 1 MeV neq cm^{-2}
HV tolerance	500 V	1000 V
Readout rate	1 MHz	40 MHz
Total data rate	~150 Gb/s	~ 2.9 Tb/s
Power consumption	~ 0.8 kW	~ 1.6 kW
Operating Temp.	-8°C	-20°C



Instrumentation: VELO test beam @ CERN October 2022

8 tracking layers with Timepix4v2 ASICs:

- 4 with 300 µm n-on-p sensors (Advacam), at 9º pitch/yaw angle for better spatial resolution
- 4 with 100 µm n-on-p sensors (Advacam), at 0º angle for better time resolution
- 3 Scintillators + constant fraction discriminators & MCP + PicoTDC as reference timing
- DUT 50 µm n-on-p sensors (Advacam), in motor stage for angle studies



DUT assembly with motion stage

Read out by 9 SPIDR4 systems:
10 Gbit ethernet via fibre

Timepix4 assemblies in gas-tight and light-tight enclosure:
Allows operation at low(er) temperatures (better time resolution)