GIE ETSI Sevilla

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Resumen

- GIE-ETSI-Sevilla Group Description
- CERN Collaborations
- Mixed Signal ASIC's design
- DAQ Full Custom Systems Design
- Monolithic Detectors (MAPS) integral design
- Relevant funding sources

Group of Electronic Engineering, GIE, School of Engineering, University of Sevilla (established since 2003)

- 7 Engineering Degrees (Aeronautics, Telecomm,

Civil, Electronics, Industrial…)

- PhD. Courses in Electronics, Signal Processing and Communications

5500 undergraduate students

15 Ph.D. students in the Electronic Engineering Dpt.

55 researchers in Group of Electronic Engineering (GIE):

-Analog and Digital VLSI design

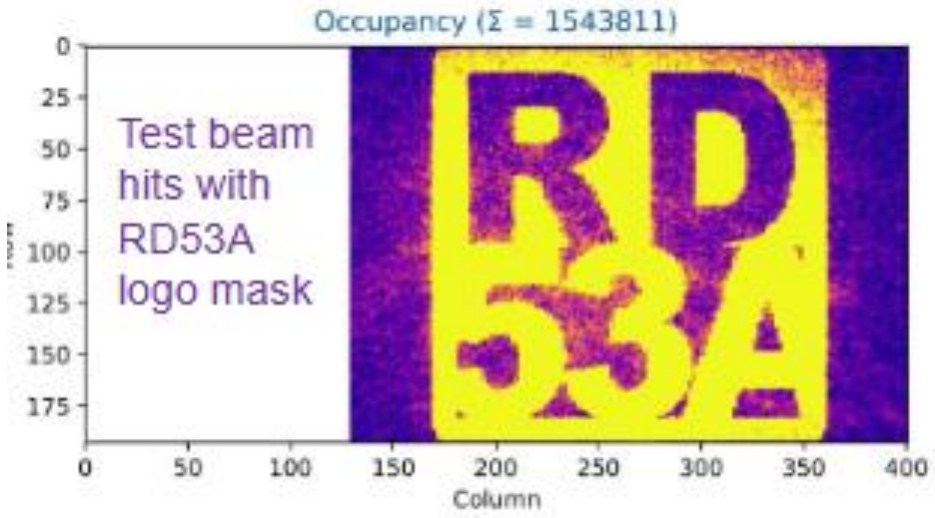
-Radiation and μElectronics

We work in microelectronics design, digital systems design (ASIC & FPGA), microelectronics design for radiation environments, pixel readout chips and monolithic detectors (MAPS). 8 senior researchers on tasks related to instrumentation for High Energy Physics, the other researchers devoted to other research projects. Strong collaboration with companies in Andalucía and Madrid, with emphasis in aeronautical and space projects.

CERN Collaborations

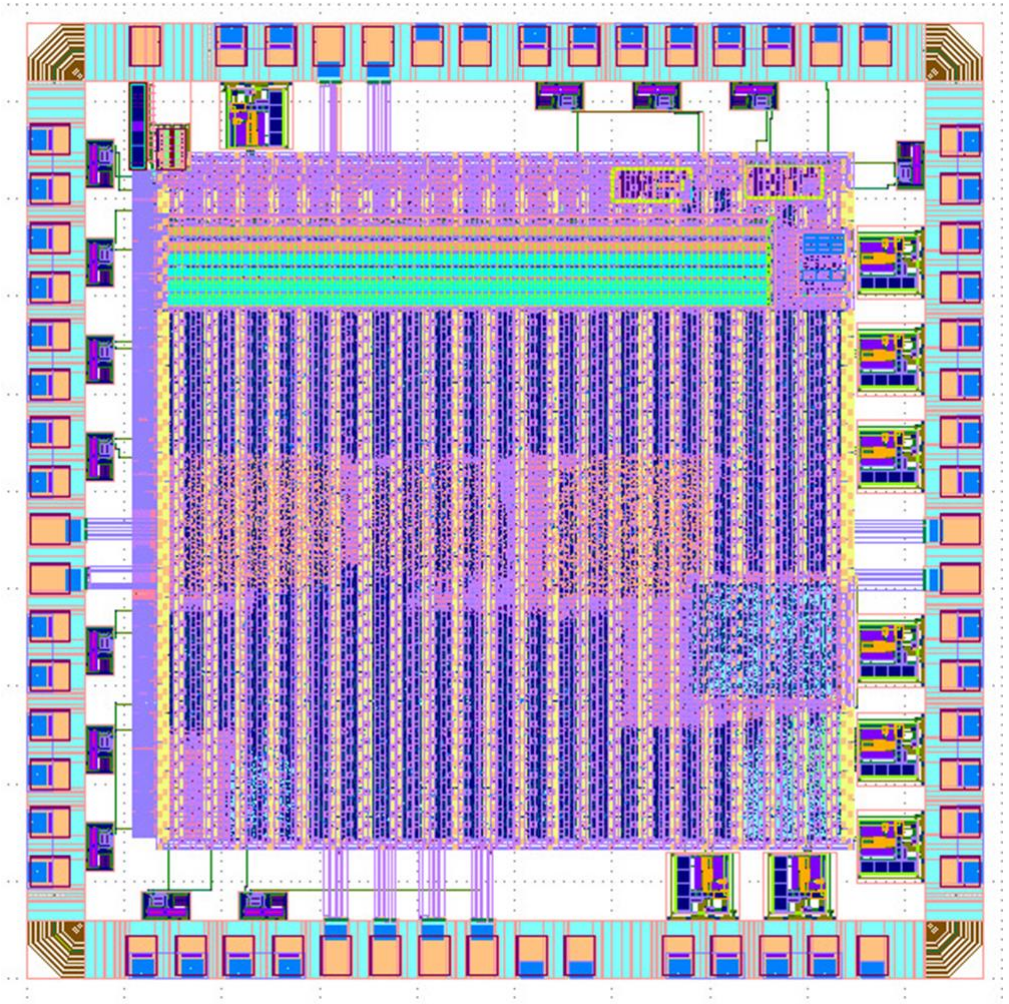
- RD50 since 2012, ongoing towards DRD3
- RD53 since 2014 up to completion (2023)
- CMS Associated Technological Institute (introduced by IFCA), ongoing

RD50

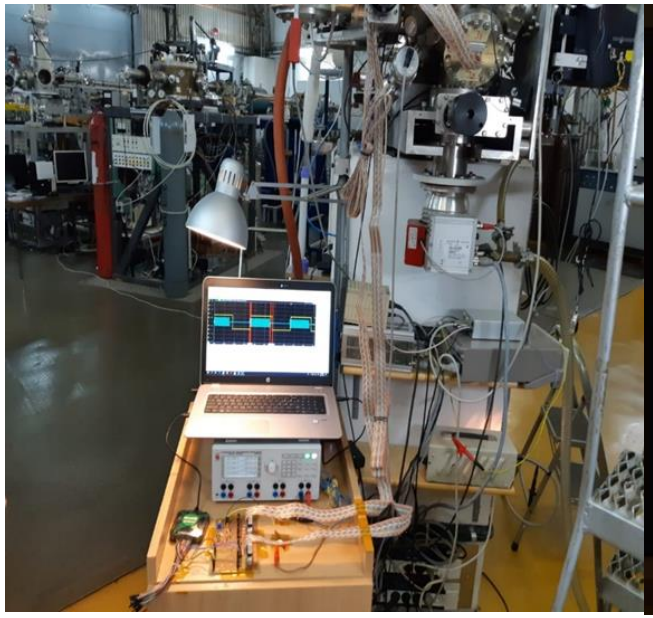


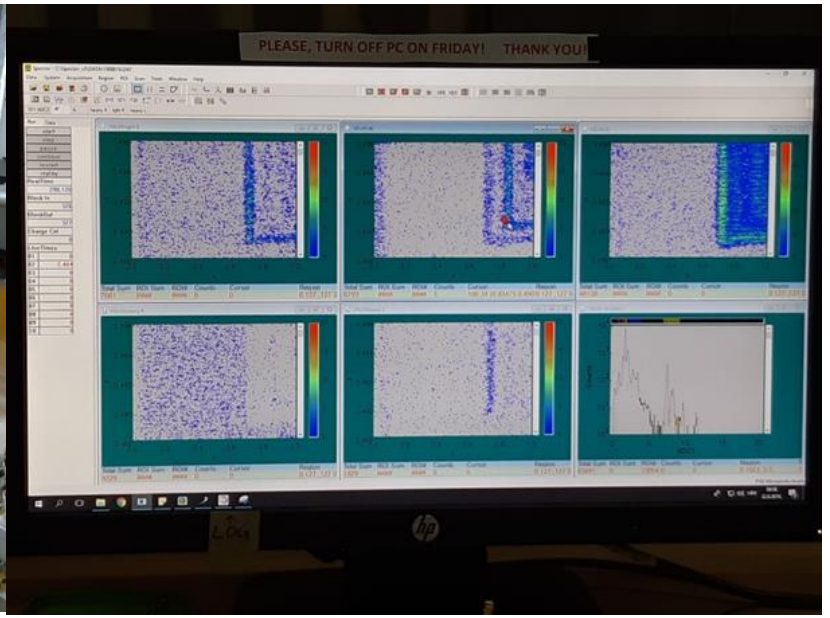
CMS

RD53



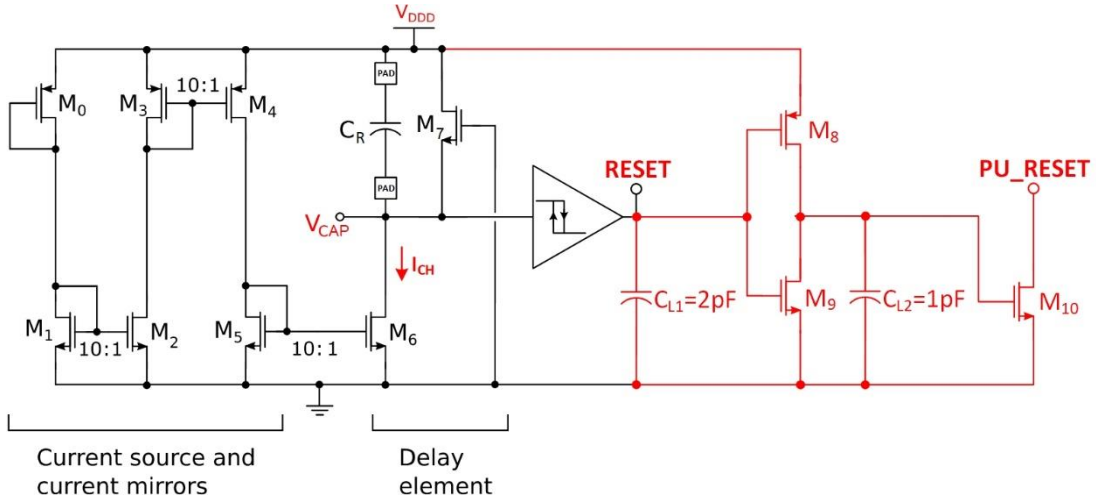
- SEU-SET chip, full custom test chip for testing Radiation Hardening By Design Structures, TSMC 65nm
- TMR and DICE flip-flops
- RD53 ROC general reset system
- Tested at Louvain-la-Neuve ion accelerator, RBI microbeam ion accelerator, Fermilab proton beam
- Lessons learned applied to RD53 chips.

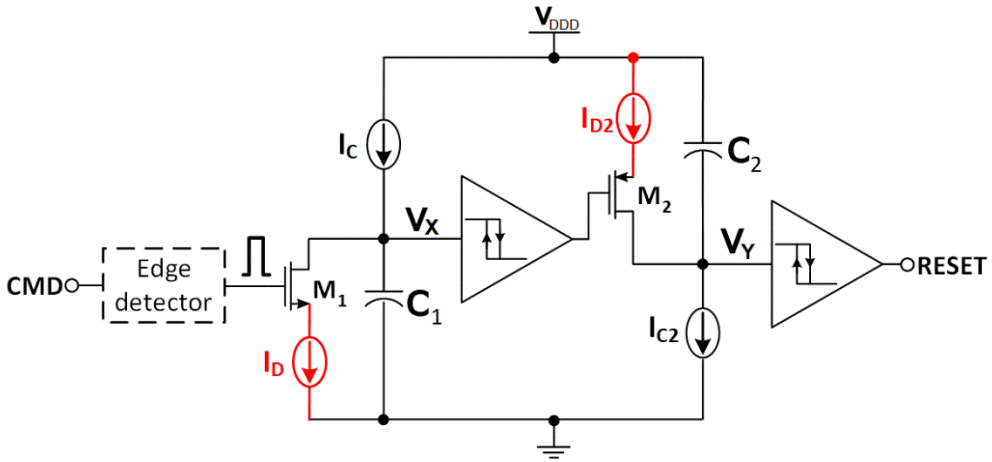




Ion Microbeam Characterization of SEU-SET chip

RD53

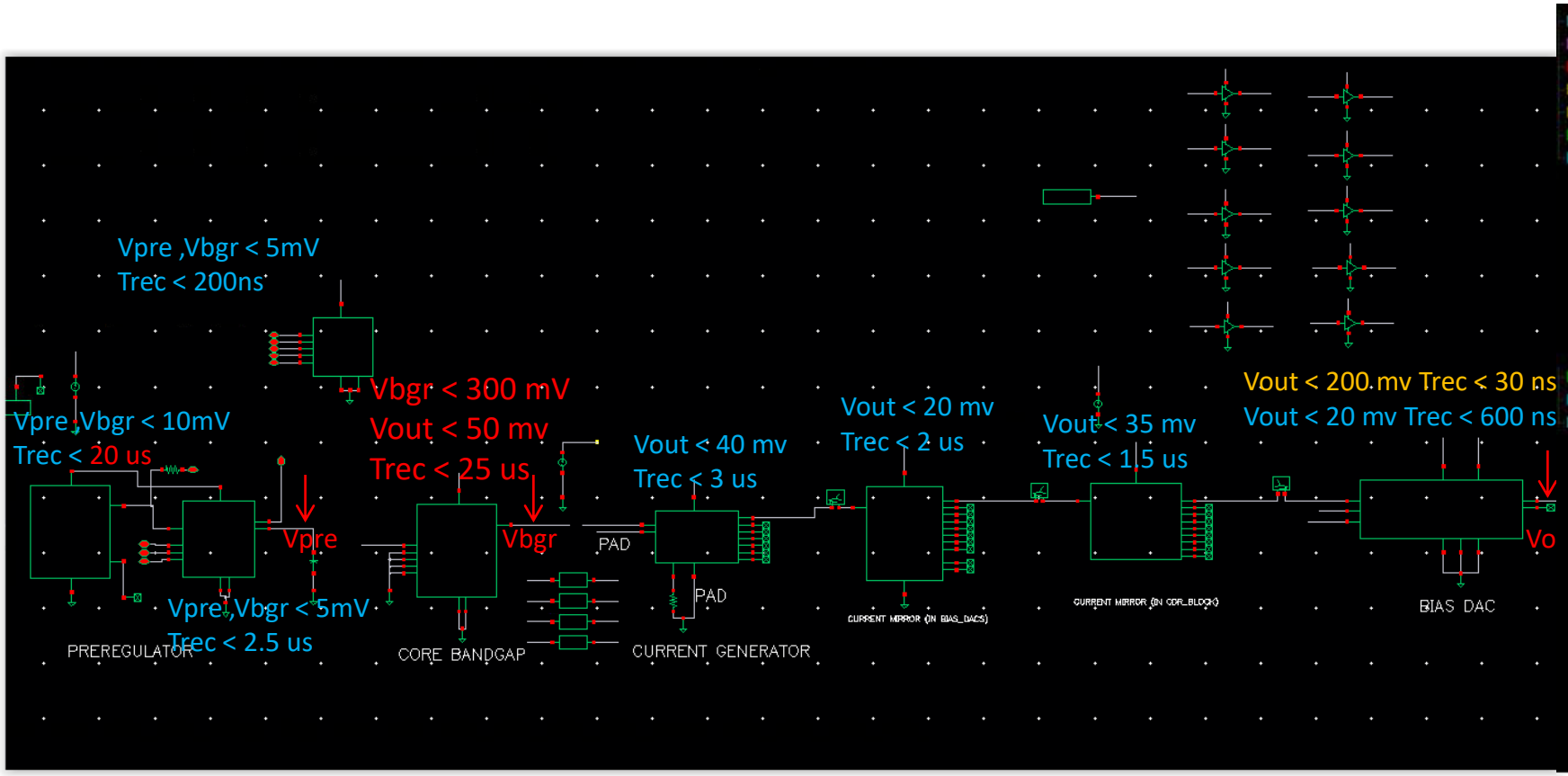


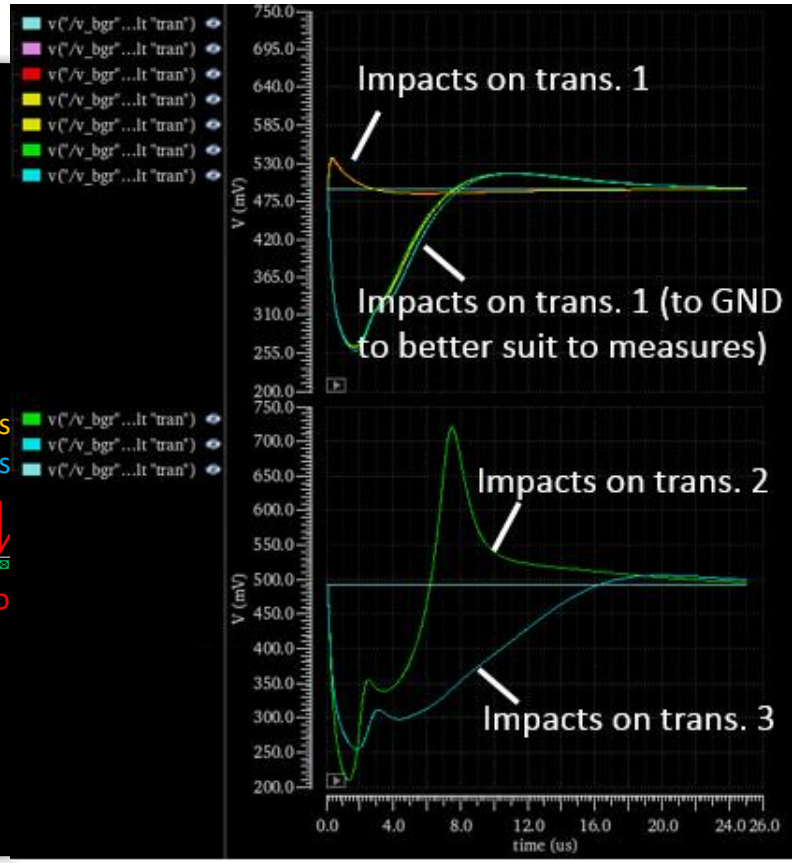


- Design of the reset system for the RD53 saga: Power On Reset, Command Reset
- Designs tested under Total Ionization Dose and Single Event Effects
- Common IPs for all the RD53 saga

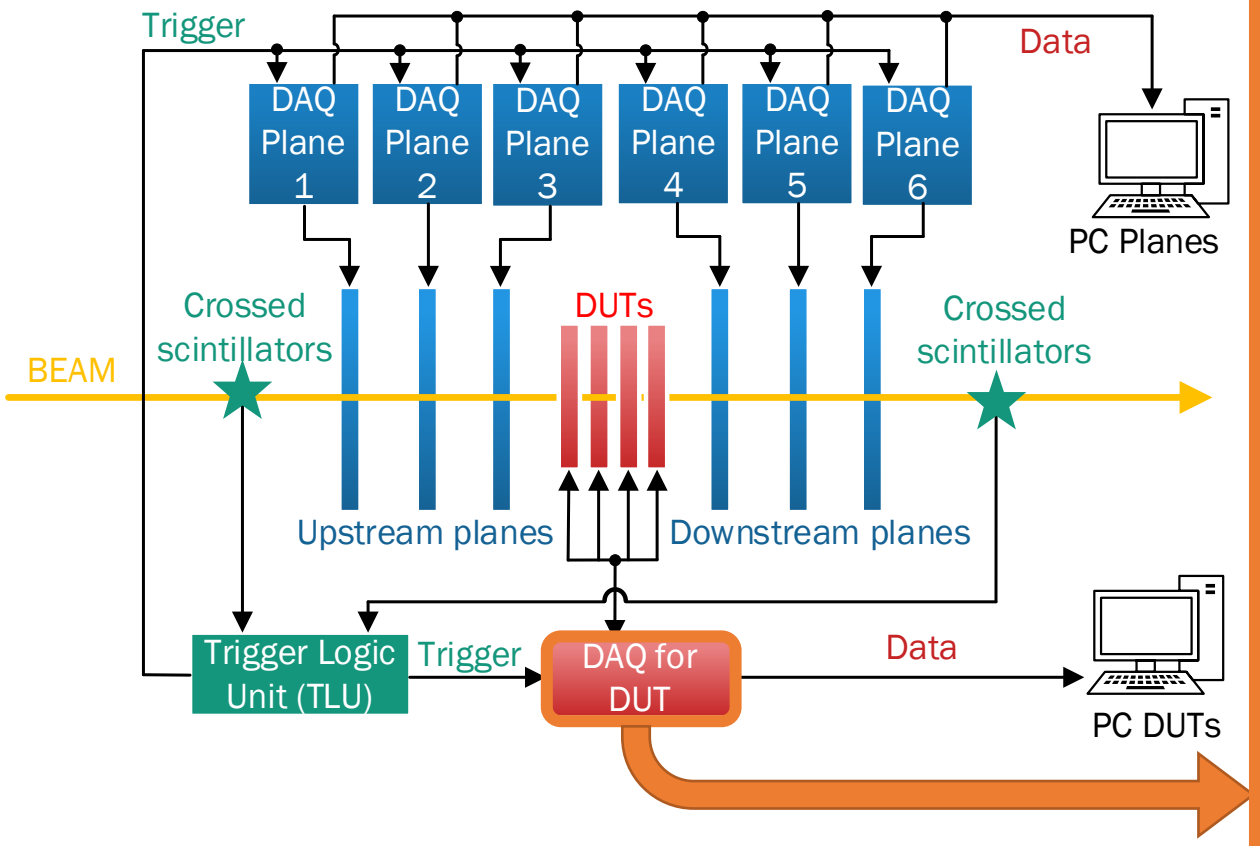
RD53

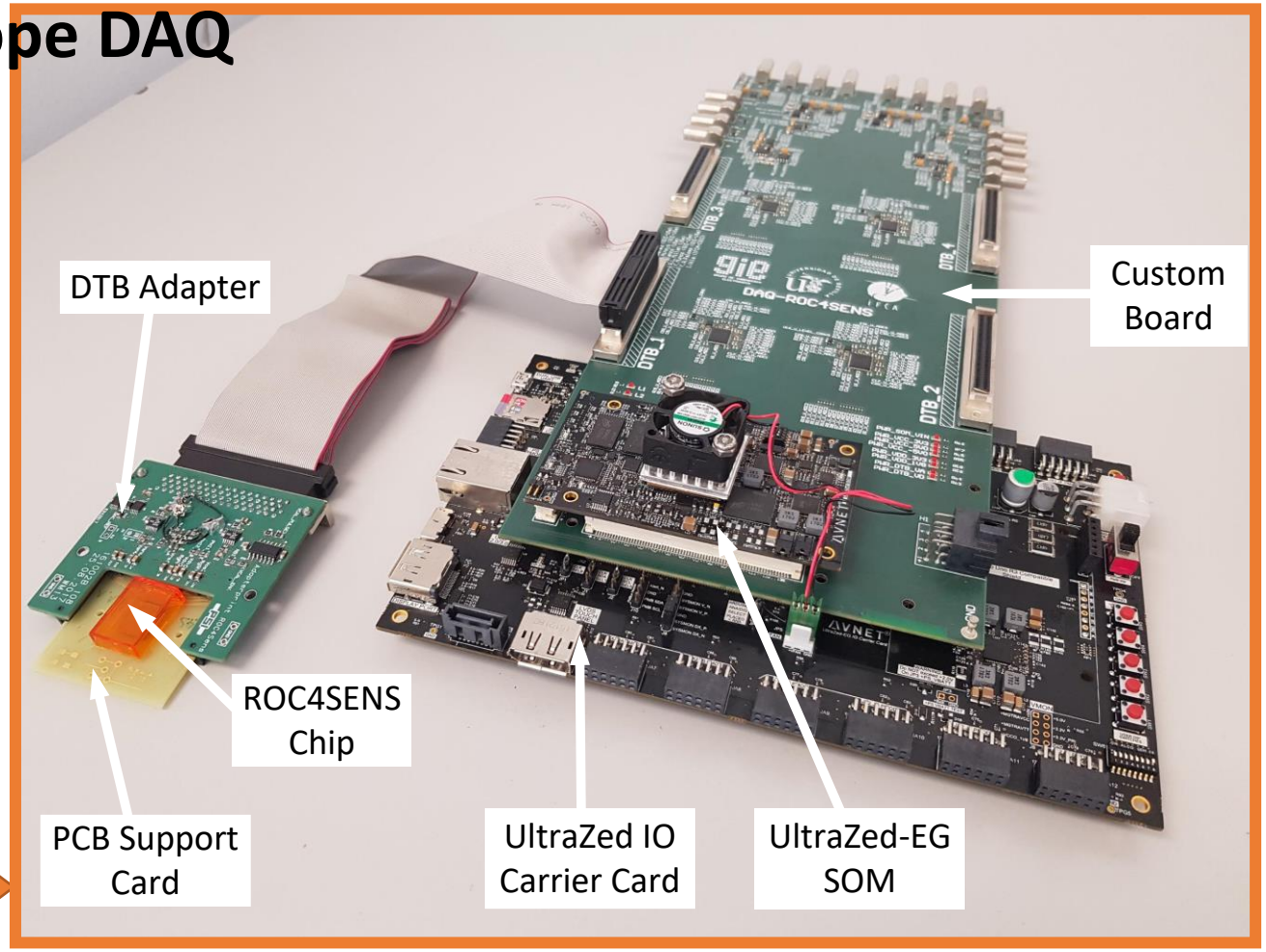
- **RD53 Blocks SET Verification by Simulation (AFTU custom software tool), redesign contributions**
- **DICE cells, TMR cells, clock spine, LDVS, Clock Generation Cells, etc**
- **Contributions to the general SEU simulation tool**





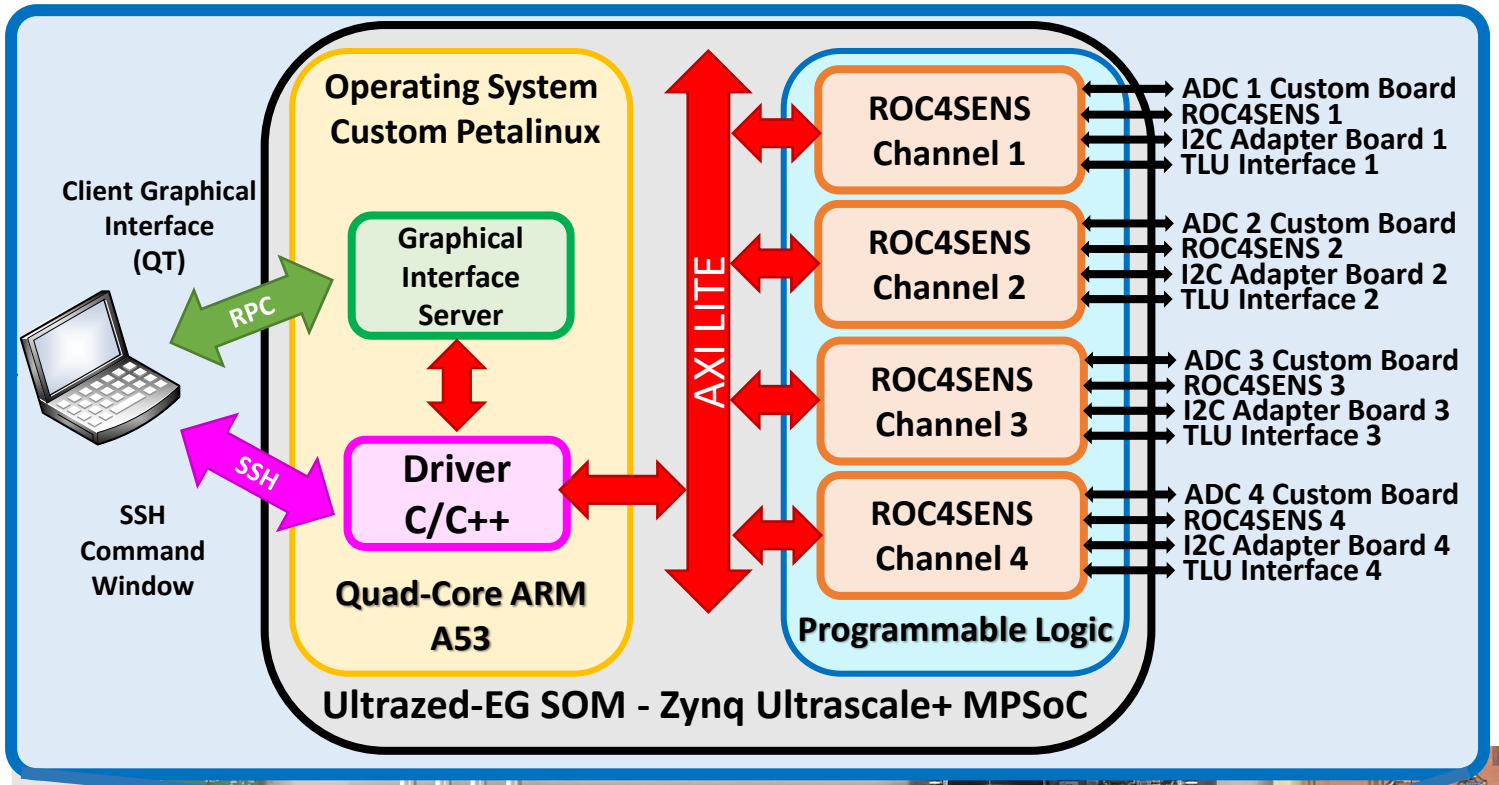
DRAD, A General Description: A Telescope DAQ

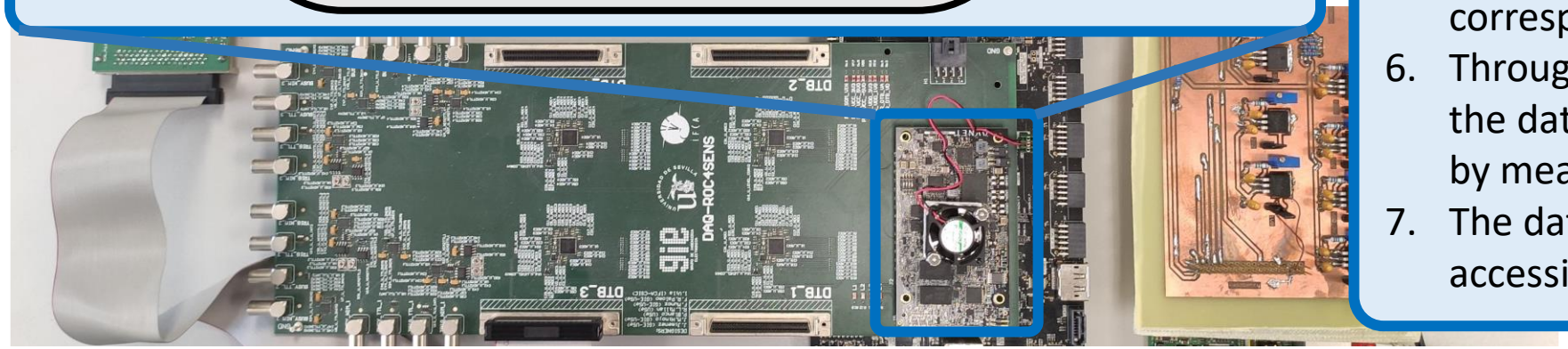




The main idea is to simplify the typical testbeam backend setup (e.g., AIDA2020 telescope) by a **standalone device** based on a powerful novel **MPSoC**, which integrates a programmable logic to implement the readout controllers and a set of multicore ARM processors to provide high-level programmability, such as application based on an architecture client-server, high-bandwidth communications, and high processing capability.

DRAD, A General Description: A Telescope DAQ

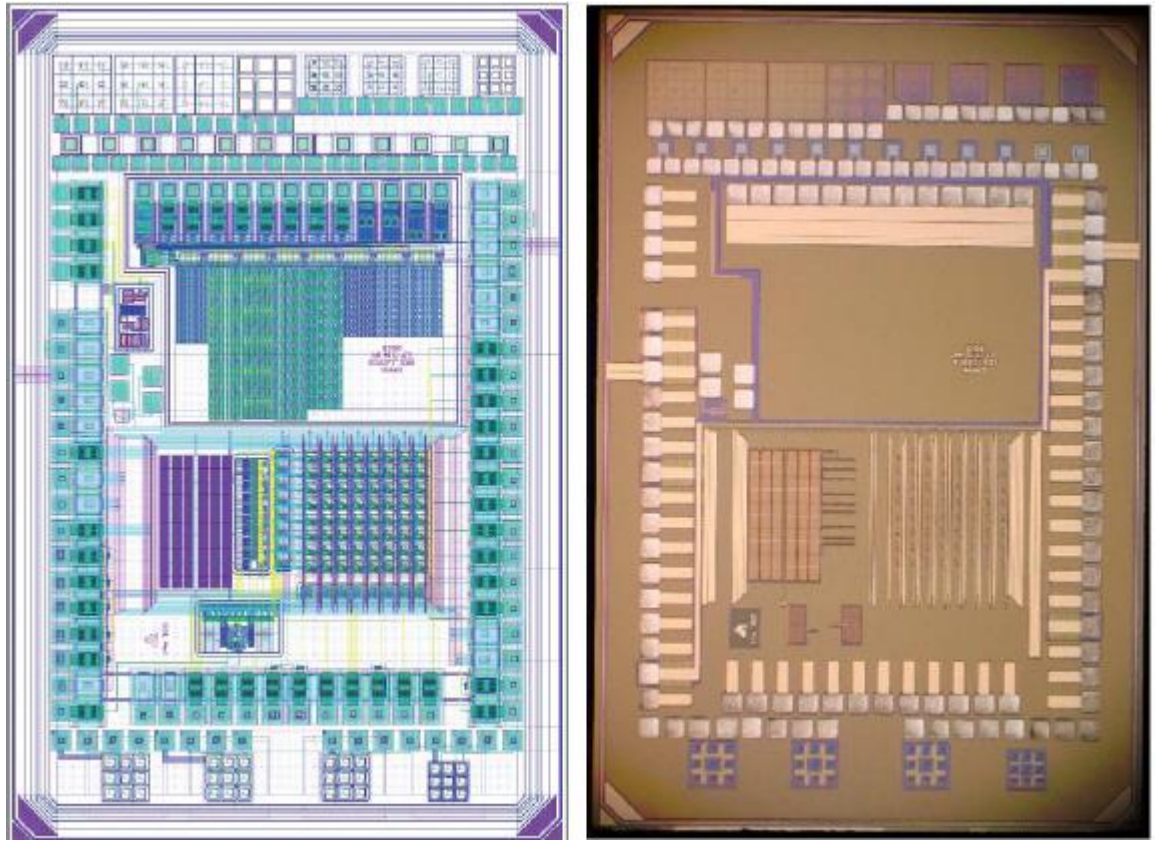




The operation of the system:

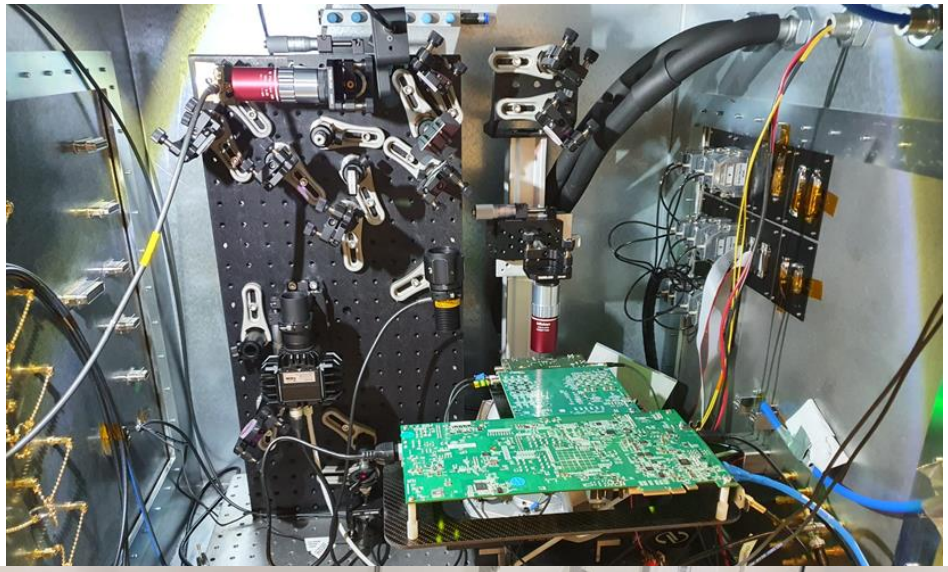
1. Starts with sending commands from the control software to a FIFO memory which is implemented in each R4S Channel.
2. Those FIFOs are processed by each R4S control unit and sent them to the corresponding block, ROC4SENS or I2C Adapter board.
3. TLU captures the event and sends a Trigger signal to corresponding Channel Block.
4. The R4S chip output is captured by the ADC.
5. The digital data is passed to the corresponding Channel Block.
6. Through the direct memory access (DMA), the data go to memory and is now available by means of driver software.
7. The data is available in the server that is accessible by RPC or SSH client.

MPW2 RD50 MAPS

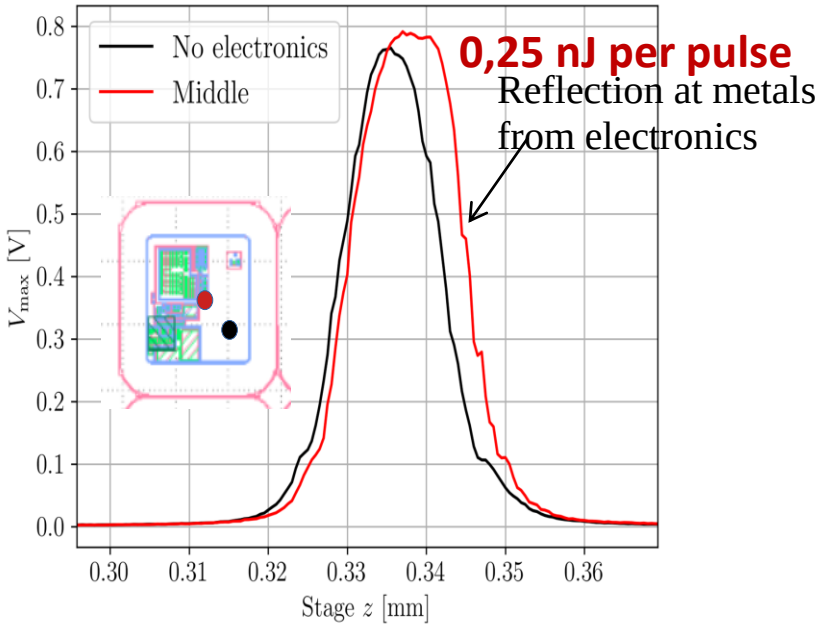


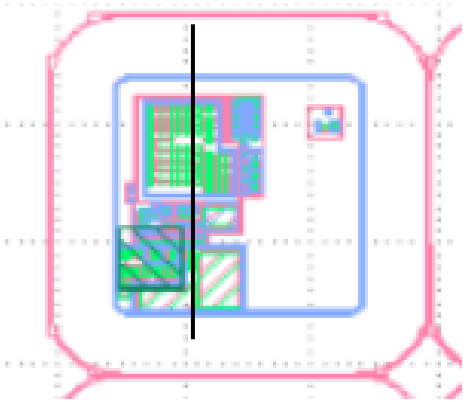
- LFoundry High Resistivity Substrate, 150nm design kit
- MPW2 is the first functional monolithic detector design made by the RD50 HVCMOS group
- We contribute here with the output buffer design and with chip characterization (electrical, under proton microbeam, under TPA laser testing)

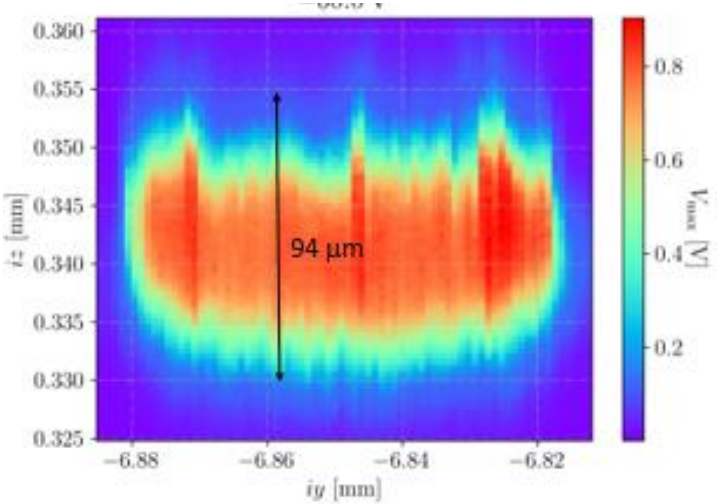
MPW2 RD50 MAPS



YZ-Scan across the electronics
0µm top side
-49µm middle side
-94µm bottom side

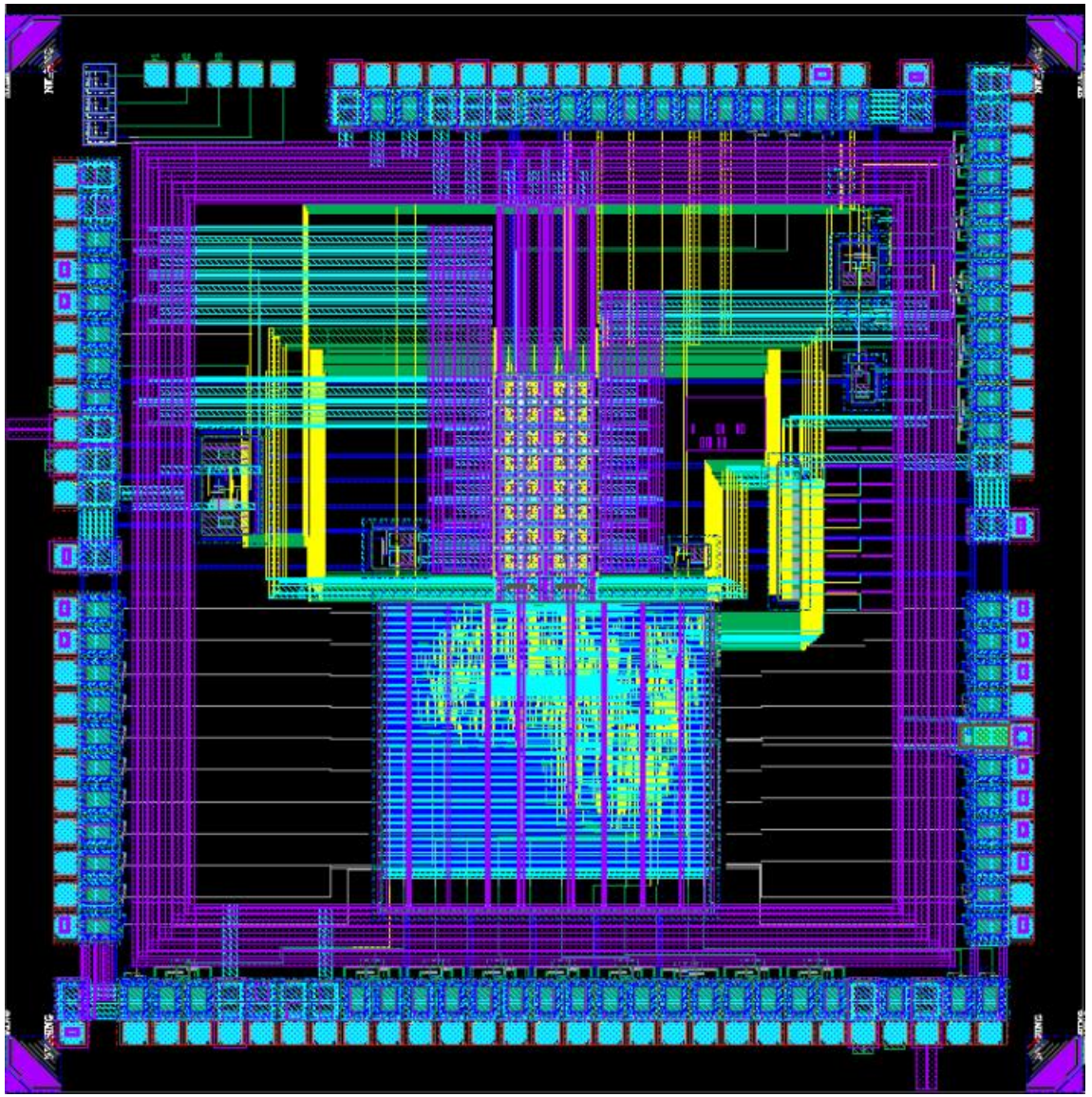






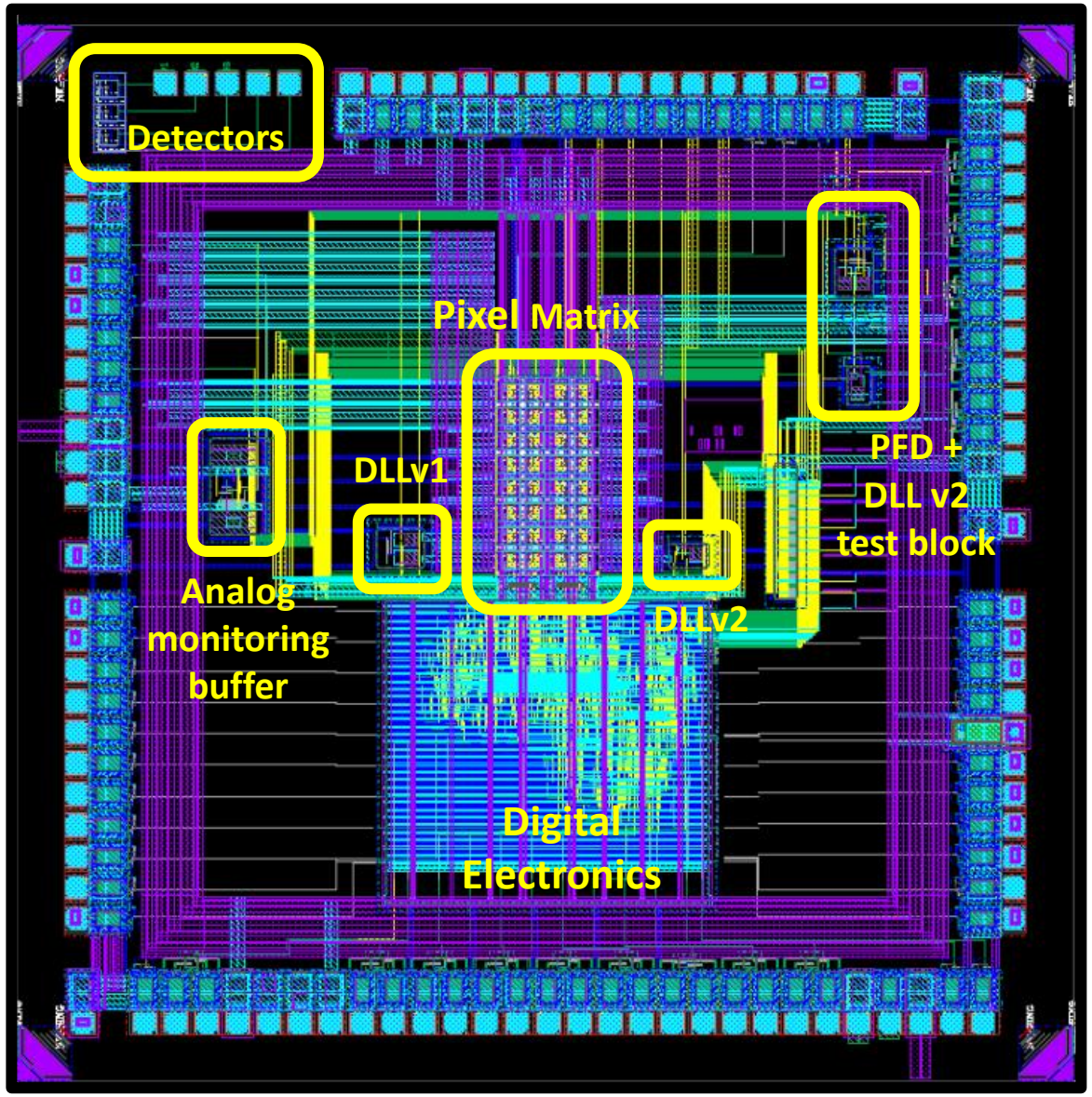
Nanomaps

- NANOMAPS (150nm) is a test chip designed by the GIE (Group of Electronic Engineering) at School of Engineering, Sevilla, and sent to LFoundry for manufacturing.
- It is derived from the MPW3 chip design and tests a new in-pixel timing circuitry.
- The design is based on 2 TDCs performing more accurate measurements of the LE and TE events and therefore, increasing the time resolution of the resulting ToT (Time over Threshold).
- The increase of accuracy will improve significantly the pixel time resolution after a ToT-based offline correction of the TW (Time Walk).
- It targets a 2 ns time resolution with low power consumption and area occupancy.
- The design is 100% integrable with the MPW3 architecture and has a low impact in the routing resources.



Nanomaps

- NANOMAPS test chip has 12 mm^2. The biasing block, the analogue buffer and most of the pixel circuitry and PADs are reused from MPW3 design.
- A 8x4 PIXEL matrix: based on the MPW3 pixel design but using a 75x75 $(\mu m)^2$ area diode. 2 double columns with 8 rows each one. Every double column has an independent DLL, with different architectures: DLL_v1 locks in the CLK rising edge, DLL_v2 locks in both rising and falling edges.
- A redesigned digital block. Based on the MPW3 in terms of slow control, monitoring, configuration and matrix data collection. New serialization and data transmission from each End Of Column FIFO to output: 5 serial-parallel registers at 80 MHz (there is no 640 MHz clock).
- Test vehicles:
  - 3 75x75 $(\mu m)^2$ detector diodes
  - One Phase Frequency Detector chain
  - One DLL_v2



Relevant Funding

Proyectos FPA Coordinados

- Desarrollo de nuevos detectores y estudios de física para los futuros colisionadores lineales (FPA2013-48387)
- Participación en el experimento CMS del LHC: Run2 y Pixel upgrade de alta luminosidad (FPA2017-152085173)

Proyectos FPA Junta de Andalucía

- Monolithic Active Pixel Sensor in Nanometrics Technology for Harsh Environments (NanoMAPS), Junta de Andalucía P18-FR-4317, 2020-2023
- Diseño electrónico para Aplicaciones de Alta Radiación (DERAD, Junta de Andalucía-FEDER 2014-2020)

Proyectos TIC

- Circuitos integrados para antenas de arrays en fase para estaciones base en constelaciones LEO, Plan Estatal 2021-23, Proyectos de Investigación Orientada, PID2021-1277120B, 2022-2025
- Exploring Modern Integrated Circuits Design in Harsh Environments, Retos 2017-2020 RTI2018-099189
- Diseño de circuitos de comunicaciones para alta radiación ambiental, Retos 2013-16 TEC2015-71072
- Validation of European High Capacity Rad-Hard FPGA and Software tools (VEGAS), Contrato 68/83, Horizon 2020
- Plataforma de Diseño y Análisis Integral de Circuitos para Aplicaciones Aerospaciales. Microprocesadores robustos, Plan Nacional 2010, TEC2010-22095
- Emulaser-Emulación mediante irradiación láser de los efectos de radiación cósmica en componentes electrónicos, OPN-Profit Plan Nacional Espacio 034/2006

Thanks for your attention

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