ASICs for photo-detectors

OMEGA design group

S. Ahmad, P. Barrillon, S. Blin, S. Callier, S. Conforti,
F. Dulucq, J. Fleury, C. de La Taille, G. Martin-Chassard,
L. Raux, N. Seguin-Moreau, D. Thienpont

http://omega.in2p3.fr

fee2011

Orsay MicroElectronics Group Associated

OUTLINE

- MAROC : 64 channels chip for multi-anode photomultiplier readout
- SPIROC : 36 channels chip for Silicon PM readout
- PARISROC : 16 channels chip for PM tube readout

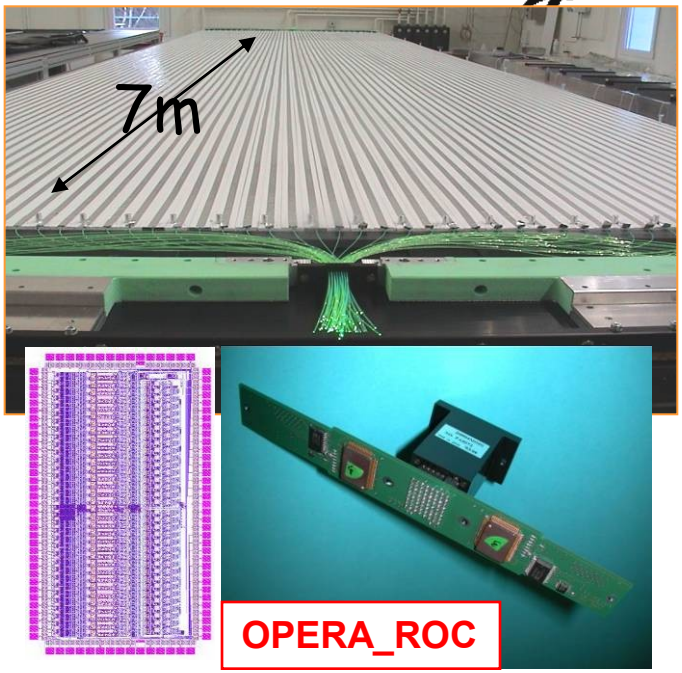
MAROC : MultiAnode Read-Out Chip

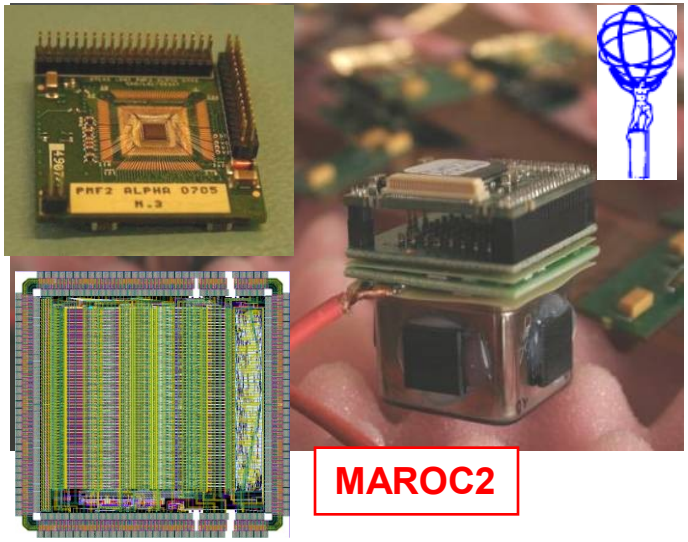
- Started with OPERA_ROC (2001)
  - 32 Channels in BiCMOS 0.8 µm for H7500
  - 3000 chips produced in 2002
  - Equiped OPERA in Gran Sasso

- MAROC1 (2004)
  - First prototype with 64 channels
  - AMS SiGe 0.35 µm (12 mm^2, Pd=5 mW/ch)

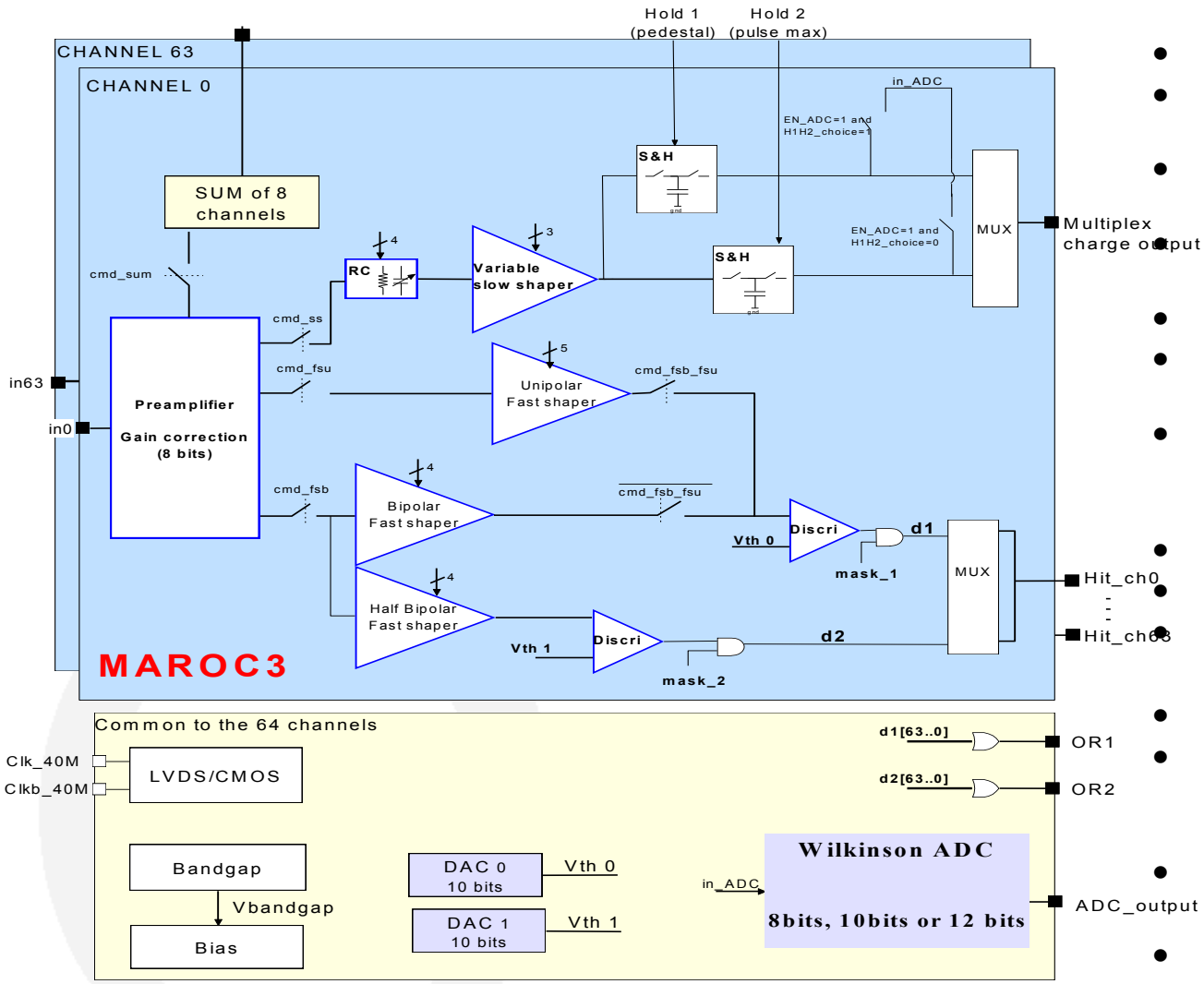
- MAROC2 (2006)
  - **1000 chips produced and bonded on a compact PCB for ATLAS luminometer (ALFA) for H7546**
  - Also equips Double-Chooz, Menphyno, medical imaging…

- MAROC3 (2009)
  - Lower power dissipation
  - Wilkinson ADC added
  - 1000 chips produced





MAROC3 – Main Features



- 64 channel inputs
- Low input impedance (50-100 Ω)
- Variable gain preamps (8 bits/ch.)
- Variable slow shaper (20-100 ns)
- 2 T&H (baseline and max.)
- 1 mux. analog charge output
- 1 digitized charge output (8, 10 or 12 bits ADC)

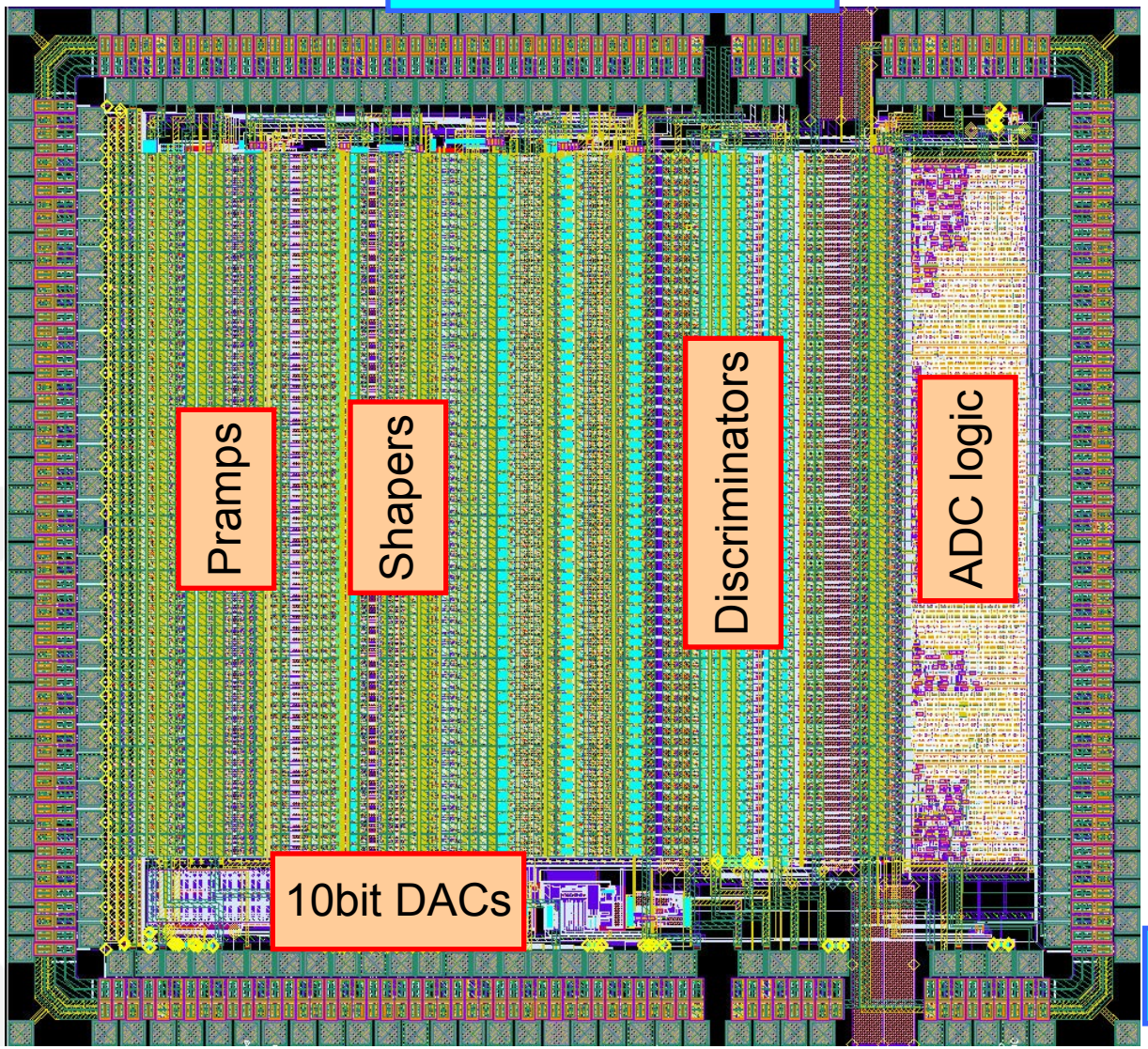
- 64 trigger outputs
- 2 OR outputs
- low digital output levels

- 10 bits DAC as threshold
- Internal bandgap for voltage references

- P = 3 mW/ch

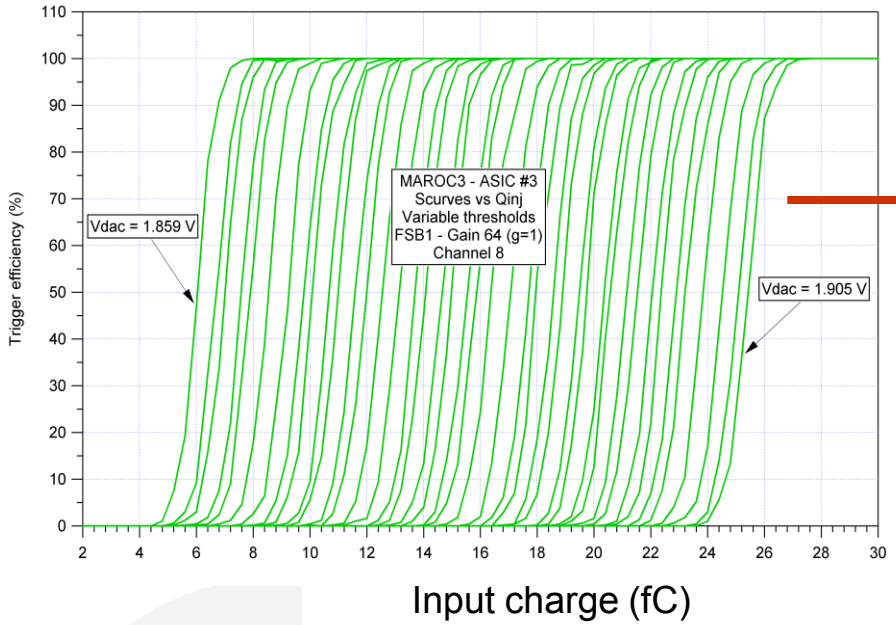
- 828 slow control parameters

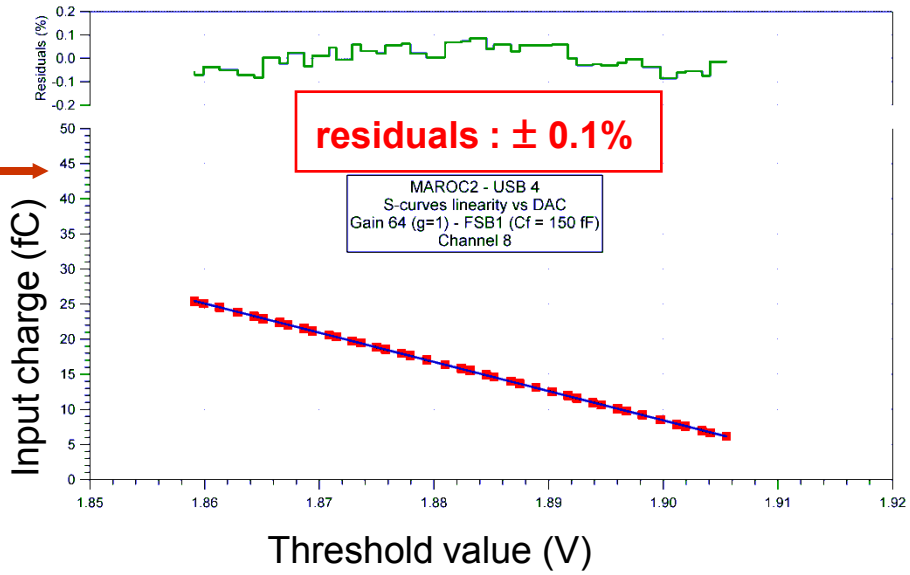
MAROC3 layout

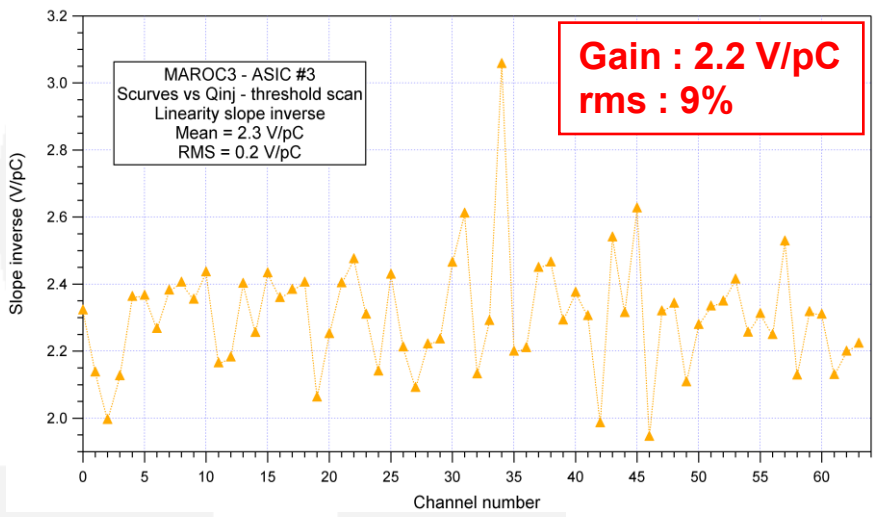


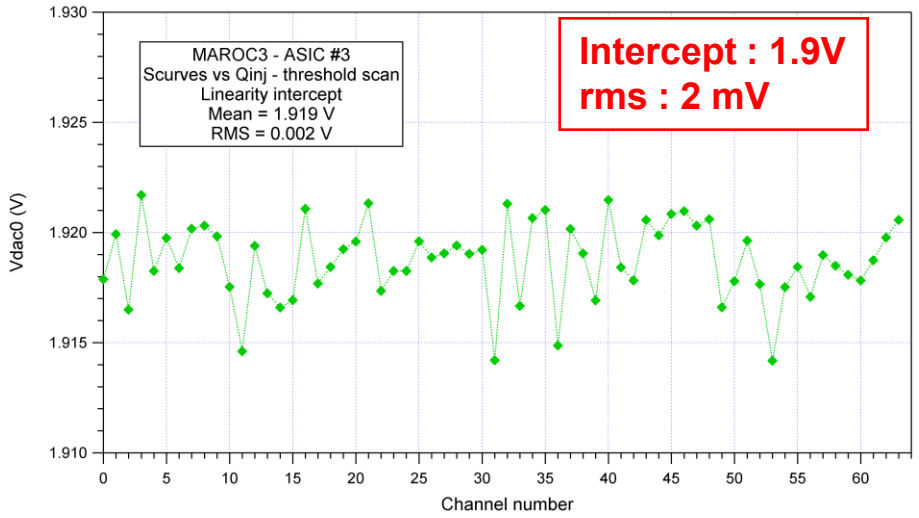
AMS SiGe 0.35µm
Package: CQFP240
Area: 16 mm2

Scurves with FSB1



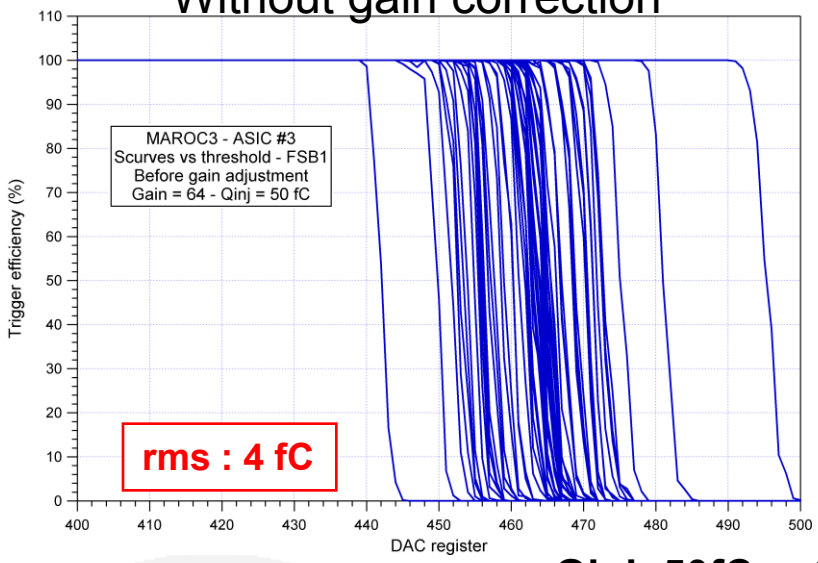




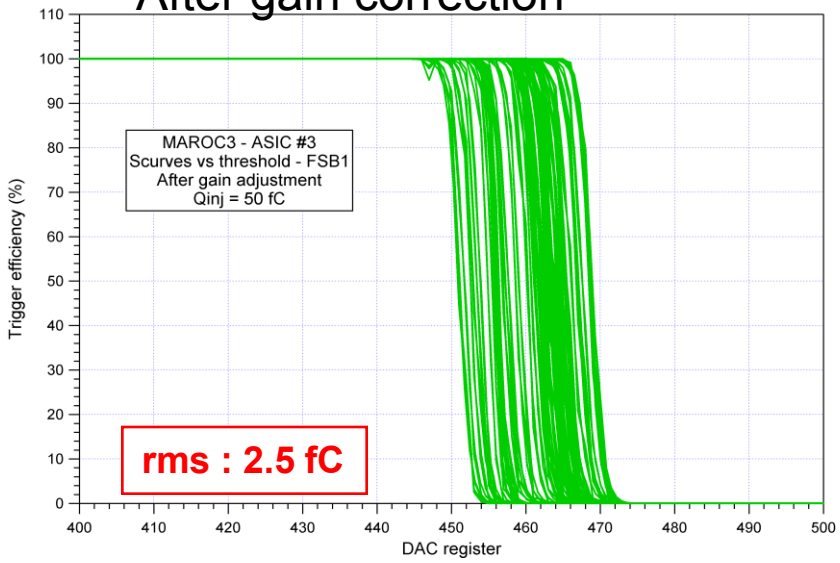


Gain correction and crosstalk

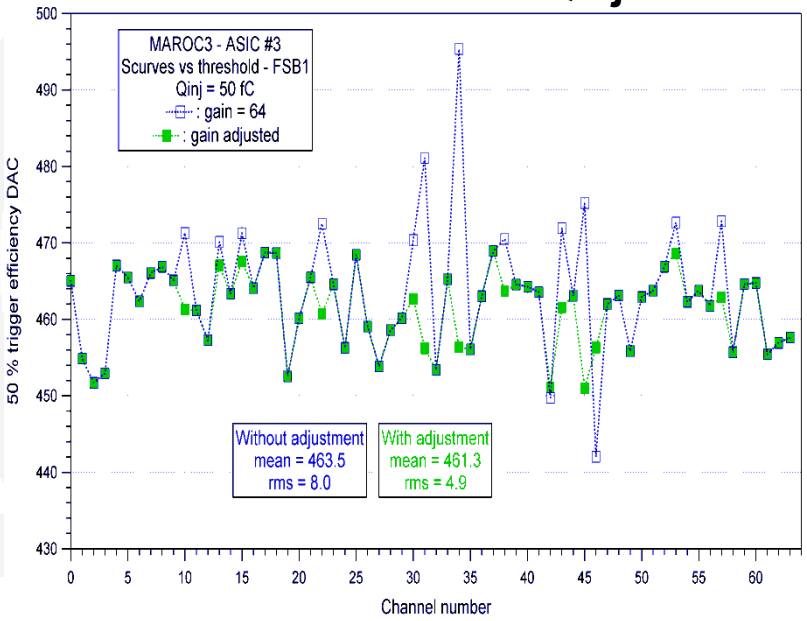
Without gain correction

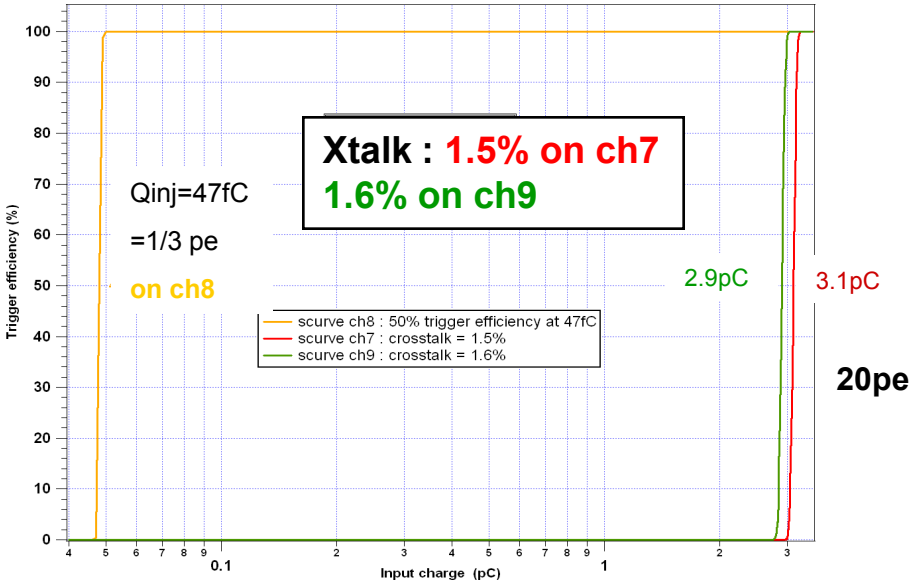


After gain correction

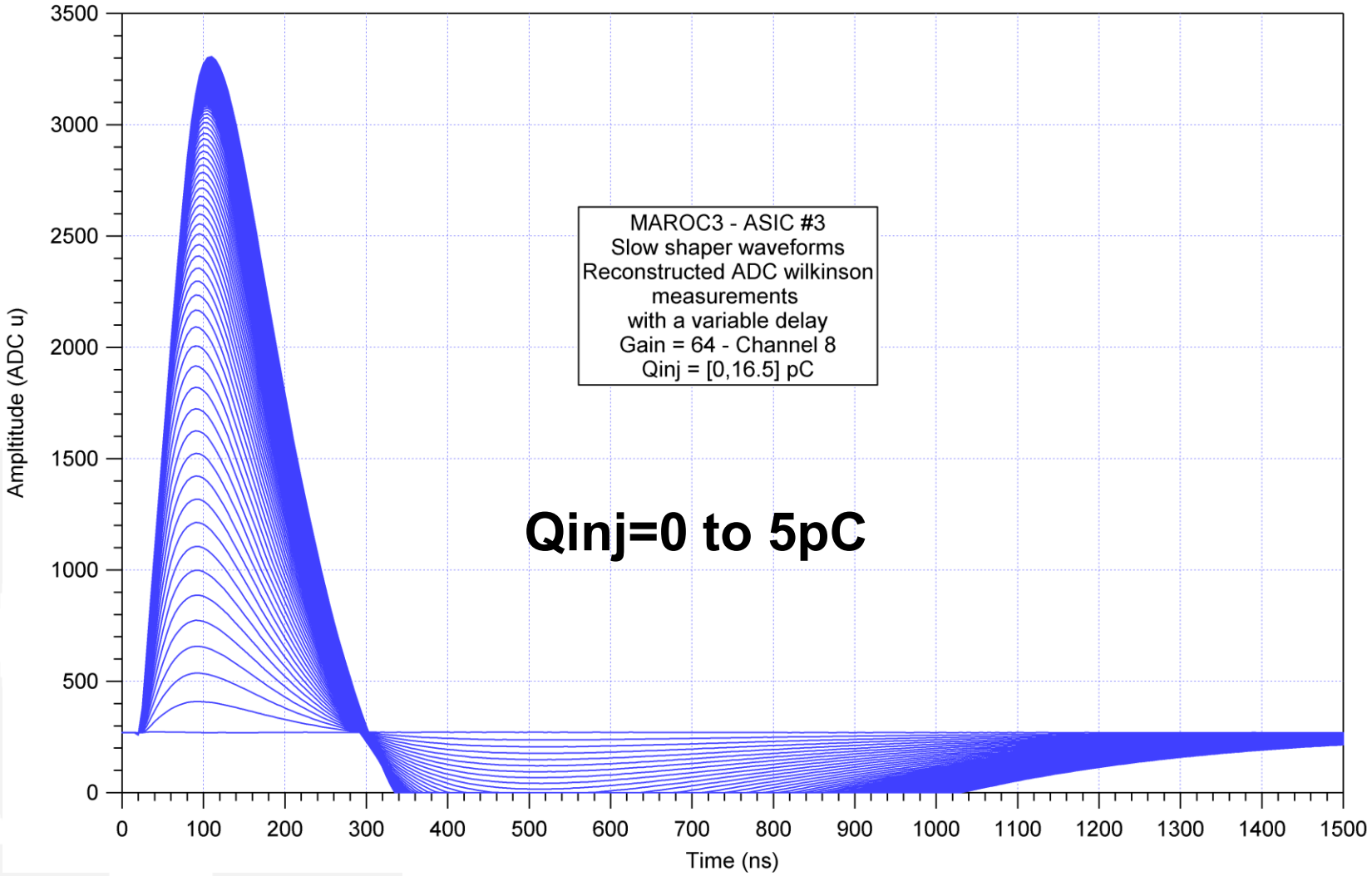


Qinj=50fC ~ 1/3 pe





Slow shaper waveforms measured by wilkinson ADC



Variant (2010) : SPACIROC for JEM/EUSO

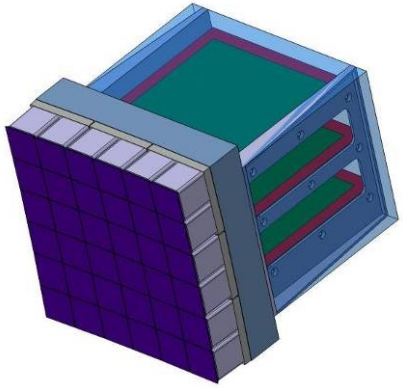
ASIC Functions:

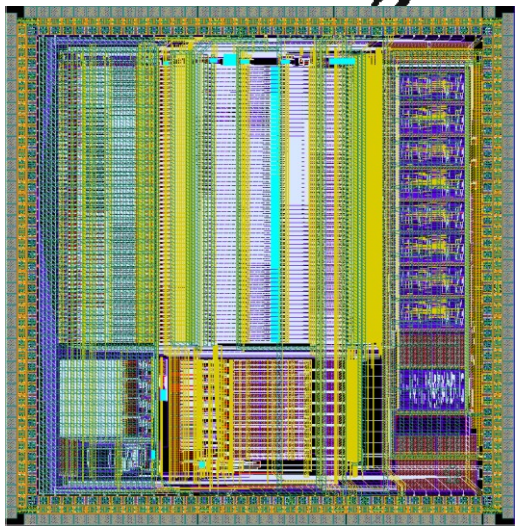
Analog part:

1. **Photoelectron counting (20-100MHz)**
2. Time Over Threshold (collab. JAXA/Riken)

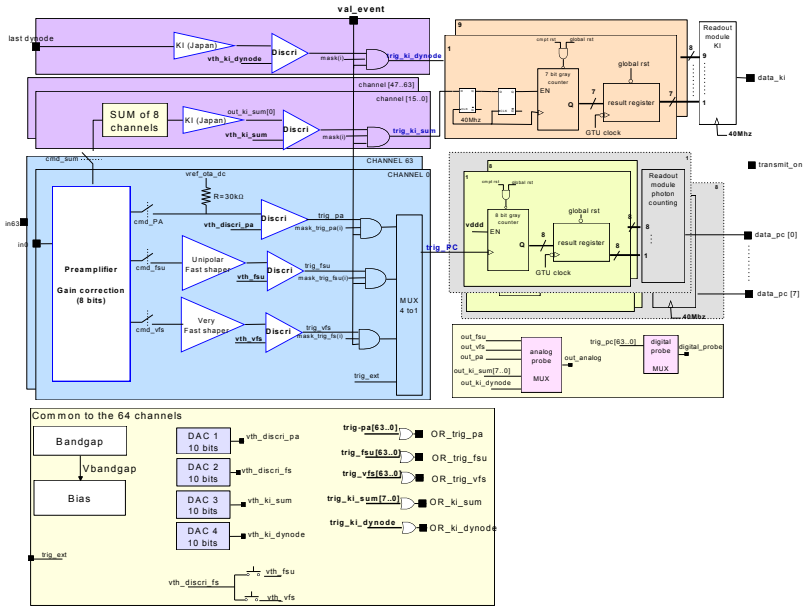
Digital part :

1. Digitization,
2. Memory,
3. Send data to FPGA for triggering





SPACIROC : 16mm²



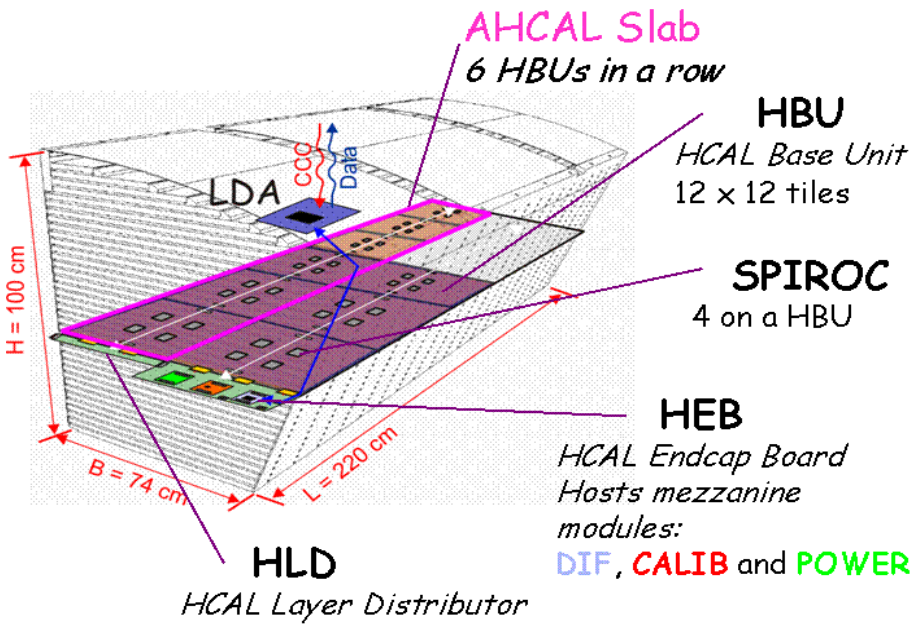
Crucial points

- **Power consumption < 1 mW/ch**
- data flow ~ 384 bits / 2.5 µs
- Radiation tolerance : triple voting

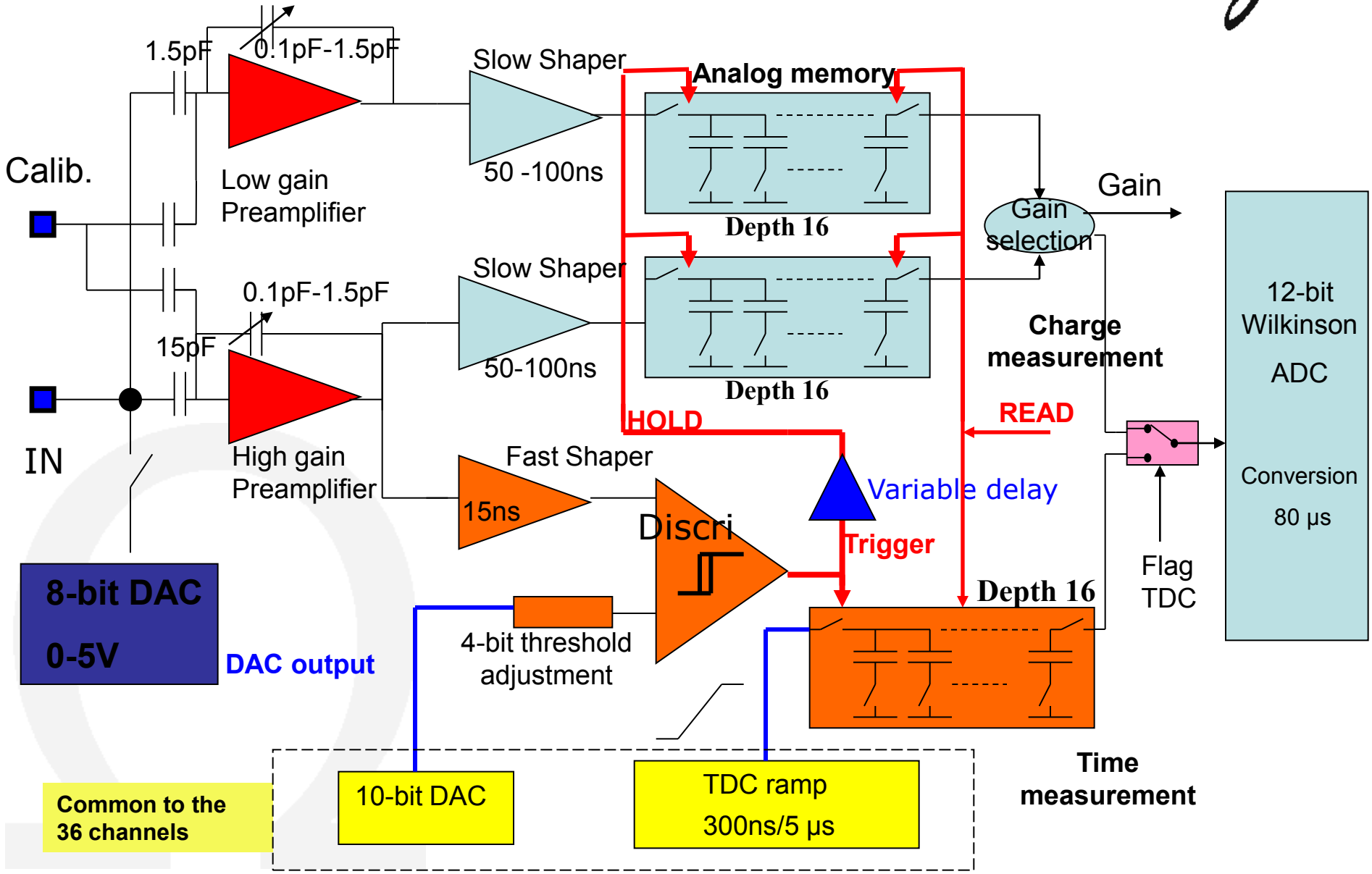
SPIROC for SiPM readout

- SPIROC : Silicon Photomultiplier Integrated Readout Chip
- Developed to read out the analog hadronic calorimeter for CALICE (ILC)
- DESY collaboration (EUDET project)
- Chip embedded in detector :
  → Power consumption is an important issue
  → few external components
- Big detector with huge number of channels (8 millions)

$(0.36m)^2$ Tiles + SiPM + SPIROC (144ch)

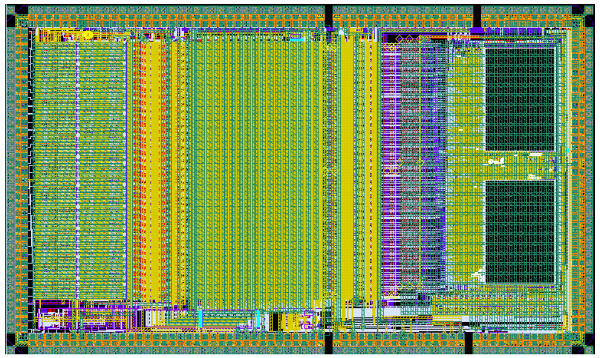


SPIROC : One channel schematic



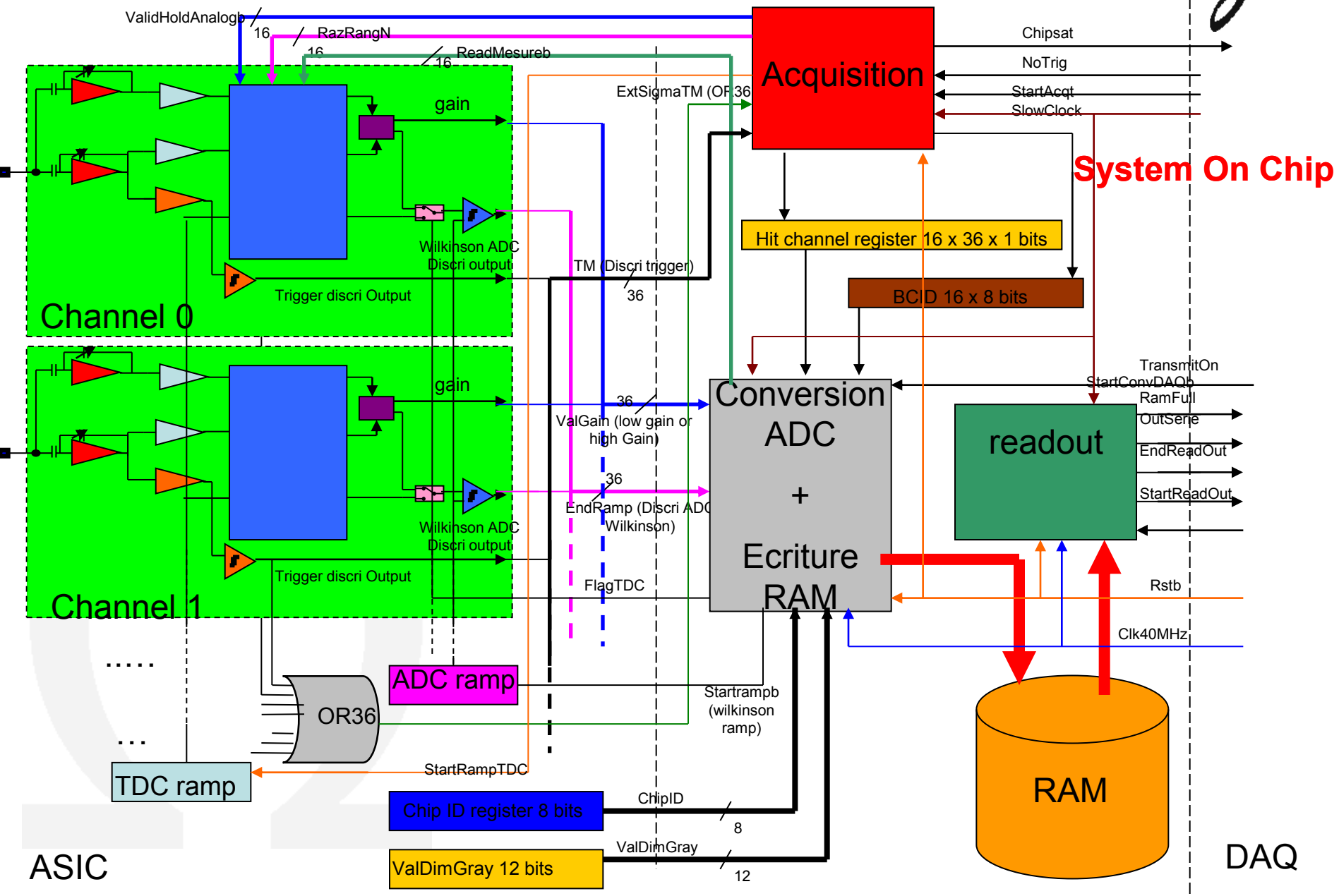
SPIROC main features

- 36 channels
- Internal input 8-bit DAC (0-5V) for individual SiPM gain adjustment
- Energy measurement : 14 bits
  - 2 gains (1-10) + 12 bit ADC: **1 pe → 2000 pe**
  - Variable shaping time from 50ns to 100ns
  - pe/noise ratio : 11
- Auto-trigger on 1/3 pe (50fC)
  - pe/noise ratio on trigger channel : 24
  - Fast shaper : ~10ns
- Time measurement :
  - 12-bit Bunch Crossing counter (step=200ns)
  - 12 bit TDC step~100 ps



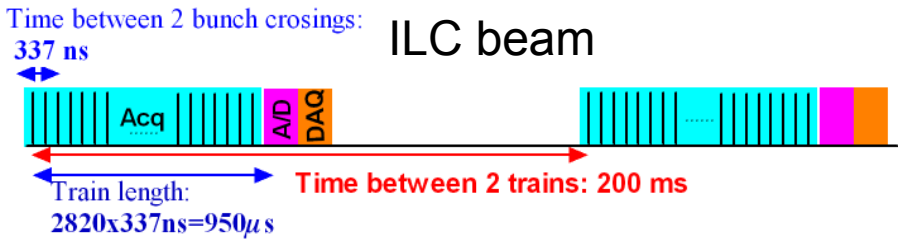
- Analog memory for time and charge measurement : depth = 16
- Low consumption : ~25µW per channel (in power pulsing mode)
- Individually addressable calibration injection capacitance
- Embedded bandgap for voltage references
- Embedded 10 bit DAC for trigger threshold and gain selection
- Multiplexed analog output for physics prototype DAQ
- 4k internal memory and Daisy chain readout

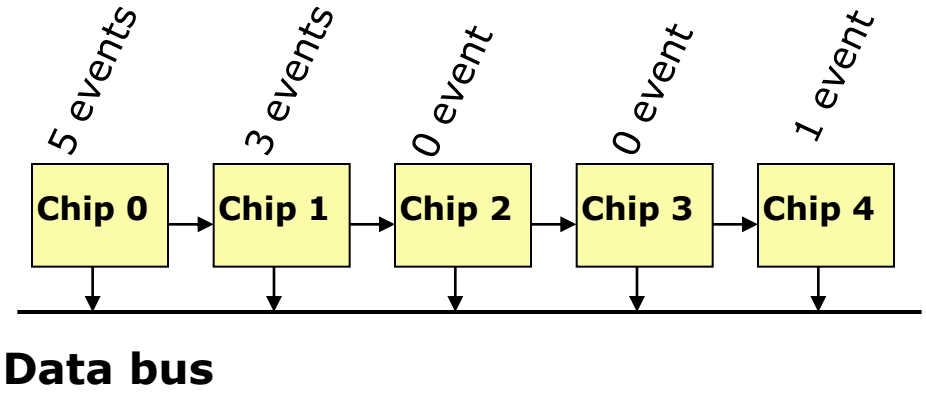
SPIROC : general schematic

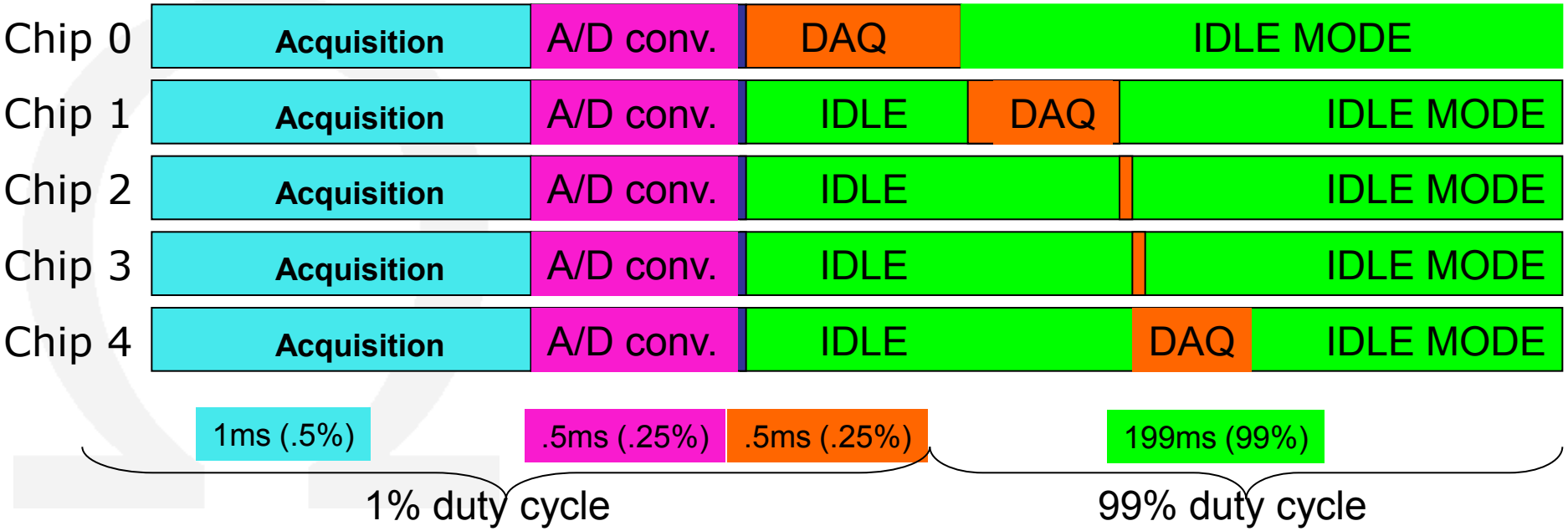


Read out by token ring and power pulsing

- Readout architecture common to all CALICE calorimeters
- Minimize data lines & power

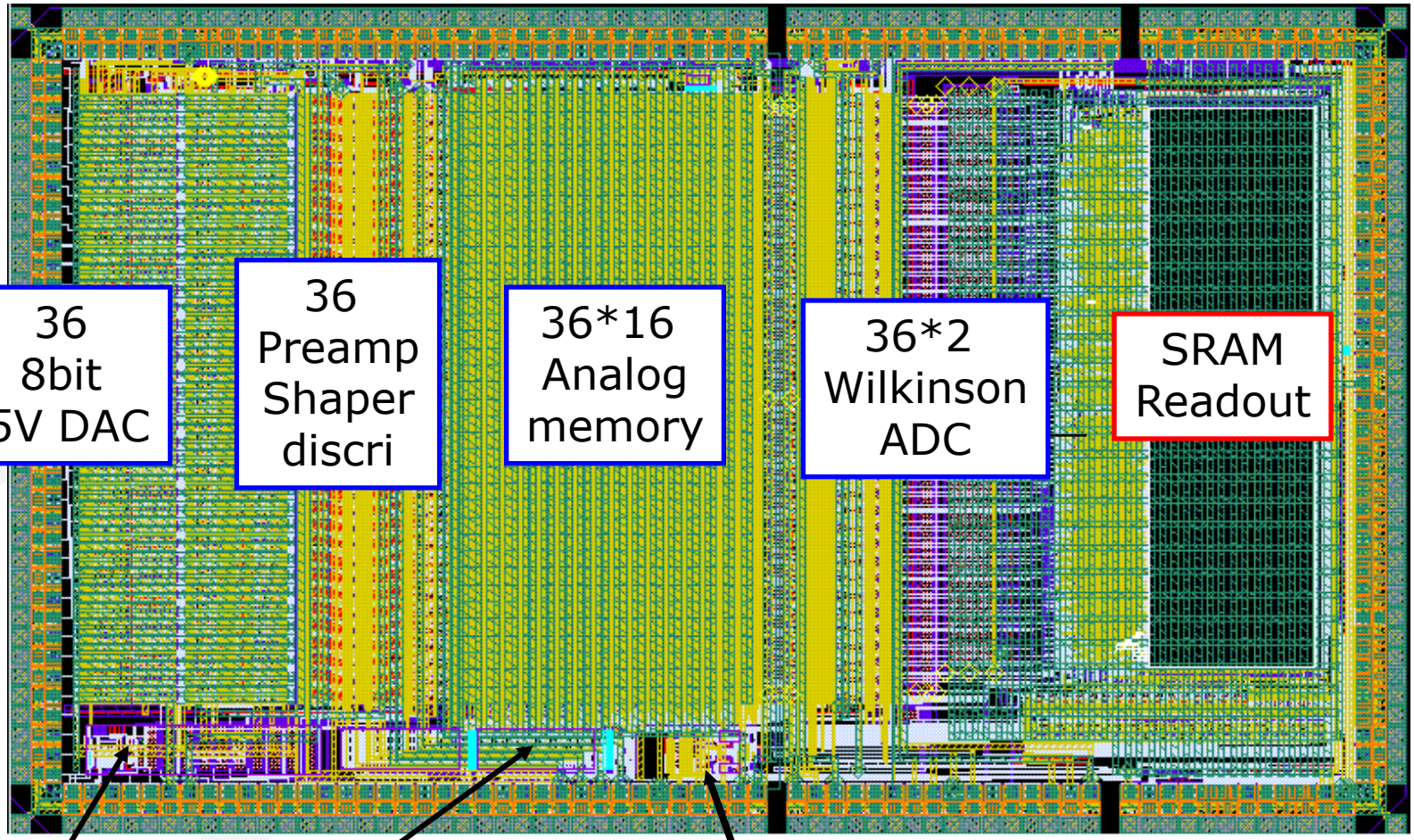






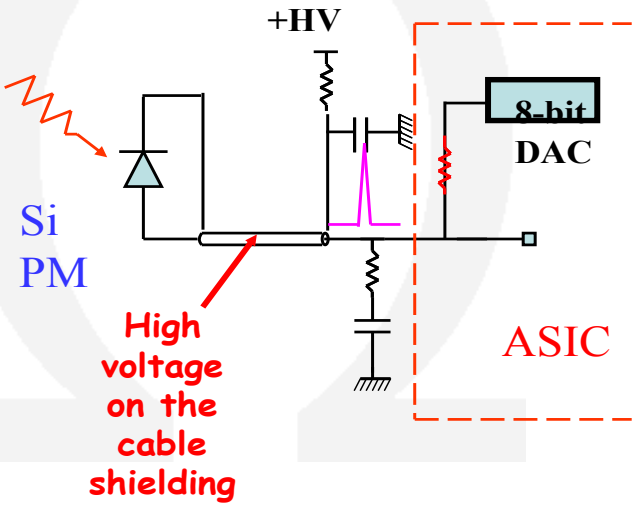
SPIROC layout

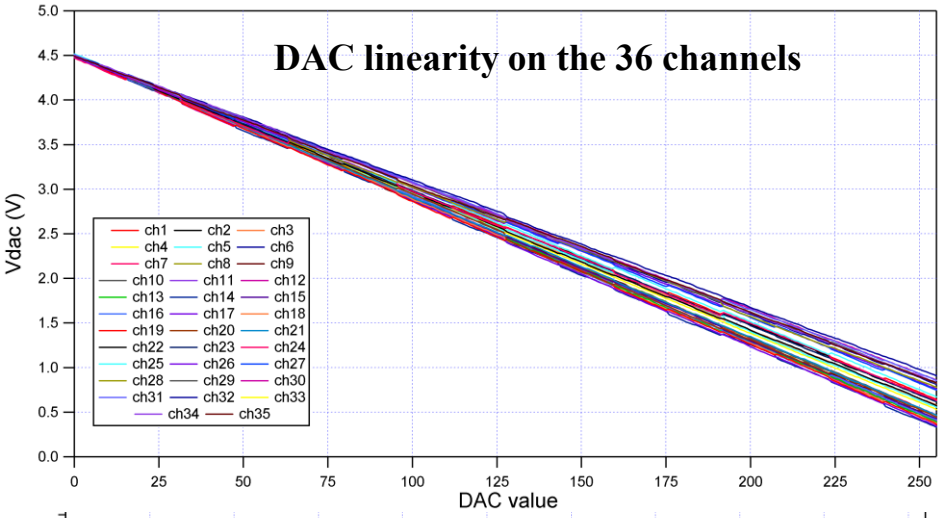
Techno : AMS SiGe 350nm - package : TQFP 208 - die size : 8x4= 32mm^2

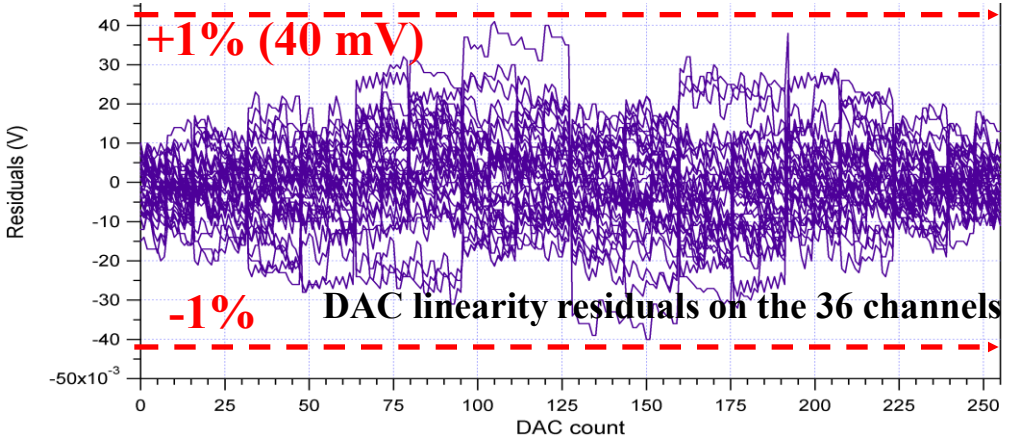


SPIROC2 input DAC

- Input DAC to optimize SiPM bias voltage
- 8-bit DAC, 5V range, LSB=20mV
- 36 DAC (one per channel)
- Ultra low power (<1µW) : no power pulsing
- Can sink 10 µA leakage current
- Linearity : ± 1%
- DAC uniformity between the 36 channels : ~3%

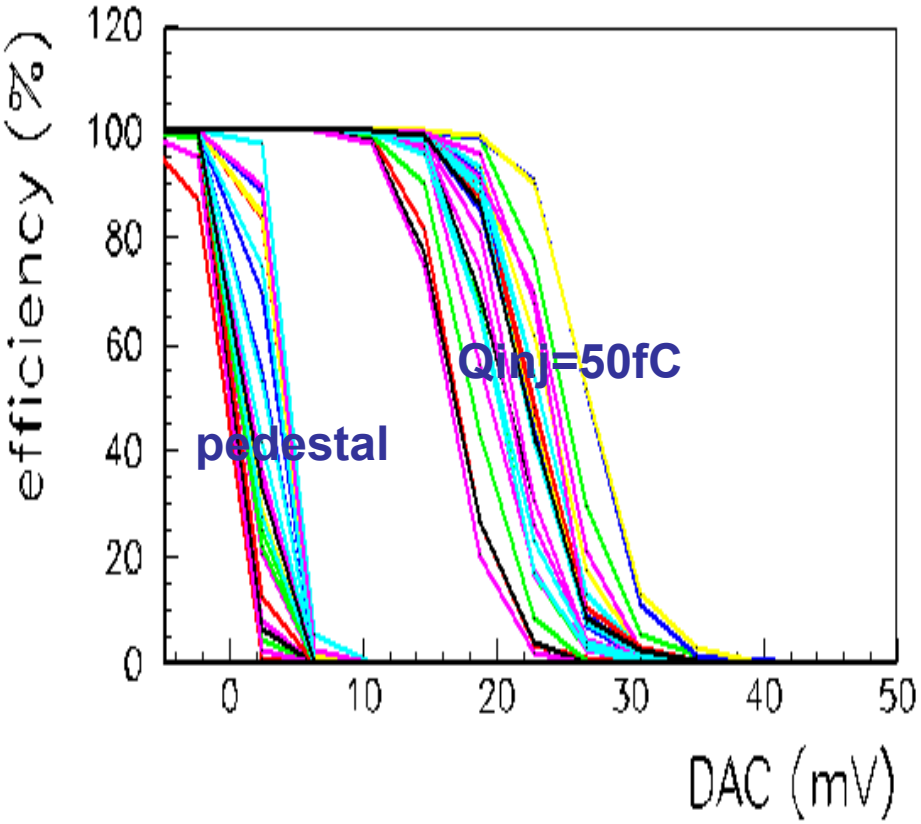


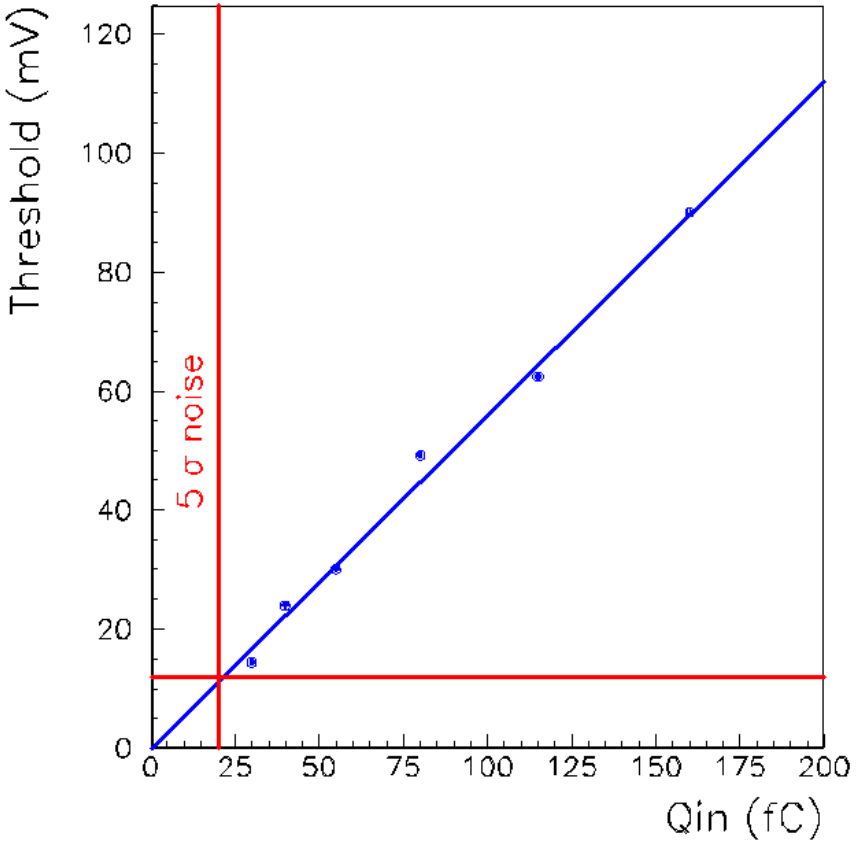




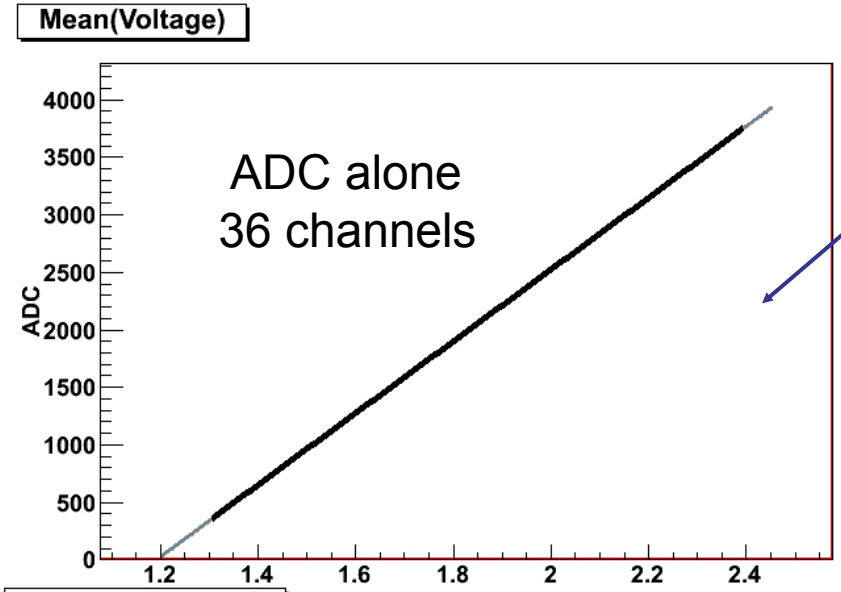
S-curves on fast shaper

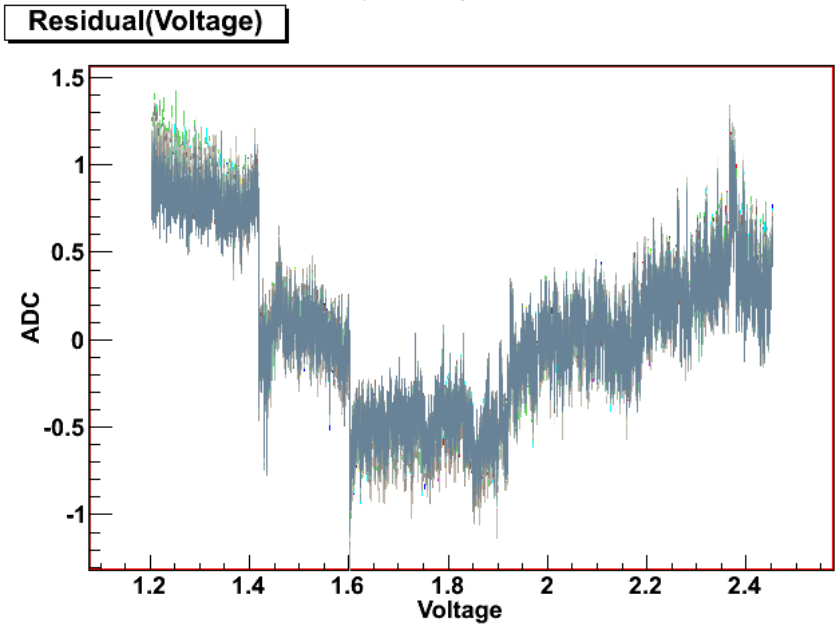
- Trigger efficiency versus Threshold (1UDAC=2mV)
- Qinj=50 fC (1/3 pe-)



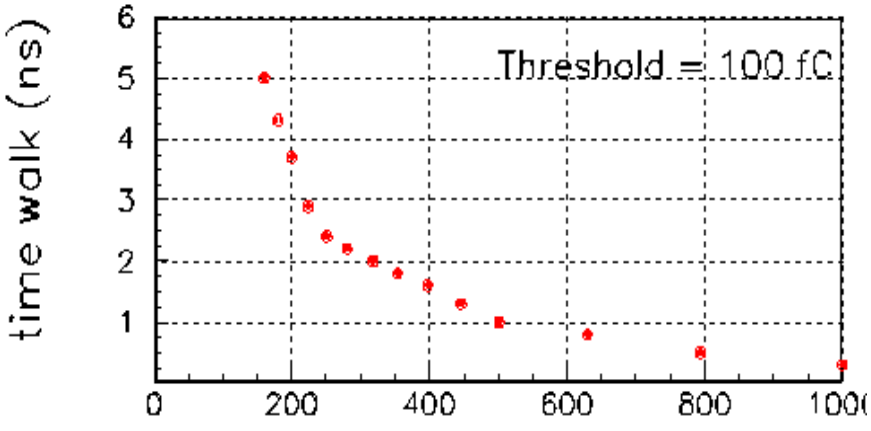


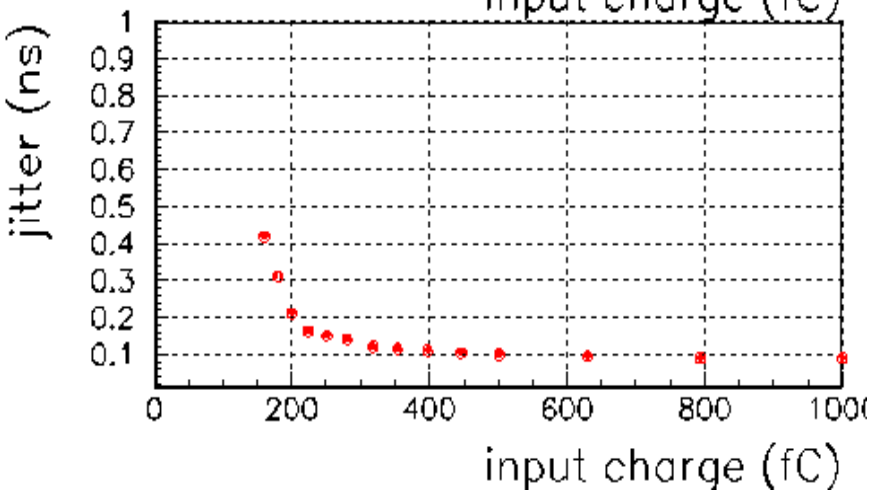
SPIROC2 performance



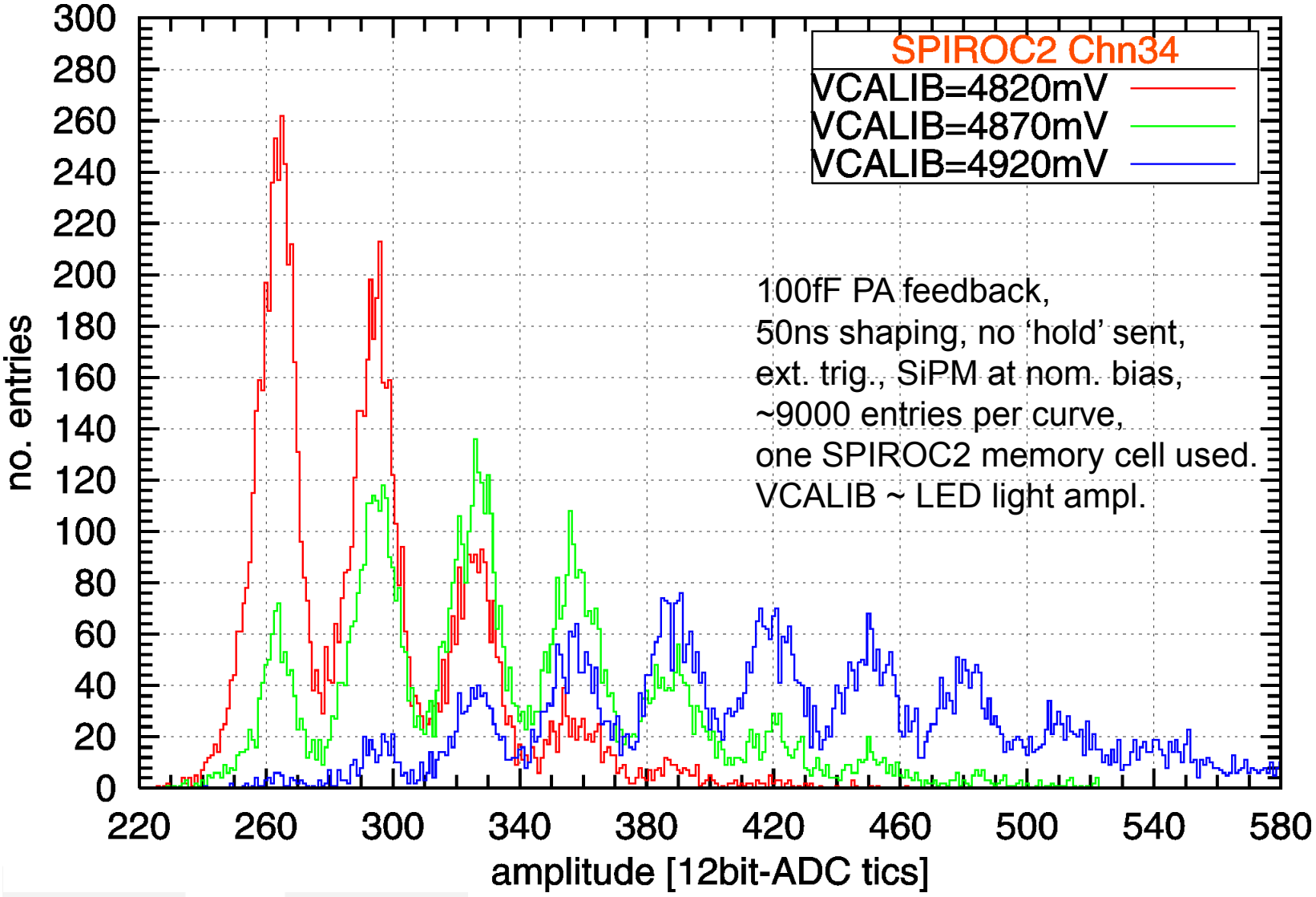


- Wilkinson ADC well suited to multichannel conversion
- Very good uniformity and linearity

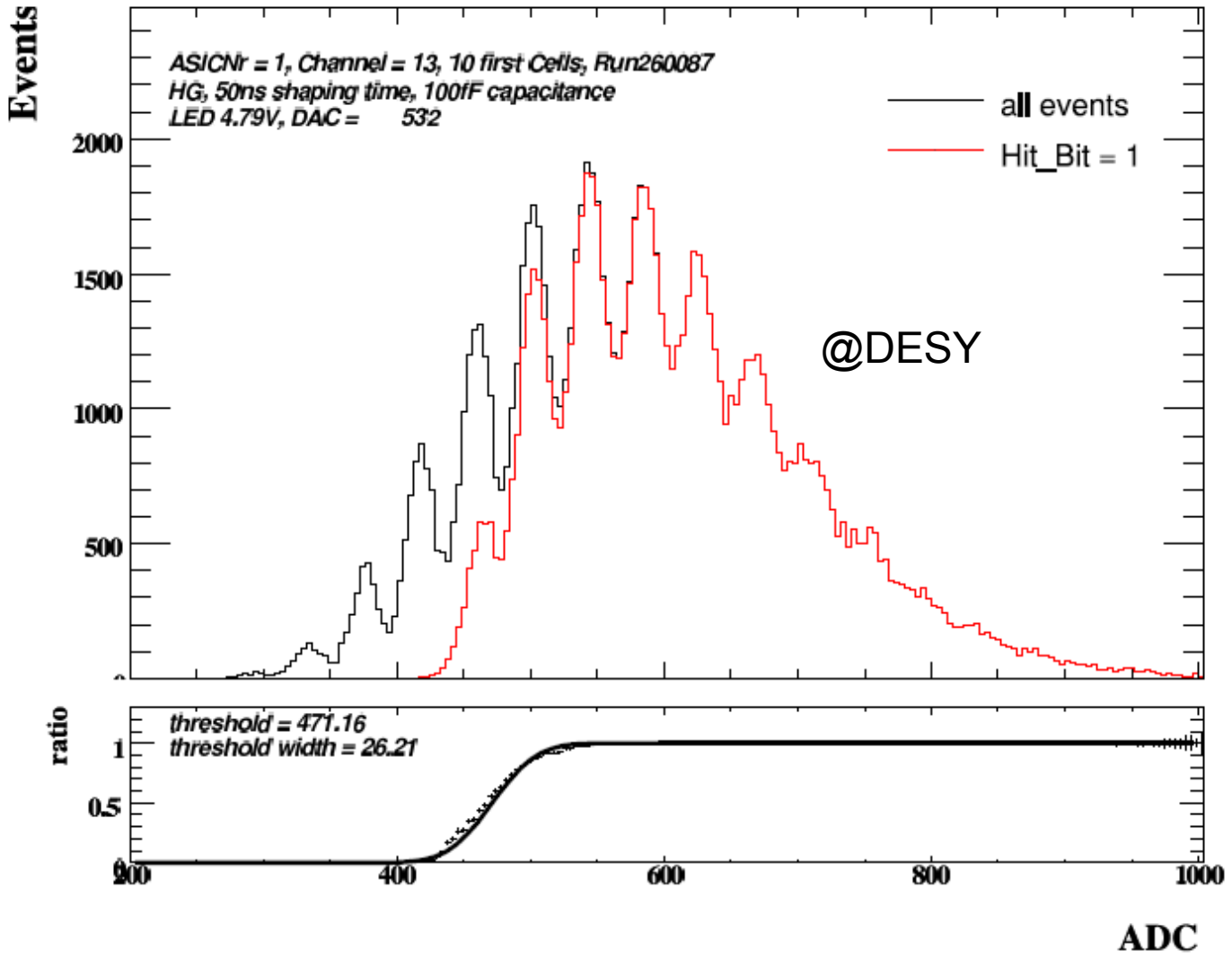




Single-Photon Peaks

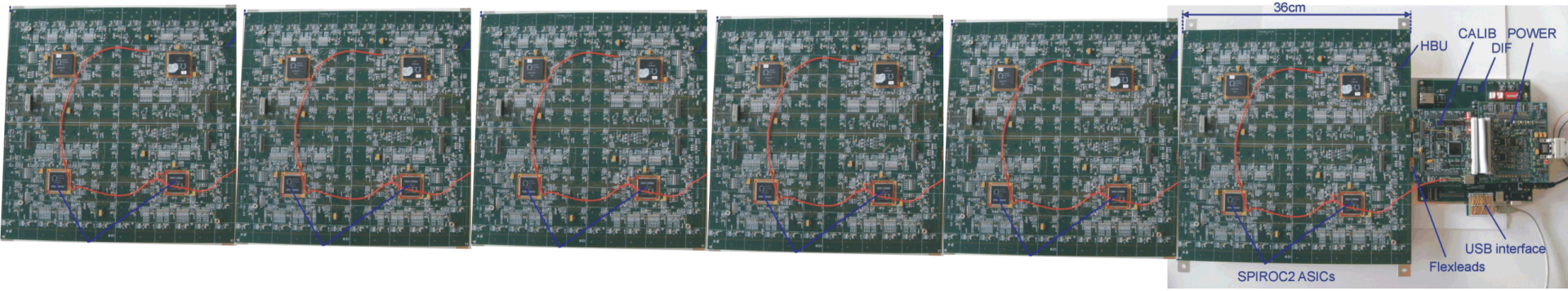


SiPM SPECTRUM with Autotrigger



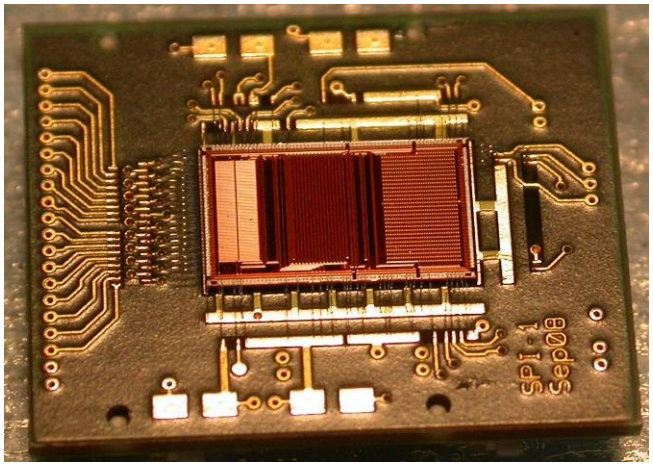
SPIROC status

- 1000 chips produced in March 2010 to make a demonstrator (Large scale tecnological prototype)



- EASIROC : analog version of SPIROC in 2009

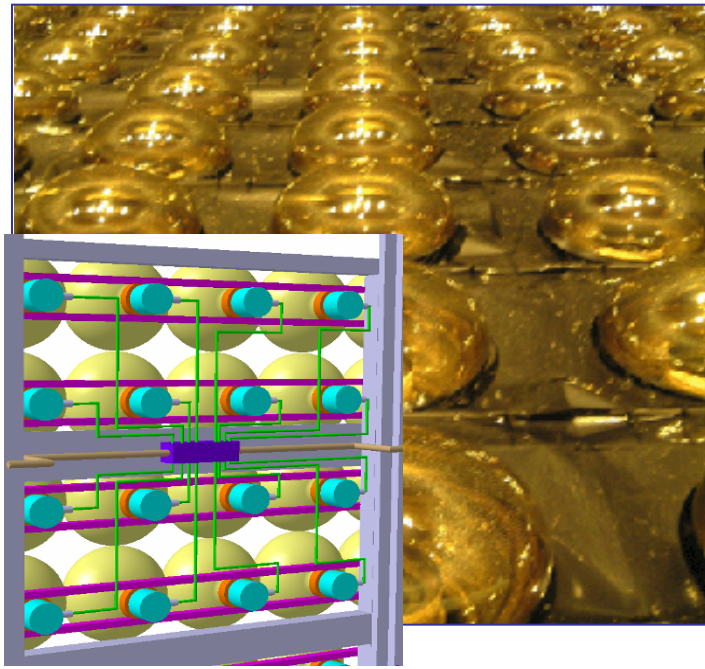
- Other applications:
  - astrophysics PEBS (Aachen),
  - PET (Roma, Pisa, Valencia),
  - nuclear physics (IPNO),
  - Vulcanology (Napoli)



PArISROC for PMm^2

- PArISROC stands for : Photomultiplier Array Integrated in SiGe Read-Out Chip

- Developed for PMm2 project which proposes to segment the very large surface of photo detection in macro pixels made of 16 photomultiplier tubes connected to an autonomous front-end electronics.



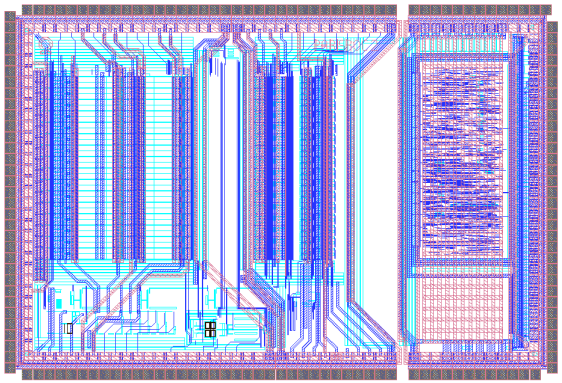
- Replace large PMTs (20") by groups of 16 smaller ones (12") with central ASIC
  - **Independent channels**
  - **Auto-trigger on 1/3 pe**
  - **charge (300 pe) and time (1 ns) measurements**
  - **Only one wire out (DATA + VCC)**
  - **common High Voltage for PMTs**

- Main applications in large Water Cerenkov

  Chip studied by LAGUNA, MENPHYS, LHAASSO…

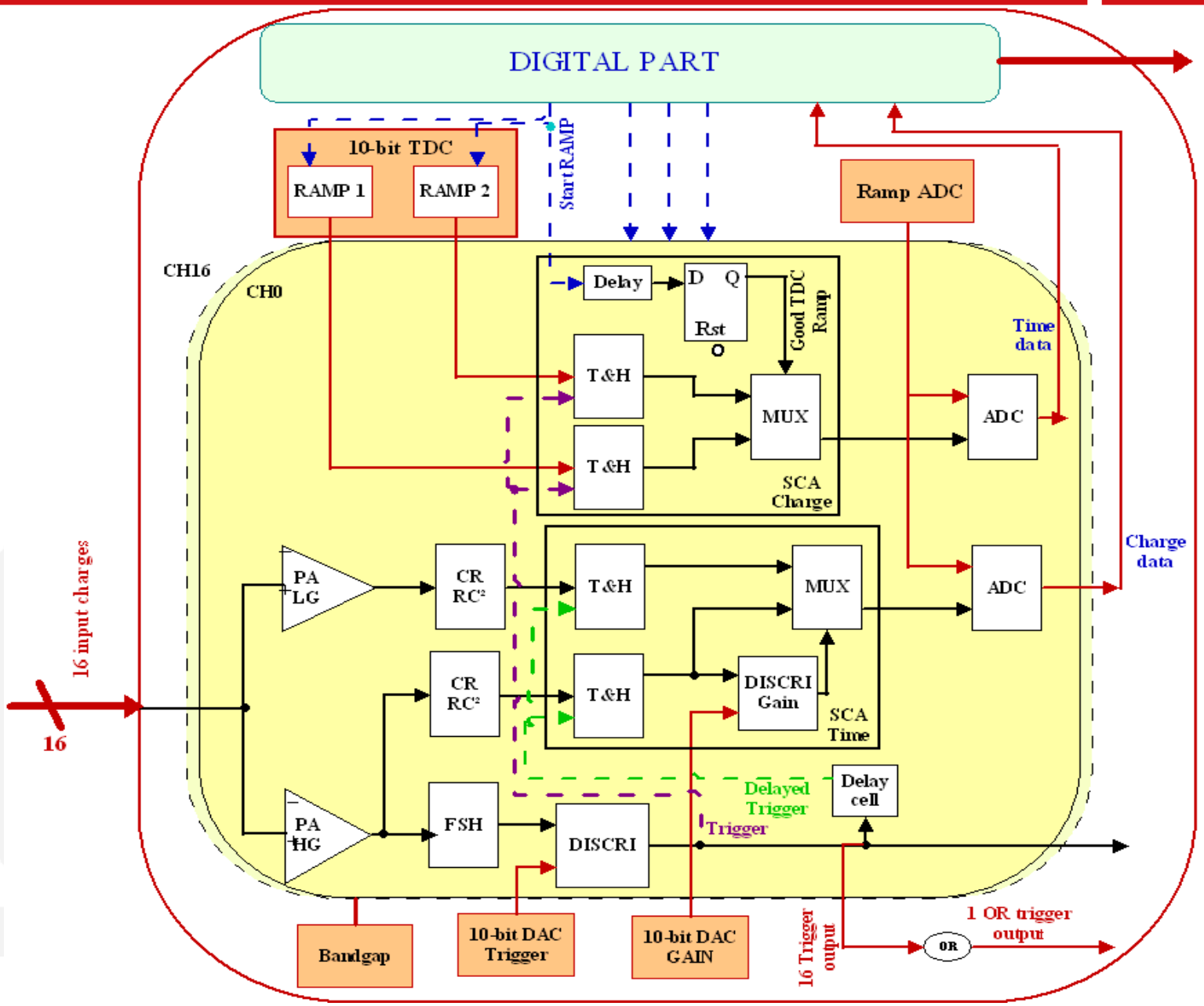
PARiSROC characteristics

- ✓ 16 preamplifier inputs
  - ✓ Input dynamic range : 0 → 300 pe (0 → 50pC) with 1% linearity good precision obtained by 2 preamps (high and low gain)
  - ✓ Variable gain by a factor 4 (8 bits) for PMTs gain adjustment
- ✓ 16 trigger outputs:
  - ✓ Fast shaper (t=15ns) + low offset discriminator
  - ✓ Threshold provided by common internal 10bit DAC
  - ✓ 100 % eficiency at 1/3 pe
  - ✓ "OR" of 16 triggers output
- ✓ 1 multiplexed charge output :
  - ✓ Slow shaper with variable shaping time : τ =25ns,50n or 100ns
  - ✓ Dual Track & Hold
- ✓ 8 to 10-bit internal ADC (Wilkinson) for charge and fine time measurement
- ✓ Internal TDC : 24 bits counter (coarse) + fine 1 ns
- ✓ One serial data output : channel number + Charge + time coarse and fine
- ✓ **Dissipation** : 5mW/ch



PARISROC – 18 mm^2

PARISROC general schematic

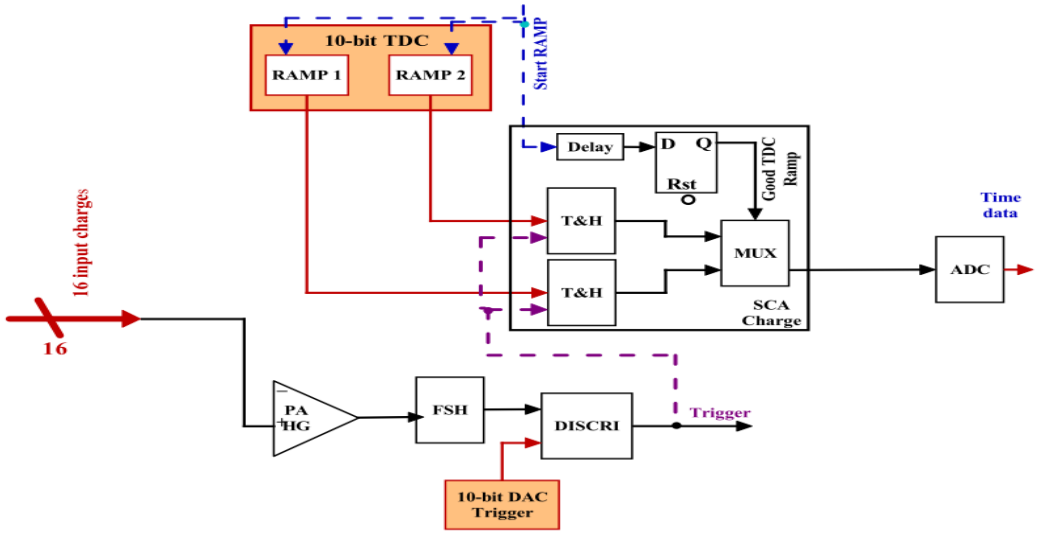


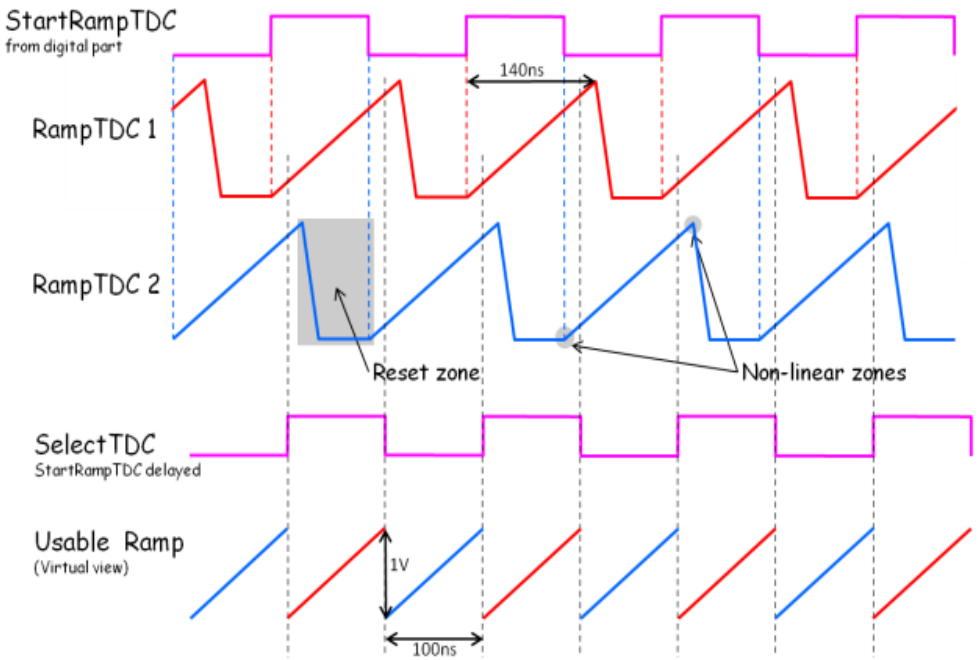
Time measurement

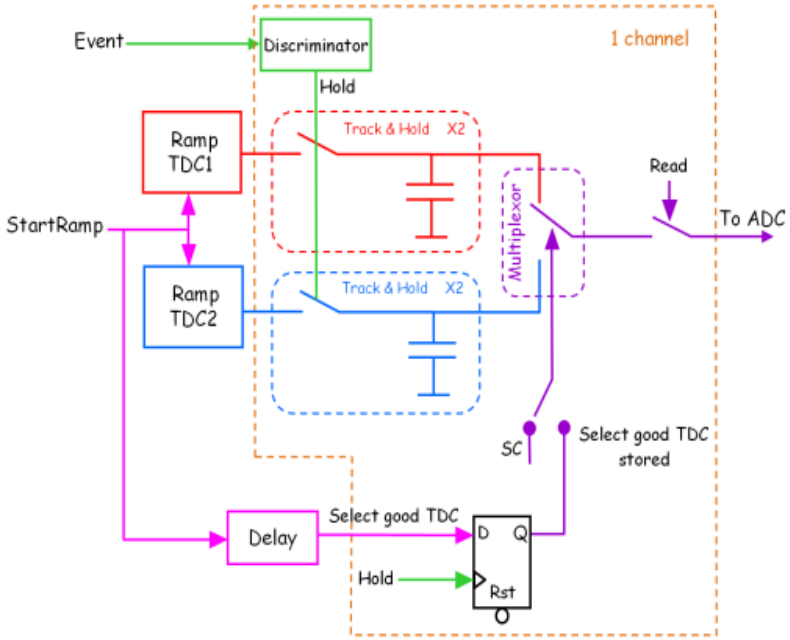
2 systems:

1. Coarse time by 24-bit gray counter
- working at 10 MHz
- with 1.67 s of dynamic
- 100 ns steps

2. Fine time by analog TDC
- 100 ns dynamic
- 100 ps step







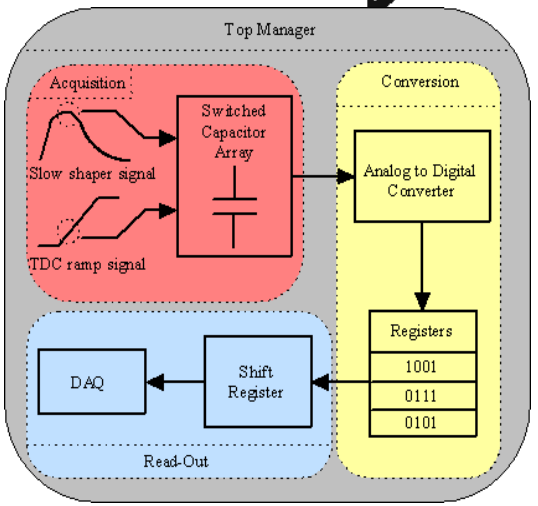
Digital part

4 modules: ***Acquisition, Conversion, Read Out and Top manager***.

Acquisition part manages the track & hold

Conversion part converts charge and time into 10 bits digital values saved in registers (RAM)

Read Out sends the data from memory to an external system



SELECTIVE READ OUT

- **Only hit channels are read**
- **Readout clock : 40 MHz**
- **Max Readout time (16 ch hit) : 25 µs**
- **51 bits of data / hit channel**

	PARIROC 2
Conversion Time	26 µs
Readout Time	25 µs
Total cycle duration	51 µs

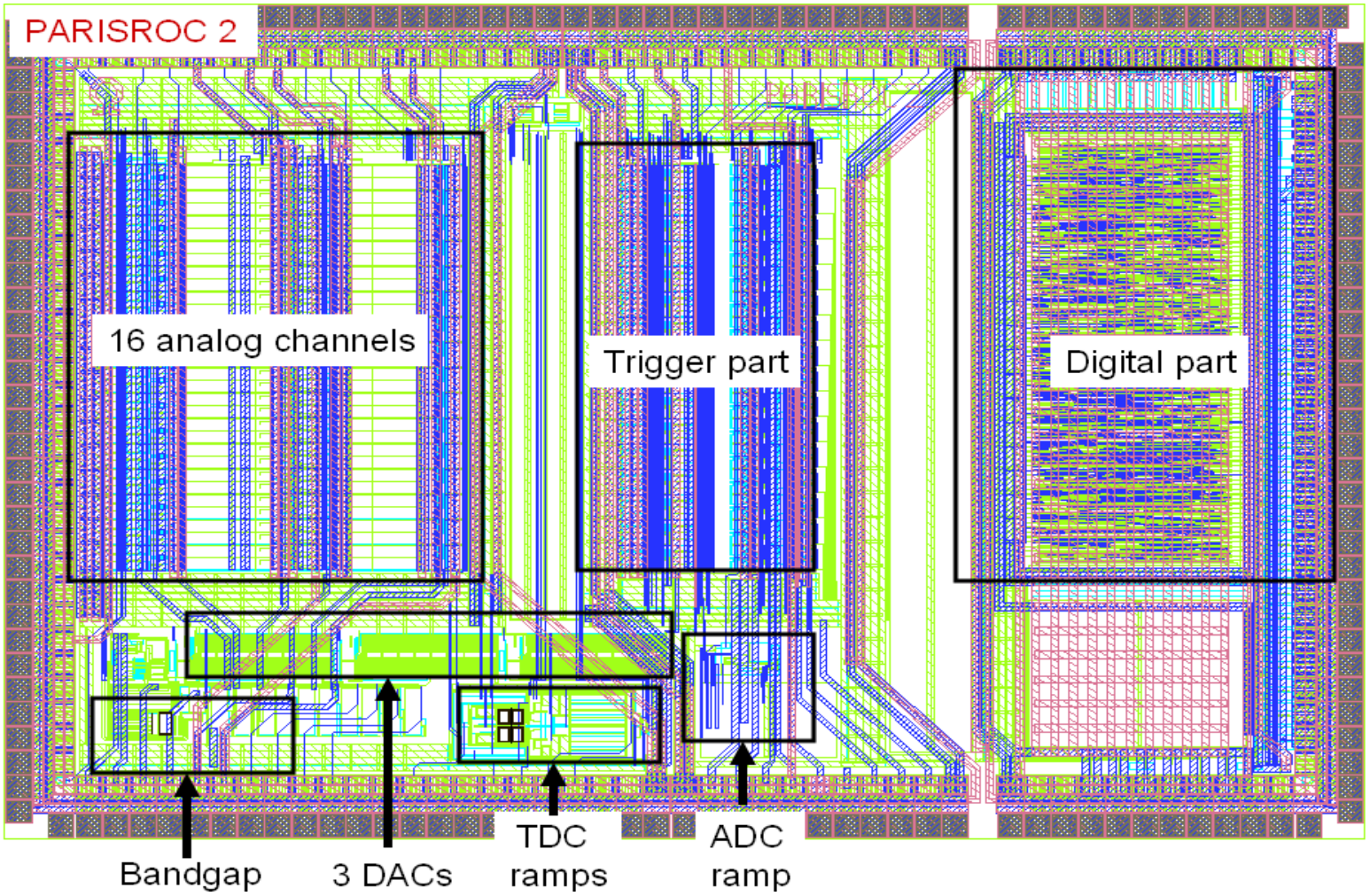
	PARIROC version 2
Channel number	4
Coarse time counter	24
Extra Coarse time	1
Gain used	1
Charge converted	10
Fine time (TDC) used	1
Fine time (TDC) converted	10
Total	51 bits

PARISROC2 layout

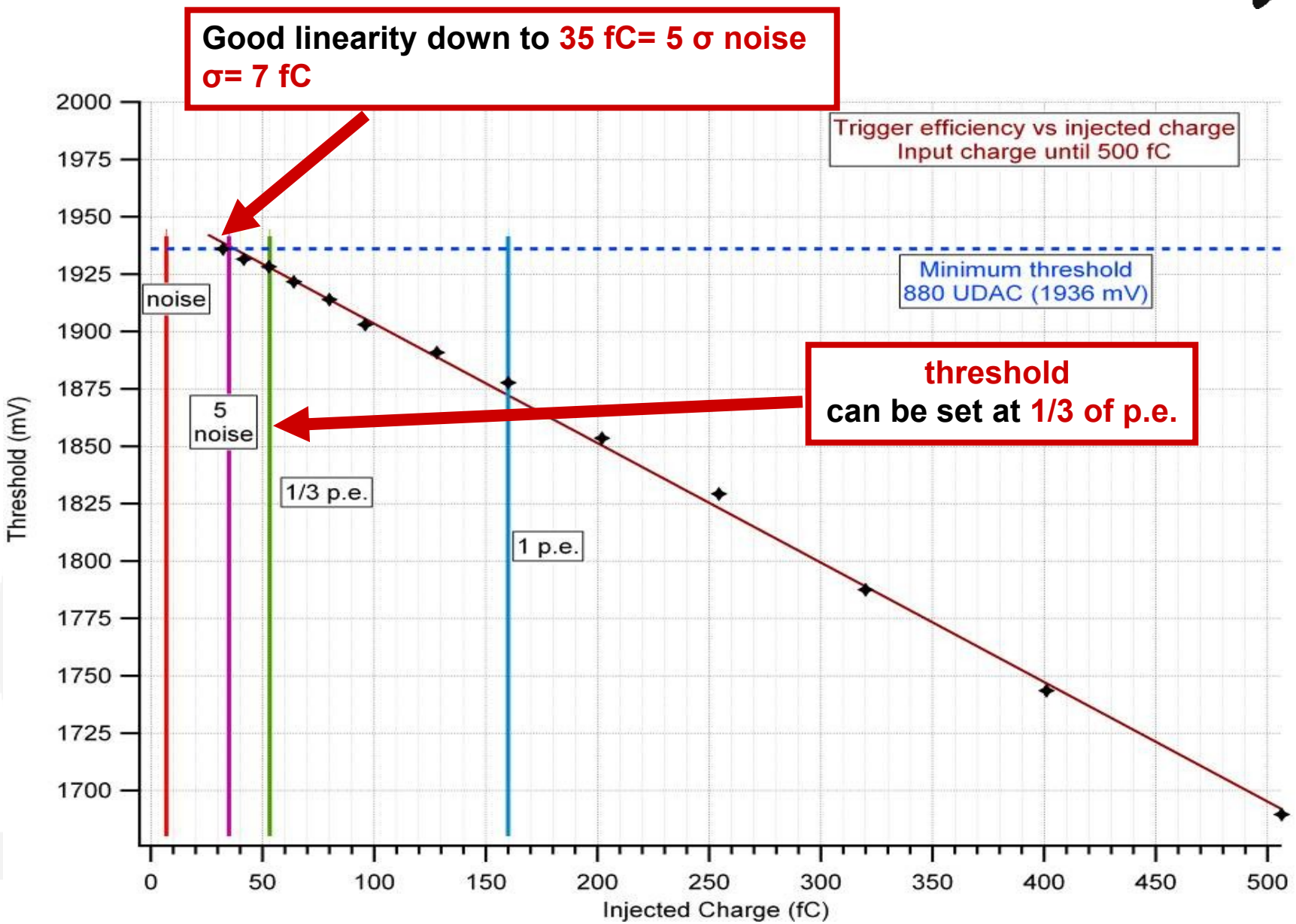
Technology: AMS SiGe 0.35 µm

Surface: 18 mm²

Package: CQFP160



Trigger efficiency



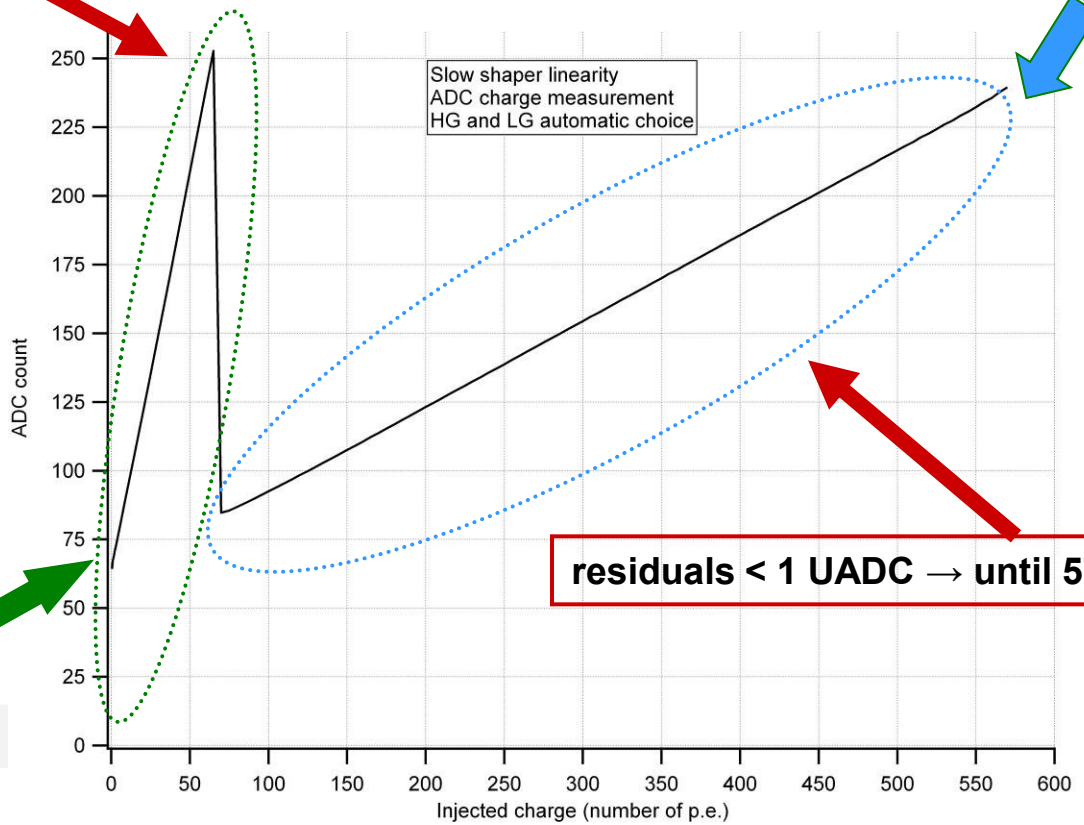
Auto-gain test (ADC measurements)

The whole chain is tested, injecting a charge at the input of the channel: the signal is amplified, auto-triggered, held in the SCA cell and converted by the ADC.

The charge measurements for different injected charges setting the gain threshold at 60 p.e.

residuals < 1 UADC → until 60 p.e.

Low gain Up to 570 p.e.



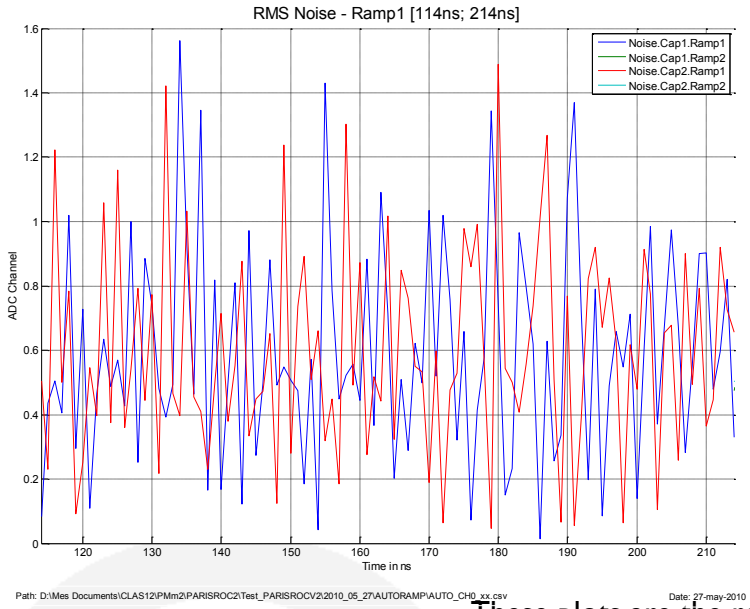
Automatic gain selection

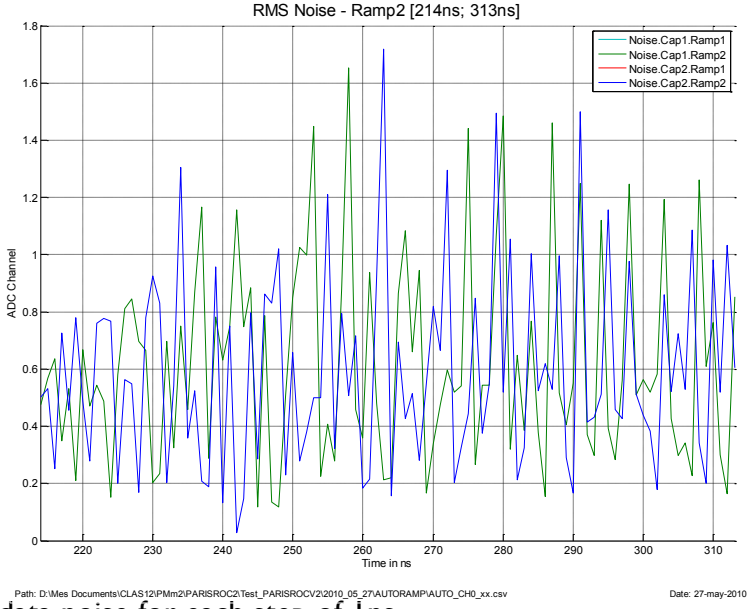
Good performance of the whole chain.

residuals < 1 UADC → until 570 p.e.

High gain Up to 60 p.e.

PARISROC TDC ramps Noise





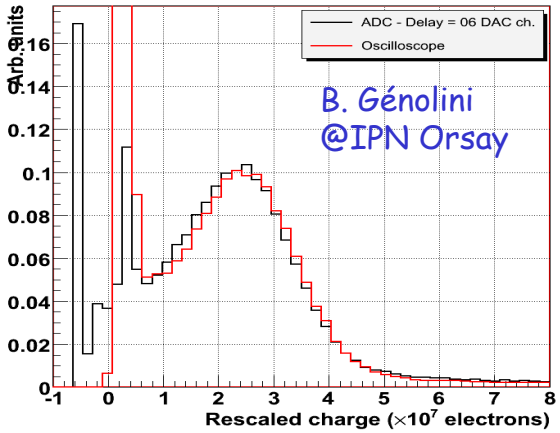
These plots are the row data noise for each step of 1ns.
Do not forget that the generator have a 107ps jitter.

Capacitor	Row Noise (Quadratic Mean)	TDC Noise (Quadratic Mean)	Max TDC Noise
Ramp1.Cap2	0.68ch = 148ps	102ps	306ps
		111ps	
Ramp2.Cap2	0.68ch = 147ps	101ps	356ps

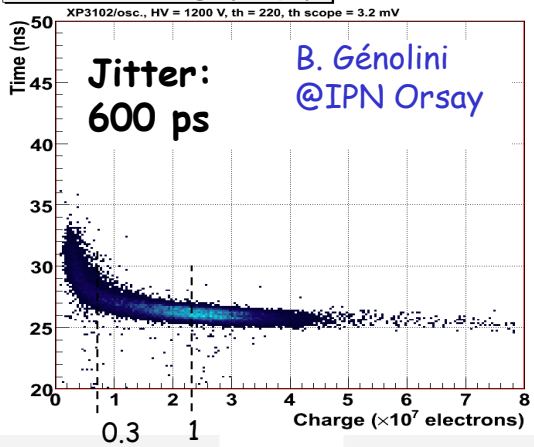
PMT measurements

PARISROC 2 ASIC has been tested with 1-inch PMT.

SER (1840 V)

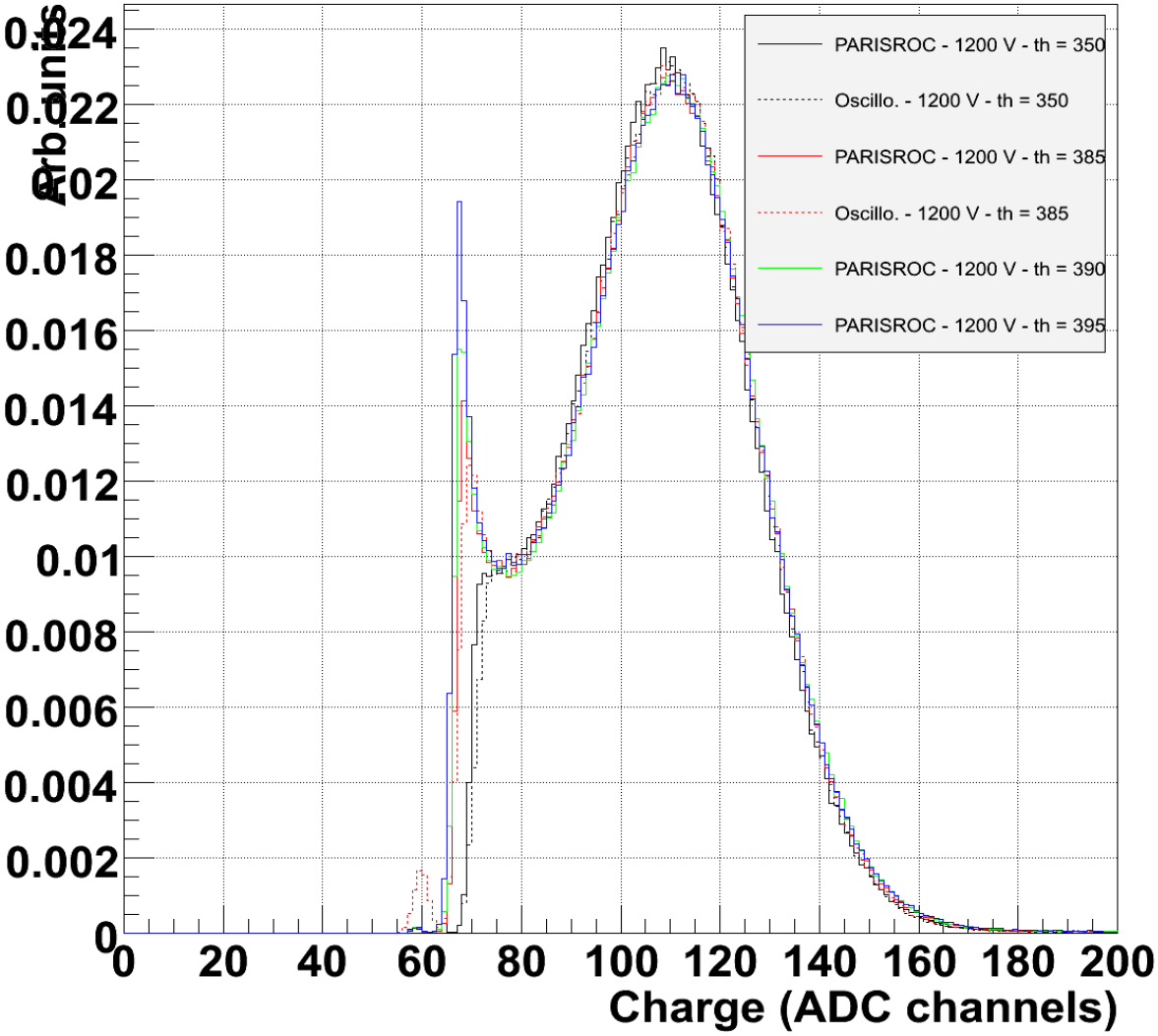


NOR16 vs charge (scope)

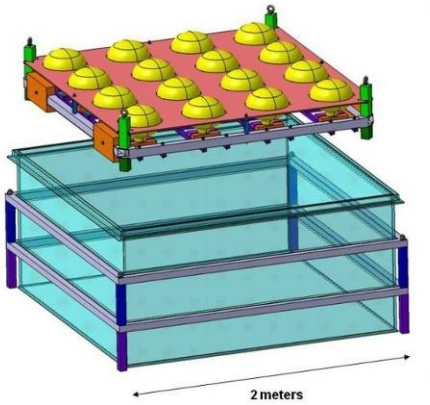


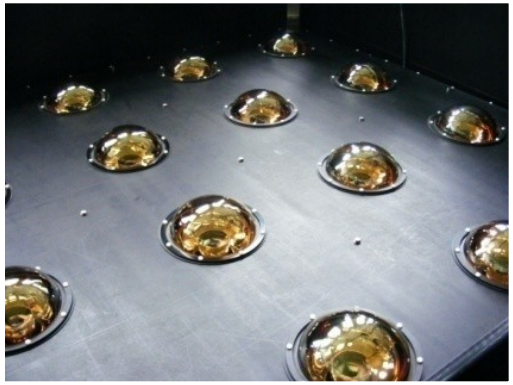
Charge spectrum

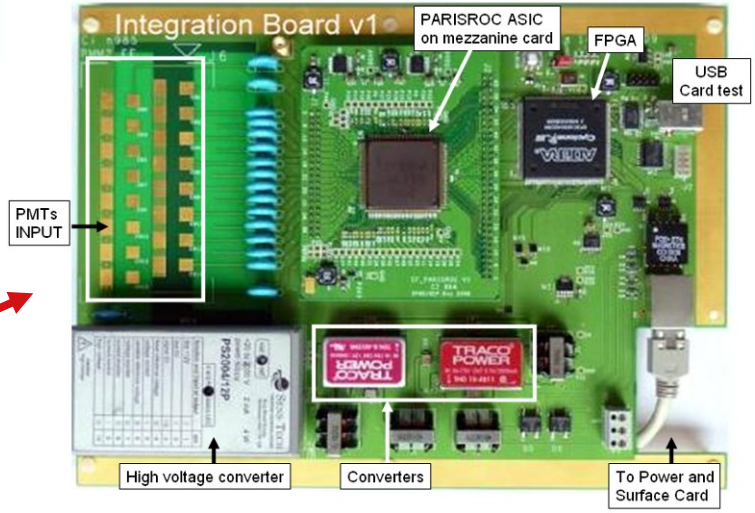
Charge histograms 1-inch PMT at a voltage of 1200 V (gain around 10^7) versus thresholds (350, 385, 390 and 395). The pedestal is at 58 ADC channels.



Demonstrator realisation







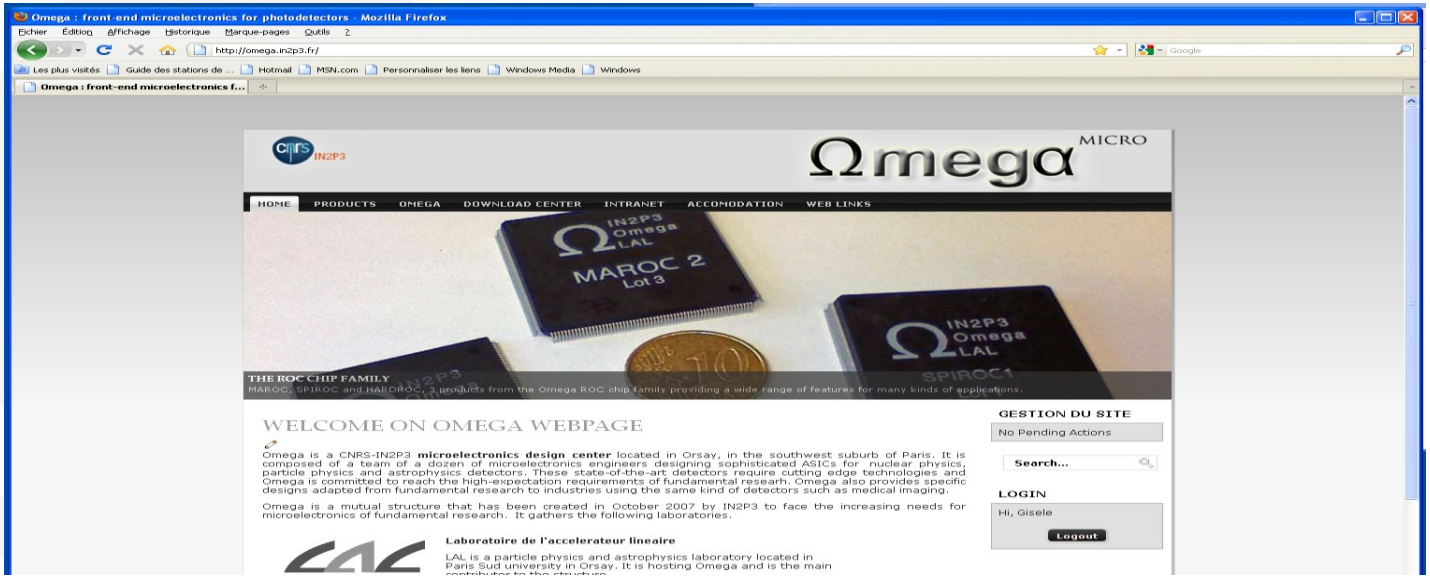
Demonstrator realized by the IPNO with 16 x 8-inch Hamamatsu tubes.

This demonstrator and the PARISROC2 ASIC in a water-tight box was put in a water tank by **MEMPHYNO** collaboration (APC and LAPP).

Conclusion

- 1000 chips MAROC and SPIROC produced in dedicated run in 2010.
- Chips (SoC) very versatile, many parameters tunable (gain, speed…)

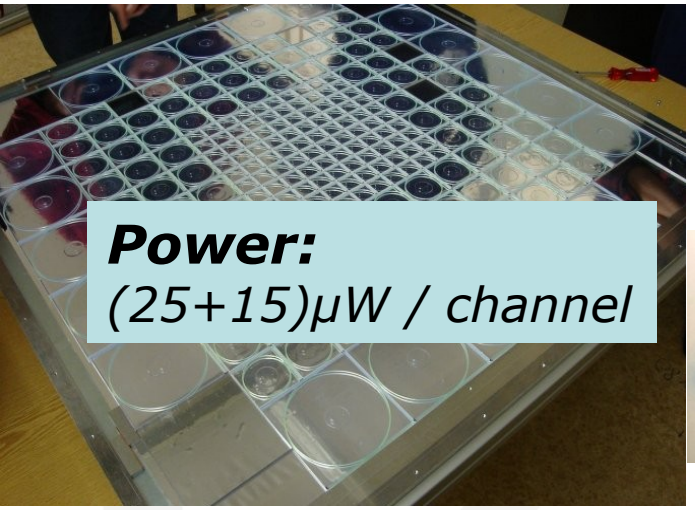
- More information on PARISROC, MAROC or SPIROC on website http://omega.in2p3.fr



Thank you for your attention

AHCAL: Technological prototype

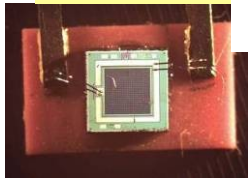
- SiPM detector: 40 layers of 1.5 m^2 2c thick steel plates interleaved with cassettes of 296 scintillating tiles (3x cm^2) readout by SiPMs
- 8 Millions of channels
- Few external components
- FE Chip embedded inside the detecto
  - Thickness:critical issue: Mother boards (HBU) are sandwiched between 2 absorber plates

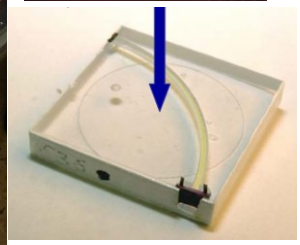


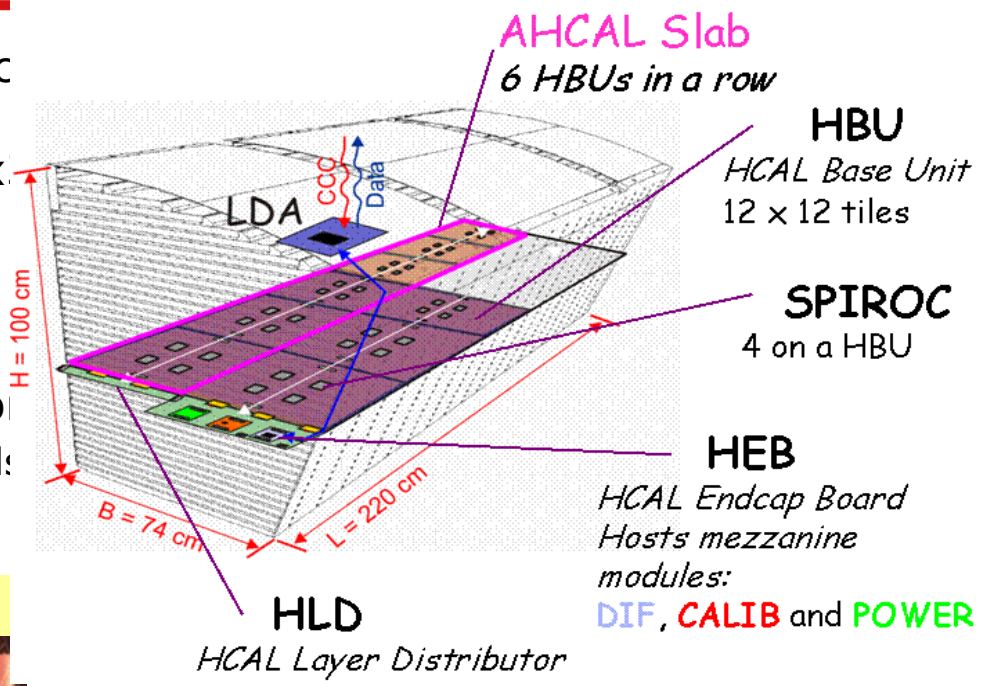
Power:
(25+15)µW / channel

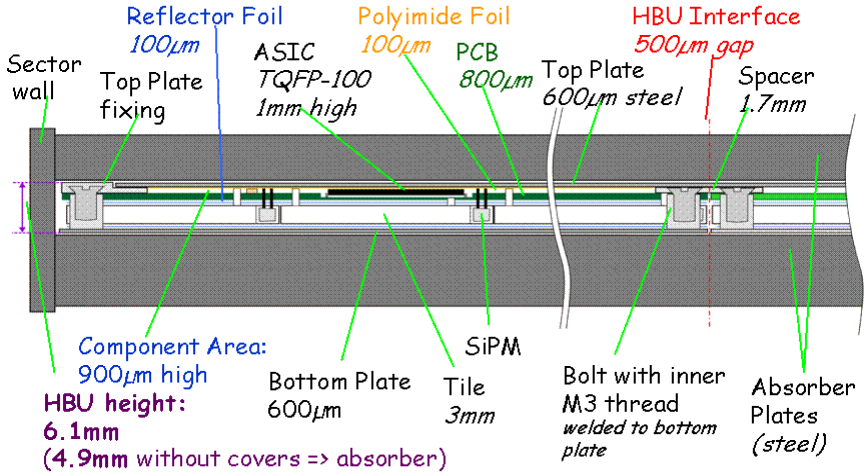
@Peter Goetlicher's talk

Mephy SiPM



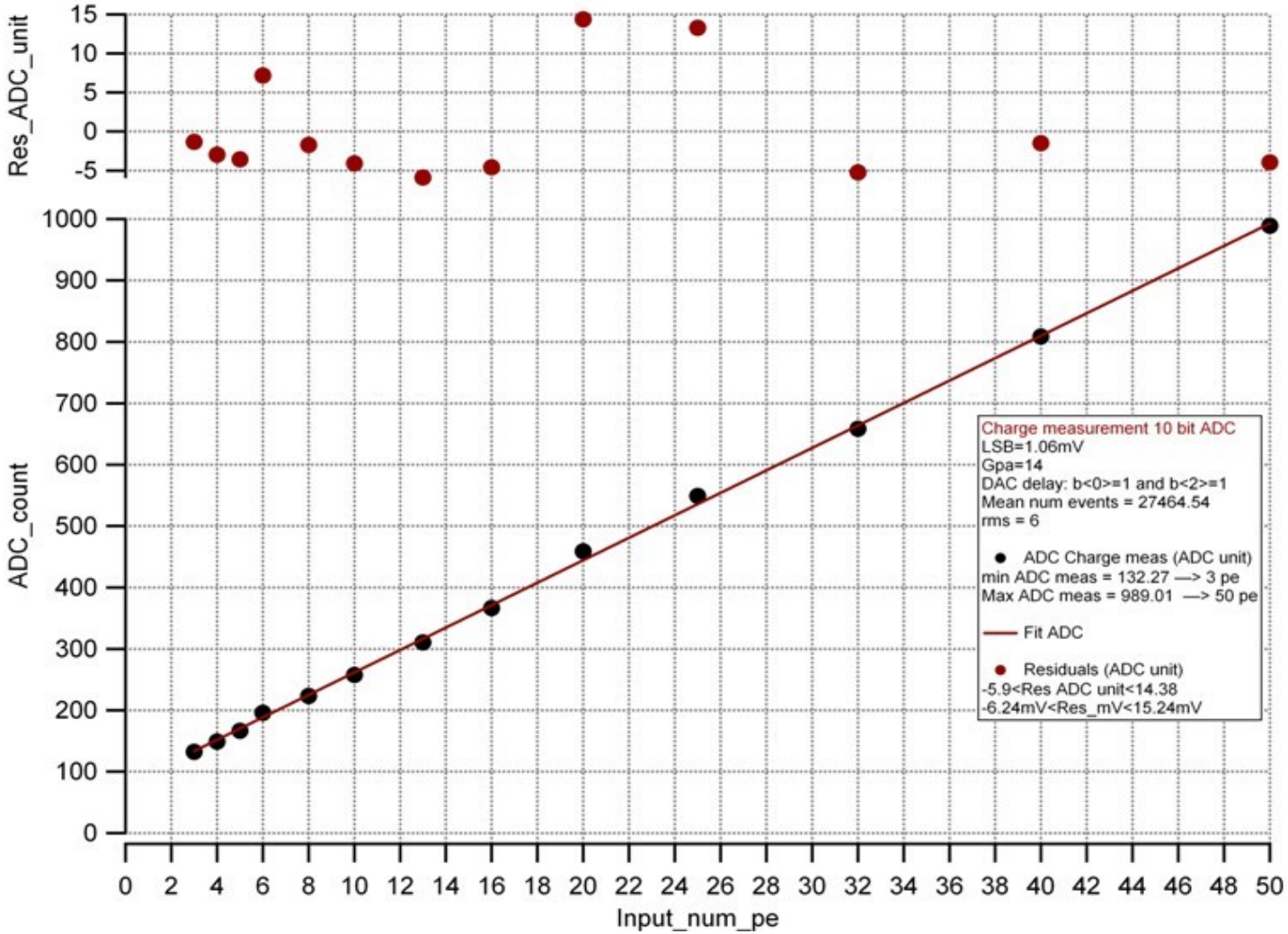




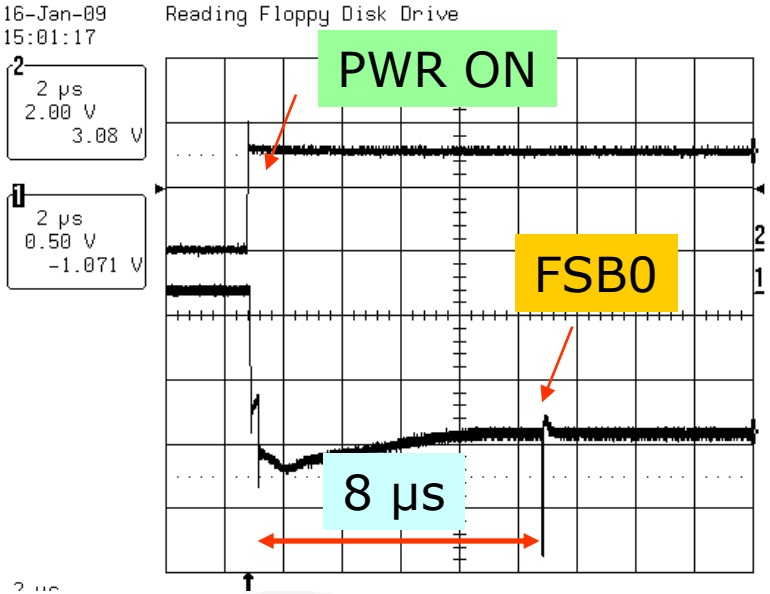


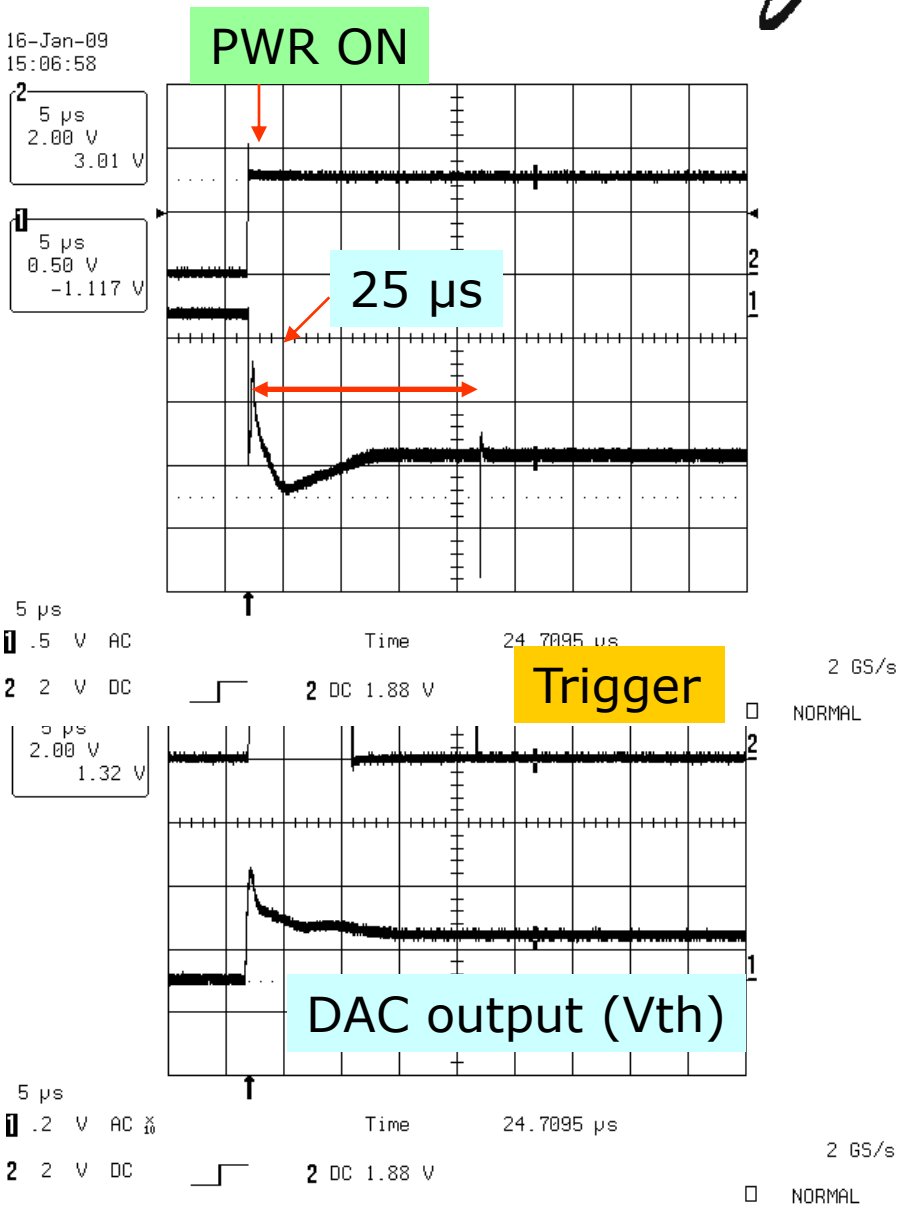
Overall behaviour in 10 bits

- Complete chain : autotrigger + T&H + internal ADC
- Linearity : 1%, noise 6 UADC



Power pulsing: « Awake » time



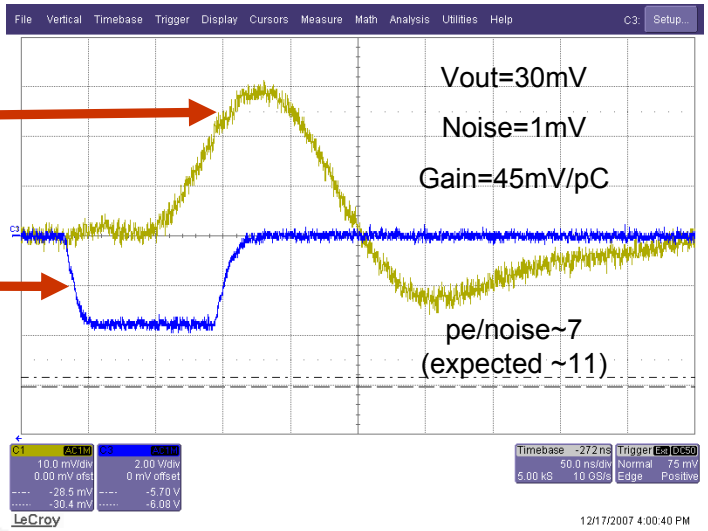


- **All decoupling capacitors removed**
- **PWR ON: ILC like (1ms,199ms)**
- **PP of the analog part:**
  - **Input signal synchronised on PWR ON**
  - **=> Awake time= 8 µs**
- **Power pulsing of the DAC:**
  - **25 µs (slew rate limited)**

SPIROC charge measurement

High gain channel output

680fC (~4 pe @SiPM gain=10^6) in SPIROC



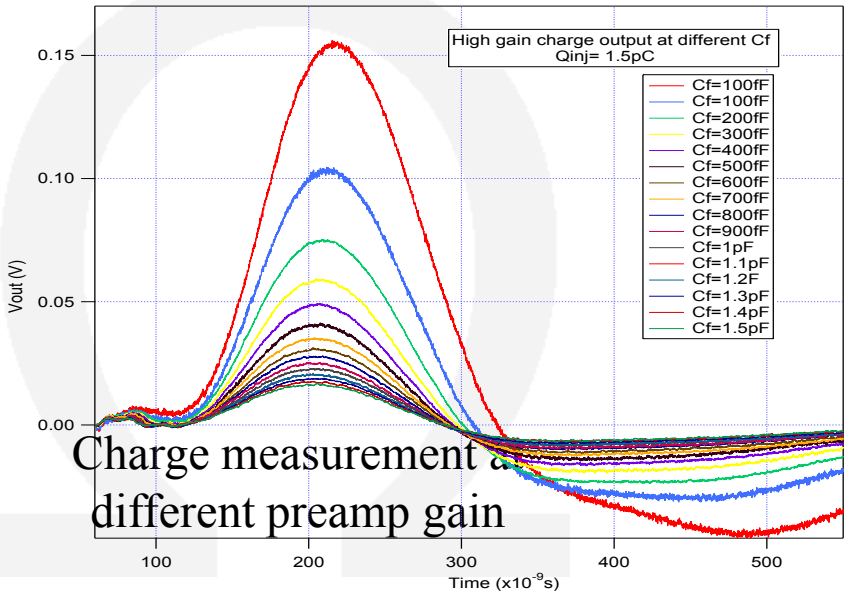
Charge measurement

Auto trigger

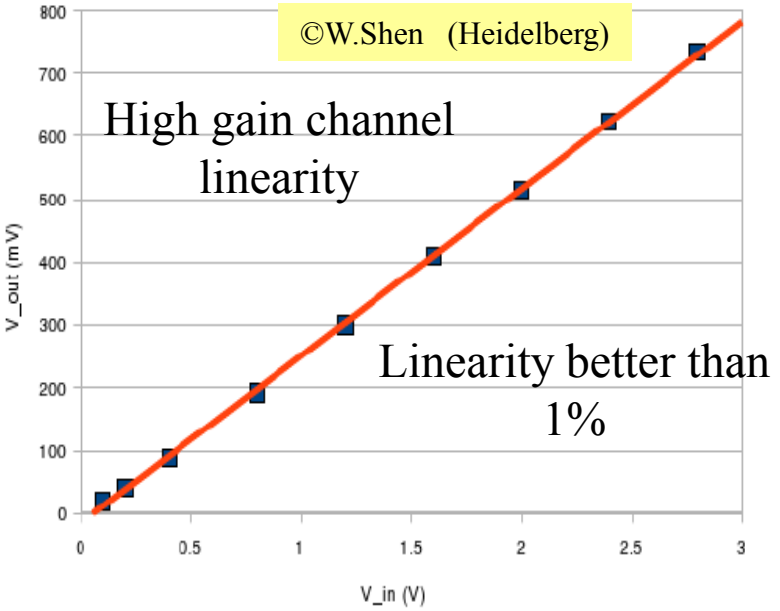
Set up:

Cf=400fF

Tau=50ns

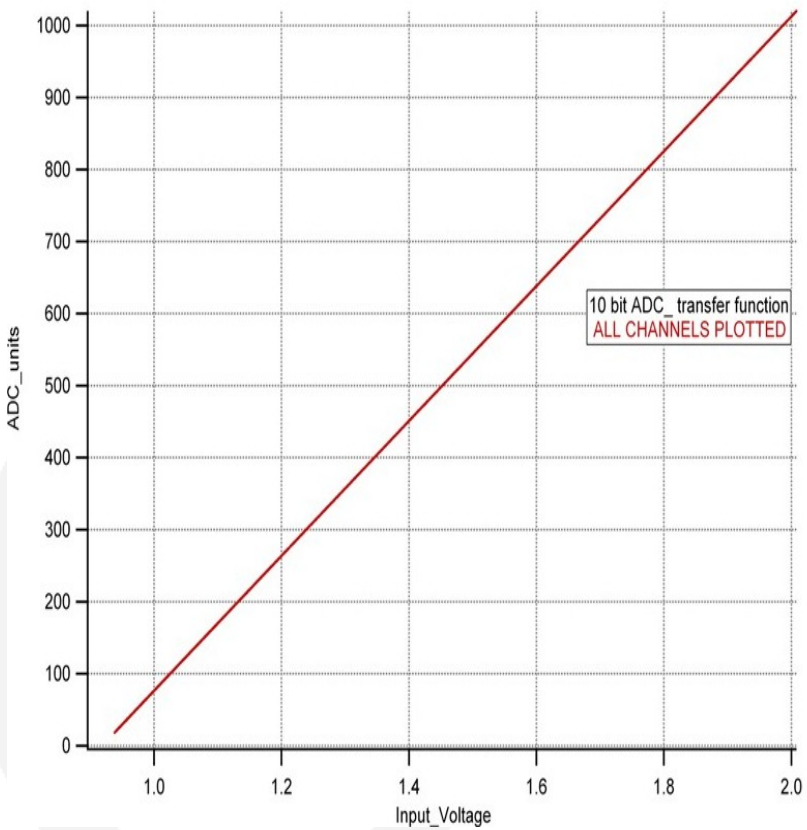


Cf = 700fF ,Tau=50ns Cc-100pF, 20dB

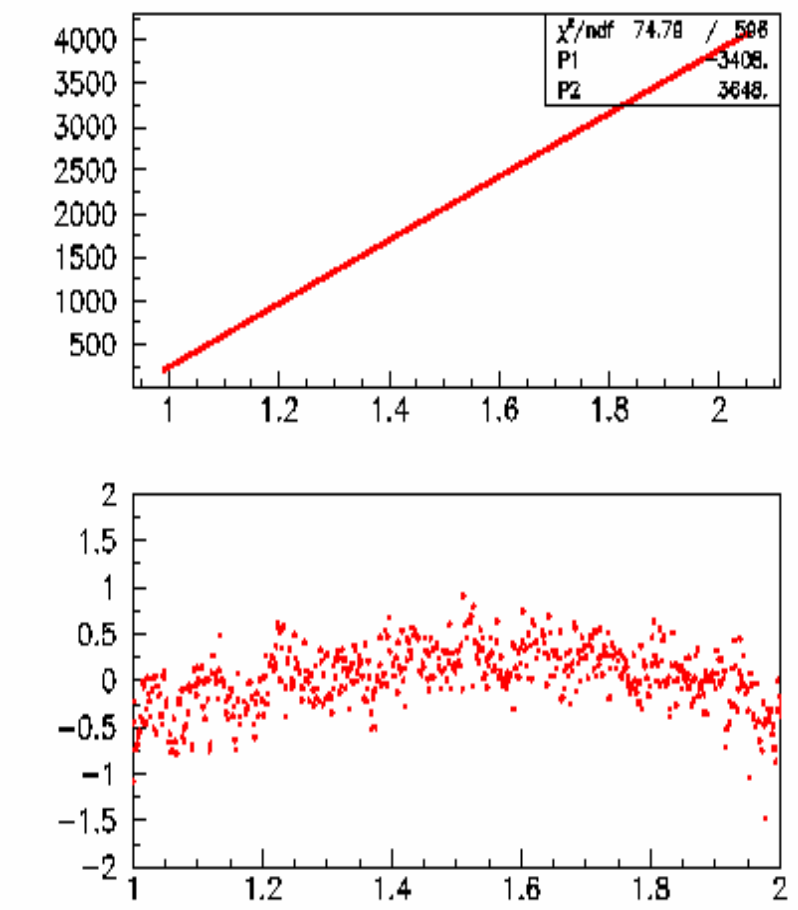


Internal Wilkinson ADC

- Wilkinson ADC well suited to multichannel conversion
- Very good uniformity and linearity



Uniformity of 10bit Wilkinson ADC
16 channels superimposed !



Linearity of 12bit Wilkinson ADC