Paul Scherrer Institute

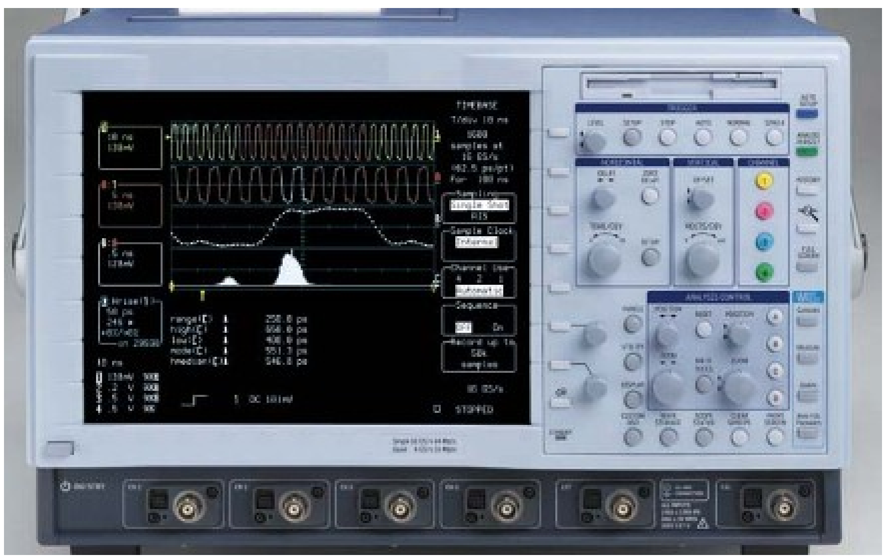
Stefan Ritt

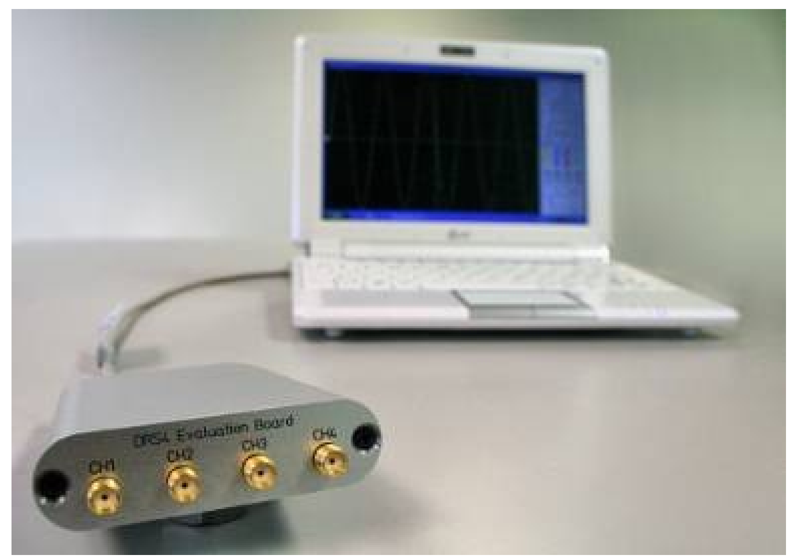
Very Fast Waveform Recorders

Question ?

4 channels
5 GSPS
1 GHz BW
8 bit (6-7)
15k€

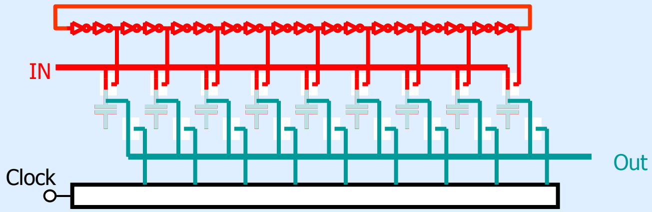
4 channels
5 GSPS
1 GHz BW
11.5 bits
900€
USB Power



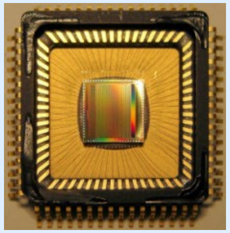


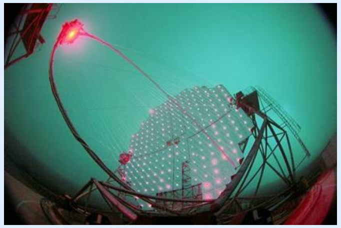
Overview

- Design Principles and Limitations of Switched Capacitor Arrays

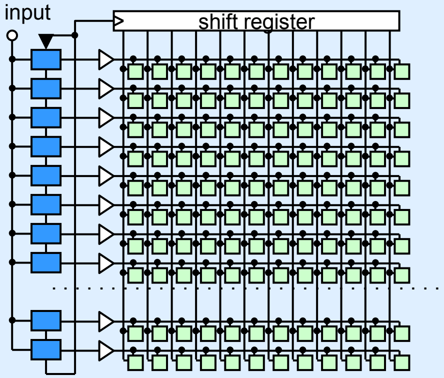


- Overview of Chips and Applications

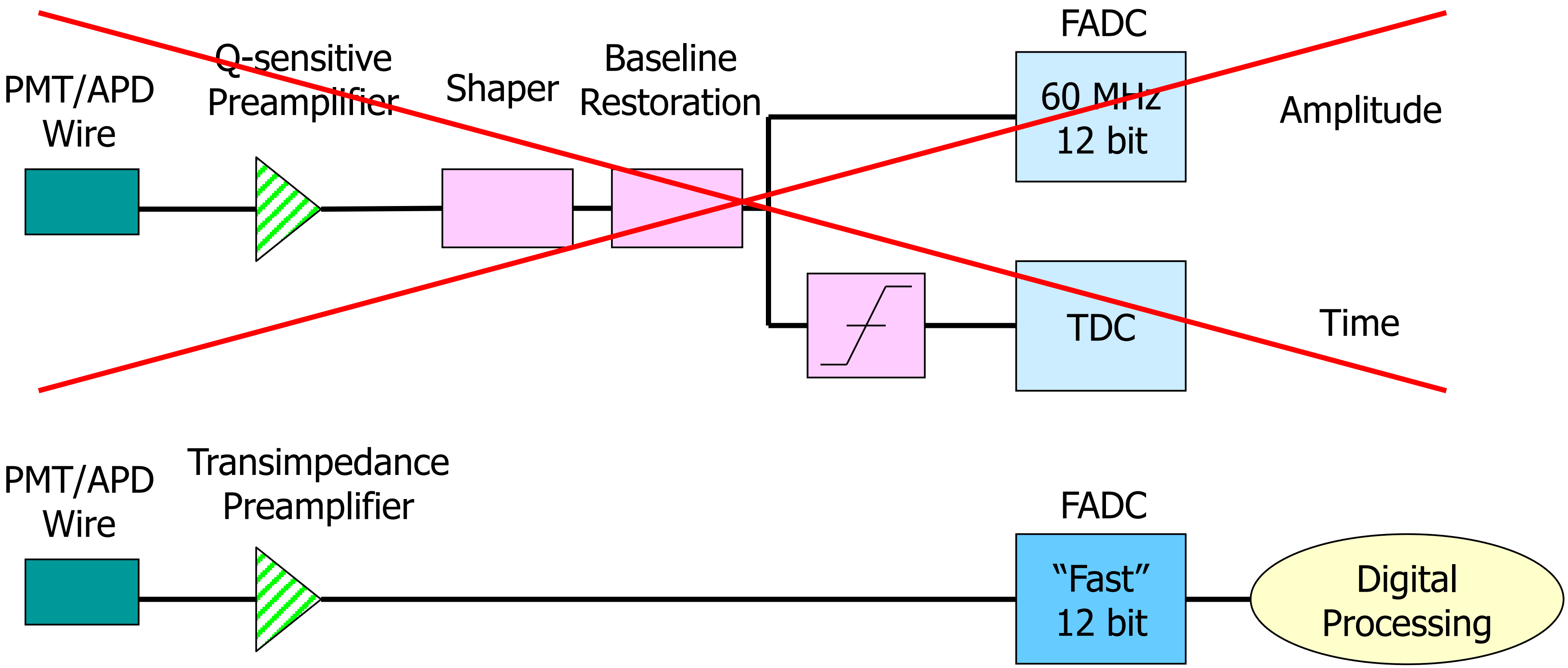




- Future Design Directions



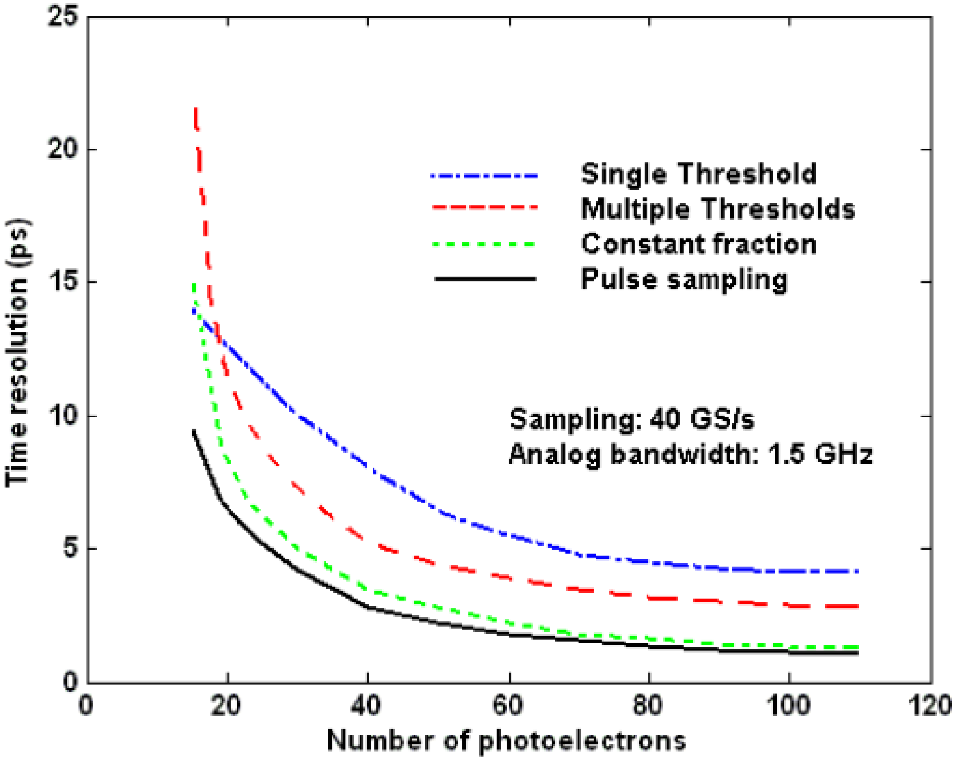
Flash ADC Technique



- Shaping stage can only remove information from the signal
- Shaping is unnecessary if FADC is "fast" enough
  = sampling speed 2x maximum frequency (Nyquist-Shannon)
- All operations (CFD, optimal filtering, integration) can be done digitally

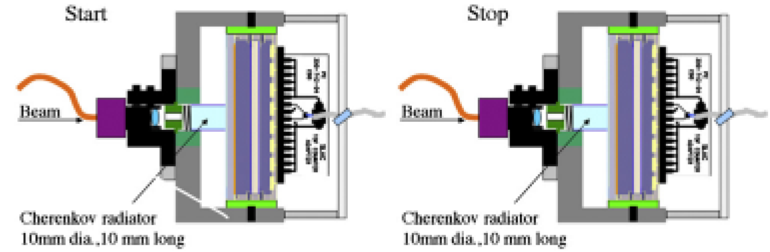
How to measure best timing?

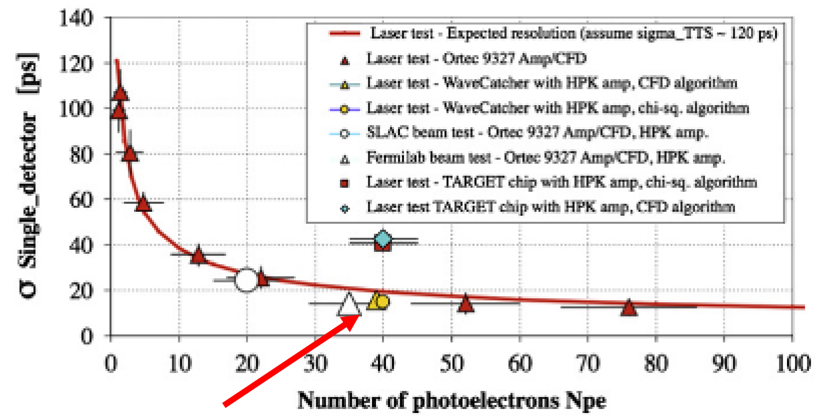
Simulation of MCP with realistic noise and different discriminators



J.-F. Genat et al., arXiv:0810.5590 (2008)

Beam measurement at SLAC & Fermilab

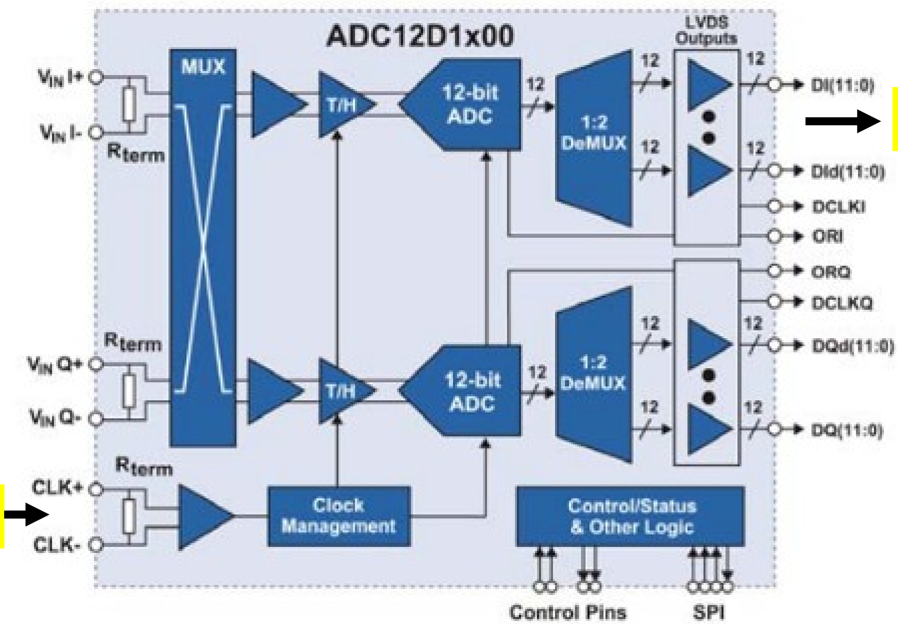




D. Breton et al., NIM **A629**, 123 (2011)

Currently available fast ADCs

- 8 bits – 3 GS/s – 1.9 W → 24 Gbits/s
- 10 bits – 3 GS/s – 3.6 W → 30 Gbits/s
- 12 bits – 3.6 GS/s – 3.9 W → 43.2 Gbits/s
- 14 bits – 0.4 GS/s – 2.5 W → 5.6 Gbits/s



24x1.8 Gbits/s

1.8 GHz!

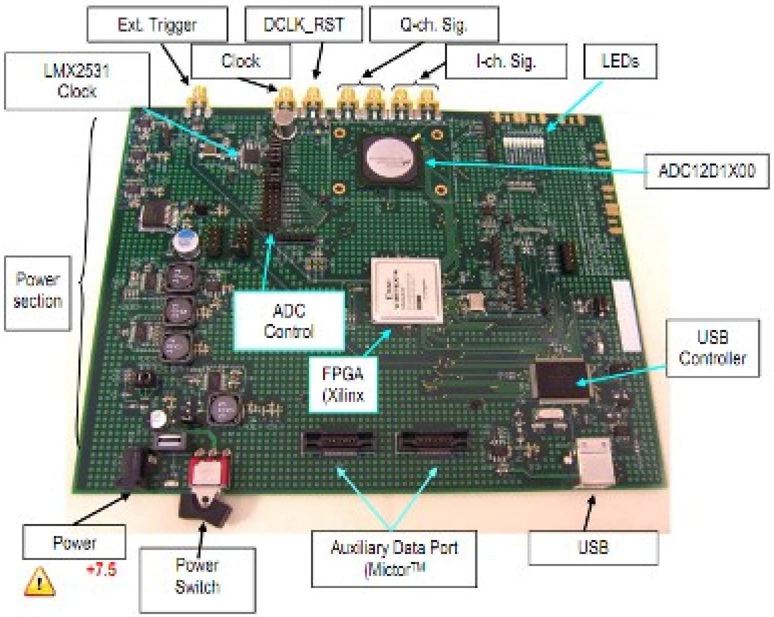
- Requires high-end FPGA
- Complex board design
- FPGA power

ADC boards

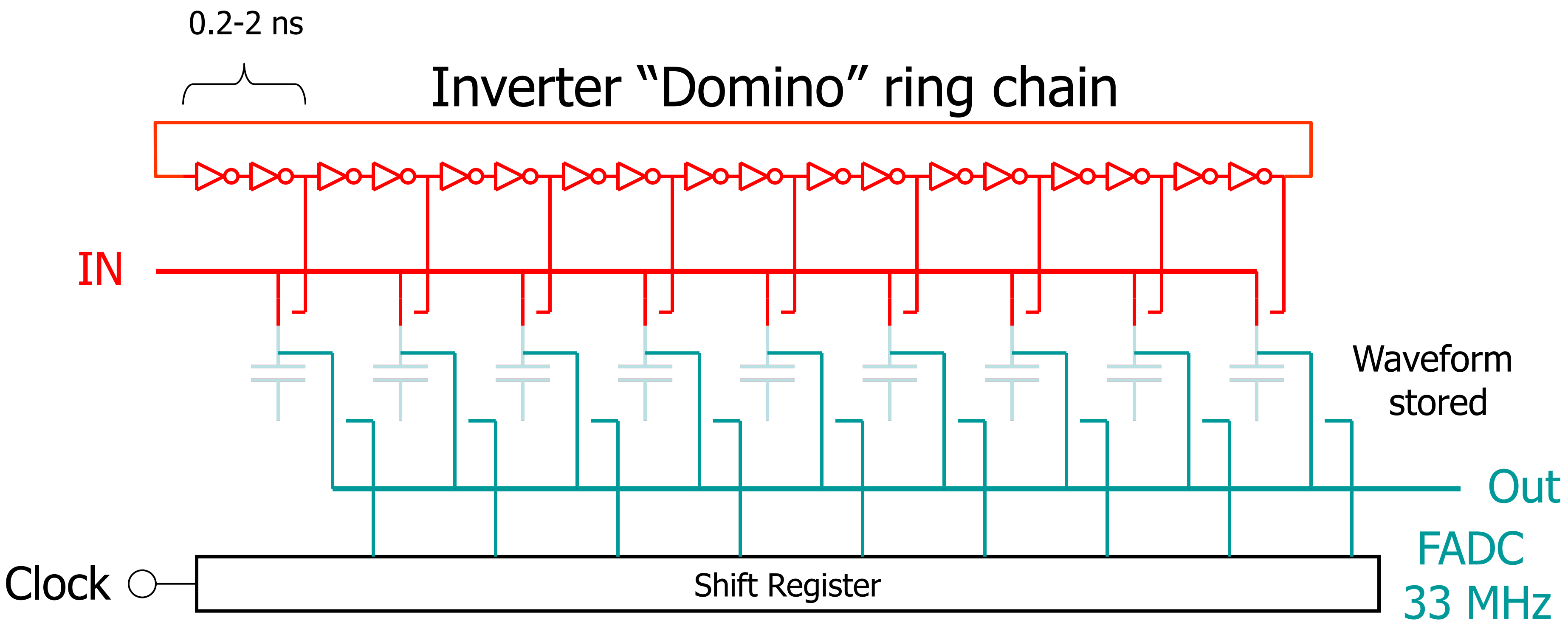
- PX1500-4:
  2 Channel
  3 GS/s
  8 bits

- ADC12D1X00RB:
  1 Channel
  1.8 GS/s
  12 bits

1-10 k€ / channel



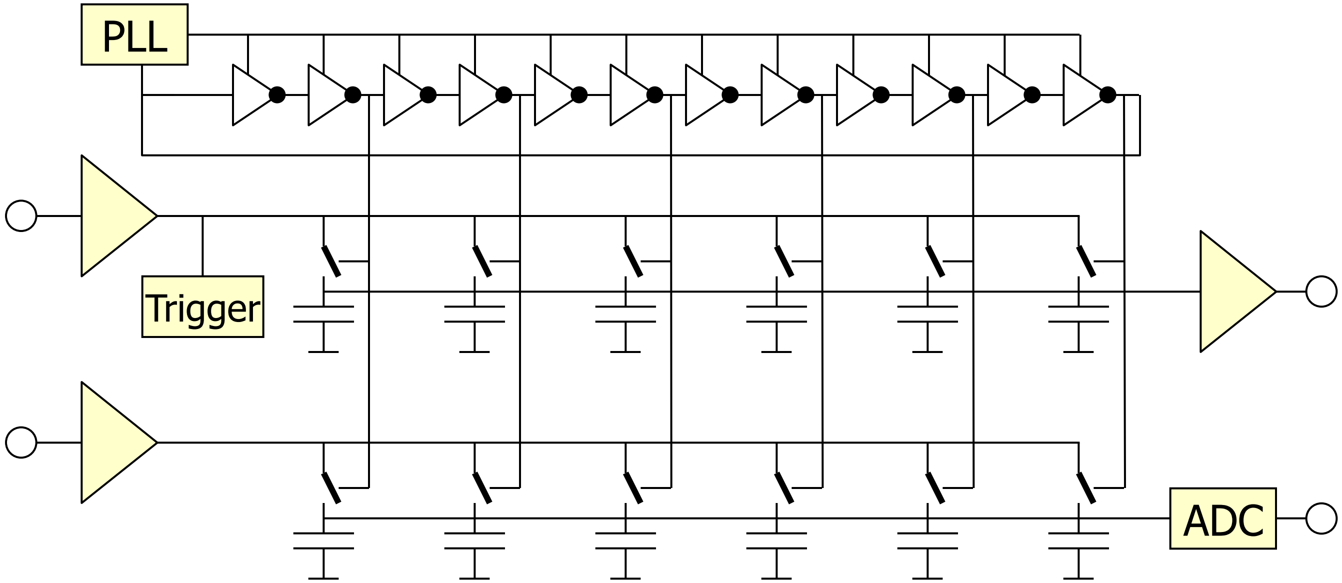
Switched Capacitor Array (Analog Memory)



"Time stretcher" GHz → MHz

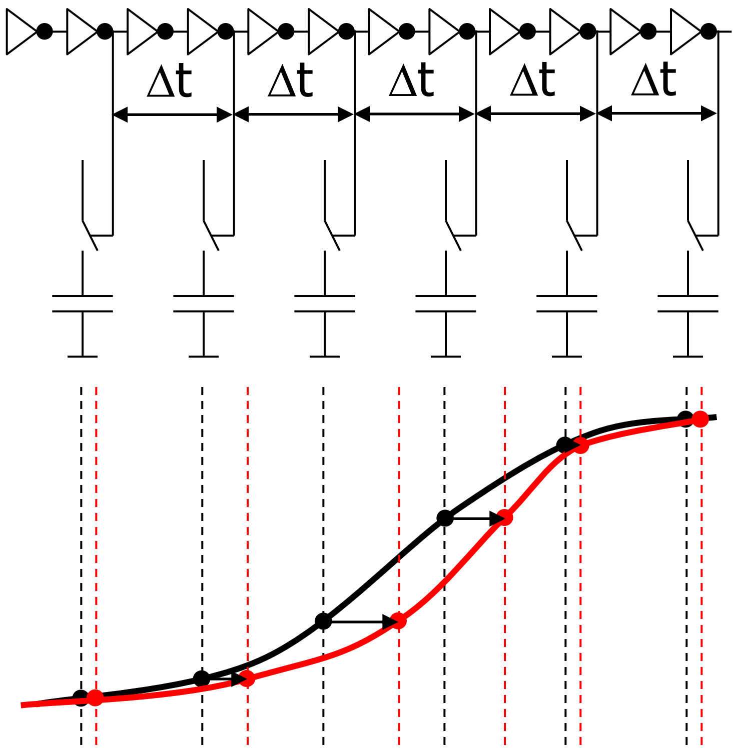
Design Options

- CMOS process (typically 0.35 … 0.13 μm) → sampling speed
- Number of channels, sampling depth, differential input
- PLL for frequency stabilization
- Input buffer or passive input
- Analog output or (Wilkinson) ADC
- Internal trigger
- Exact design of sampling cell



Pros and Cons

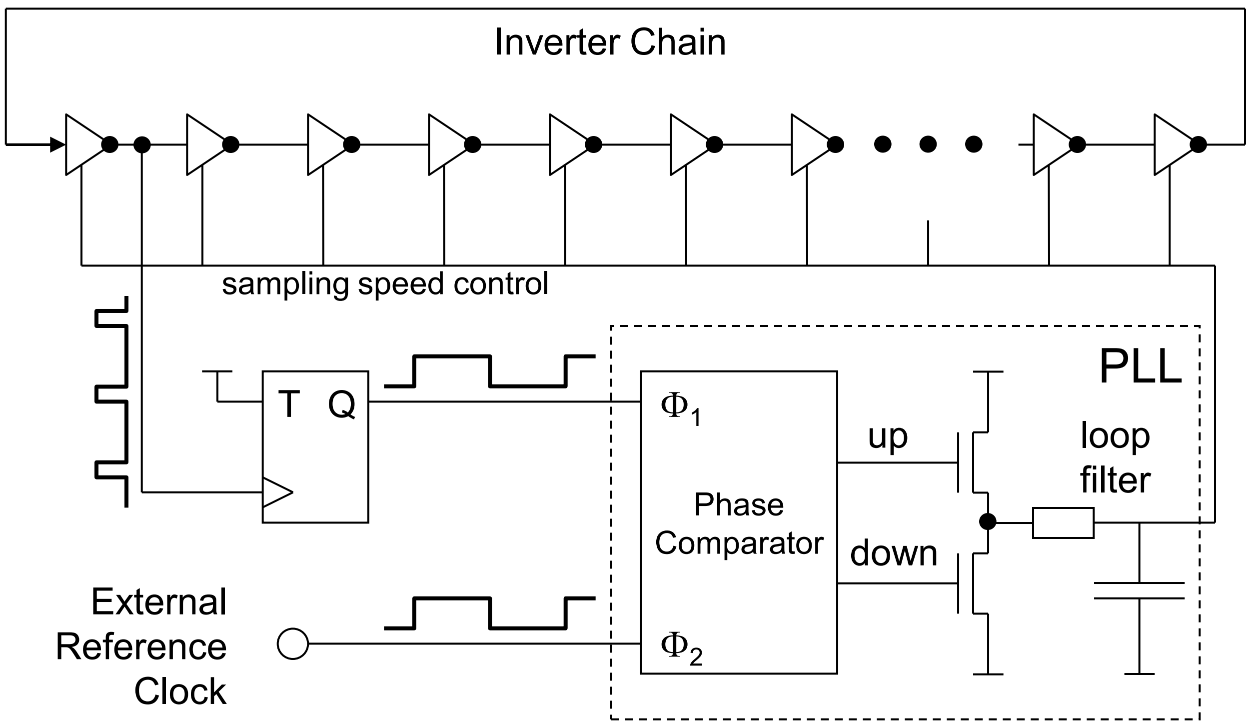
- Cons
  - Unstable timing
    $\rightarrow$ PLL
  - Nonlinear timing
    $\rightarrow$ calibrate
  - Limited sampling depth
    $\rightarrow$ maximize number of cells
  - No continuous acquisition
    $\rightarrow$ reduce readout speed



- Pros
  - High speed (5 GHz) high resolution (12 bit resol.)
  - High channel density (9 channels on 5x5 mm^2)
  - Low power (10-40 mW / channel)
  - Low cost (~ 10€ / channel)

Phase Locked Loop

- On-chip PLL locks sampling frequency to external reference clock
- Good stability over wide temperature and V_{dd} range
- Residual jitter ~3 – 30 ps depending on chain length



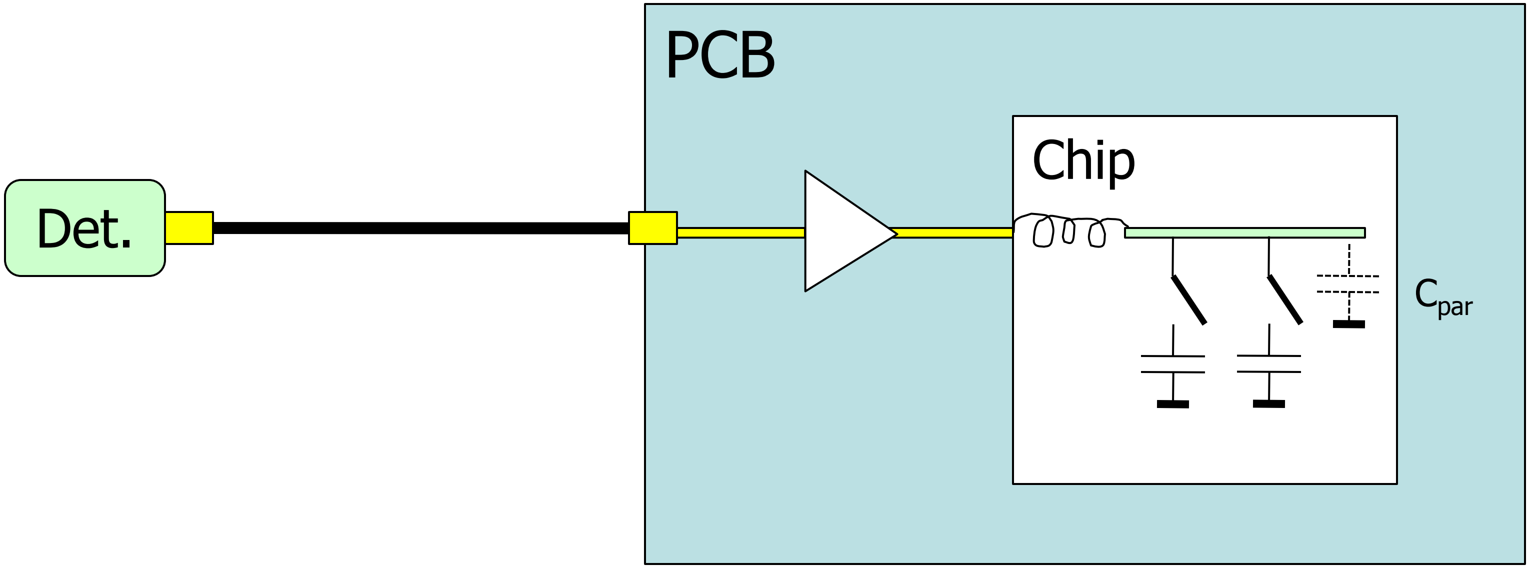
Limits on analog bandwidth

- External sources
  - Detector
  - Cable
  - Connectors
  - PCB
  - Preamplifier
- Internal sources
  - Bond wire
  - Input bus
  - Write switch
  - Storage cap

Bond wire, Input bus → Low pass filter

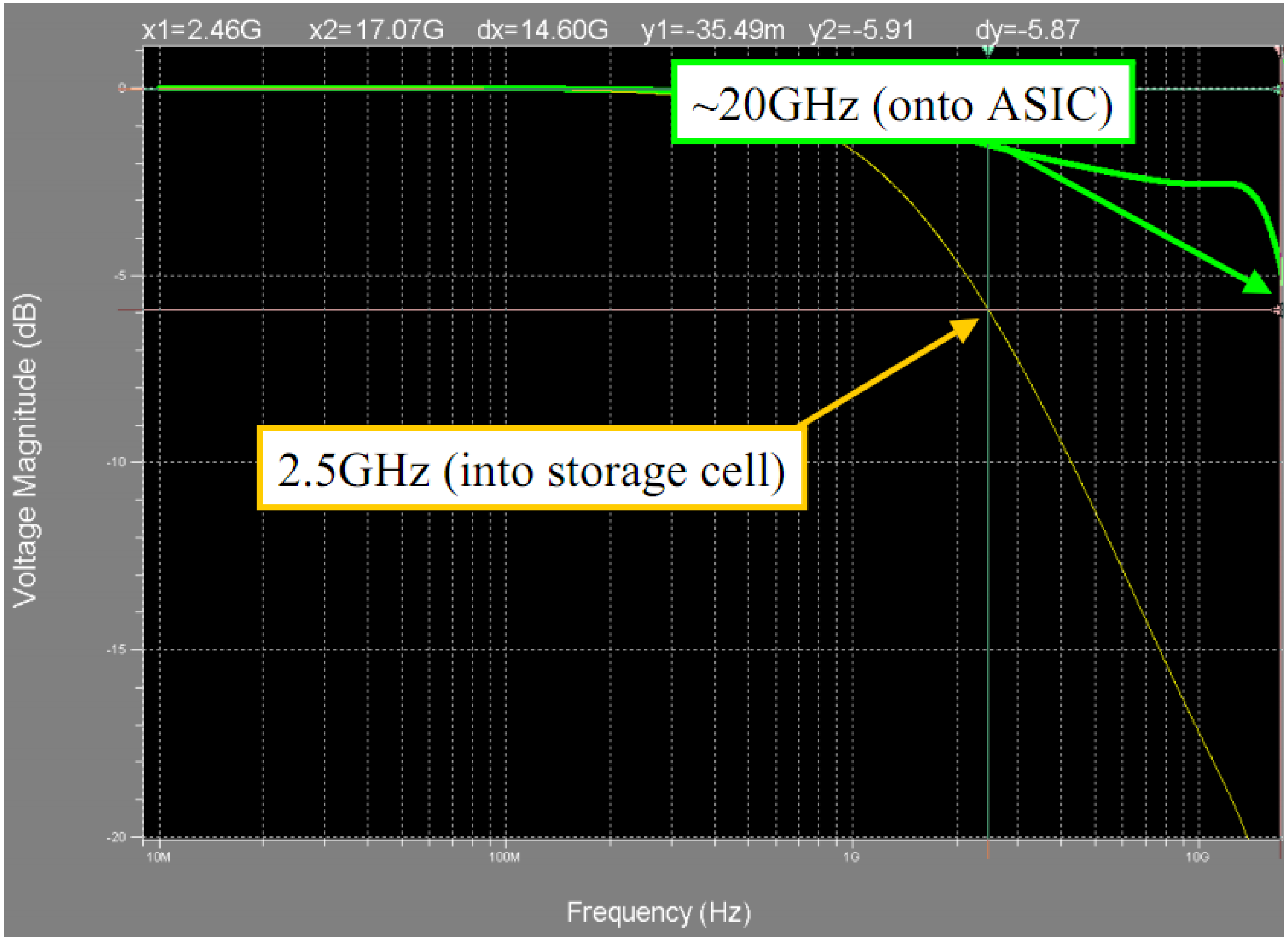
Write switch, Storage cap → Low pass filter

$$f_{3\,db} = \frac{1}{2\pi RC}$$



Bandwidth STURM2 (32 sampling cells)

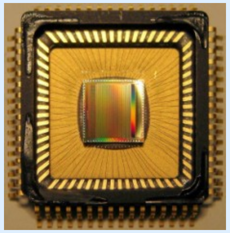
Bump-bonding (optimized) input coupling

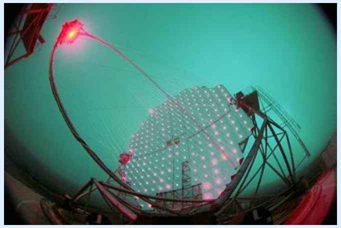


G. Varner, Dec. 2009

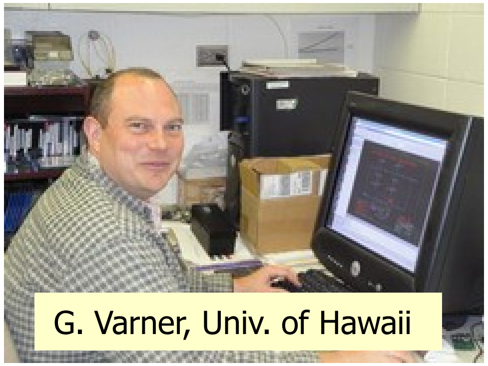
Part 2

- Overview of Chips and Applications





Switched Capacitor Arrays for Particle Physics

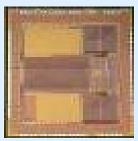


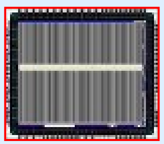
G. Varner, Univ. of Hawaii

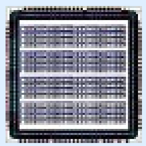
E. Delagnes
D. Breton
CEA Saclay

H. Frisch et al., Univ. Chicago

STRAW3 | LABRADOR3 | TARGET



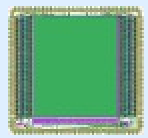




- Many chips for different projects (Belle, Anita, IceCube …)
- Bufferend and unbuffered
- Deep arrays (up to 64k)
- Wilkinson ADC on chip

www.phys.hawaii.edu/~idlab/

AFTER | SAM | MATACQ



- Buffered (f_{3db}~300 MHz)
- Low noise (~12 bits)
- Short PLL → good timing

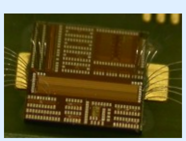
matacq.free.fr

PSEC1 - PSEC4

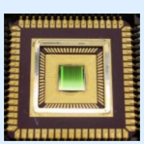
- Goal: Measure 1 ps (!)
- 130 nm IBM
- 18 GSPS
- 256 sampling cells
- Influenced by G. Varner
- Wilkonson ADC on chip

psec.uchicago.edu

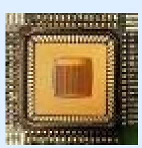
DRS1 | DRS2 | DRS3 | DRS4



2002



2004



2007

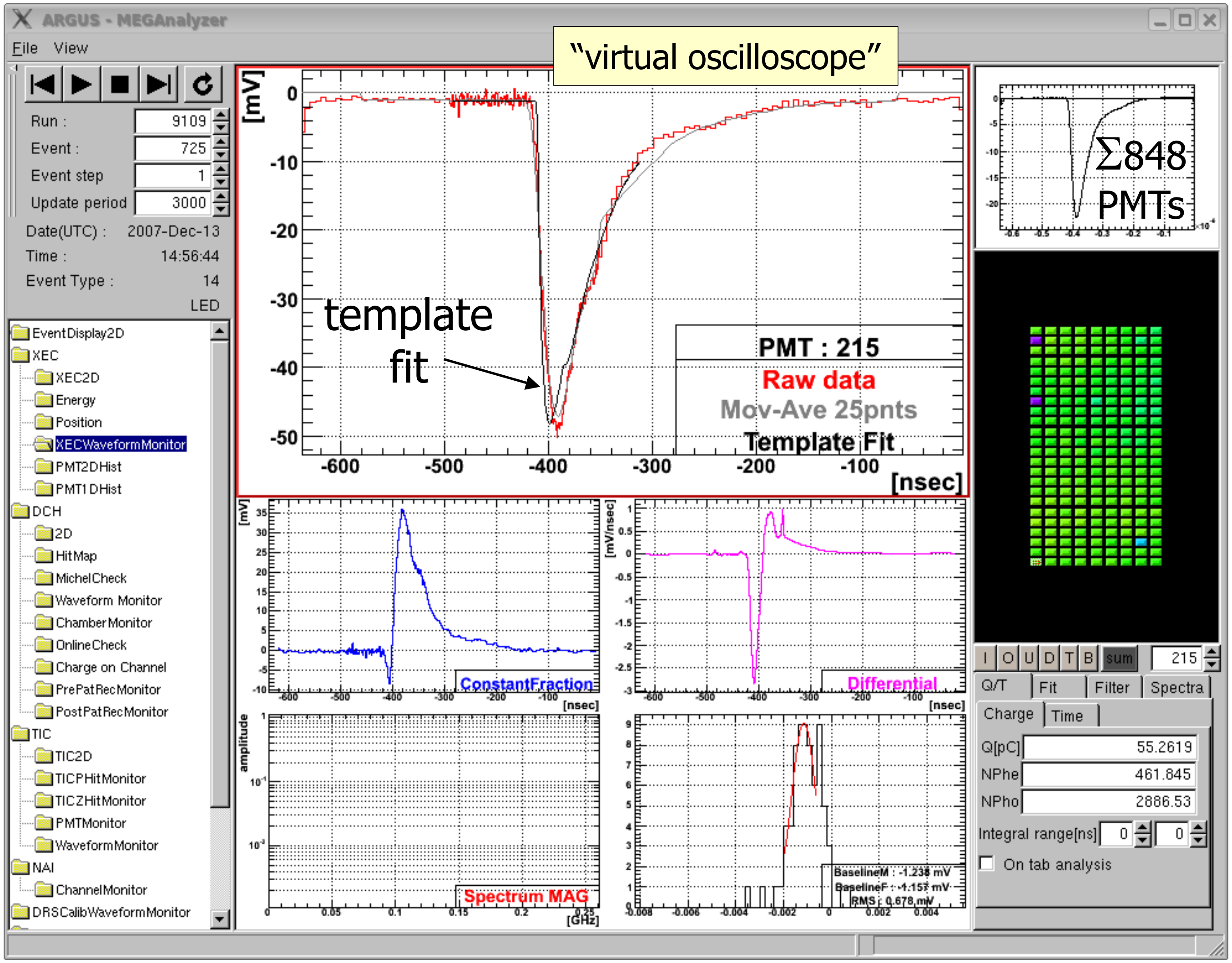
2008

- Universal chip for many applications
- 8+1 channels 1024 sampling cells
- 5 GSPS, 950 MHz analog BW
- 1 μs readout time for short pulses

SR
R. Dinapoli
PSI, Switzerland

drs.web.psi.ch

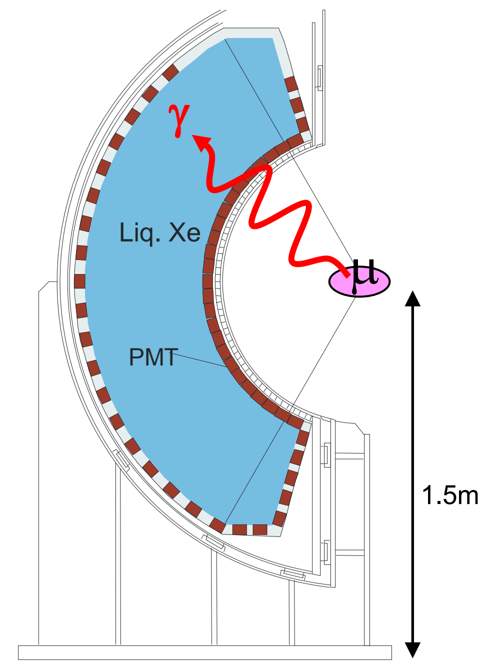
MEG On-line waveform display



$\mu^+ \rightarrow e^+\gamma$

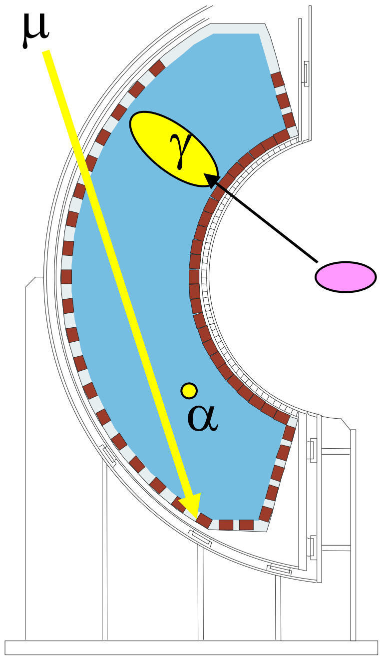
At 10^{-13} level

3000 Channels Digitized with DRS4 chips at 1.6 GSPS

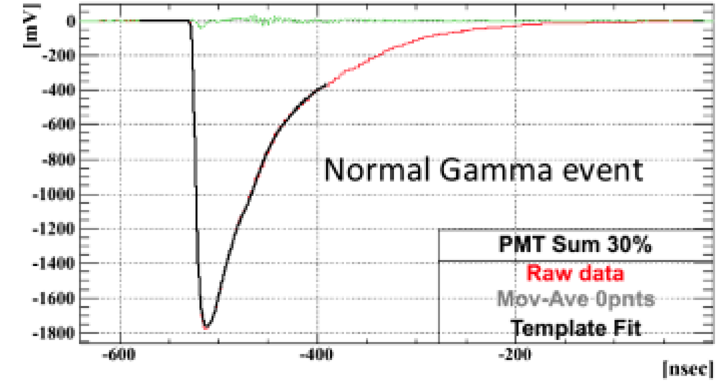


Drawback: 600 TB data/year

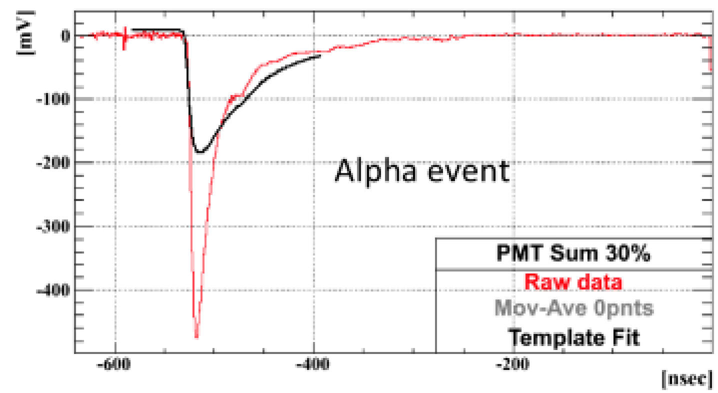
Pulse shape discrimination



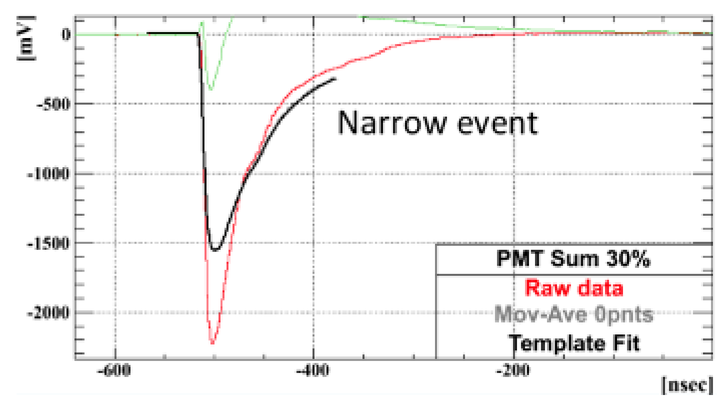
γ



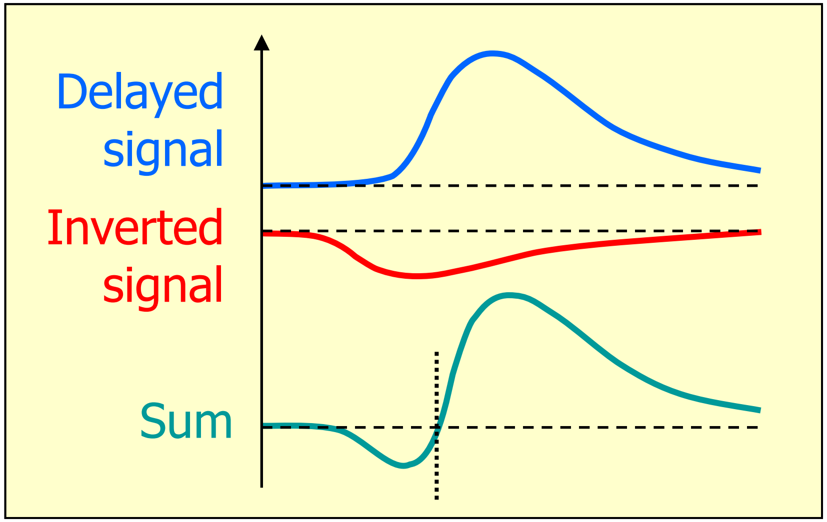
α

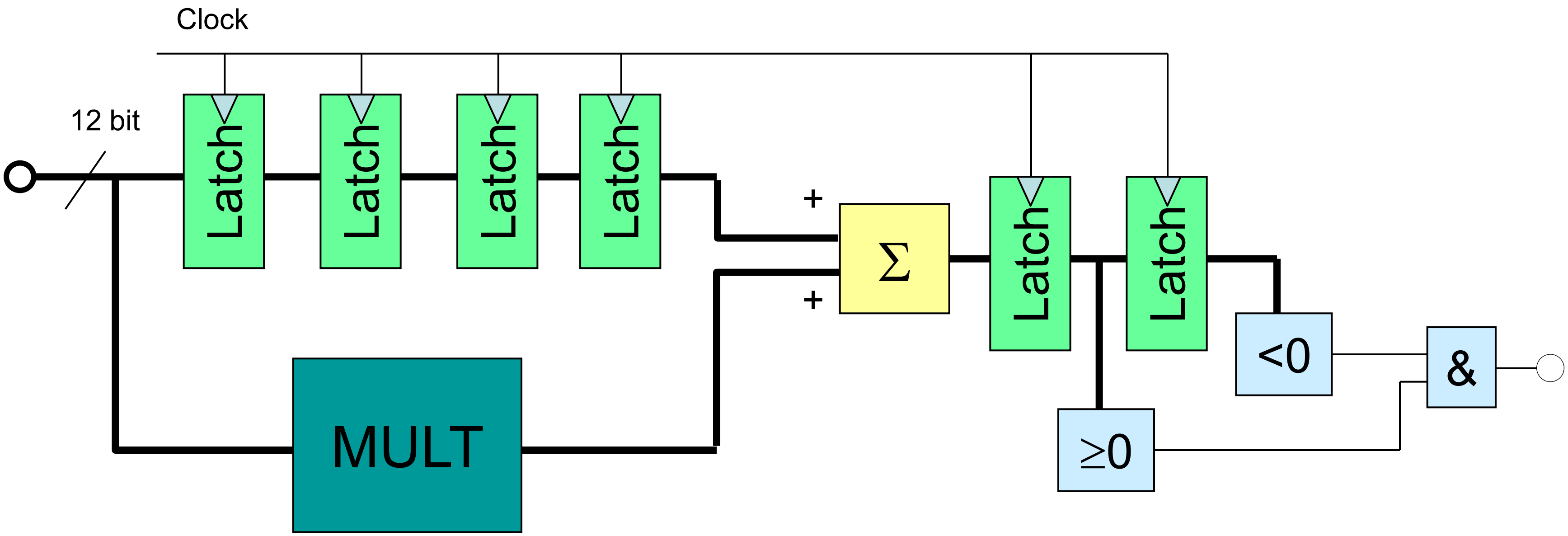


μ

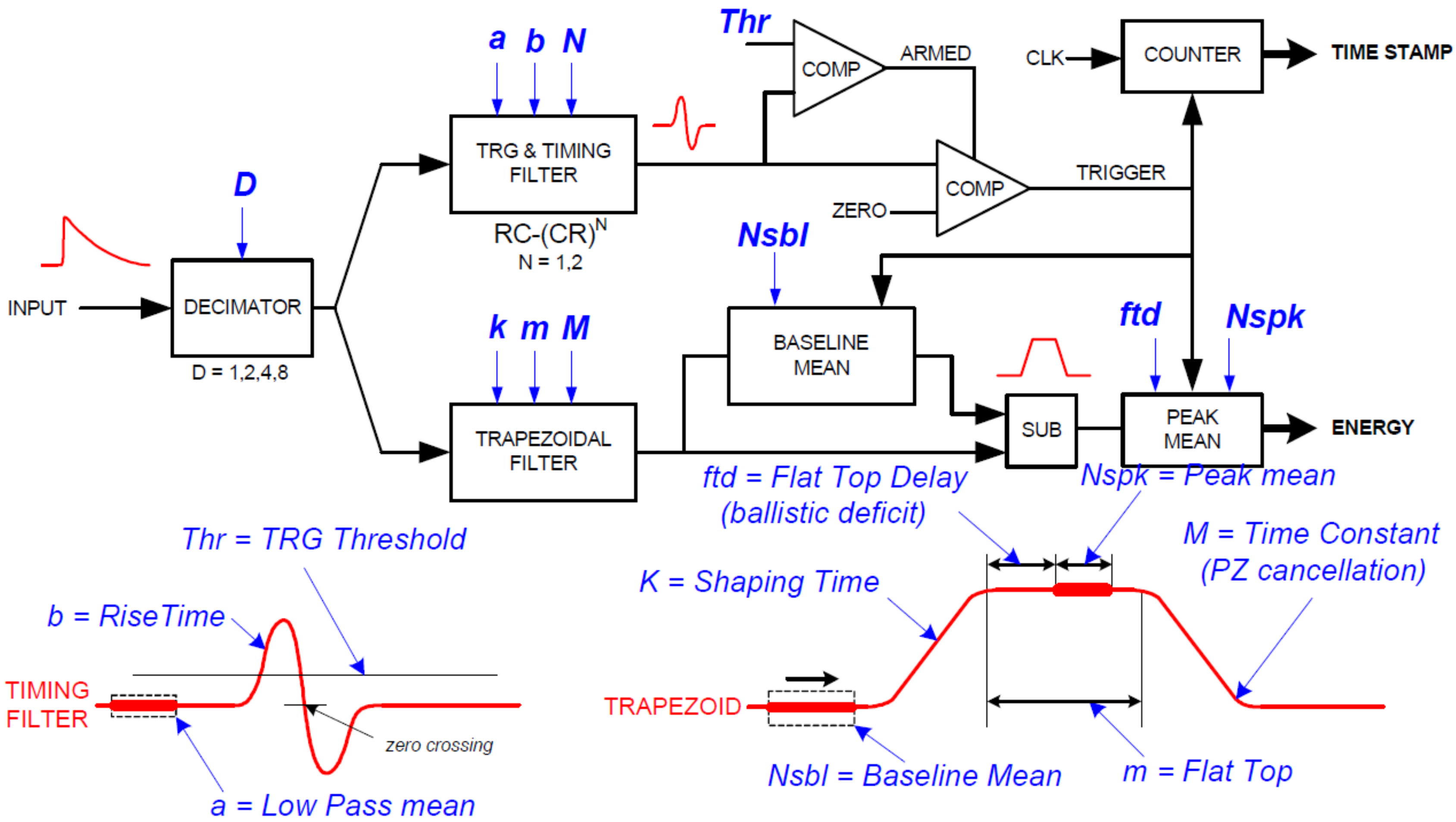


Constant Fraction Discr.





Digital Pulse Processing (DPP)



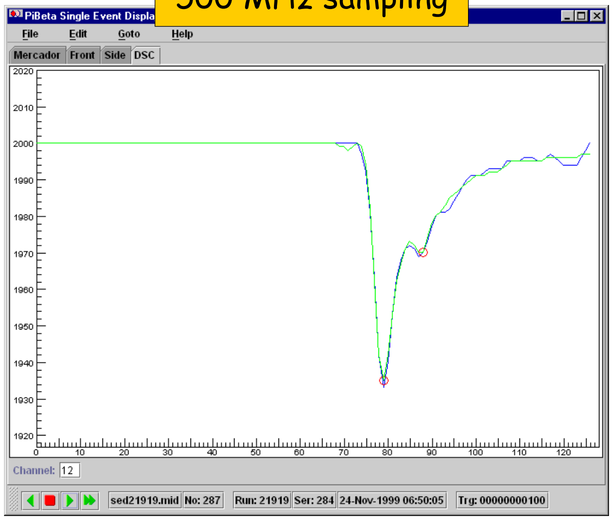
C. Tintori (CAEN)

V. Jordanov *et al.*, NIM **A353**, 261 (1994)

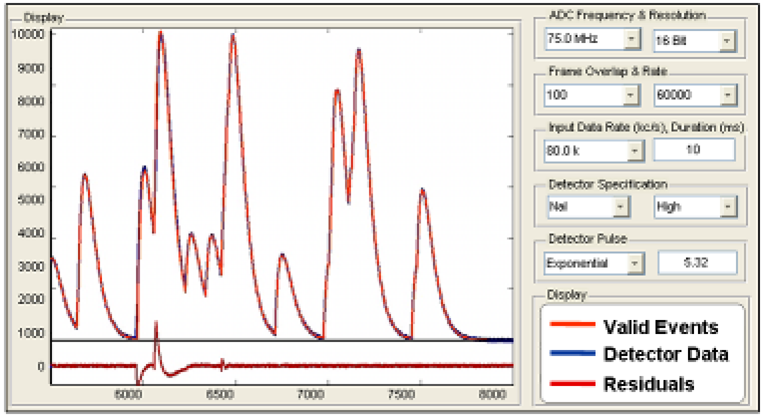
Template Fit

- Determine "standard" PMT pulse by averaging over many events → "Template"
  - Find hit in waveform
  - Shift ("TDC") and scale ("ADC") template to hit
  - Minimize χ^2
  - Compare fit with waveform
  - Repeat if above threshold
- Store ADC & TDC values

πβ Experiment
500 MHz sampling



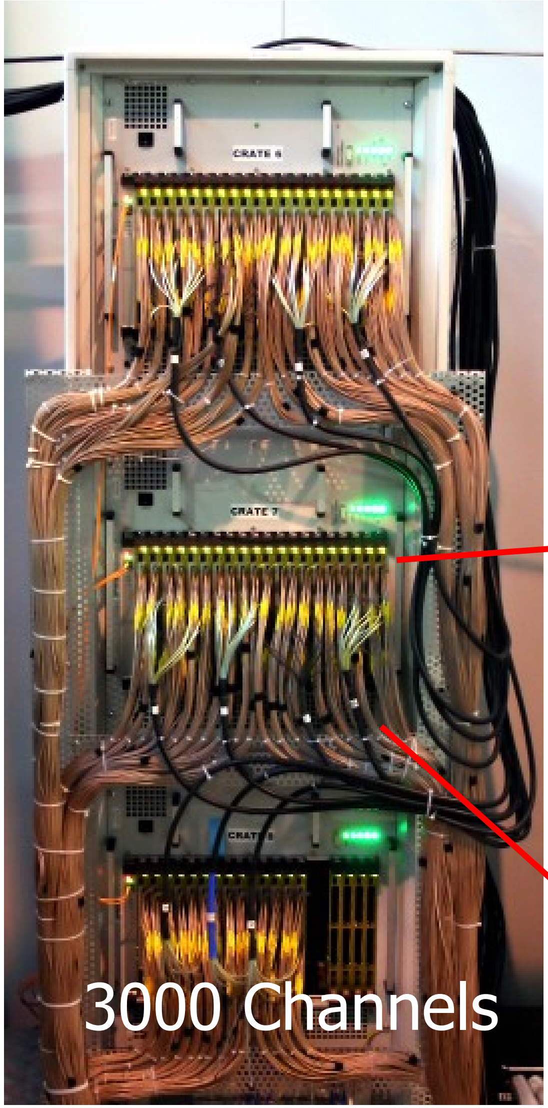
• At 1,000 kc/s less than 10% of events cannot be decoded.

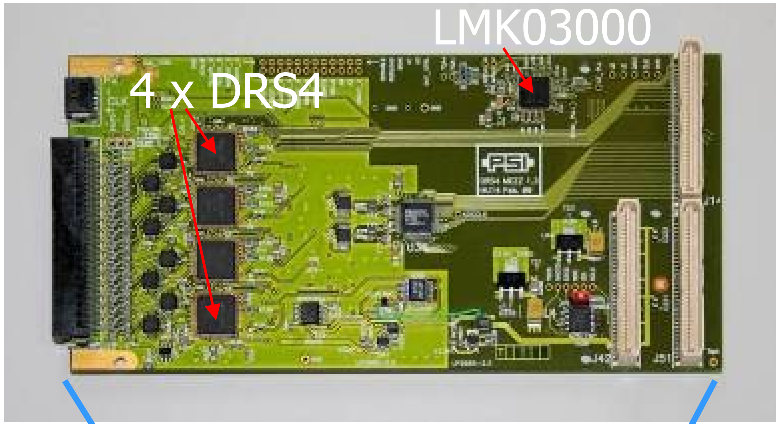


14 bit
60 MHz

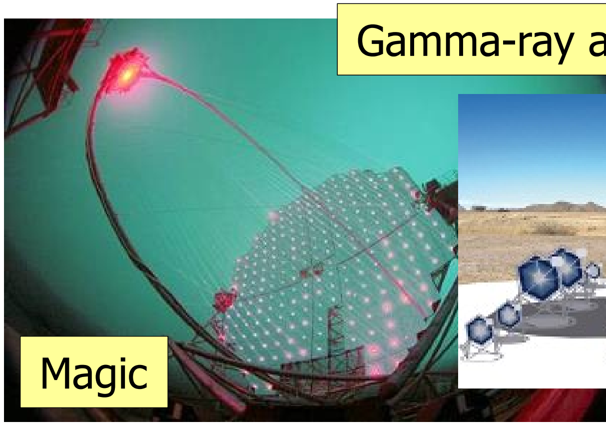
www.southerninnovation.com

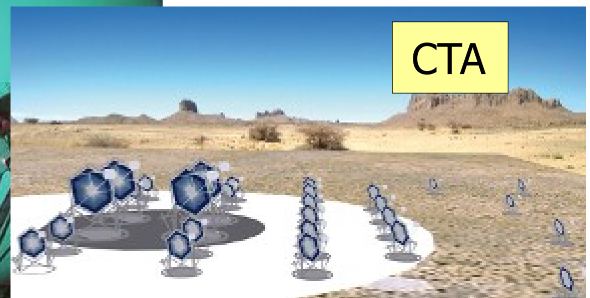
DRS4 @ MEG

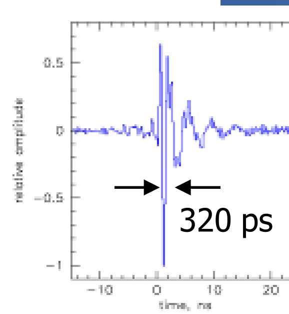


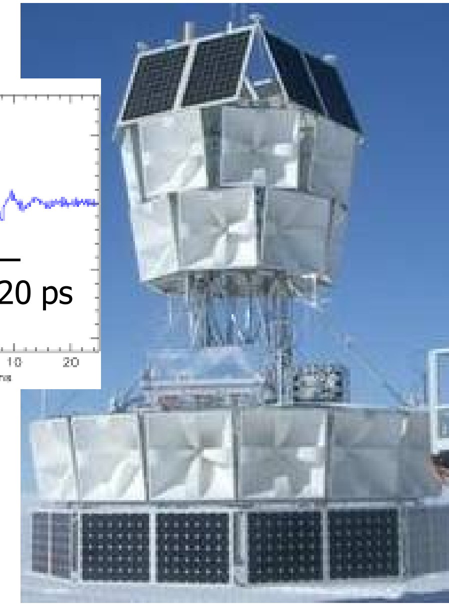


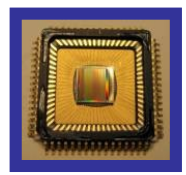
Applications

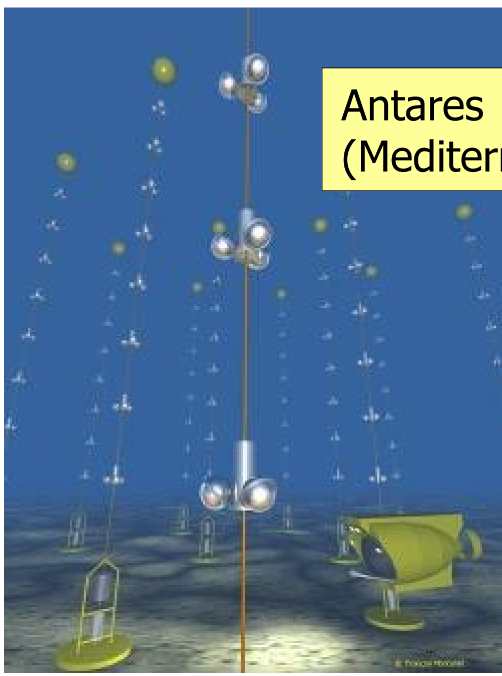


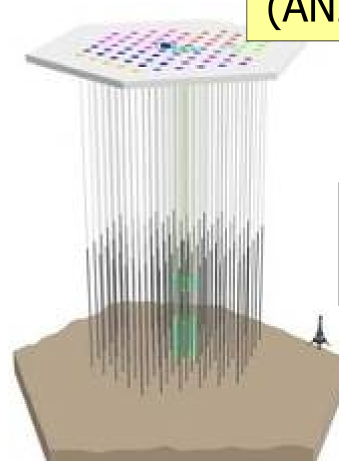




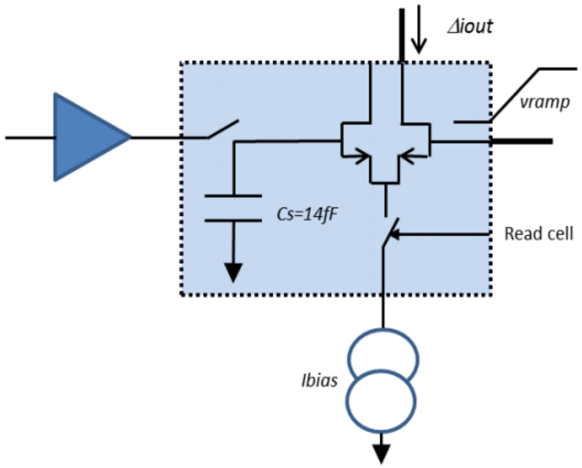


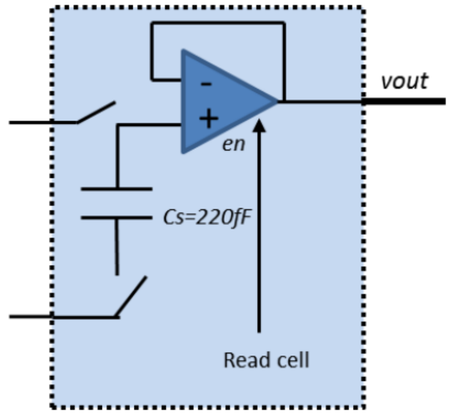


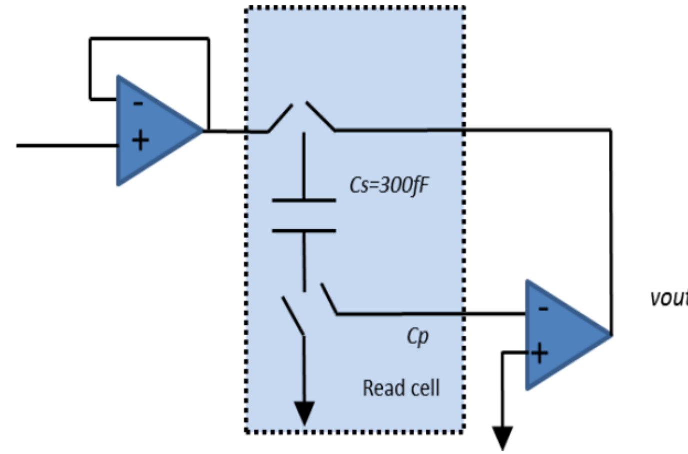




Different Sampling Cells







BLAB (G. Varner)

- Buffered input
- Wilkinson readout
- Very small cell

DRS4 (SR+RD)

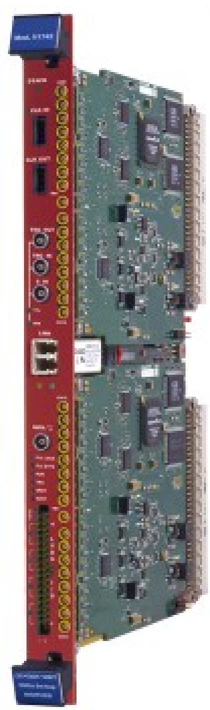
- Passive differential input
- Closed loop OPAMP
- One OPAMP/cell

SAM (E. Delagnes)

- Buffered input
- Feedback OPAMP
- One OPAMP/ 32 cells

Things you can buy

- DRS4 chip (PSI)
- 32+2 channels
- 12 bit 5 GSPS
- > 500 MHz analog BW
- 1024 sample points/chn.
- 110 μs dead time



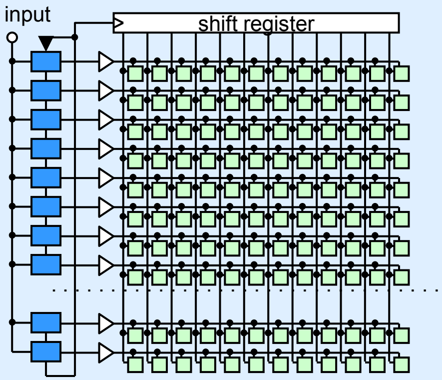
- MATACQ chip (CEA/IN2P3)
- 4 channels
- 14 bit 2 GSPS
- 300 MHz analog BW
- 2520 sample points/chn.
- 650 μs dead time

- DRS4 Evaluation Board
- 4 channels
- 12 bit 5 GSPS
- 750 MHz analog BW
- 1024 sample points/chn.
- 500 events/sec over USB 2.0

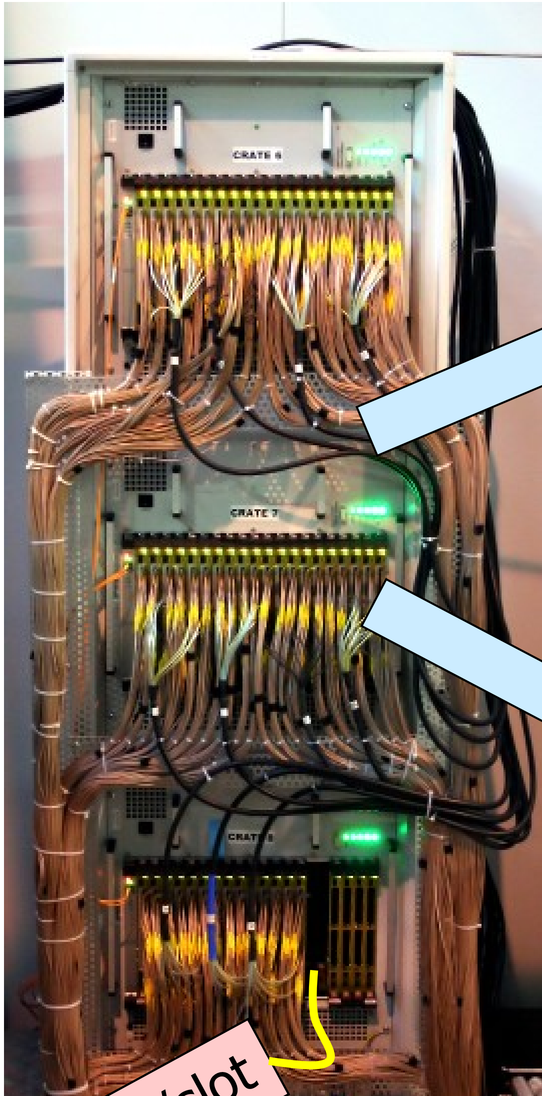
- SAM Chip (CEA/IN2PD)
- 2 channels
- 12 bit 3.2 GSPS
- 300 MHz analog BW
- 256 sample points/chn.
- On-board spectroscopy

Part 3

- Future Design Directions

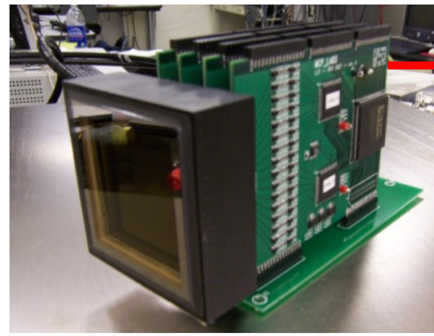


Away from crate-based systems

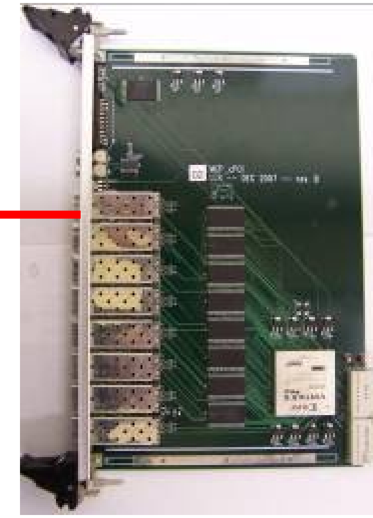


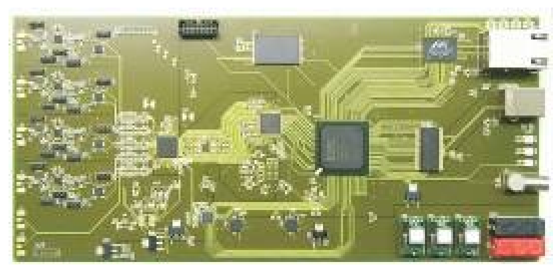
1 k€/slot

G. Varner: BLAB2 readout system for f-DIRC



fiber optics



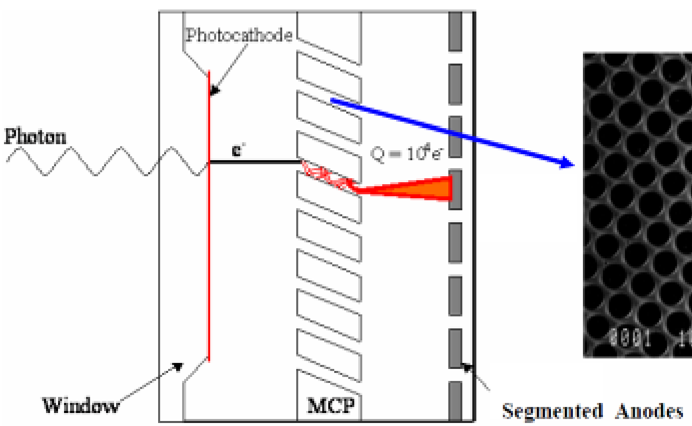


GBit Ethernet

WaveDREAM Board (H. Friedrich, ETH/PSI)

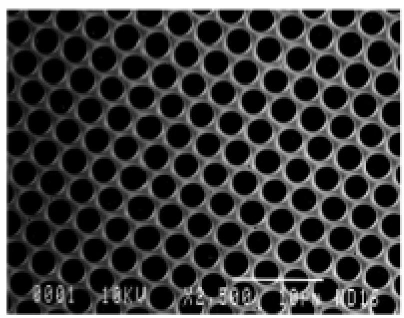
Faster sampling

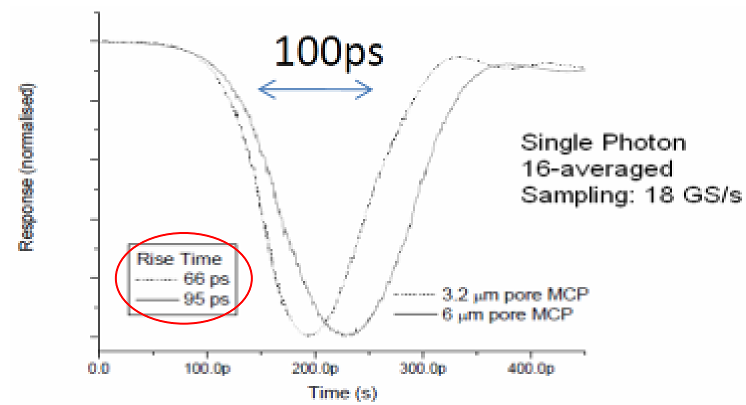
- Nyquist-Shannon: **Sampling rate** must be 2x the highest frequency coming from detector
- **Analog Bandwidth** must match signal from detector
- Fastest pulses coming from Micro-Channel-Plate PMTs:
  70 ps rise time → **4-5 GHz BW** → **10 GSPS**
- Current limit: ~1 GHz with reasonable sampling depth



J. Vallerga

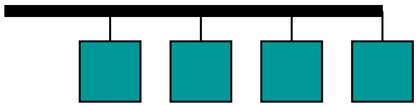
3μm pores

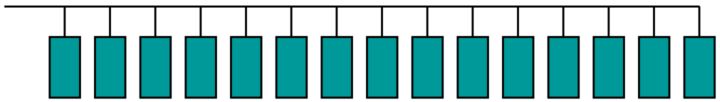




J. Milnes, J. Howoth, Photek

Next Generation SCA





Short sampling depth ⟷ Deep sampling depth

- Low parasitic in… capacitance
- Wide input bus
- Low R_{on} write switches

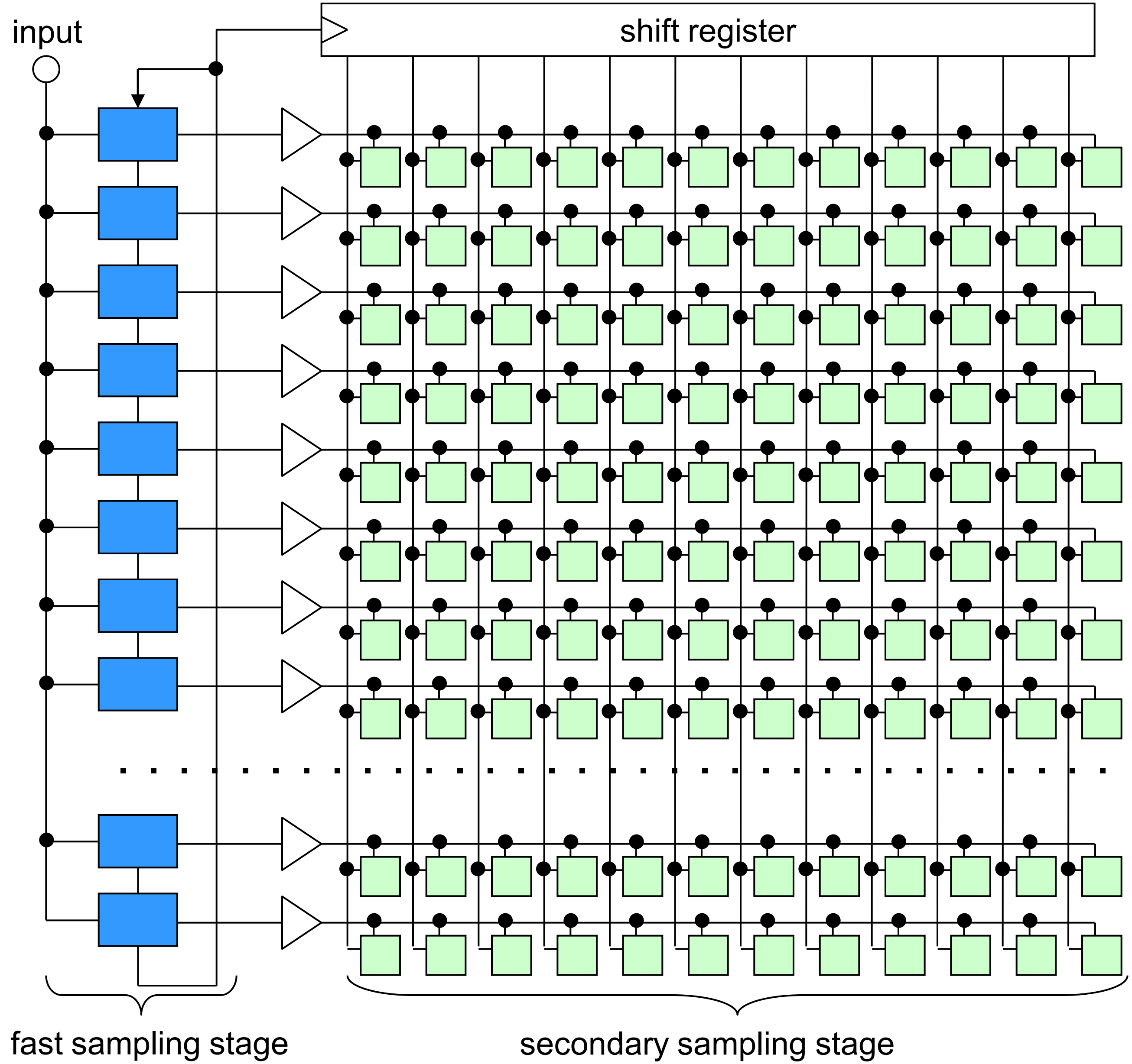
$\rightarrow$ High bandwidth

- …long waveforms
- …modate long trigger delay
- Faster sampling speed for a given trigger latency

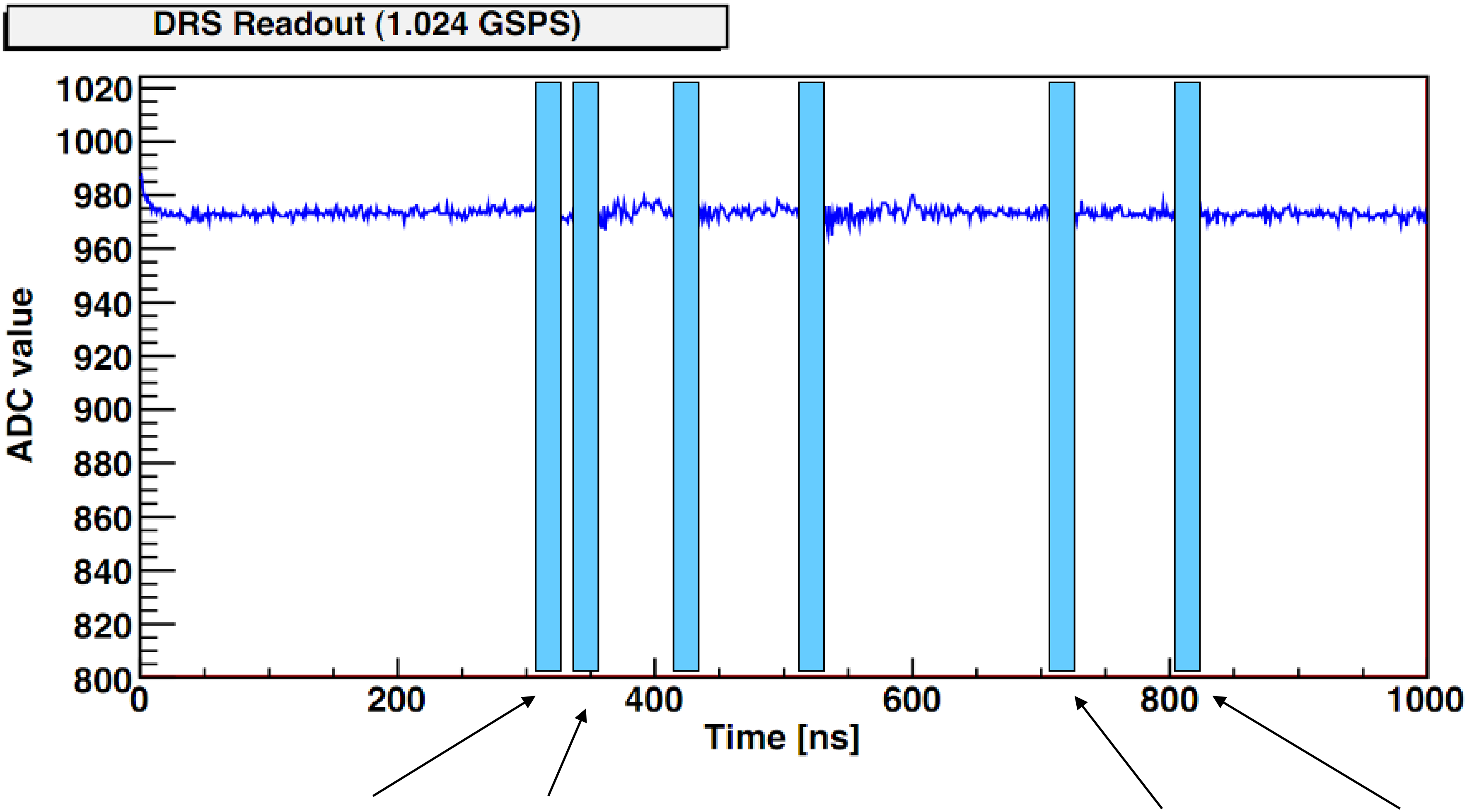
How to combine best of both worlds?

Cascaded Switched Capacitor Arrays

- 32 fast sampling cells (10 GSPS)
  → 1 ps resolution
- 100 ps sample time, 3.1 ns hold time
- Hold time long enough to transfer voltage to secondary sampling stage with moderately fast buffer (300 MHz)
- Shift register gets clocked by inverter chain from fast sampling stage



Typical Waveform



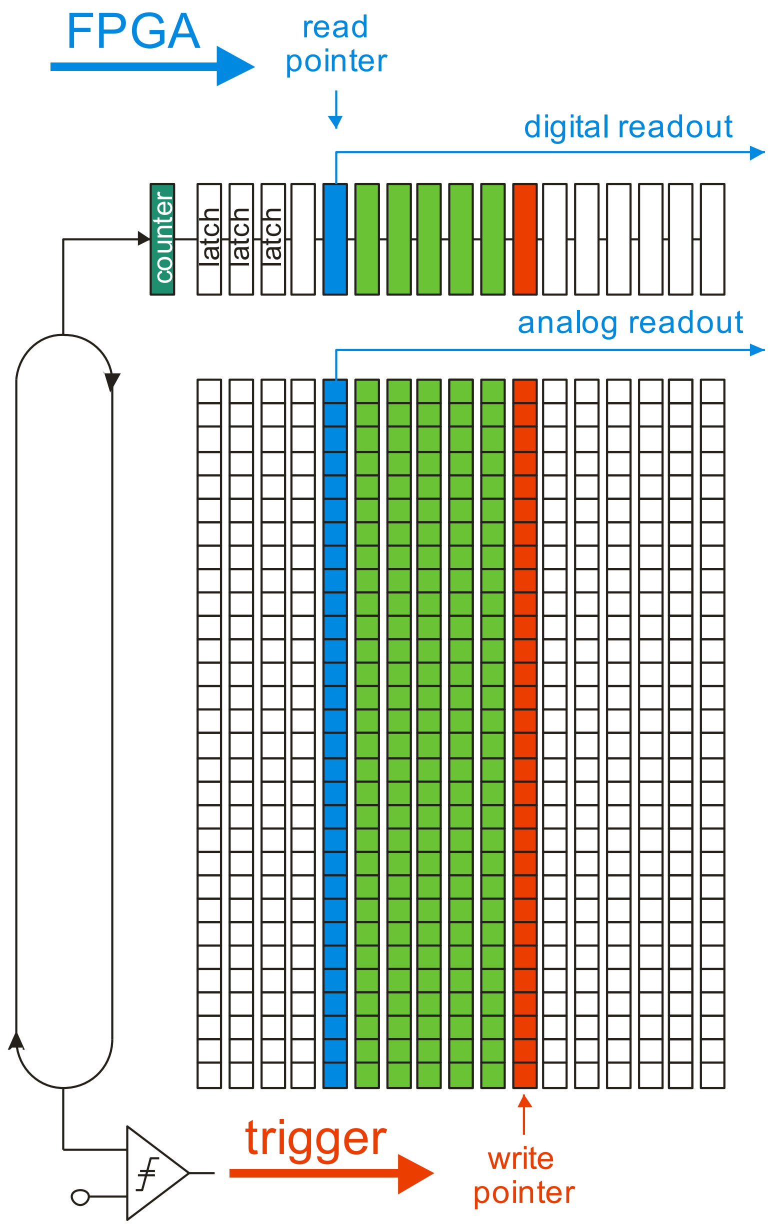
Only short segments of waveform are of interest

Dead-time free acquisition

Self-trigger writing of 128 short
   32-bin segments (4096 bins total)
   Storage of 128 events
Simultaneous writing and readin… of
   segments
Quasi dead ti…
Data …
- … ontinuously
- A… tells FPGA when there is new data
- Possibility to skip segments → analog buffer for HEP experiments (LHC, ILC)

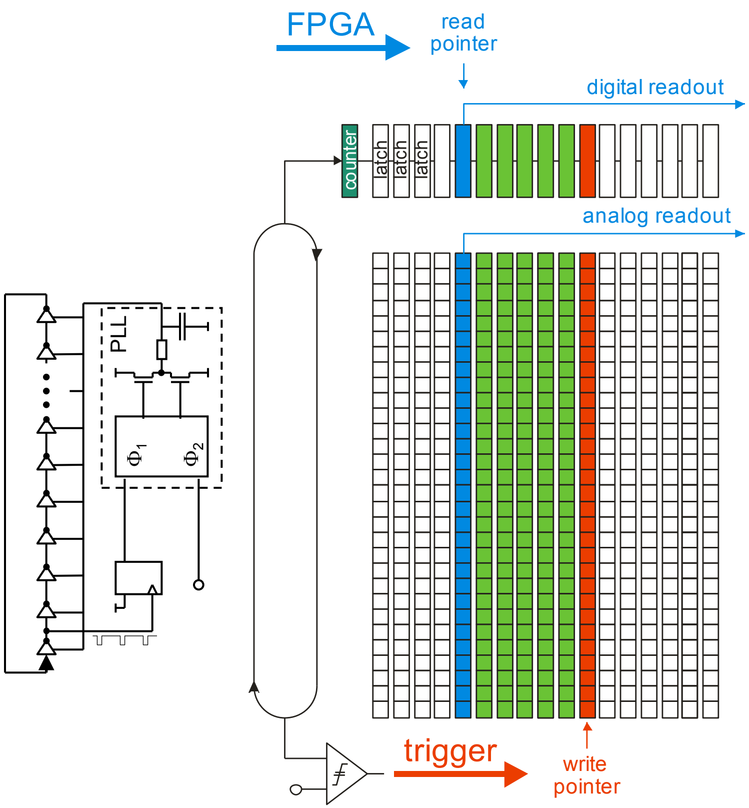
Coarse timing from
   300 MHz counter
Fine timing by waveform
   digitizing and analysis in FPGA
20 * 20 ns = 0.4 μs readout time
   → 2 MHz sustained event rate (ToF-PET)
Attractive replacement for CFD+TDC

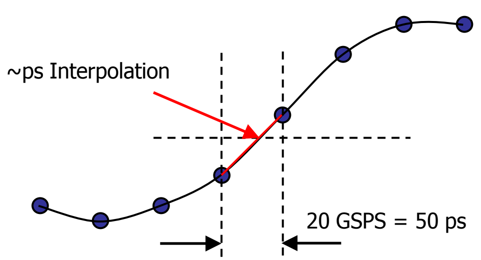
DRS5
planned for 2013



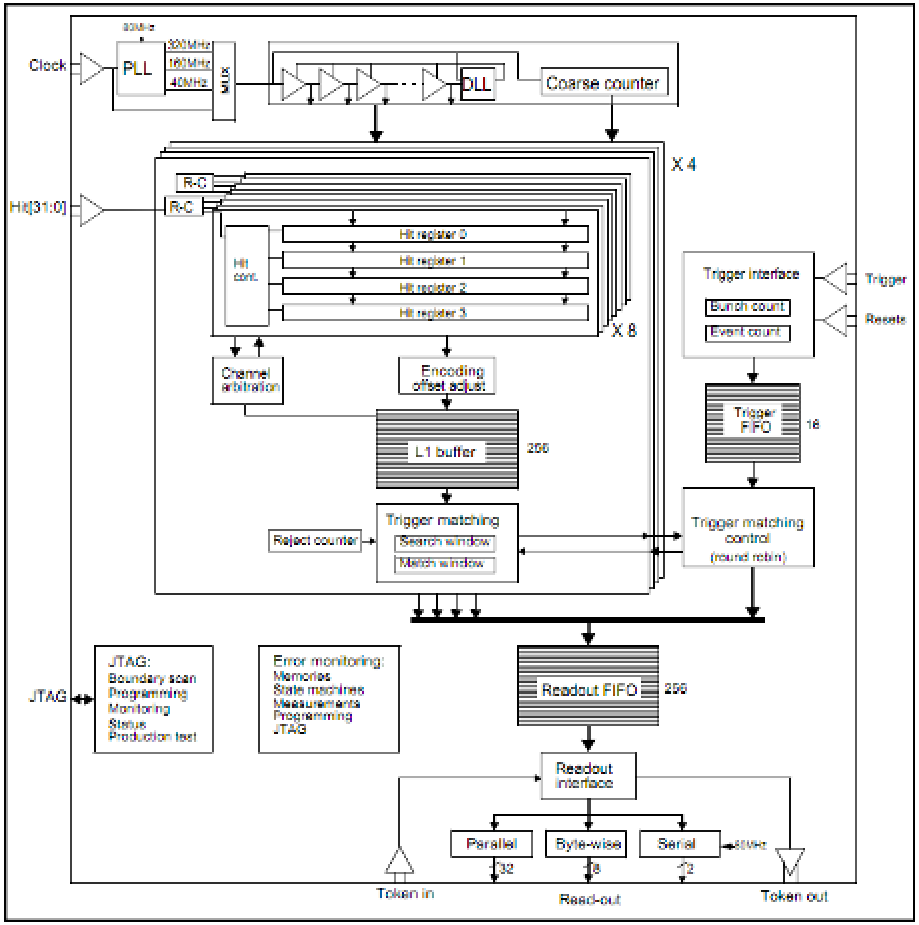
SCA a better TDC?

DRS5 (PSI)

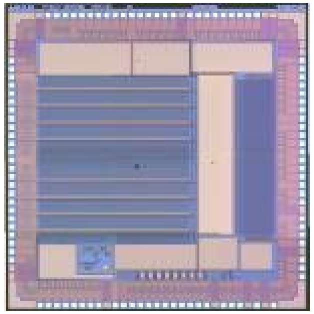


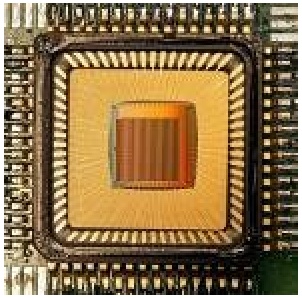


HPTDC (CERN)

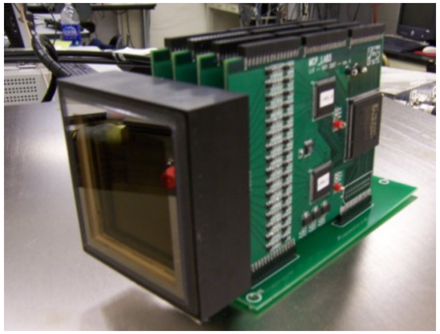


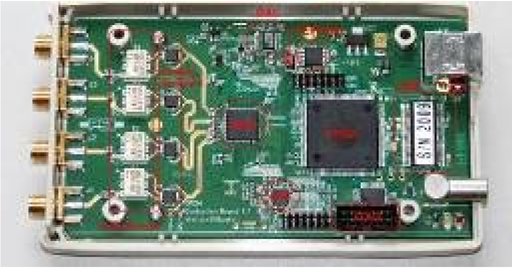
Conclusions

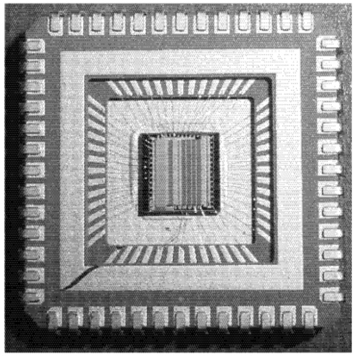




- SCA technology offers tremendous opportunities
- Several chips and boards are on the market for evaluation
- New series of chips on the horizon might change front-end electronics significantly





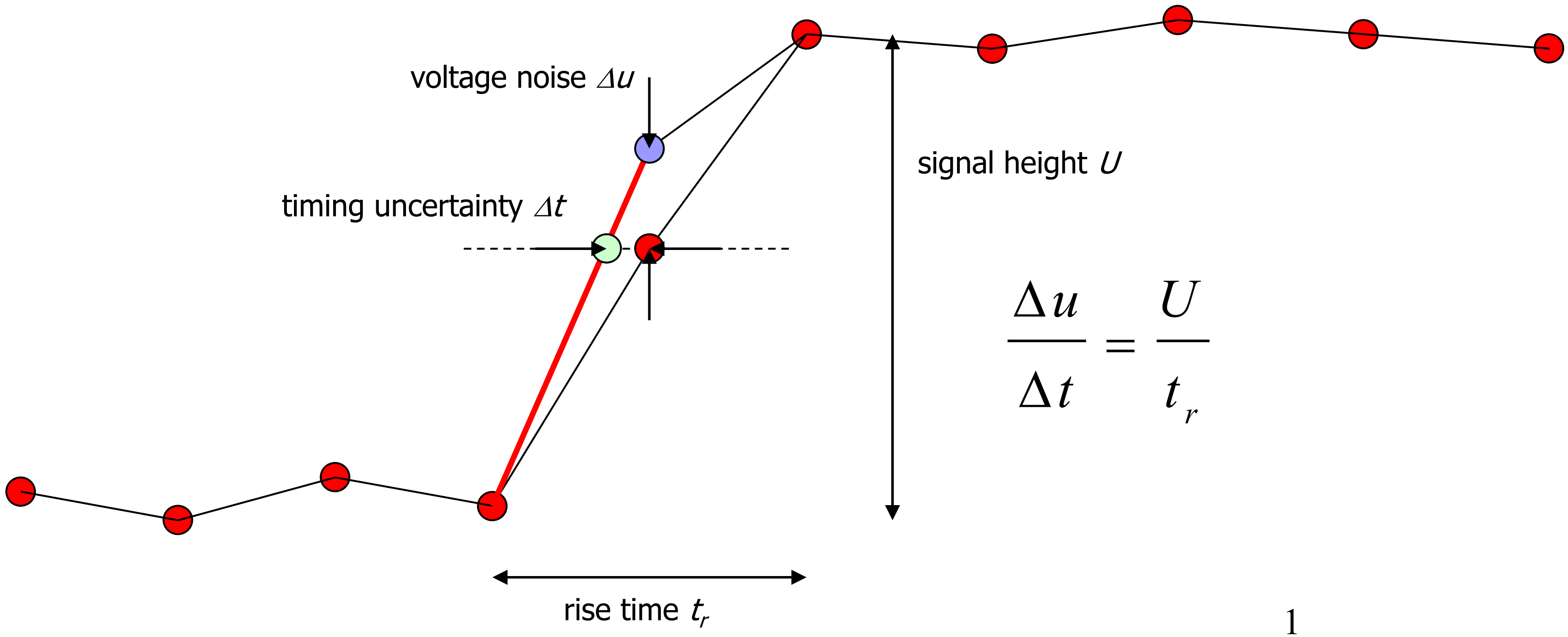


End of excursion

Enjoy the “real” excursion

Taken with www.photosynth.net

How is timing resolution affected?



$$\frac{\Delta u}{\Delta t} = \frac{U}{t_r}$$

$$t_r \approx \frac{1}{3 f_{3dB}}$$

$$\Delta t = \frac{\Delta u}{U} \cdot t_r = \frac{\Delta u}{U\sqrt{n}} \cdot t_r = \frac{\Delta u}{U} \cdot \frac{t_r}{\sqrt{t_r \cdot f_s}} = \frac{\Delta u}{U} \cdot \frac{\sqrt{t_r}}{\sqrt{f_s}} = \frac{\Delta u}{U} \cdot \frac{1}{\sqrt{3 f_s \cdot f_{3dB}}}$$

number of samples on slope

Simplified estimation!

How is timing resolution affected?

$$\Delta t = \frac{\Delta u}{U} \cdot \frac{1}{\sqrt{3 f_s \cdot f_{3dB}}}$$

Assumes zero aperture jitter

	U	Δu	f_s	f_{3db}	Δt
today:	100 mV	1 mV	2 GSPS	300 MHz	~10 ps
optimized SNR:	1 V	1 mV	2 GSPS	300 MHz	1 ps
next generation:	100 mV	1 mV	20 GSPS	3 GHz	0.7 ps
next generation optimized SNR:	1V	1 mV	10 GSPS	3 GHz	0.1 ps

How to achieve this?

includes detector noise
in the frequency region of the rise time
and aperture jitter