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CMOS at 77-300K for the readout of very large LAr TPCs

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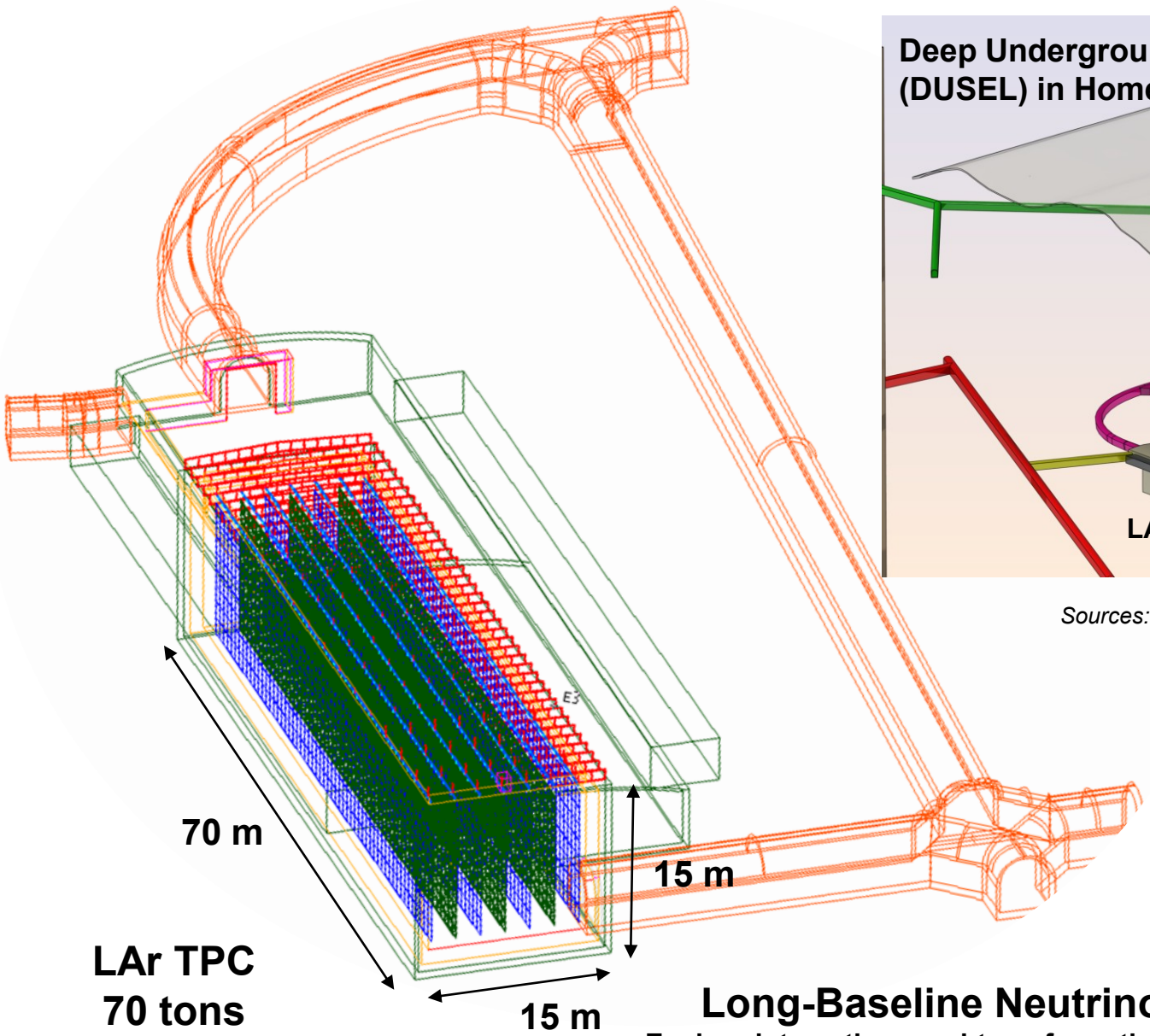
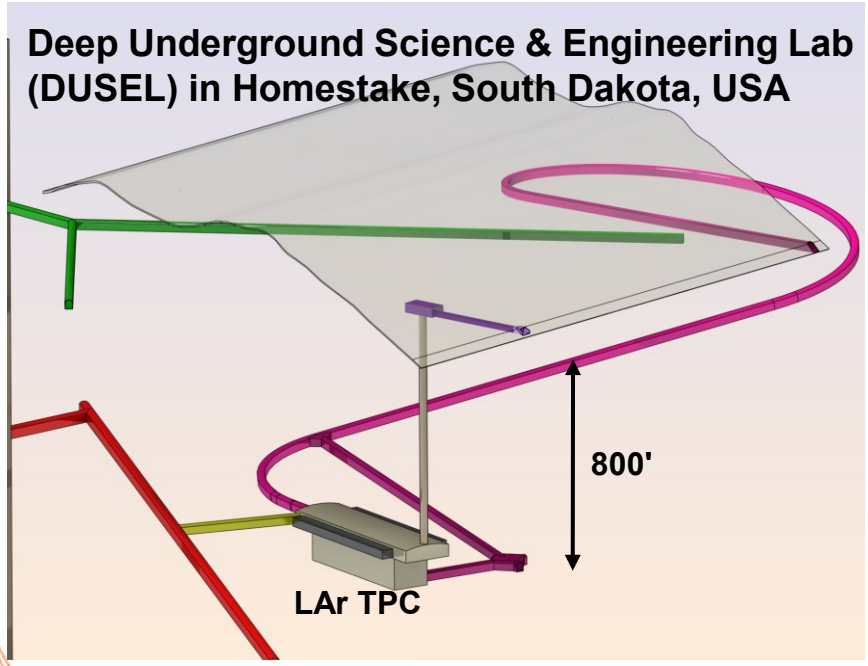
Liquid Argon (LAr) TPC for LBNE at DUSEL



LAr TPC
70 tons

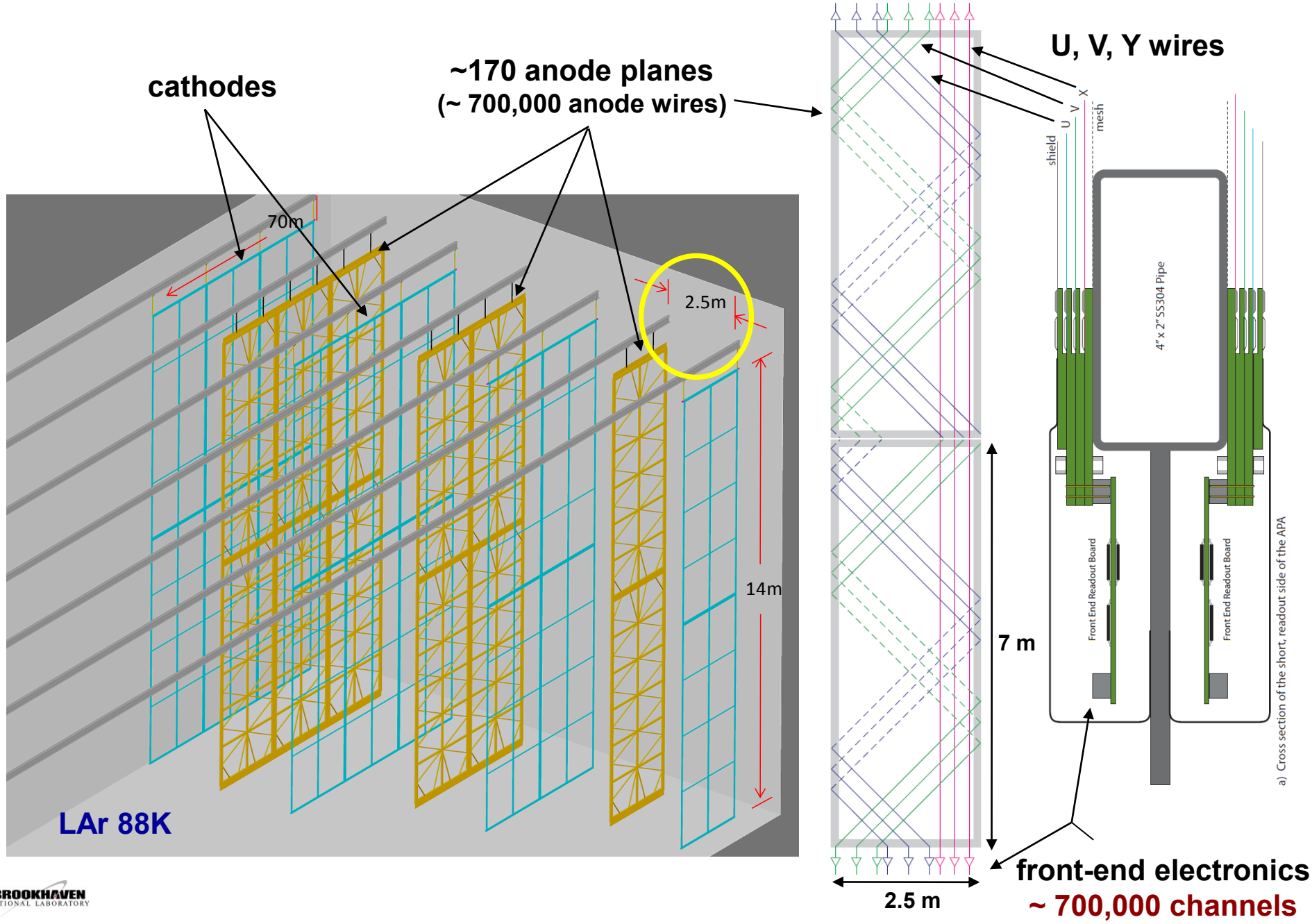


Sources: S. Hentschel & Jacobs Associates

Long-Baseline Neutrino Experiment (LBNE)

Explore interactions and transformations of the world's highest-intensity neutrino beam by sending it from Fermilab more than 1,000 kilometers straight through the Earth to the largest particle detectors ever built.

Liquid Argon (LAr) TPC - Architecture



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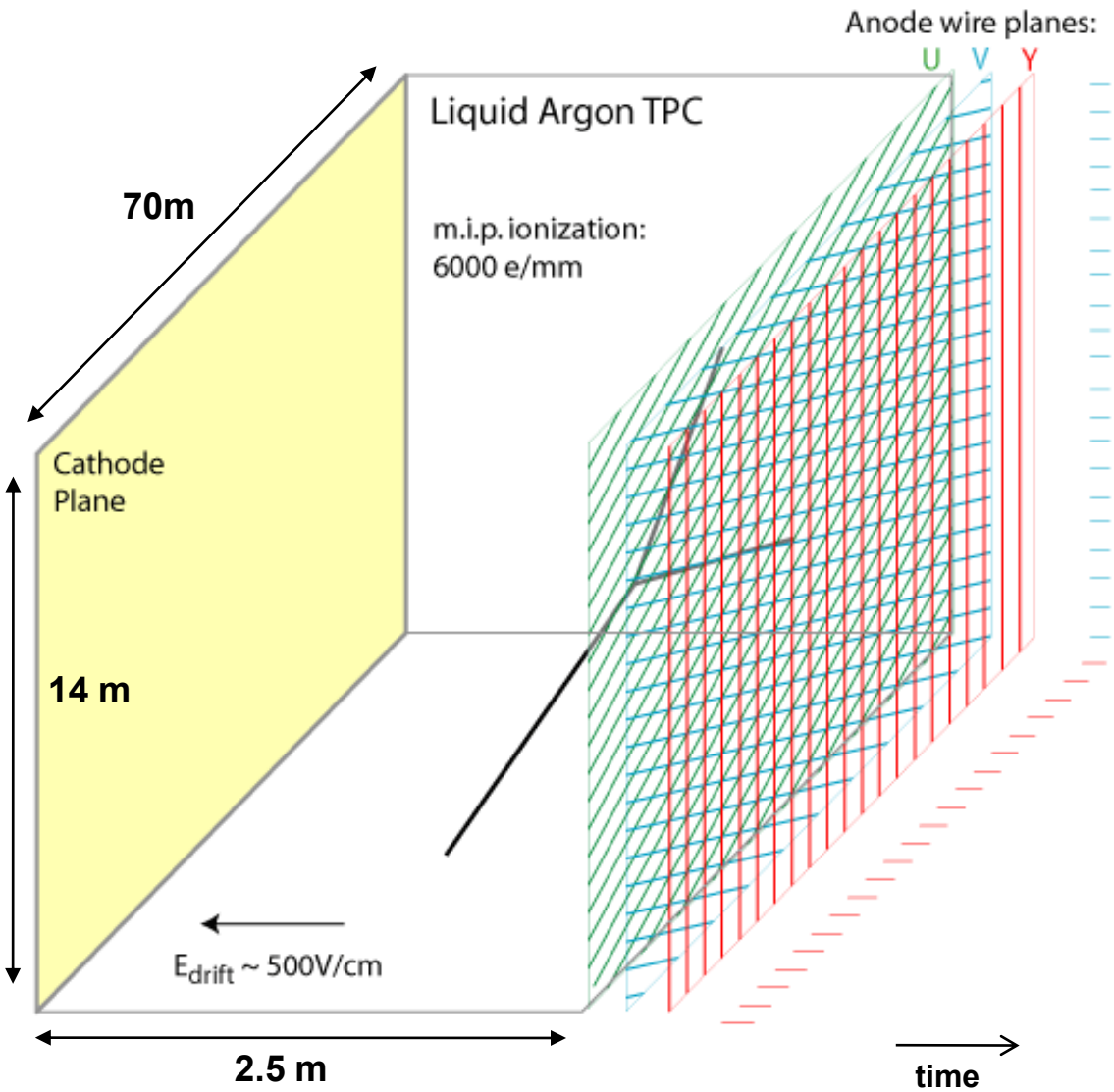
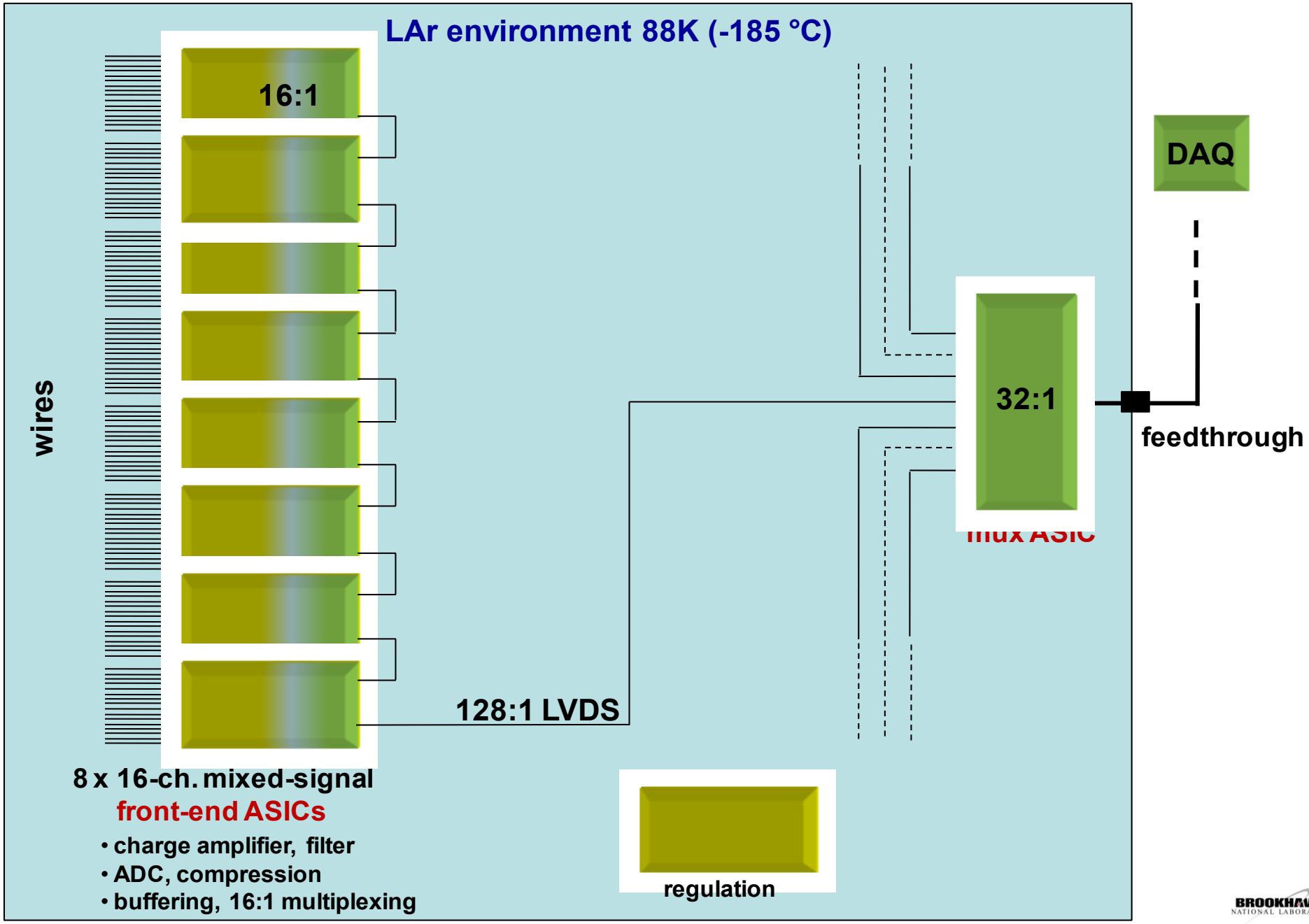
LAr TPC - Operation



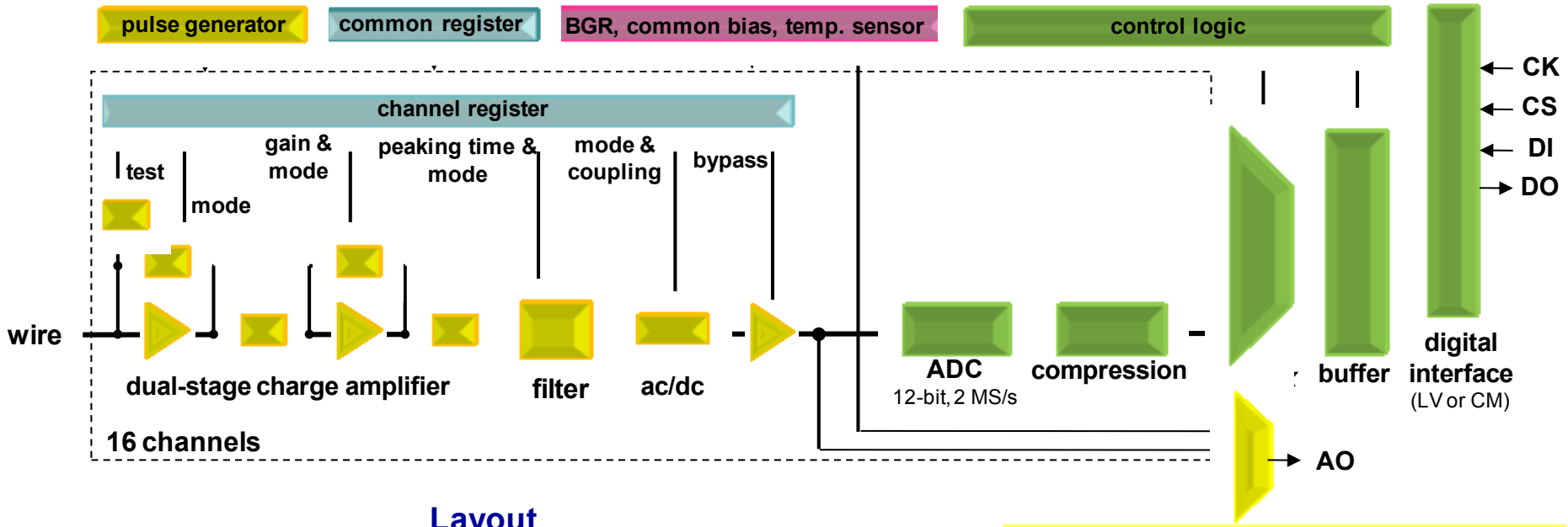
- ~ 700,000 anode wires
  - up to 200 pF
  - collecting (Y)
  - non-collecting (U,V)
- charge amplification
  - range 300 fC
  - ENC < 1,000 e^-
- sample/buffer events
  - ADC 12-bit, 2 MS/s
  - 3,000 deep buffer
- digital multiplexing
  - 4096:1 two stages
  - collab. with FNAL
- power constraint
  - < 10 mW / channel
- operation in LAr
  - 88K, > 20 years

LAr TPC - Cold Electronics

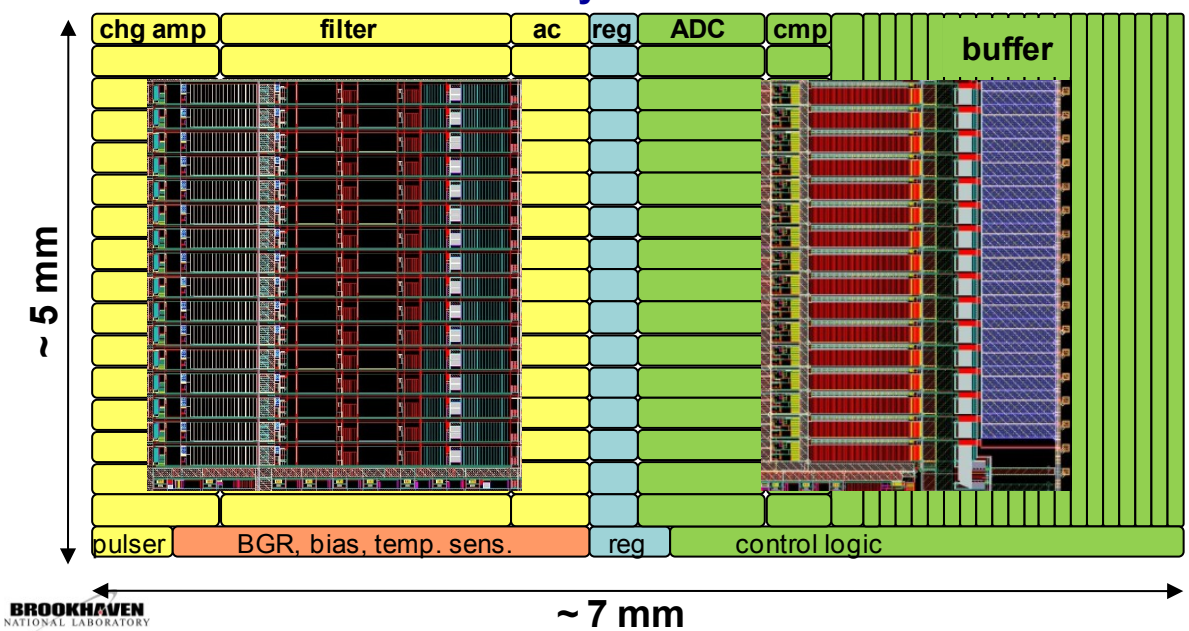


Front-End ASIC

Block Diagram



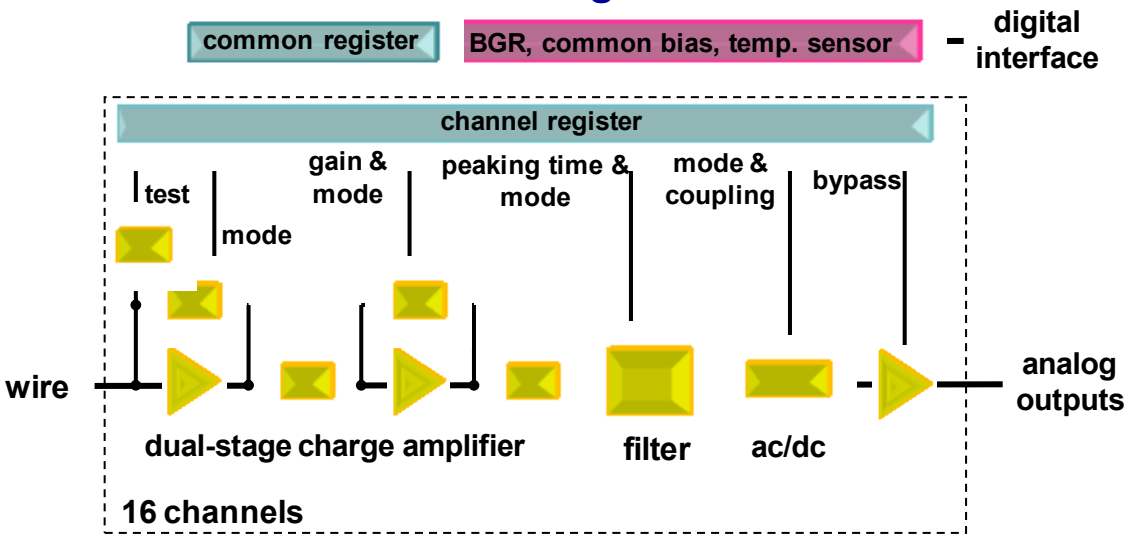
Layout

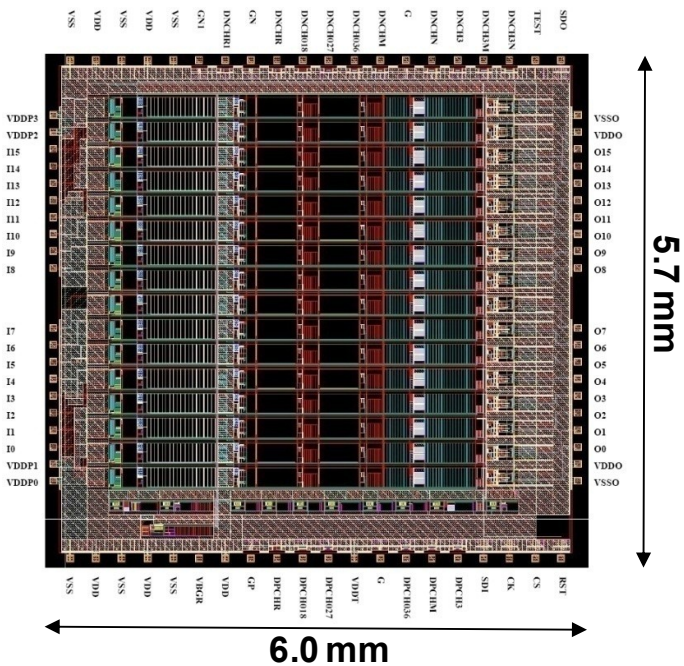


- 16 channels
- charge amplifier (adj. gain)
- high-order filter (adj. time constant)
- ac/dc, adjustable baseline
- test capacitor, channel mask
- ADC (12-bit, 2 MS/s)
- compression, discrimination
- multiplexing and digital buffering
- LV or CM digital interface
- pulse generator, analog monitor
- temperature sensor
- LAr environment (> 20 years at 88K)
- estimated total size ~ 6 x 8 mm²
- estimated power ~ 10 mW/channel

Analog ASIC

Block Diagram



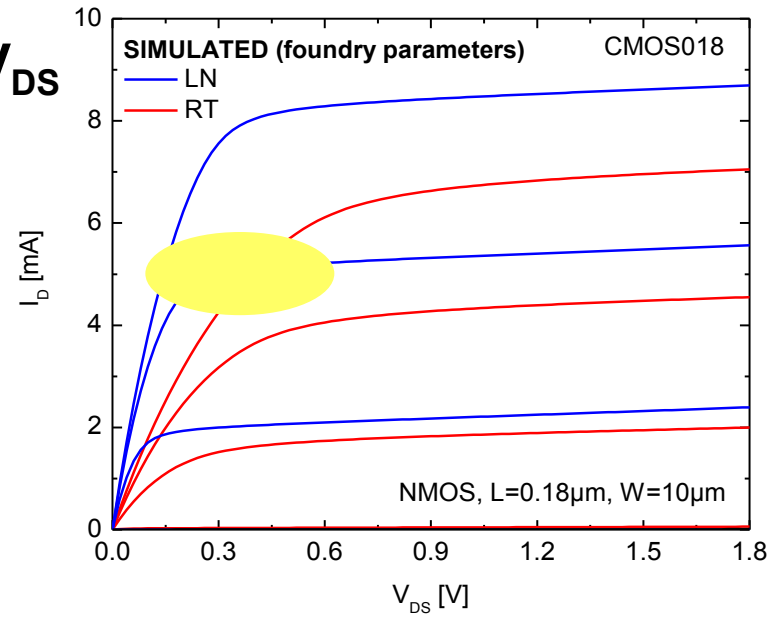


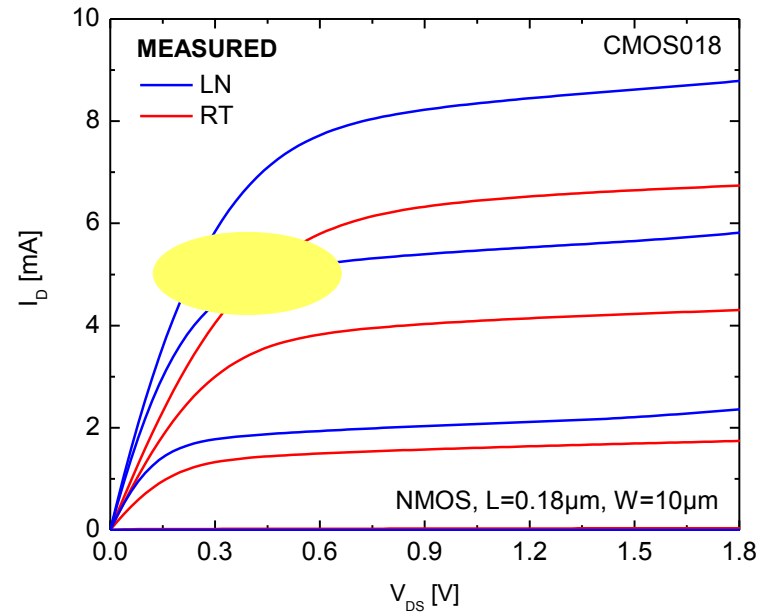
- 16 channels
- charge amplifier, high-order filter
- adjustable gain: 4.7, 7.8, 14, 25 mV/fC
  (charge 55, 100, 180, 300 fC)
- adjustable filter time constant
  (peaking time 0.5, 1, 2, 3 μs)
- selectable collection/non-collection mode
  (baseline 200, 800 mV)
- selectable dc/ac coupling (100μs)

- rail-to-rail analog signal processing
- band-gap referenced biasing
- temperature sensor (~ 3mV/°C)
- 136 registers with digital interface
- 5.5 mW/channel (input MOSFET 3.9 mW)
- single MOSFET test structures
- ~ 15,000 MOSFETs
- designed for room (300K) and cryogenic (77K) operation
- technology CMOS 0.18 μm, 1.8 V, 6M, MIM, SBRES

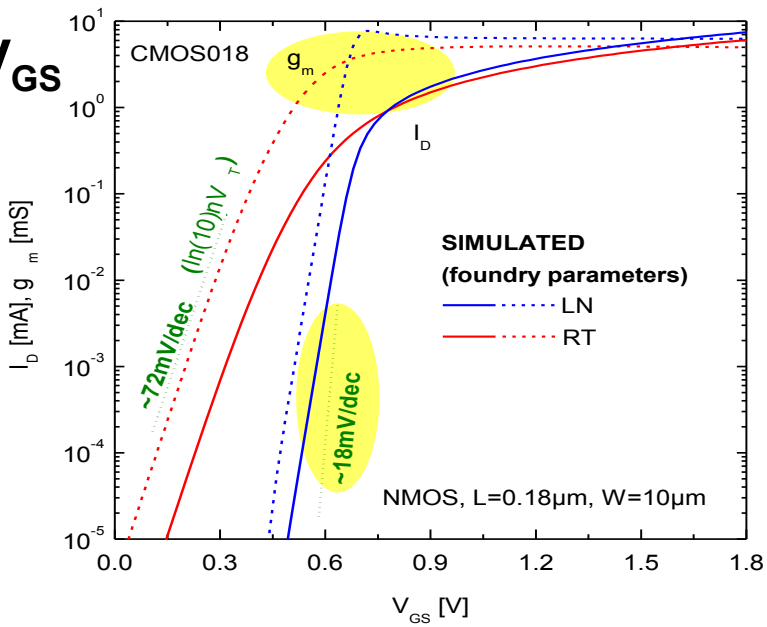
MOS Static Model

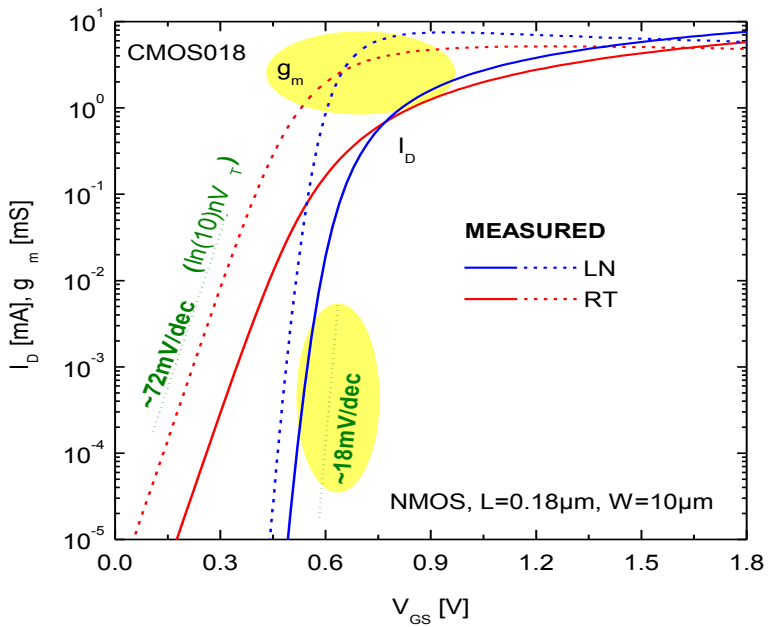
I_D vs V_{DS}





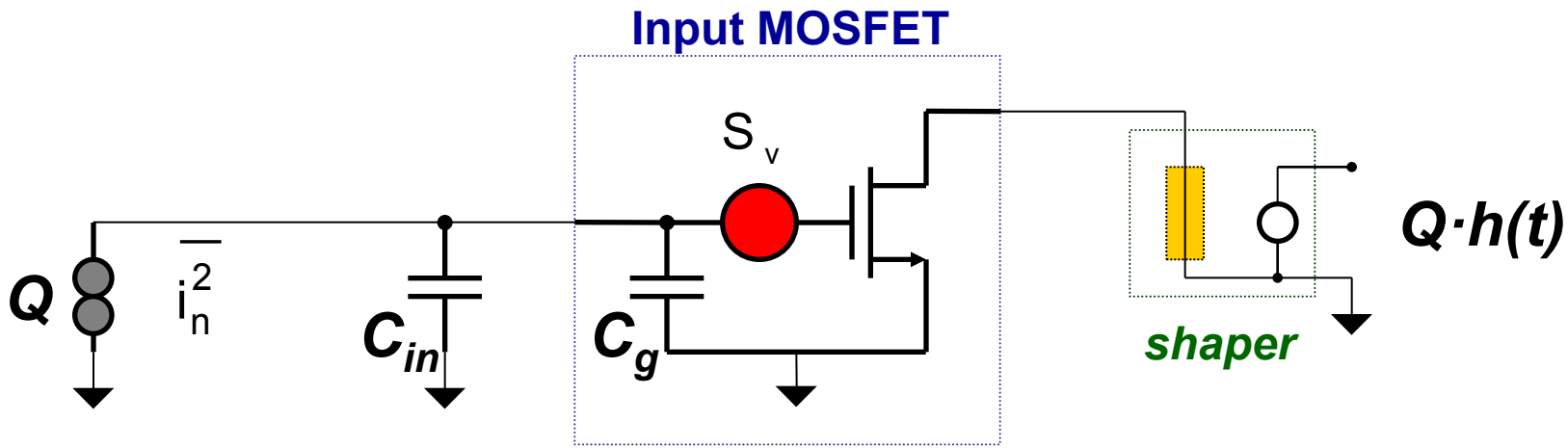
I_D vs V_{GS}





Some differences in <u>saturation voltage</u>, <u>sub-threshold slope</u>, <u>transconductance</u>

Input MOSFET Optimization



low-frequency **white**

$$S_v \approx \frac{K_f(IC, L, T)}{C_{ox} WLf^{\alpha_f(IC, L, T)}} + \alpha_w(IC, L, T)\, n\, 4kT \frac{\gamma(IC)}{g_m(IC, L, T)}$$

$$n \approx 1.3$$

$$\mu_{77K} \approx 5 \times \mu_{300K}$$

$$IC_{77k} \approx 3 \times \mu_{300K}$$

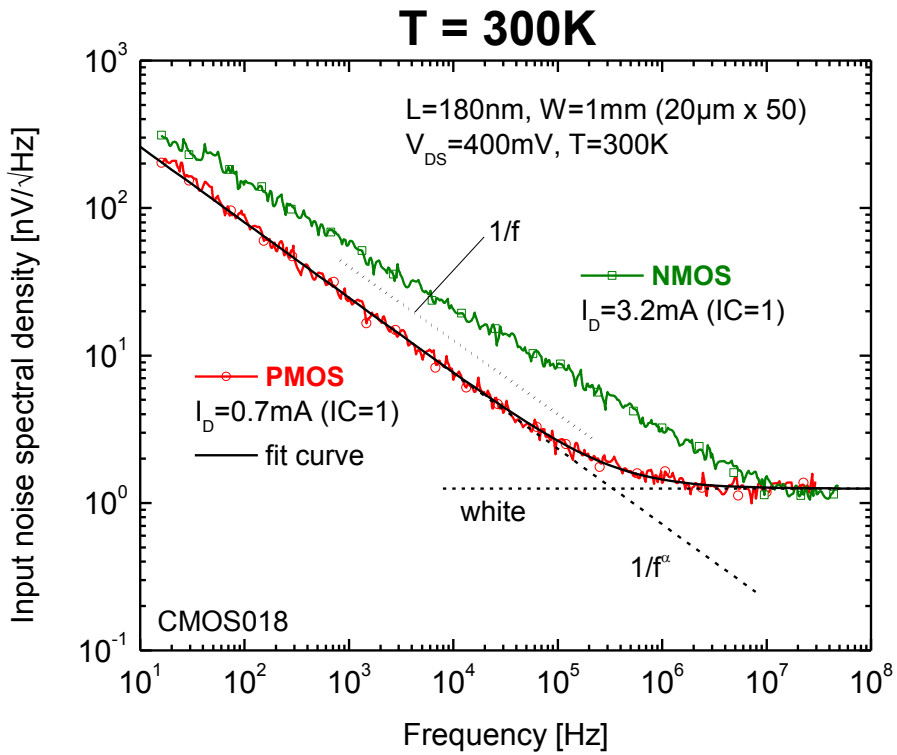
$$\gamma \approx \frac{1}{1+IC}\left(\frac{1}{2} + \frac{3}{2} IC\right)$$

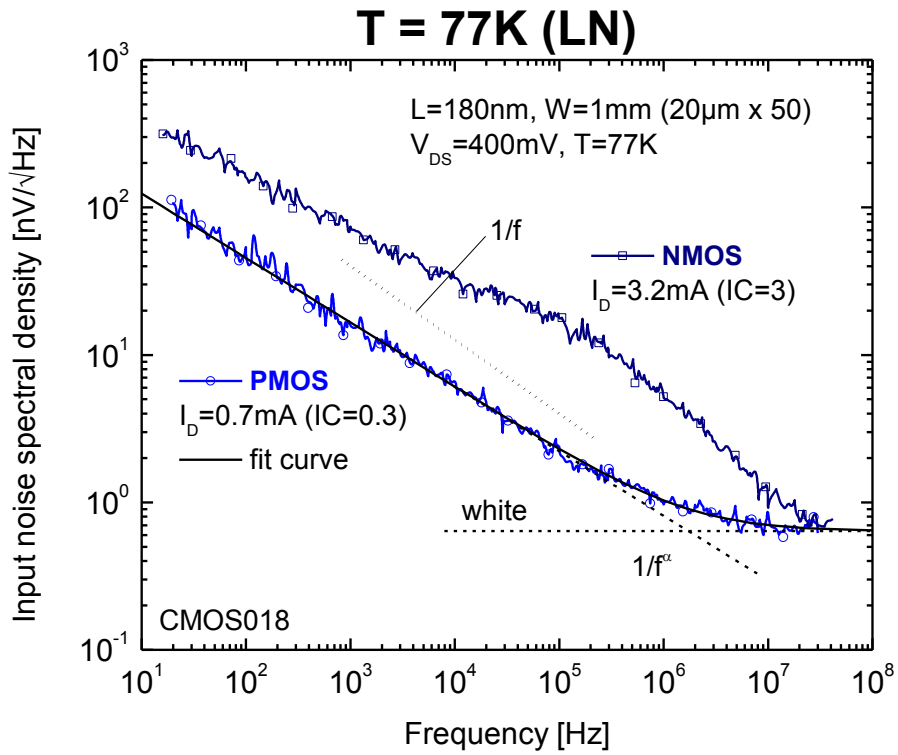
$$IC^{\circ} = \frac{I_D}{2n\mu(T)\, C_{ox} \frac{W}{L} V_T^2}$$

° inversion coefficient

$$ENC^2 = \left[C_{in} + C_{gw}(IC, \mathbf{L}) \cdot \mathbf{W}\right]^2 \left[\frac{1}{\tau_p} \frac{n\alpha_w(IC, L, T)\, \gamma(IC)\, 4kT}{g_{mw}(IC, \mathbf{L}, \mathbf{T}) \cdot \mathbf{W}} + \frac{1}{2} \frac{(2\pi)^{\alpha_f(IC, L, T)}}{\tau_p^{1-\alpha_f(IC, L, T)}} \frac{K_f(\mathbf{IC}, \mathbf{L}, \mathbf{T})}{C_{ox} \mathbf{WL}}\right]$$

Noise Model - White





White noise decreases considerably with T

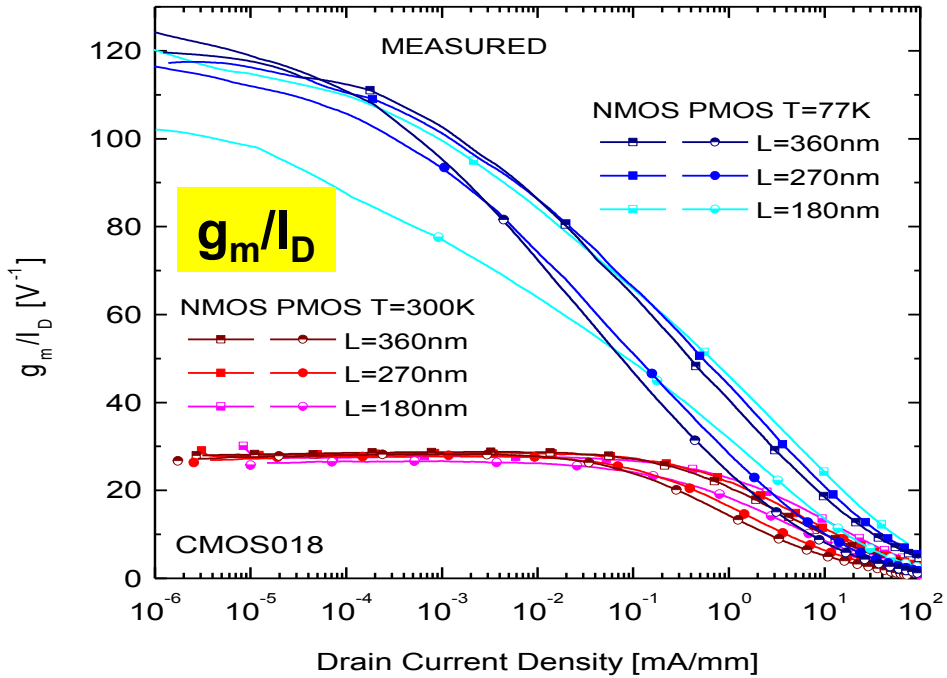
Noise Model - White

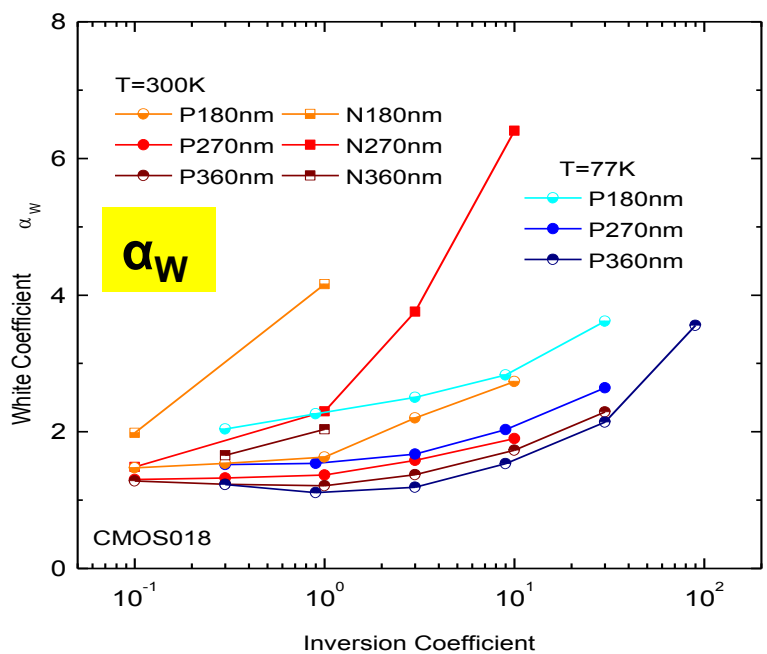
White at given current decreases since

- **T decreases**
- **g_m increases**

$$\frac{g_m}{I_D} \rightarrow \frac{q}{nk_BT} = \begin{cases} \sim 30 & \text{at} \quad T = 300\,K \\ \sim 116 & \text{at} \quad T = 77\,K \end{cases}$$

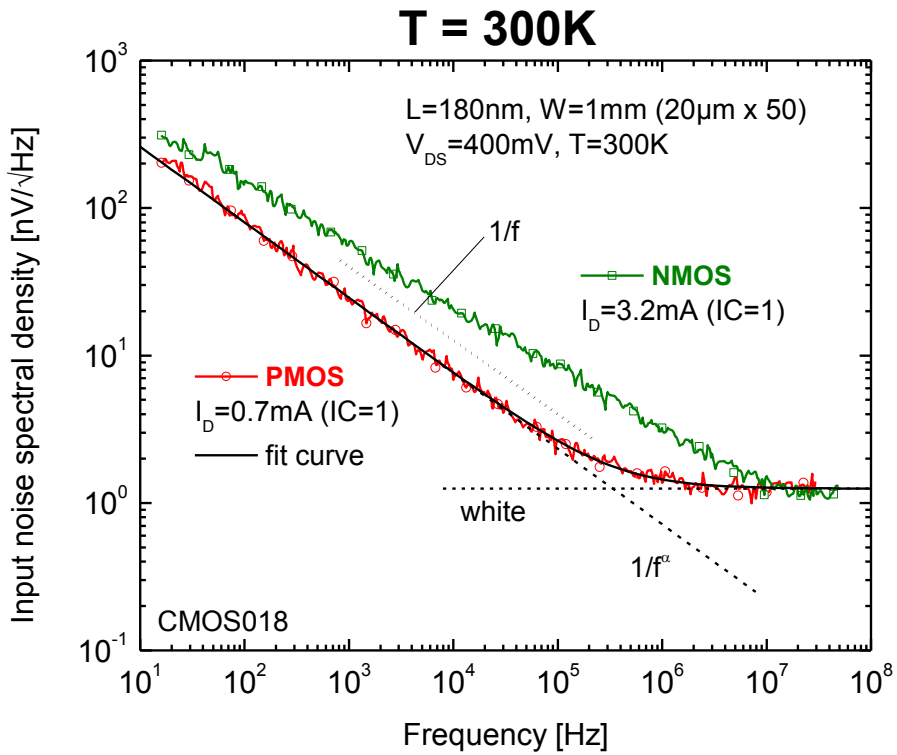
$$\alpha_w(IC, L, T)\, n\, 4kT \frac{\gamma(IC)}{g_m(IC, L, T)}$$

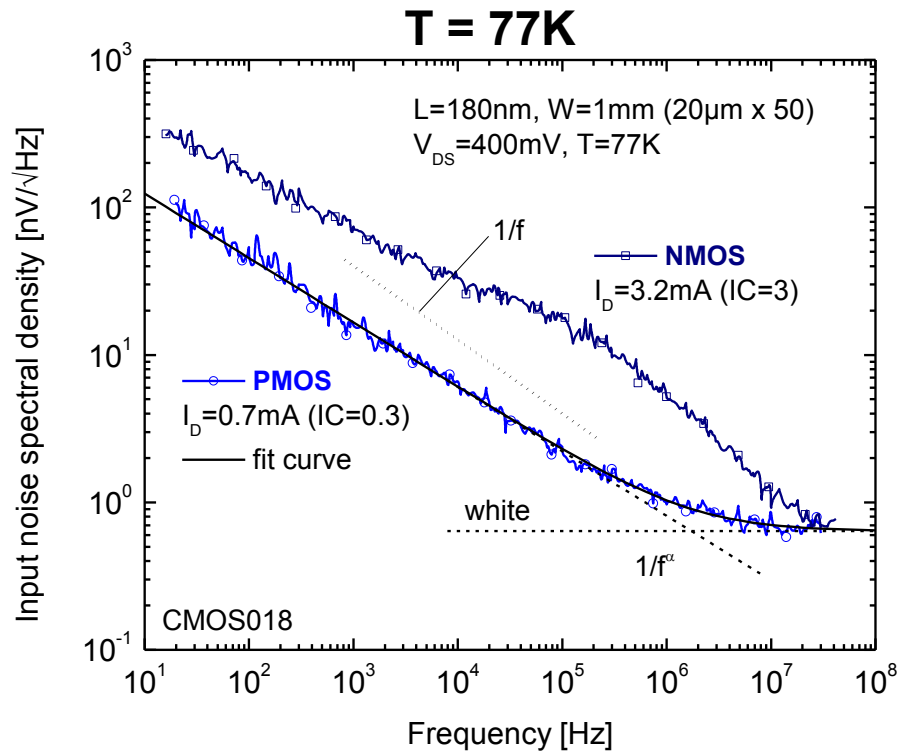




- **always larger than unity**
- **general increase with**
  - **drain current density**
  - **inverse of channel length**
  - **inverse of temperature**

Noise Model - Low Frequency

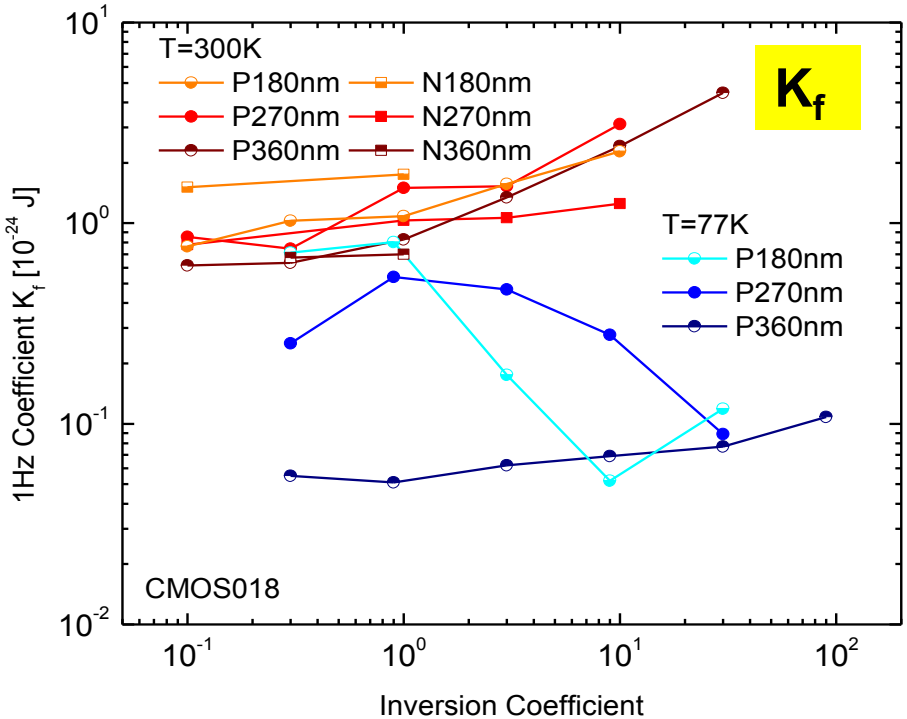




- comparable K_f
- NMOS
  - slope <1
- PMOS
  - slope >1

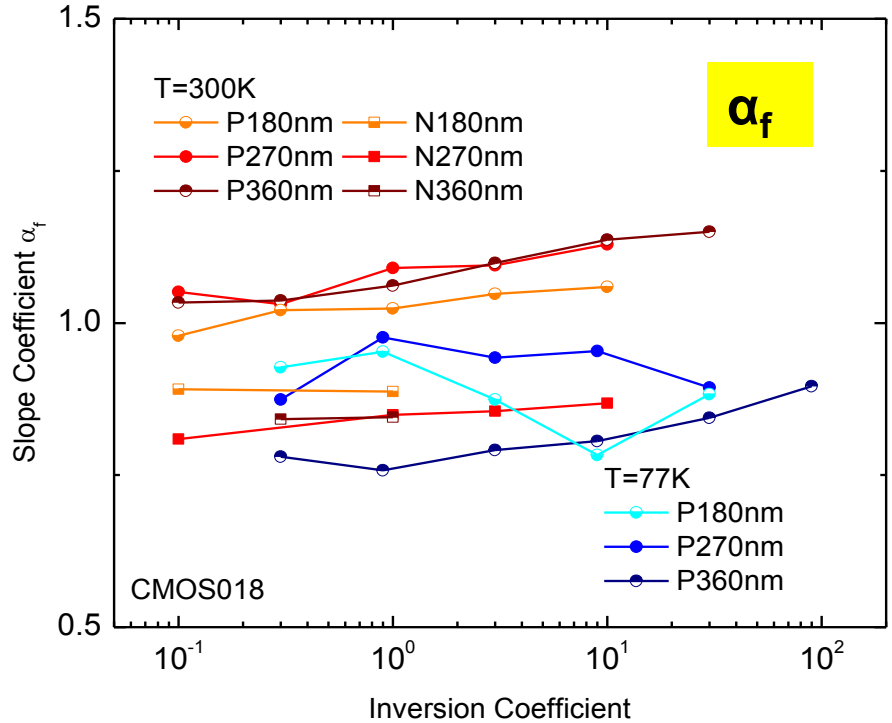
- NMOS
  - K_f ~ same
  - lorentzian packet
- PMOS
  - K_f lower
  - slope < 1

Noise Model - Low Frequency



- somewhat dependent on fitting
- K_f and α_f decrease with temperature
- change in $K_f \rightarrow$ change in α_f (slope)

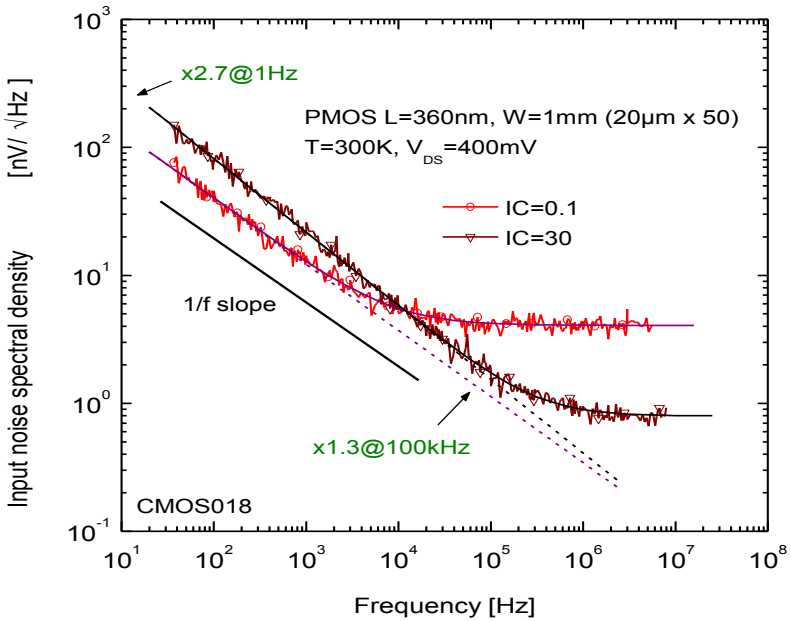
$$\frac{K_f(IC, L, T)}{C_{ox} W L f^{\alpha_f(IC, L, T)}}$$

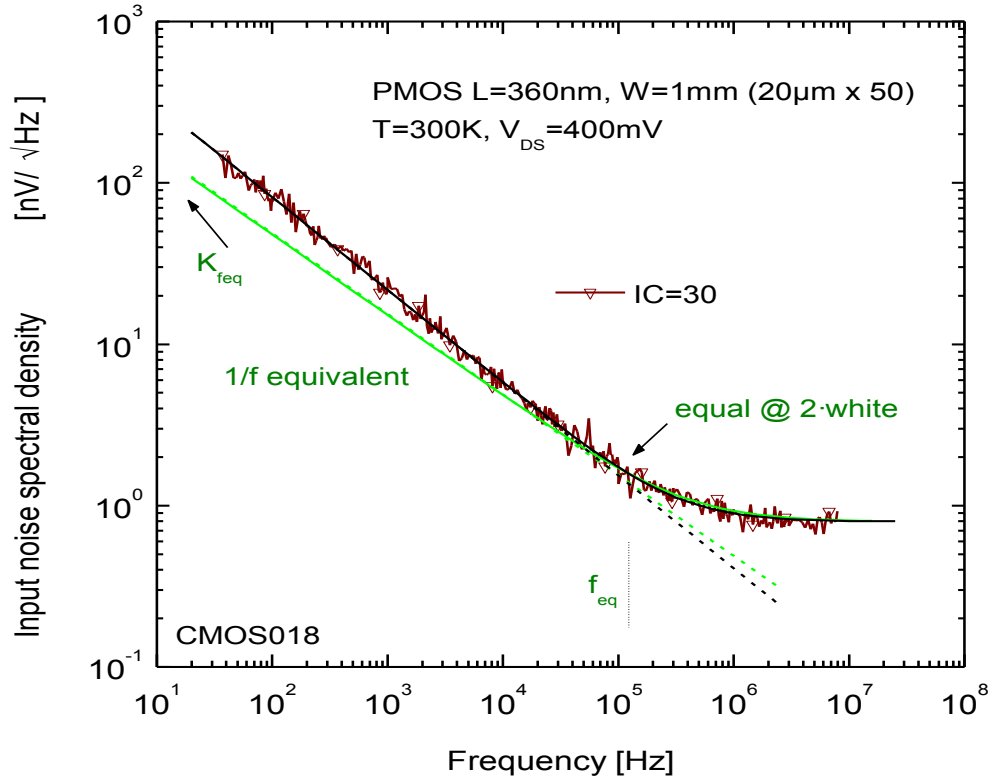


Equivalent 1/f (K_{feq})

PMOS 360 nm at 300K

35 µA/mm and 11 mA/mm





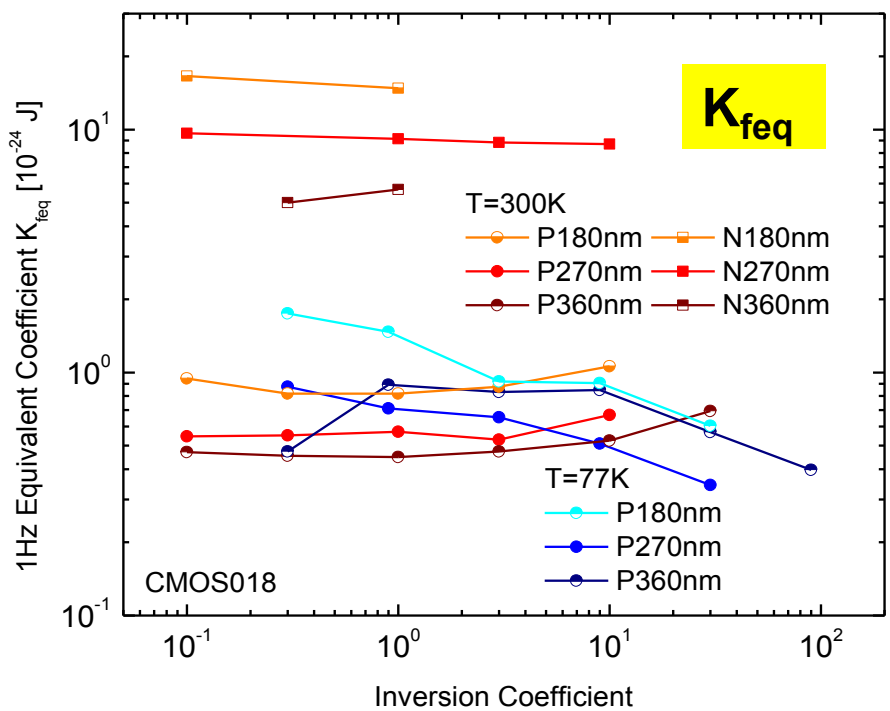
- **as K_f increases, slope increases (α_f increases)**

<u>Equivalent 1/f</u>: equal value at twice the white component (four times in power)

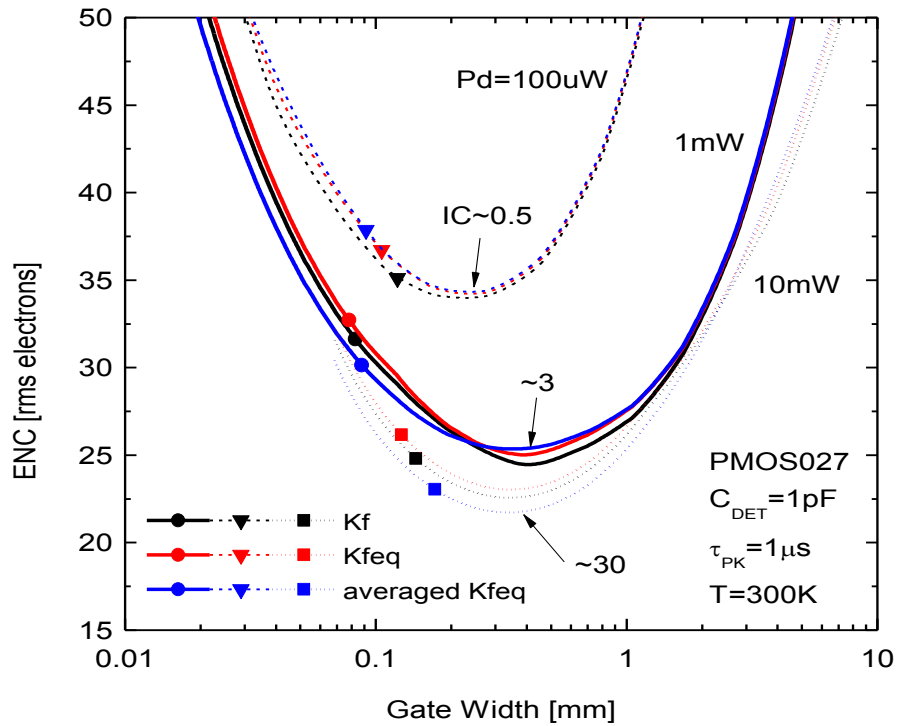
$$\frac{K_{feq}}{C_{ox} W L f_{eq}} + \text{white} = S_v(f_{eq}) \quad \text{where} \quad S_v(f_{eq}) = 4 \times \text{white}$$

$$\Rightarrow K_{feq} = C_{ox} W L f_{eq} \, 3 \times \text{white}$$

Equivalent 1/f (K_{feq})



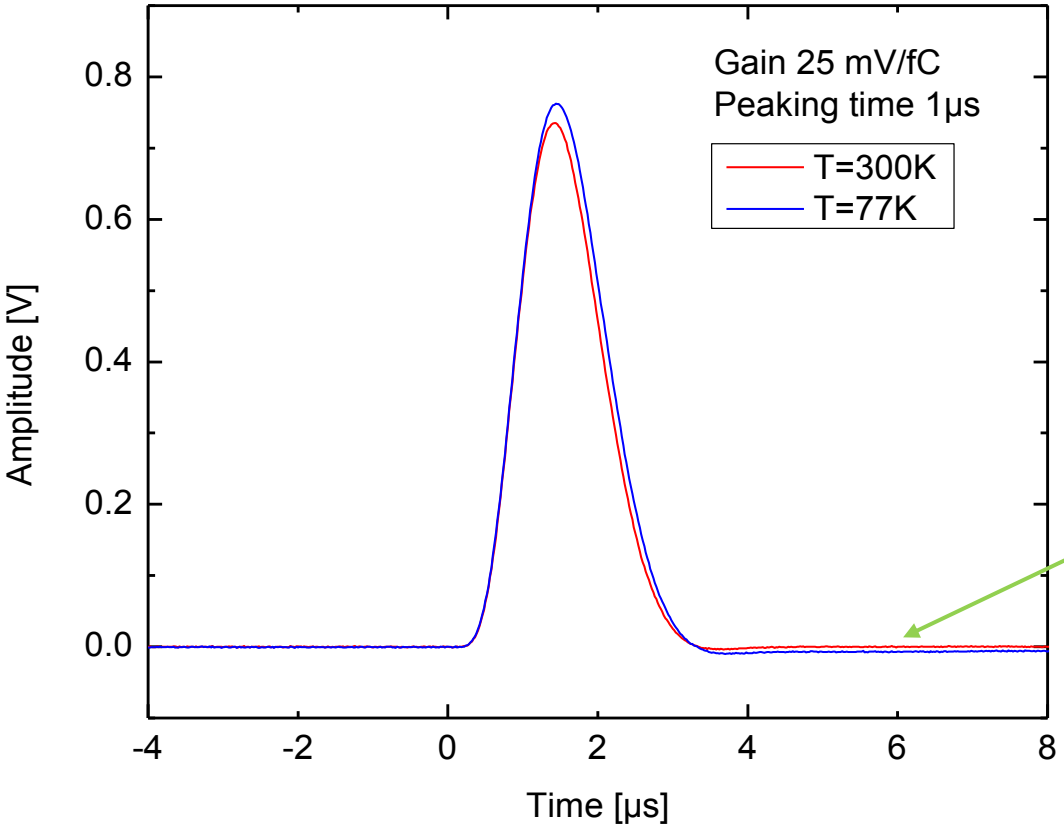
Optimum W: example for 1 pF



- dependence on drain current density is now modest

- negligible error in optimization
- averaged K_{feq} can also be used
- small error in estimate for large relative power (large mW/pF)

Signal Measurements



Bandgap Reference

$$V_{BGR} \approx \begin{cases} 1.185 \text{ V at } 300\ ^\circ\text{K} \\ 1.164 \text{ V at } 77\ ^\circ\text{K} \end{cases}$$

variation ≈ 1.8 %

Temperature Sensor

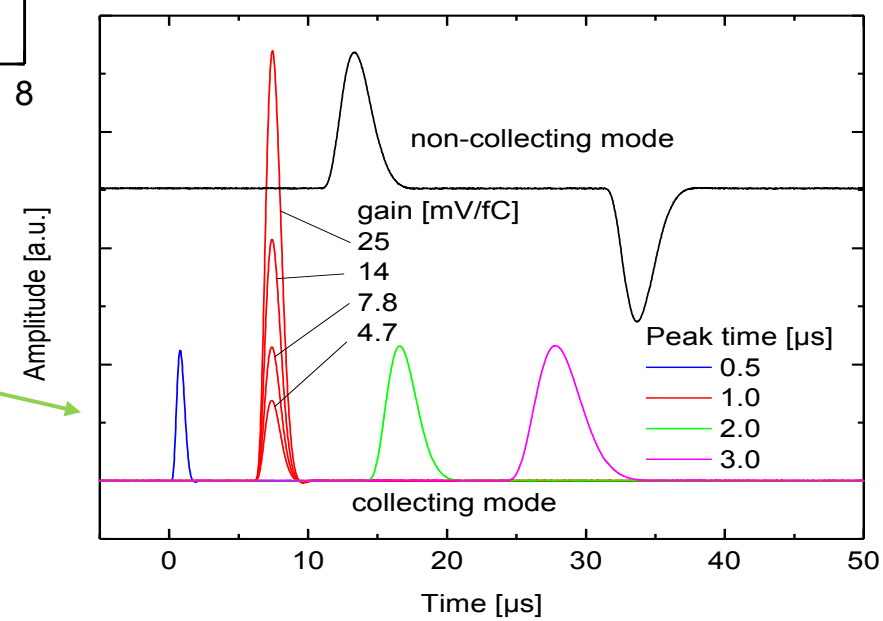
$$V_{TMP} \approx \begin{cases} 867.0 \text{ mV at } 300\ ^\circ\text{K} \\ 259.3 \text{ mV at } 77\ ^\circ\text{K} \end{cases}$$

~ 2.86 mV / °K

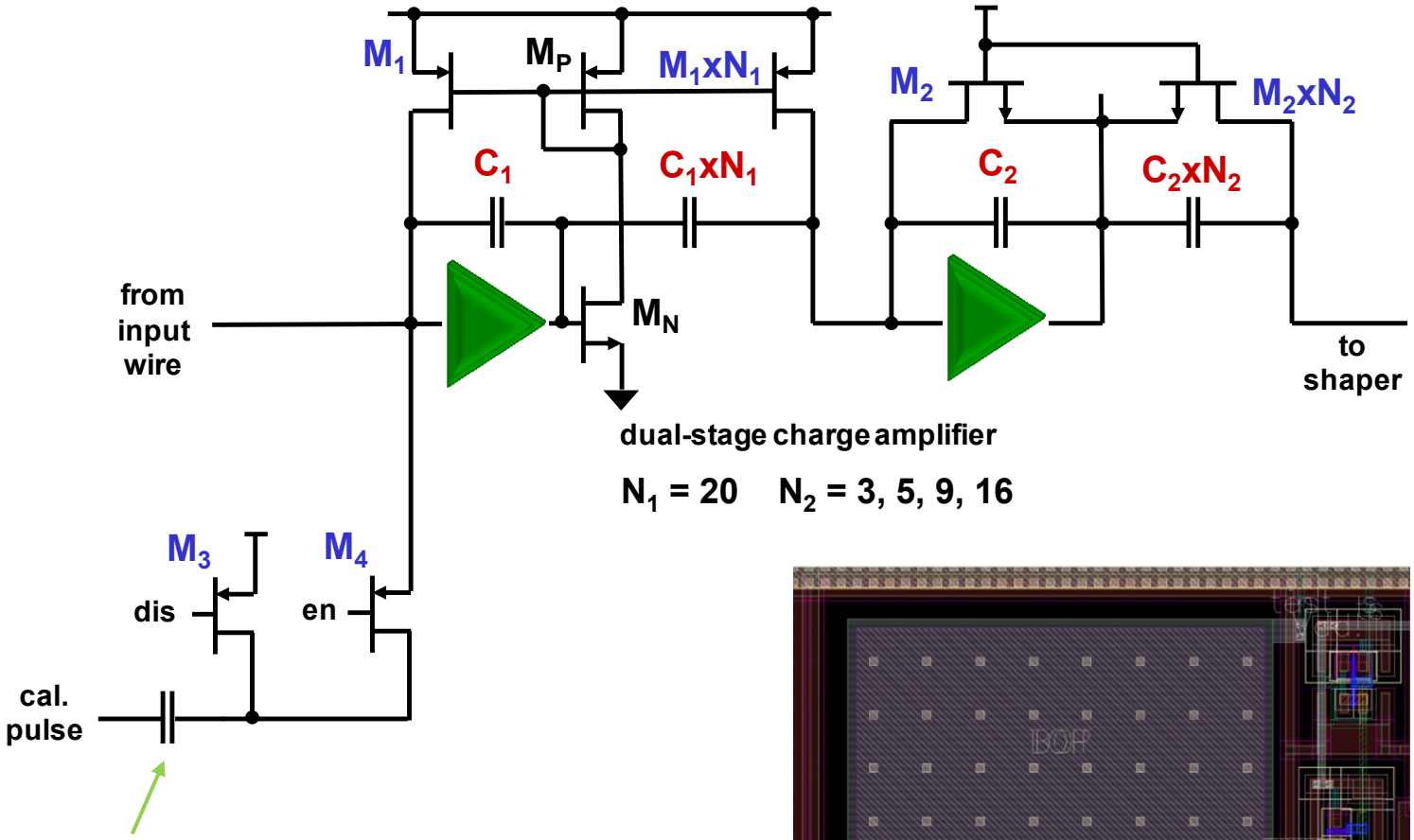
Pole-zero cancellation at 77K
to be addressed in next revision

Adjustable gain, peaking time and baseline

maximum charge 55, 100, 180, 300 fC



Calibration Scheme



$C_{INJ} \approx 180$ fF

Integrated injection capacitance (10 x 18 μm²)

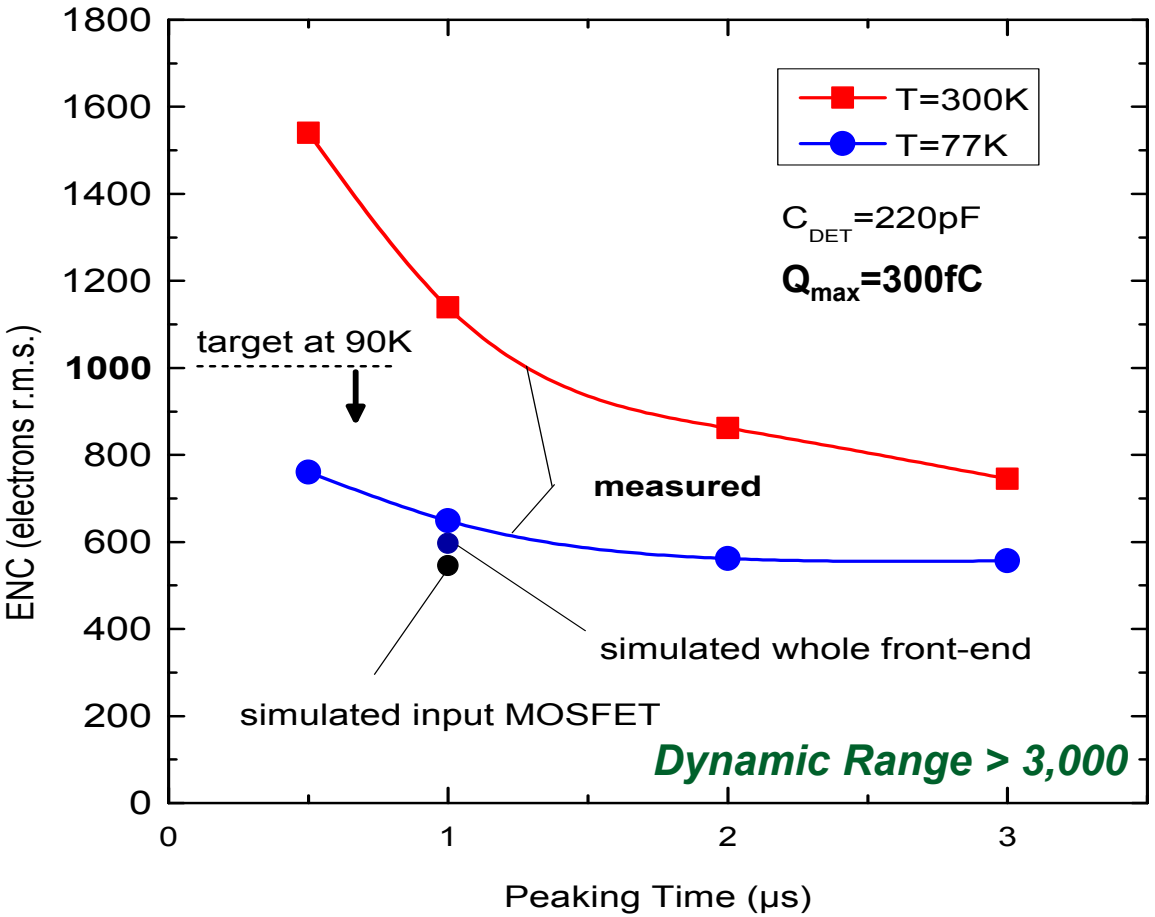
Disabled (grounded) when unused

Measured with high-precision external capacitance

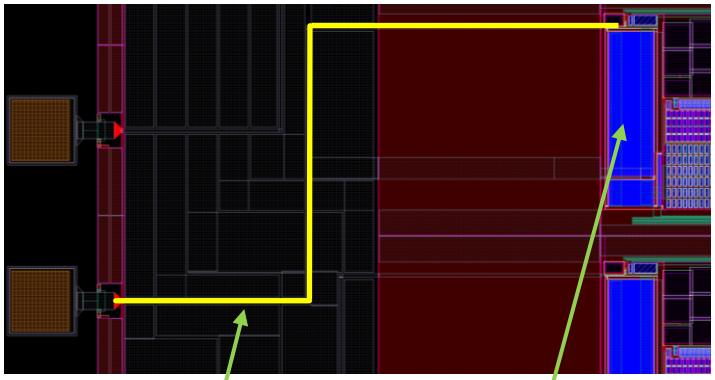
$$C_{INJ} \approx \begin{cases} 184 \text{ fF at } 300 \text{ K} \\ 183 \text{ fF at } 77 \text{ K} \end{cases}$$

change ~ 0.5%

Noise Measurements

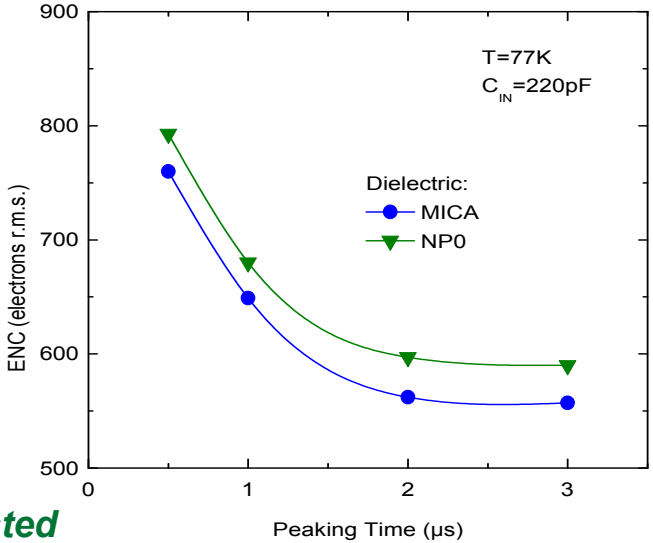


Layout Detail



Input Line
L ≈ 1 mm
W = 3.5 μm
(M3 + M4)
R_{77K} ≈ 3 Ω
R_{300K} ≈ 12 Ω

Input MOSFET
L = 270 nm
W = 10 mm
(50μm x 200)
$g_{m,77K}$ ≈ 90 mS (11 Ω)
$g_{m,300K}$ ≈ 45 mS (22 Ω)



Measurements affected by:

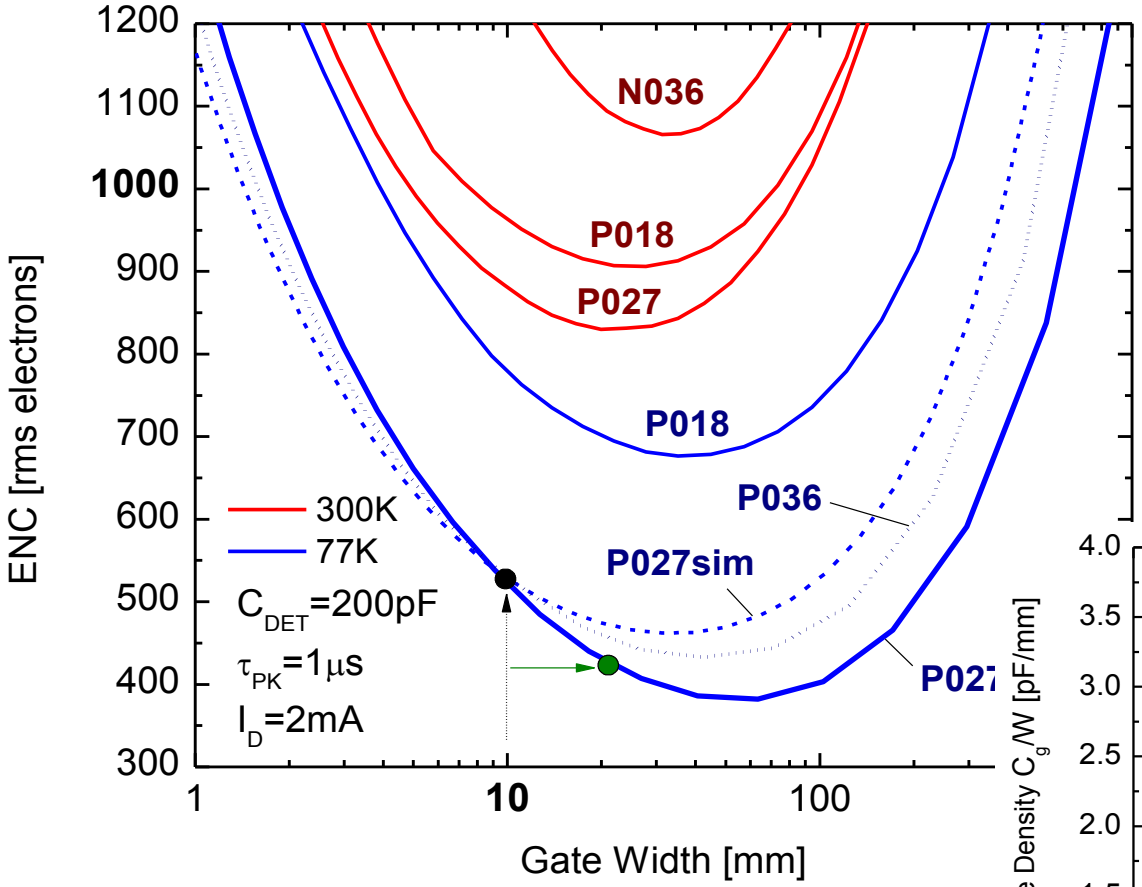
- **input line parasitic resistance**
  - **~ 150 e⁻ at 77 K (~ 590 e⁻ at 300K)**
  - **addressed in next revision**
- **C_{IN} dielectric noise (not present in wire)**
  - **~ 60 e⁻ at 77 K**

$$dENC \approx \sqrt{2kTC_{IN}\,tg\,\delta}$$

$$\approx \begin{cases} 200\ e^- \text{ for NPO} \\ 60\ e^- \text{ for MICA} \end{cases}$$

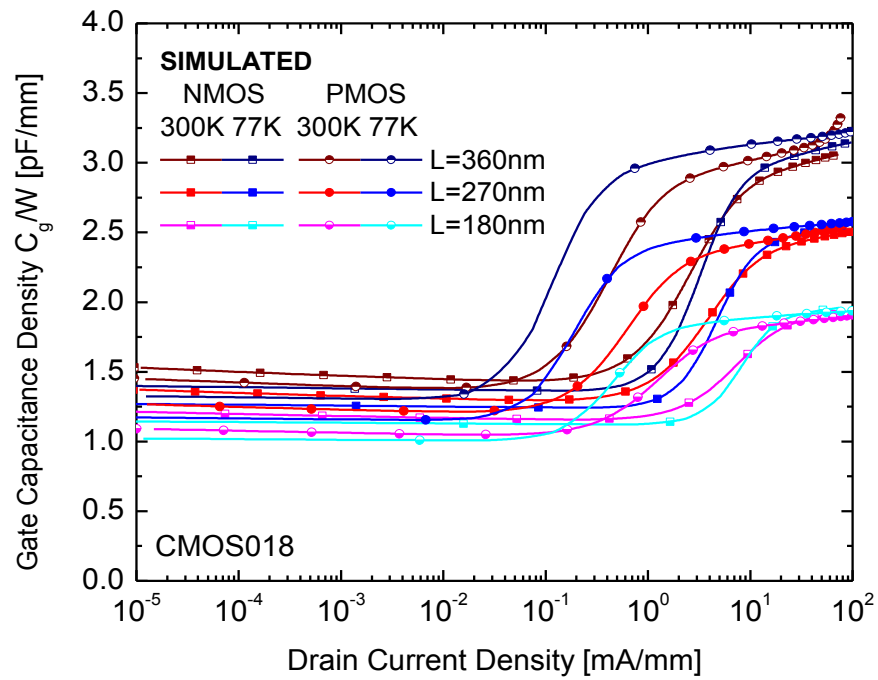
ASIC revision designed and fabricated, currently being tested

MOSFET Optimization for LAr TPC



C_g(IC,L) determinant in the selection of L

$$W_{opt} = \frac{C_{in}}{C_{gw}\left[1 - 2\frac{IC}{C_{gw}}\frac{\partial C_{gw}}{\partial IC}\right]}$$



Selected size and operating point:
original (simul. noise) vs revised (meas. noise)

- **I_D = 2 mA (3.6 mW)**
- **W/L = 10 mm / 270 nm** **20 mm / 270 nm**
- **IC_{300K} ≈ 0.4** **0.3** **IC_{77K} = 1.25** **1**
- **g_{m_300K} ≈ 45 mS** **48 mS** **g_{m_77K} = 90 mS** **118mS**
- **C_{g_300K} ≈ 14 pF** **25 pF** **C_{g_77K} = 18 pF** **28 pF**

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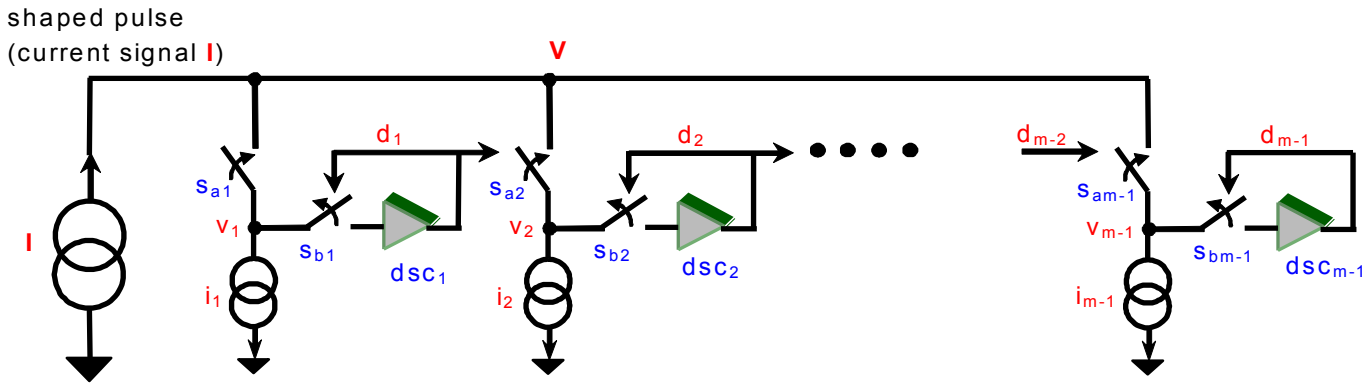
ADC - Architecture

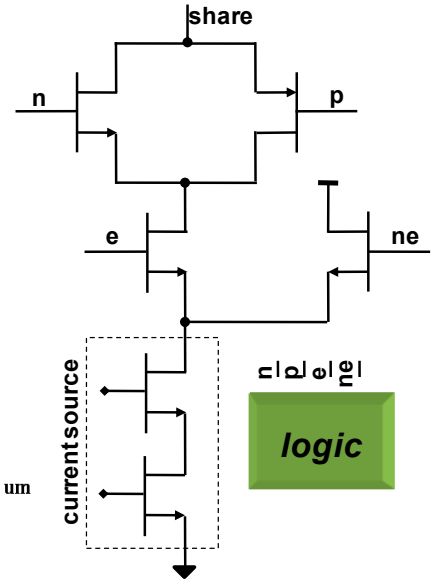
Clockless low power ADC stage (demonstrated in ASIC for SNS)

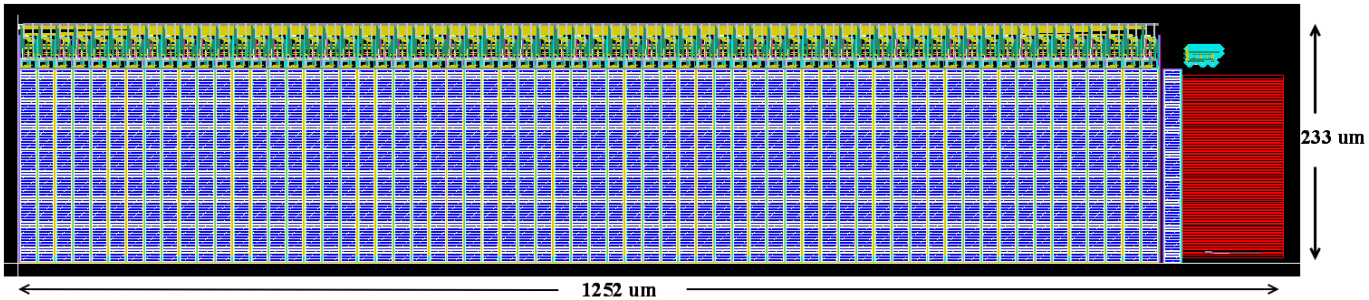


Current mode ADC

- **dual stage** 6-MSBs in 150ns, 6-LSBs in 250ns
- single trigger conversion per stage
- **12-bit resolution**
- **2 MS/s** conversion rate
- power dissipation **3.6 mW at 2 MS/s**
- **power-down** option for low rate applications
  - wake up in few tens of ns
- layout size: 0.23 mm x 1.25 mm

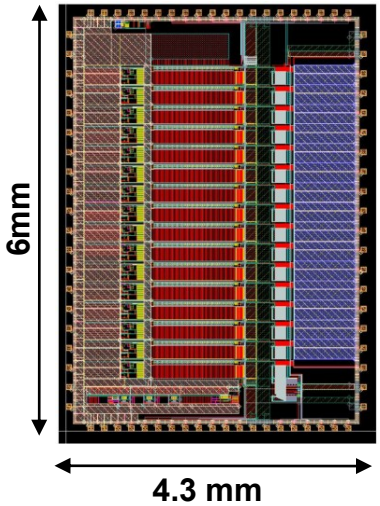
ADC cell



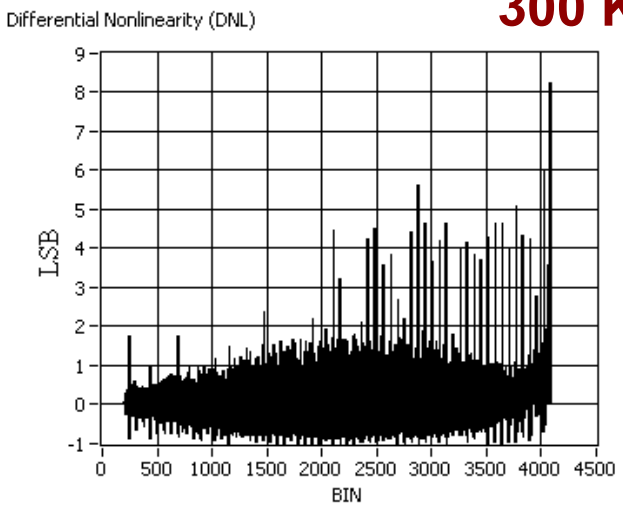


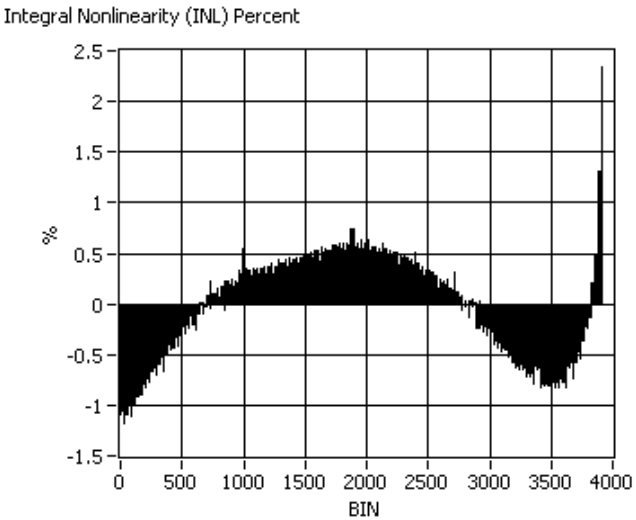
ADC - Preliminary Results

16-channel ADC+buffer



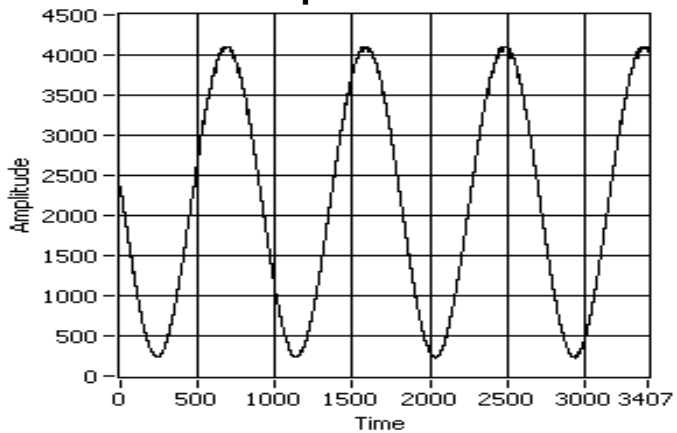
300 K



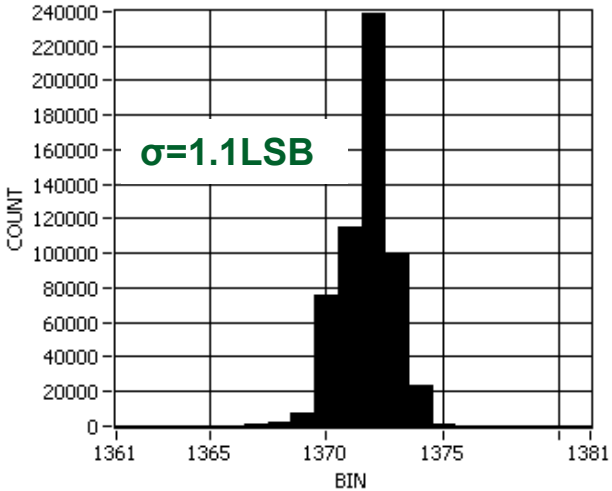


77 K

ADC output - 1.4 V sine



ADC output - 500mV dc

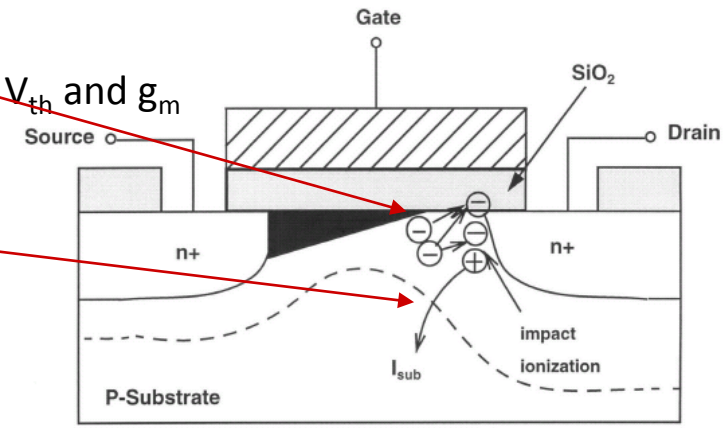


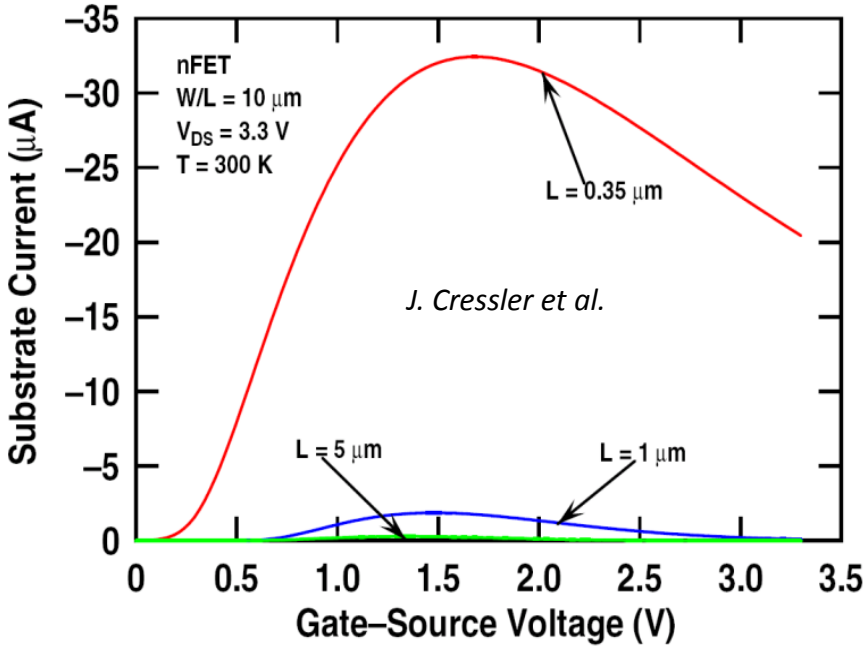
- operation **verified at room and cryogenic temperatures**
- **differential non-linearity** limited by **timing design error** in control circuit
- **integral non-linearity** limited by **mismatch (linear → common centroid)**

ASIC revision being designed, to be fabricated in July

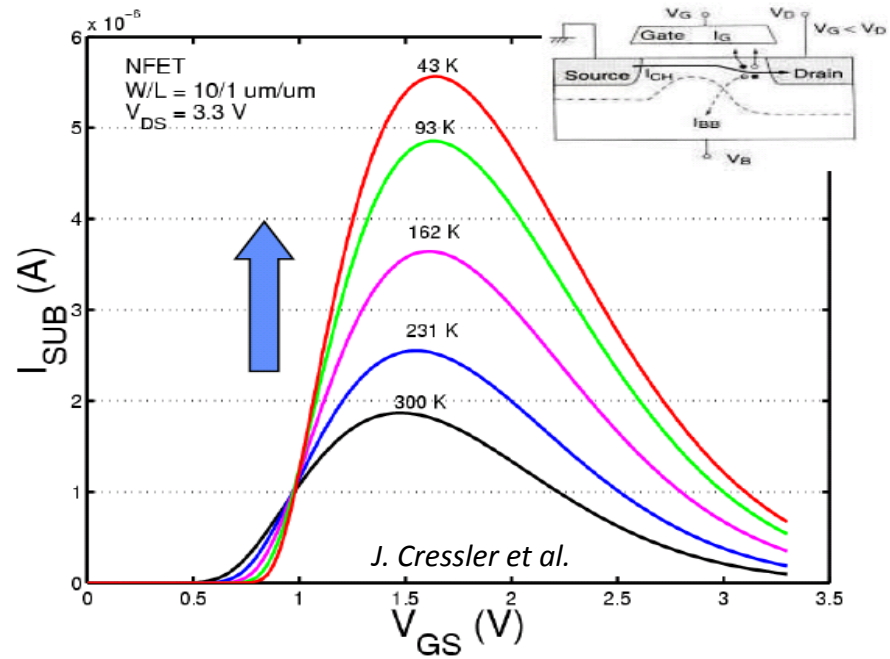
Lifetime - Basic Mechanism

- **Degradation is due to impact ionization**
  - charge trap in oxide, interface generation → shift in V_{th} and g_m
- **Substrate current is a monitor of impact ionization**
  - increases with **drain voltage**
  - is higher in **short channel** devices
  - has a **maximum** at $V_{GS} \approx V_{DS}/2$





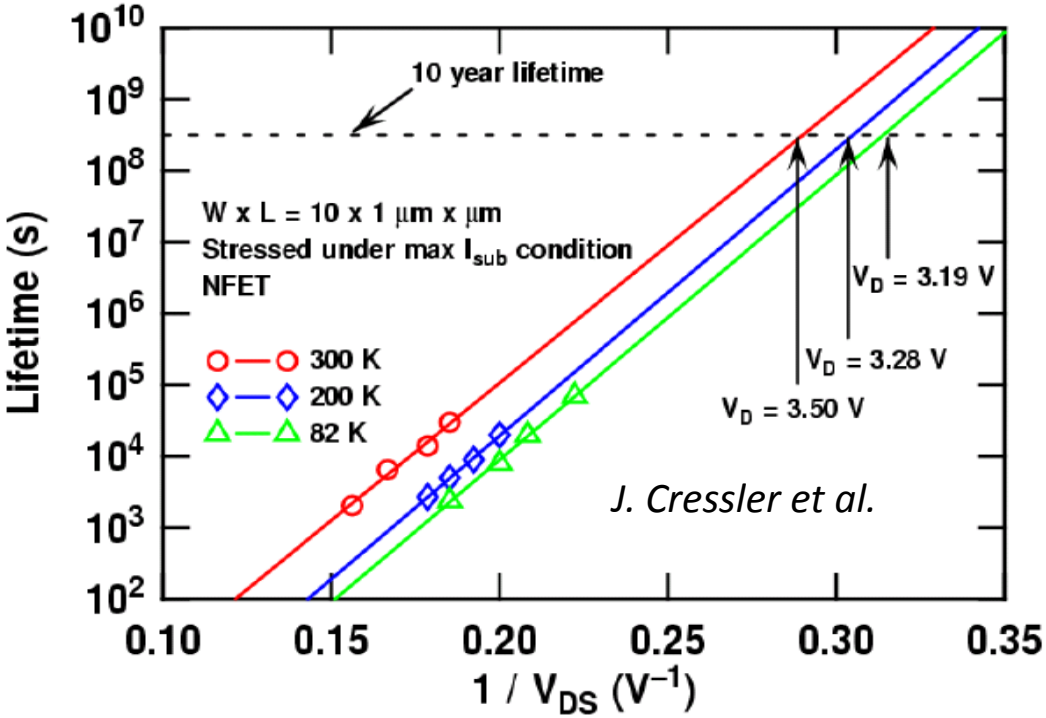
- **increases as the temperature decreases**



Commercial technologies are rated 10 years lifetime (10% g_m shift) in continuous ring oscillator operation: T = 300 K, L = L_{min}, V_{ds} = nominal V_{DD}+5%, $V_{GS} \approx V_{DS}/2$)

Lifetime - Design Guidelines

Accelerated tests at increased V_{DS} allow extrapolation of lifetime



Desired lifetime at low temperature can be achieved by:

1. **decreasing V_{DS}** (e.g. decreasing the supply voltage)
2. **decreasing J_D** (i.e. decreasing the drain current density)
3. **increasing L** (i.e. non-minimum channel length devices)

Design guidelines can be obtained for:

analog circuits

- operate devices at **low current density**
- use **non-minimum channel length L**

digital circuits

- operate devices at **-10% of nom. V_{DD}**
- use **non-minimum channel length L**
- operate at **low clock frequency**

Accelerated tests at cryogenic temperature are being performed to verify guidelines

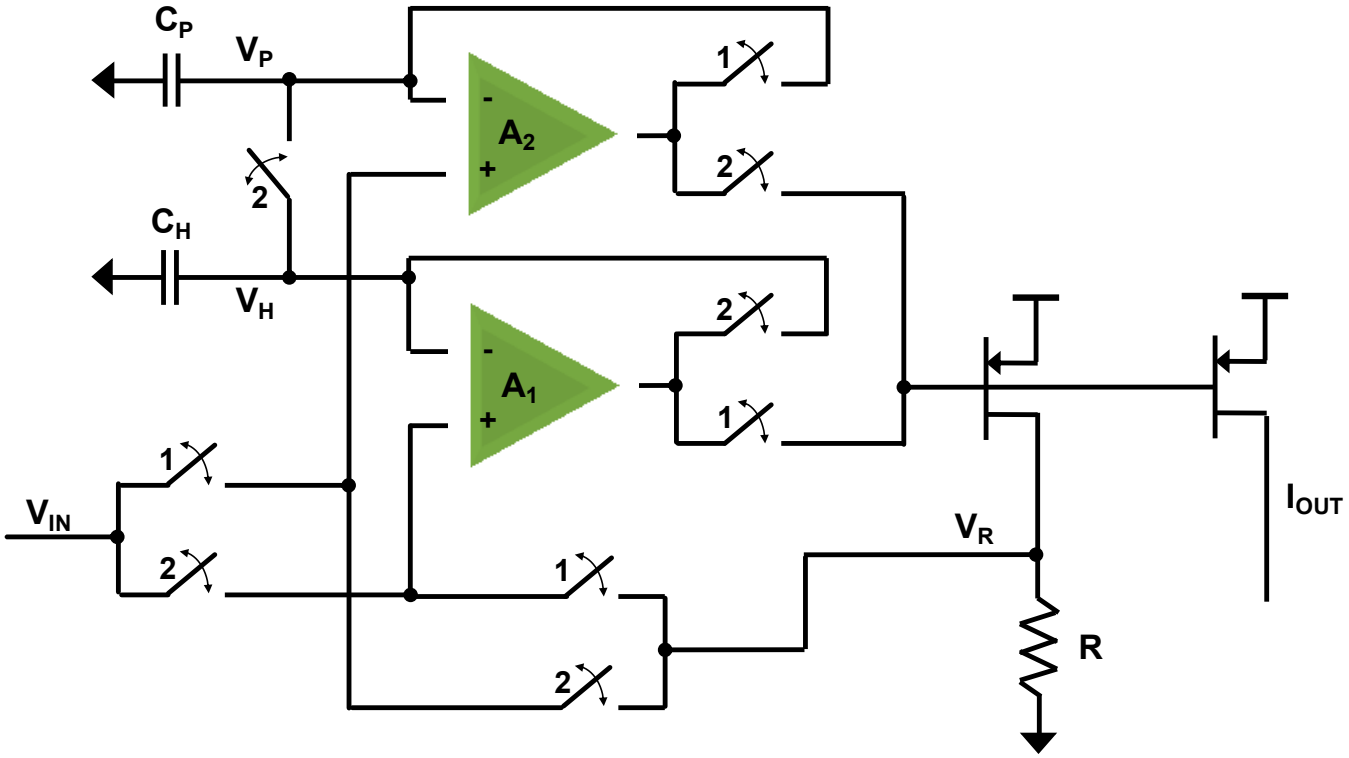
Conclusions and Future Work

- CMOS performs better at cryogenic temperatures
- Defined and predictable design for cryogenic T is possible
- Low-noise at cryogenic T demonstrated
  - ENC < 1,000 e^- at 200pF ~5mW/ch.
  - characterization and modeling of CMOS 180nm
  - equivalent 1/f (K_{feq})
- Long lifetime at cryogenic T possible with guidelines
- Critical building blocks (front-end, ADC) developed
- Future work
  - optimize ADC, improve static models
  - merge and finalize

Acknowledgment

J. Triolo, D. Pinelli, The MOSIS Service

Sample-Hold and V/I - Architecture



- during ADC encoding 2 is closed and V_R tracks V_{IN} through V_H
  - the loop on V_R closes with A_2
  - the voltage V_H includes the offset from A_1
- sample occurs by opening 2 and closing 1
  - the loop on V_R closes with A_1
  - the offset from A_1 is now subtracted
  - the output signal settles in less than 50 ns
  - in the mean time V_P tracks V_{IN}
- after the conversion (during ADC encoding) 1 is open and 2 is closed ...