



# The LPD Detector and Readout Chip for XFEL

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Science and Technology Facilities Council

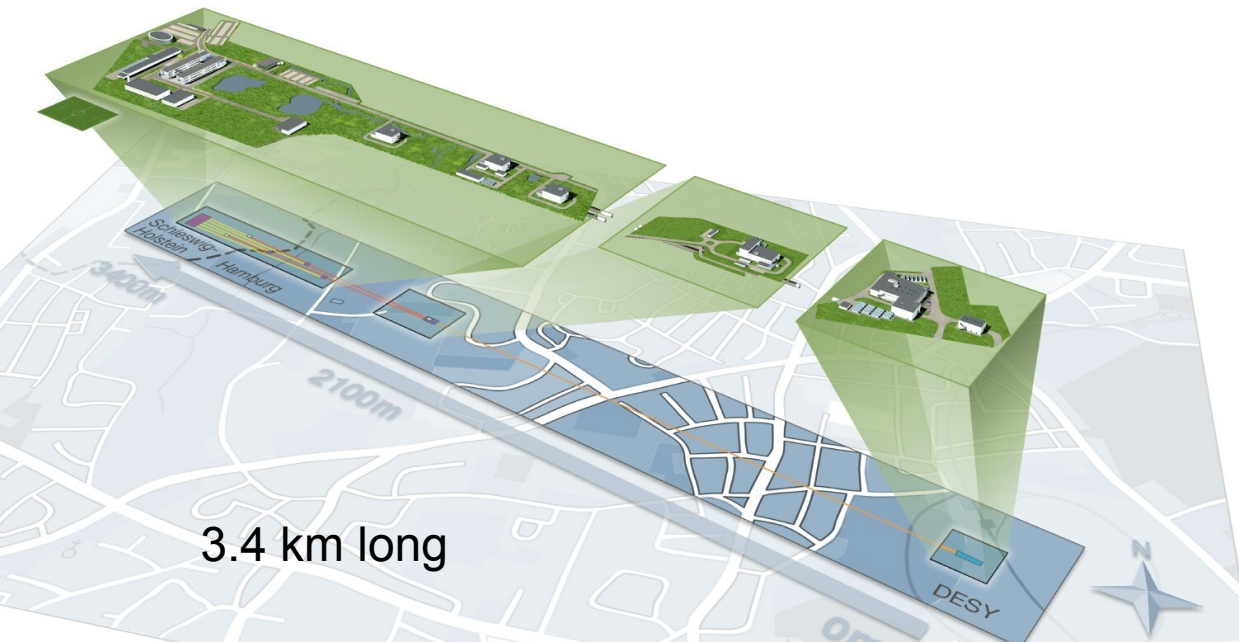
Rutherford Appleton Laboratory



- Introduction to the Application and Overview of the LPD Instrument
- Details of ASIC Design
- Summary of Characterisation Results
- Future Developments

# Introduction

- The European XFEL
  - Hamburg, Germany
  - Currently under construction, to be finished around 2014, first experiments 2015
  - ~2700 X-ray flashes per second. Arriving in bunches of 3000
  - <100 fs pulse duration

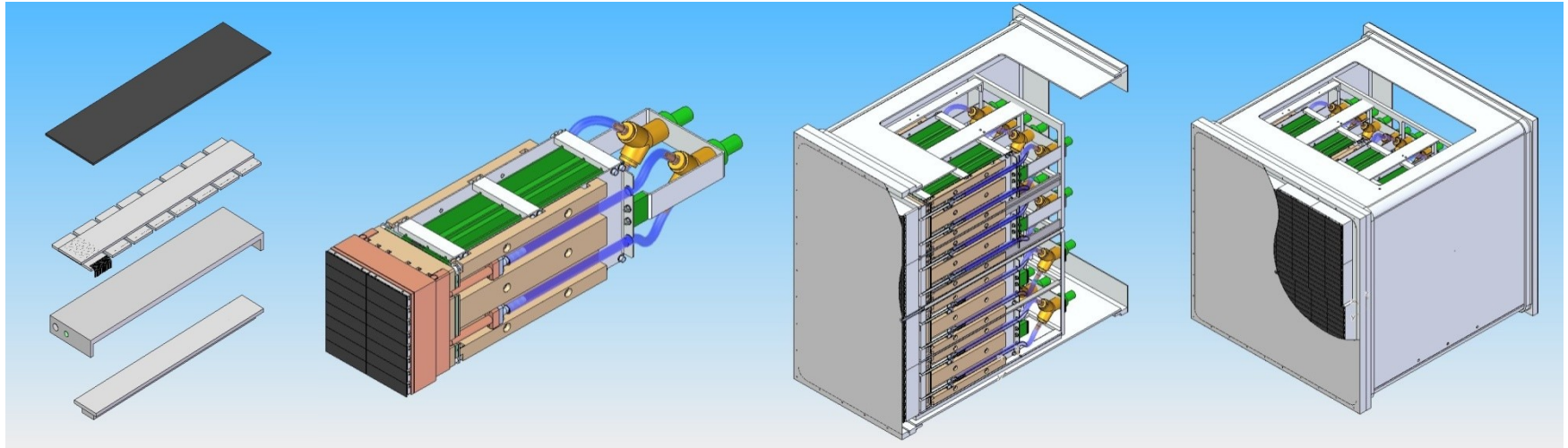


- Megapixel, based around **500um Pixel**
- High dynamic range, **~1 to  $1 \times 10^5$  photons** per pixel per pulse
- **222nsec** Integration and reset time (4.5MHz)
- Large memory depth, **512 frame**.
- **Veto** – for efficient use of memory.
- On Chip ADCs Readout is split between **sixteen 12-bit ADCs**
- Radiation Hard

## Differences/Advantages

- Large pixel size **reduces radiation dose** per unit area of silicon.
- Large memory depth allows **more frames** to be stored for each cycle.
- Cyclic memory write process gives the ability to **deal with lag in the trigger signal** up to the full memory depth.
- Command word interface allows **expanded modes of operation**, e.g. alternate reset timing

# The LPD Detector



8 Chips, 4,096 Pixels  
Scale = 6.4cm

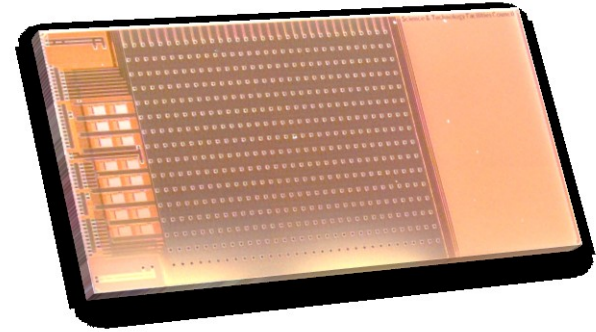
128 Chips, 65,536 Pixels  
Scale = 12.8cm

2048 Chips, 1,048,576 Pixels  
Scale = 51.2cm

- Complete Detector System
- Scalable system, Detector tiles -> Super-module -> Mega Pixel
- Detectors, Readout Chip, FEM DAQ board, Power, Mechanics, Cooling

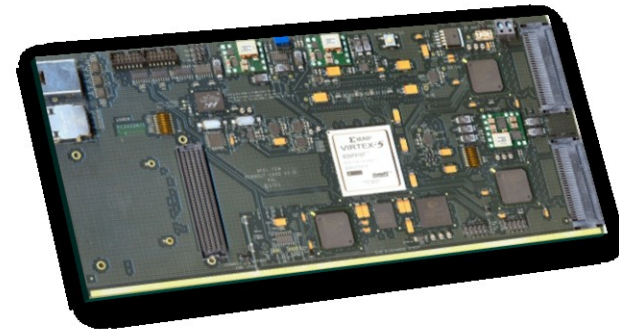
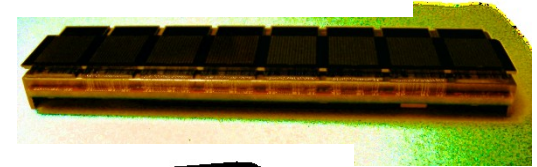
# Programme to date

- Prototype ASIC complete and in test
- Detectors manufactured
- First Detector Tile Modules bonded and awaiting test.
- DAQ card (FEM) manufactured and in test
- Power card manufactured and in test
- Super-Module mechanics and cooling in place ready to populate with Detector Tiles

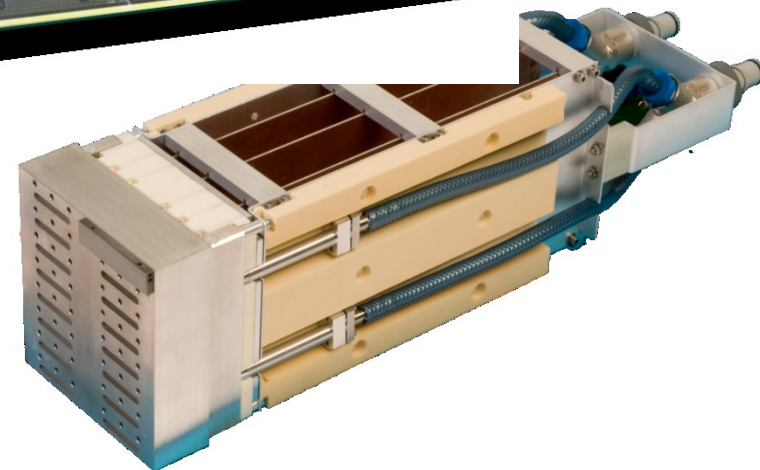


SIC

Detector Tile Module

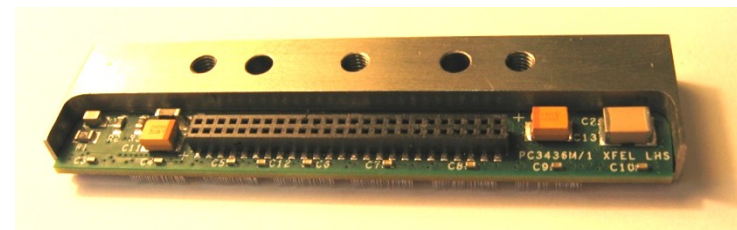
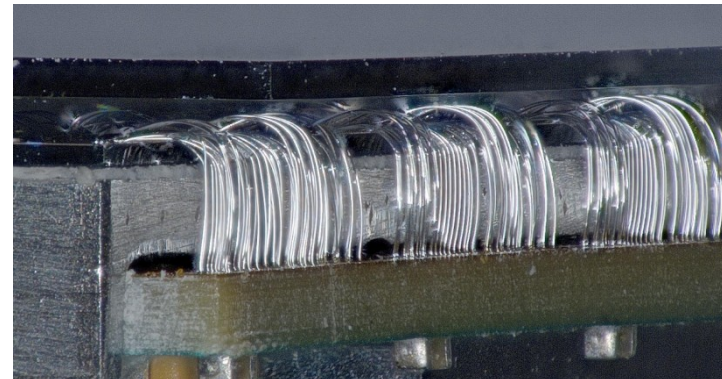
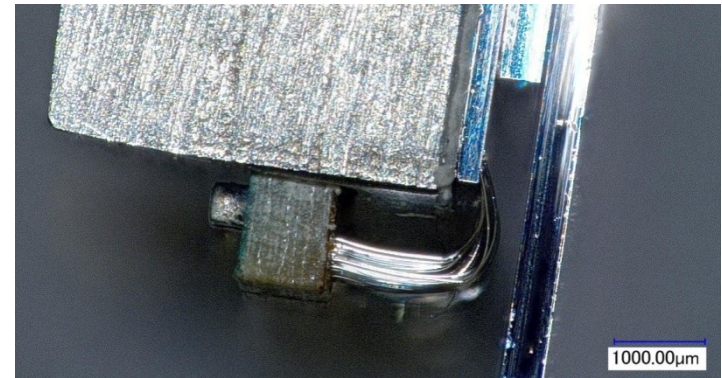
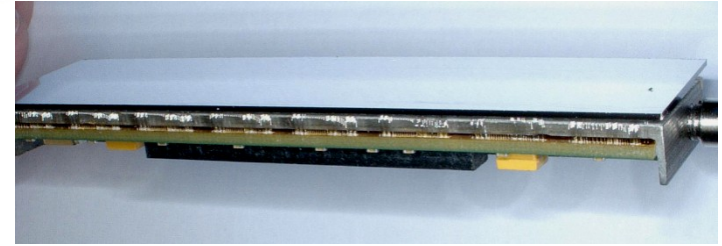
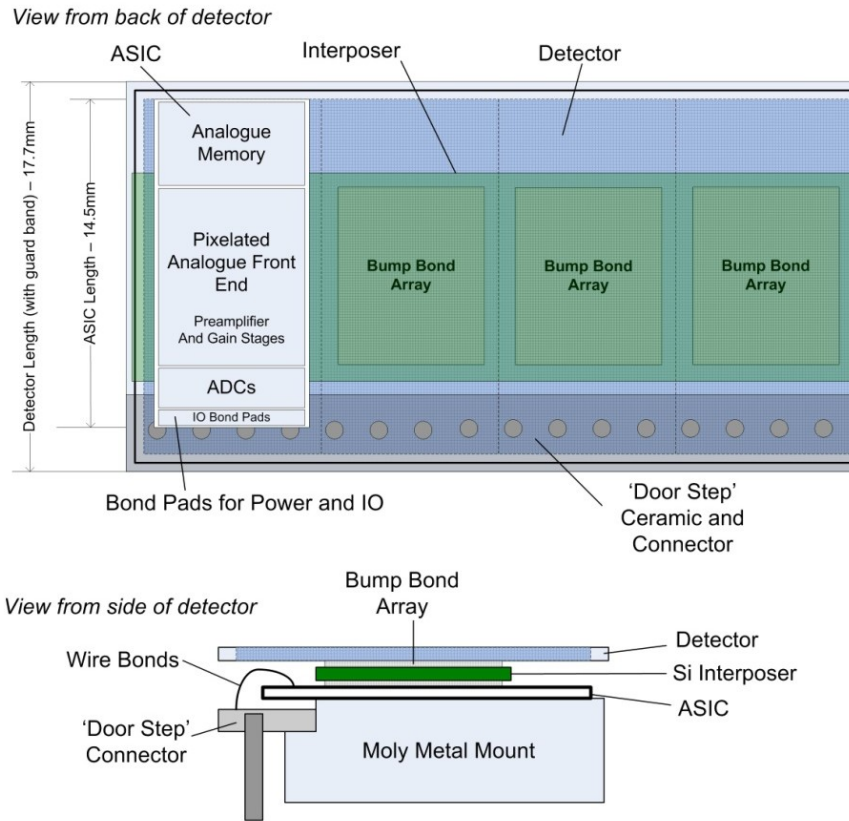


DAQ Card



Super-I

# The Detector Tile



- Detector, Interposer and ASIC
- Wire bonding and Connector PCB hidden behind the footprint of the detector

# Chip Overview

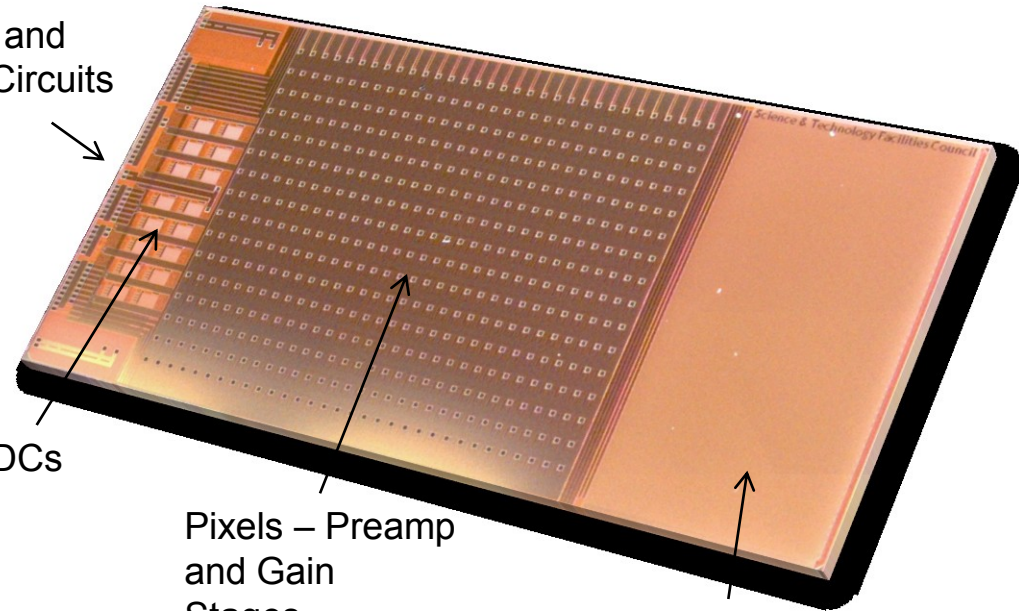
- Pixel
  - Preamp
  - Gain Stages
- Memory
- ADCs
- Control
  - Slow Registers
  - Fast Command Interface

IO Pads and  
Control Circuits

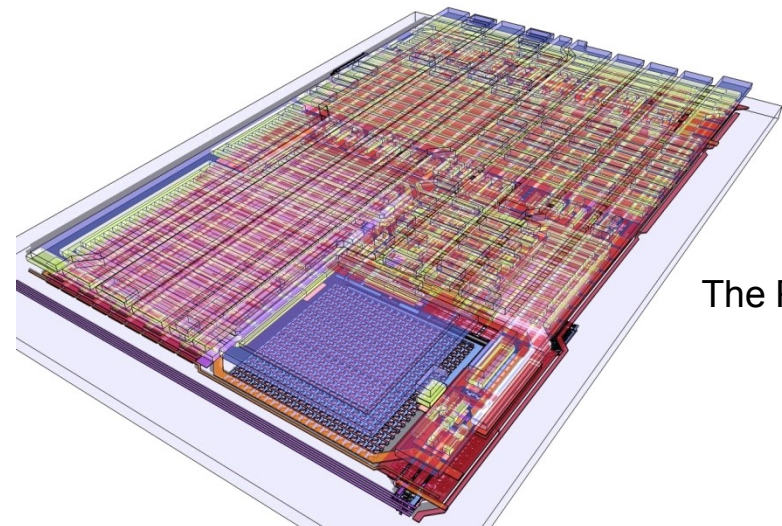
ADCs

Pixels – Preamp  
and Gain  
Stages

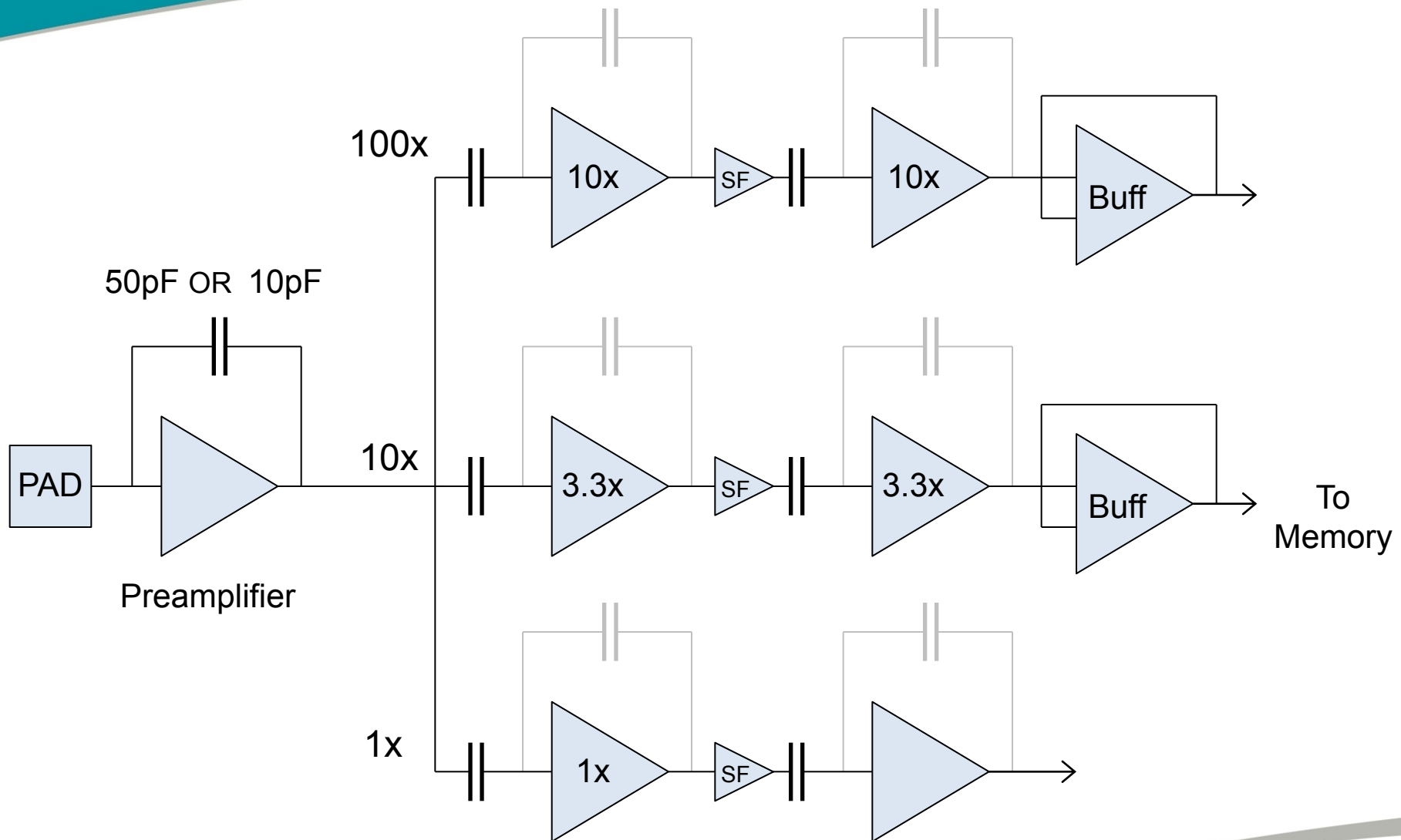
Analogue Memory



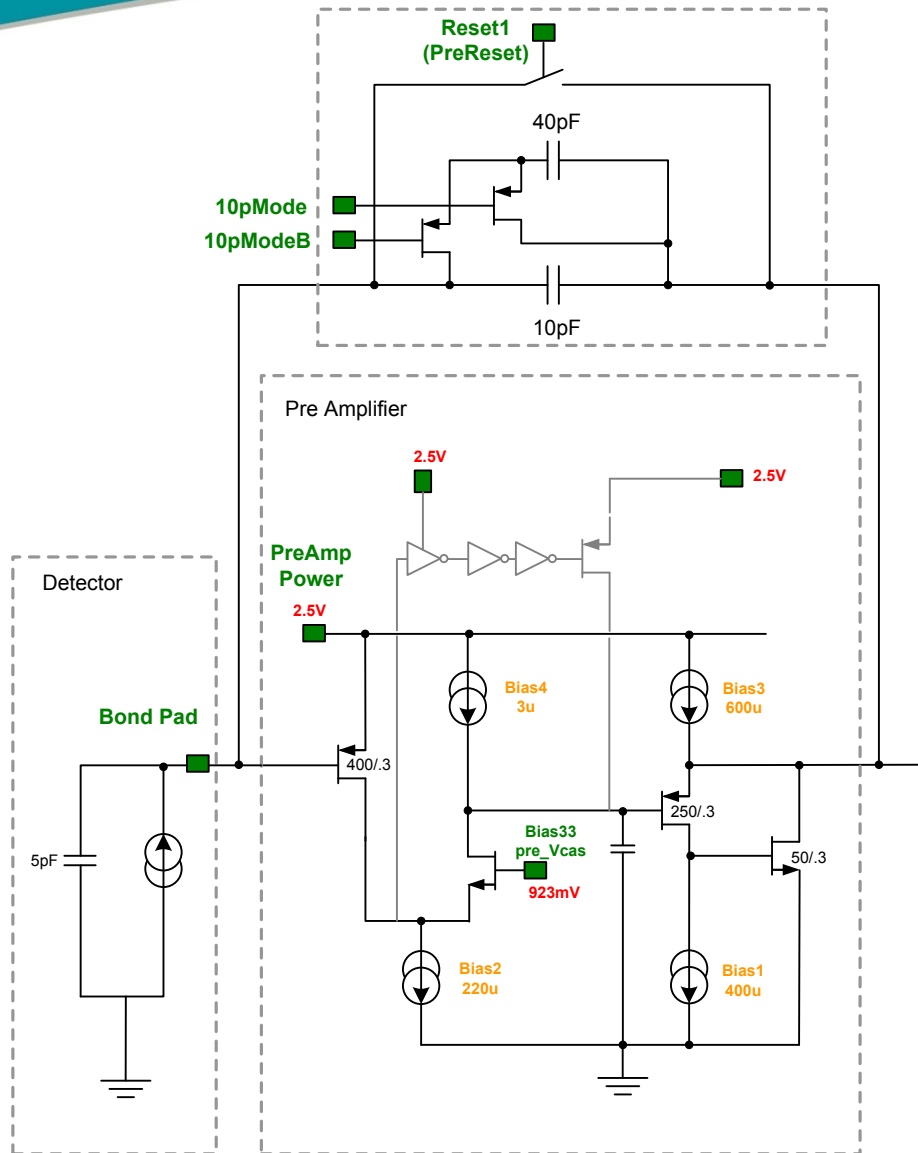
The Pixel



# The Pixel

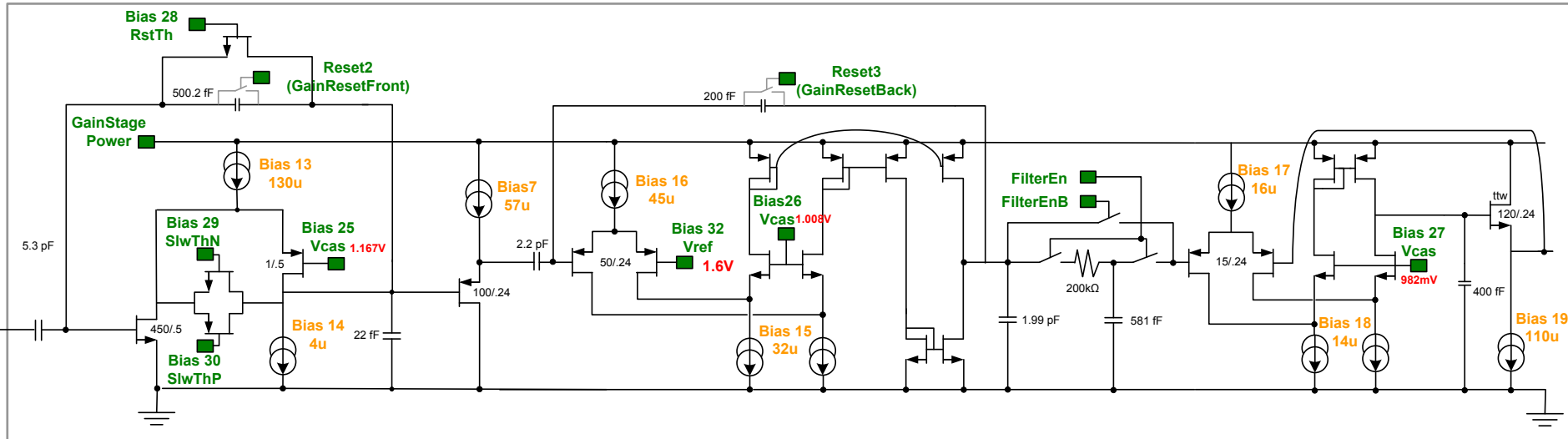


# Preamplifier



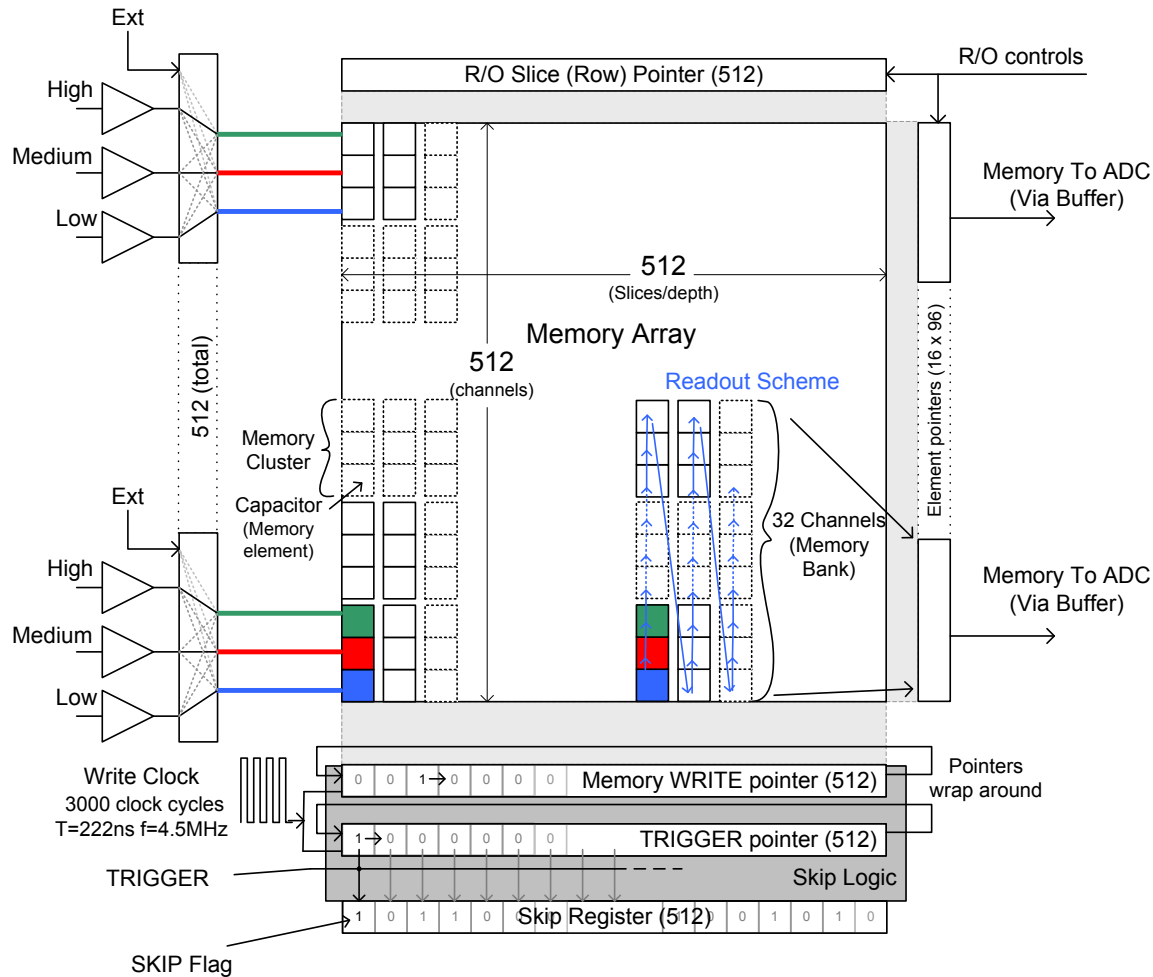
- Optimised for low noise and high dynamic range
- Selectable feedback 50pF (default) or 10pF
- Reset slew compensation circuit to allow 222nsec integration and reset

# Gain Stages – 100x

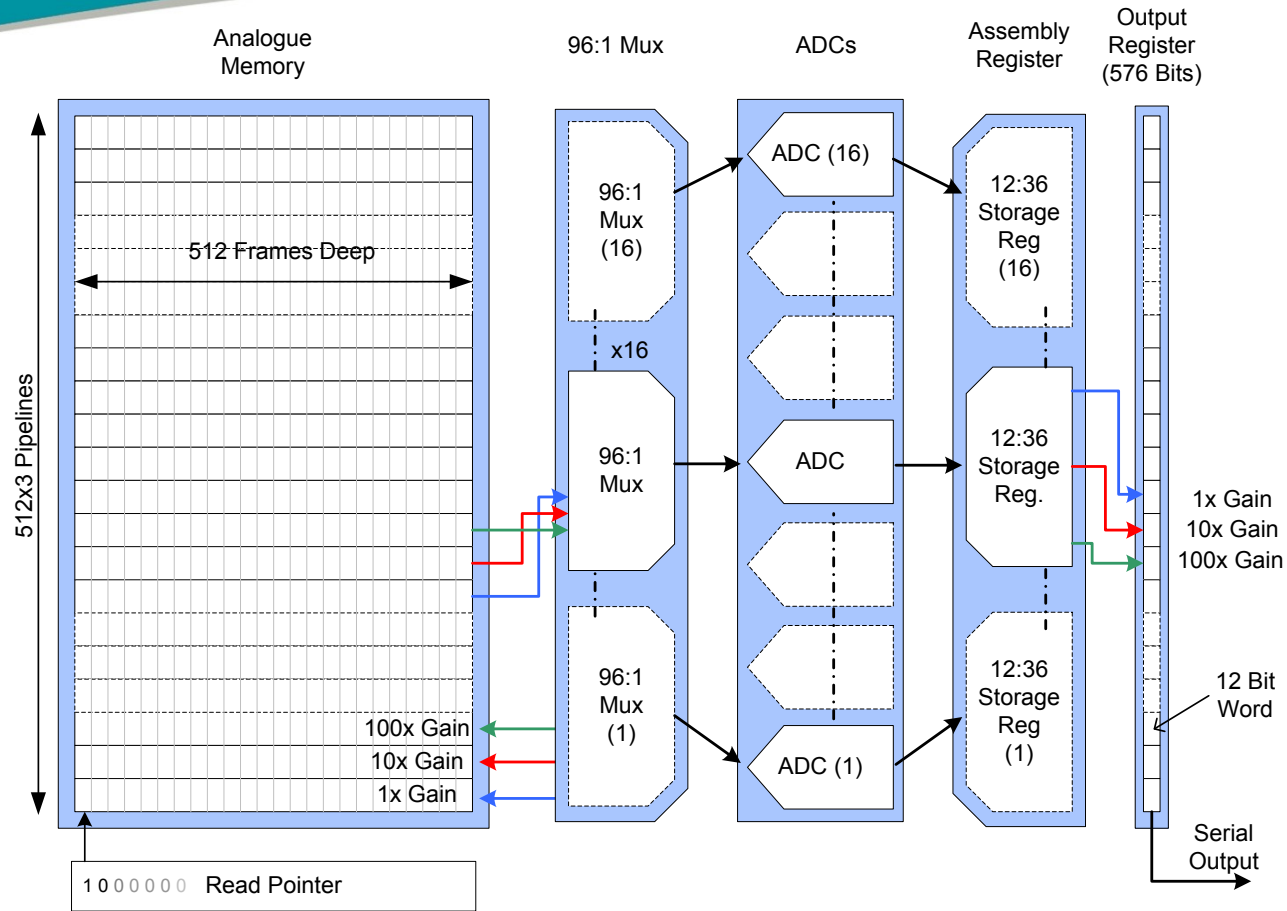


- 100x achieved using **two 10x amplifiers**.
- **Staggered resets** across preamp, and front and back gain amplifiers
- **Recovery from saturation** of the 100x channel achieved with 3 extra transistors to help restore amplifier to correct operating points

# Memory



- 512 Frames, 512x3 Channels
- Storage element, gate capacitance  $\sim 20\text{fF}$
- Source follower readout
- Veto implemented using trigger flag registers to save frames
- Gain Multiplexer allows external voltages to be written to memory



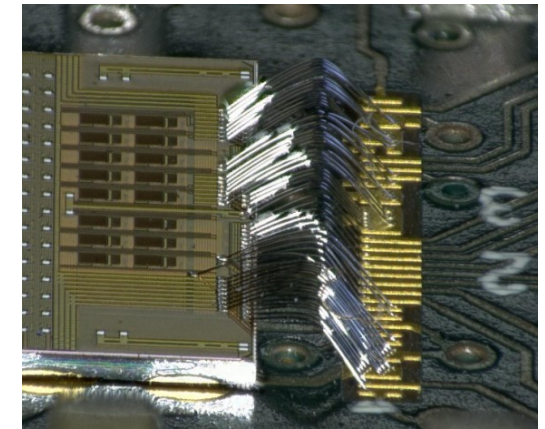
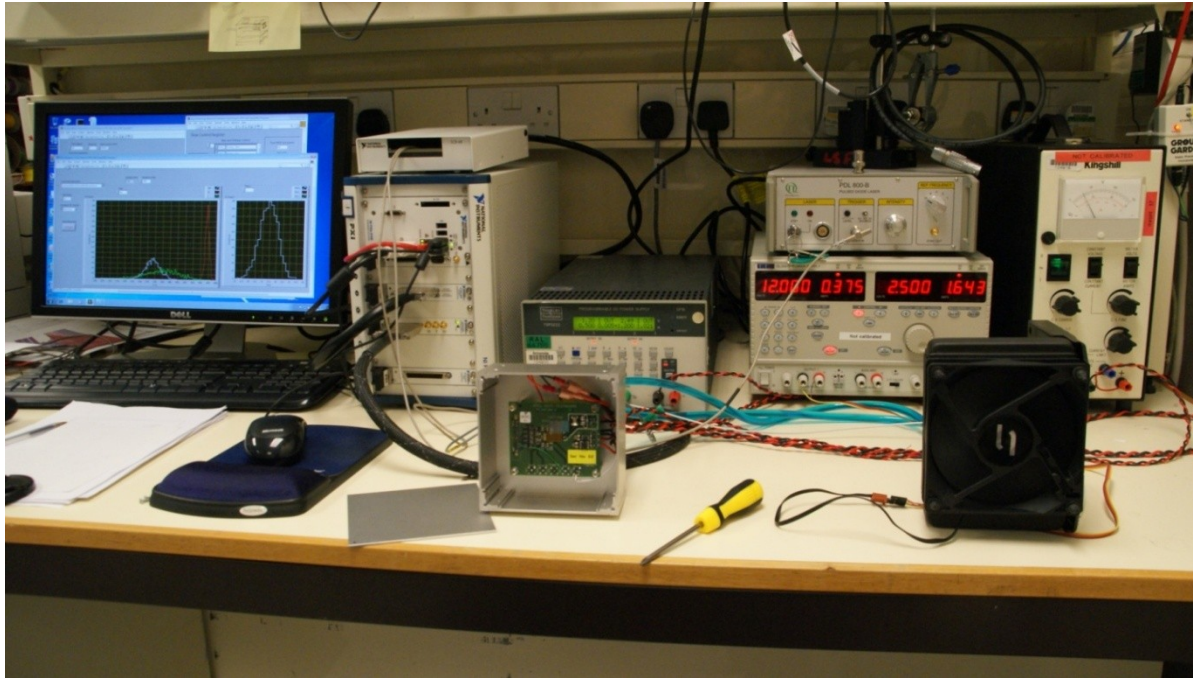
- 16 Successive approximation ADC – 12 Bit
- Storage registers gather outputs from 3 gains for rapid comparison and sparcification on the DAQ board.

- Minimal digital IO
  - 100MHz Master Clock
  - Slow Control Registers programmed once at start up (~3.9 K bits)
  - Command Interface via fast LVDS input (100MHz)
  - LVDS Data Output (100MHz)
- Command decoder and state machine generate control signals. Resets, Pointer etc.

1	0x00	NOP	no operation
2	0x01	STAND_BY	low power mode
3	0x02	POWER_UP	normal power
4	0x03	ON_CHIP_RESET_DISABLE	switch to manual rst
5	0x04	ON_CHIP_RESET_ENABLE	switch to auto rst
6	0x05	RESET_PRE_AMP	manual rst 1
7	0x06	RESET_GAIN_FRONT	manual rst 2
8	0x07	RESET_GAIN_BACK	manual rst 3
9	0x09	TEST_MODE_D	pseudo random no.
10	0x0A	TUNE_MODE	1s and 0s
11	0x0B	CLEAR_SKIP_REGISTER	rst skip reg
12	0x0C	RESET_WRITE_POINTER	rst write pointer
13	0x0D	RESET_TRIGGER_POINTER	rst trigger pointer
14	0x0E	START_WRITE_POINTER	start pointer
15	0x0F	START_TRIGGER_POINTER	start pointer
16	0x10	TRIGGER_FLAG_SET	puts flag in skip reg
17	0x11	READ_OUT_DATA	start memory read
18	0x12	REMOVE_RESET_PRE_AMP	manual rst 1 off
19	0x13	REMOVE_RESET_GAIN_STAGE1	manual rst 2 off
20	0x14	REMOVE_RESET_GAIN_STAGE2	manual rst 3 off
21	0x15	CLOCK_DIV_SEL	change clock div
22	0x16	SELF_TEST_EN	calibrate En
23	0x17	STOP_READ_OUT	end readout cycle
24	0x18	RESET_STATE_MACHINE	return to IDLE state
25	0x5A5A5	SYNC_RESET	sync commands

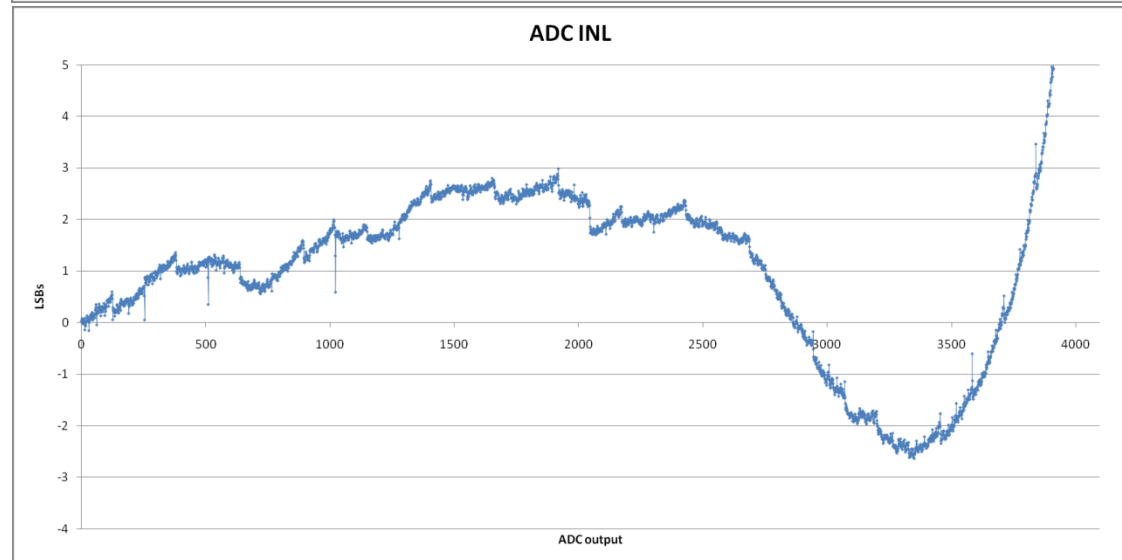
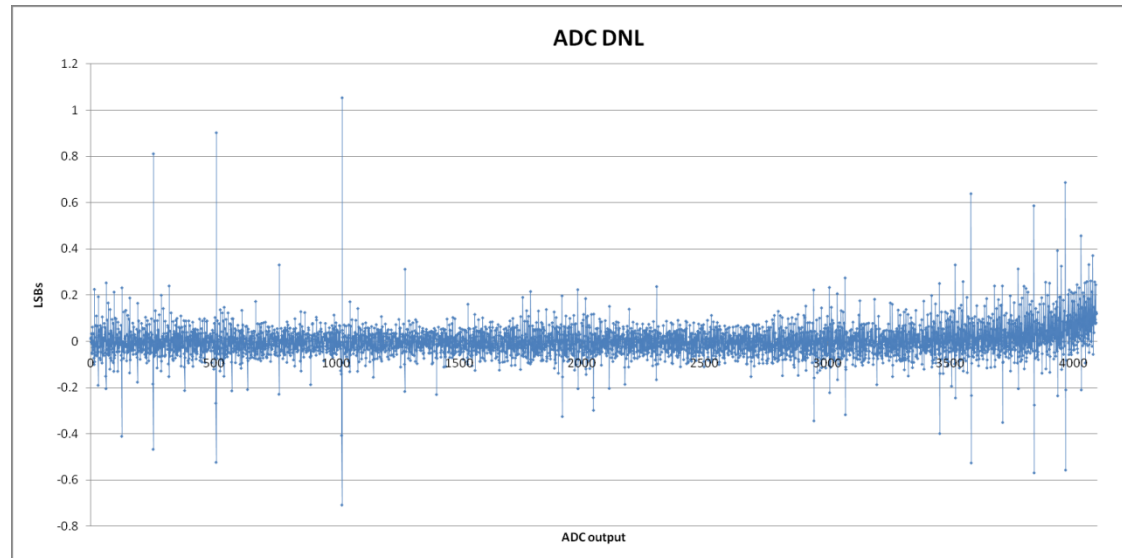
- **512 Channels** per ASIC including preamp and gain stages connected to 500um pixels
- High dynamic range, **1 to  $1 \times 10^5$  photons** per pixel per pulse
- Full range is rec. by **3 parallel gain stages - 1x, 10x and 100x**
- Chip control is driven by a **command word interface**. E.g. 'Trigger' a frame capture.
- **512 frame memory depth** continuously stores all three gains, saving whenever a trigger is received.
- Readout is split between **sixteen 12-bit ADCs**
- Output **data rate 94Mbps** per ASIC (running continuously)
- Designed in **IBM 130nm** technology.

# Test Setup/Results

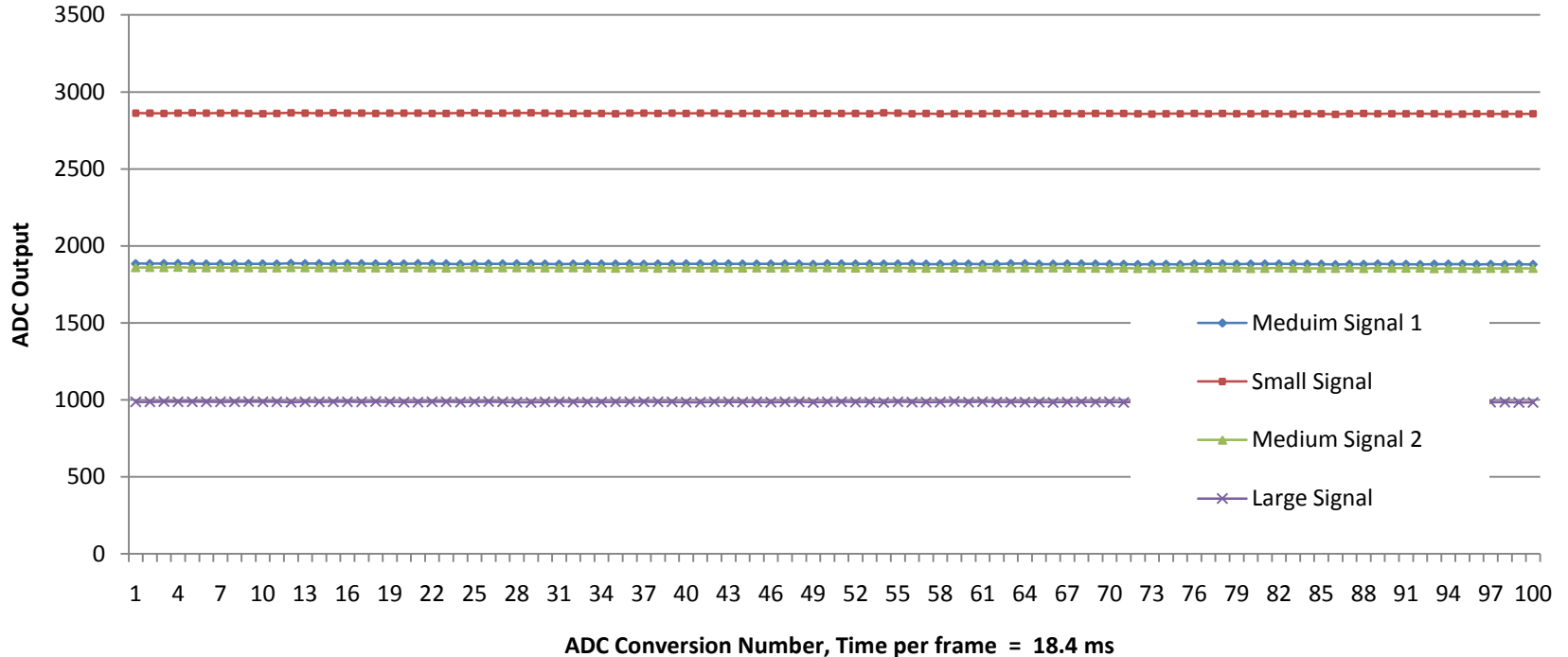


- Single chip test system, independent of full system complications
- National Instruments crate with 100MHz IO cards
- Peltier combined with water cooling ~30 deg C

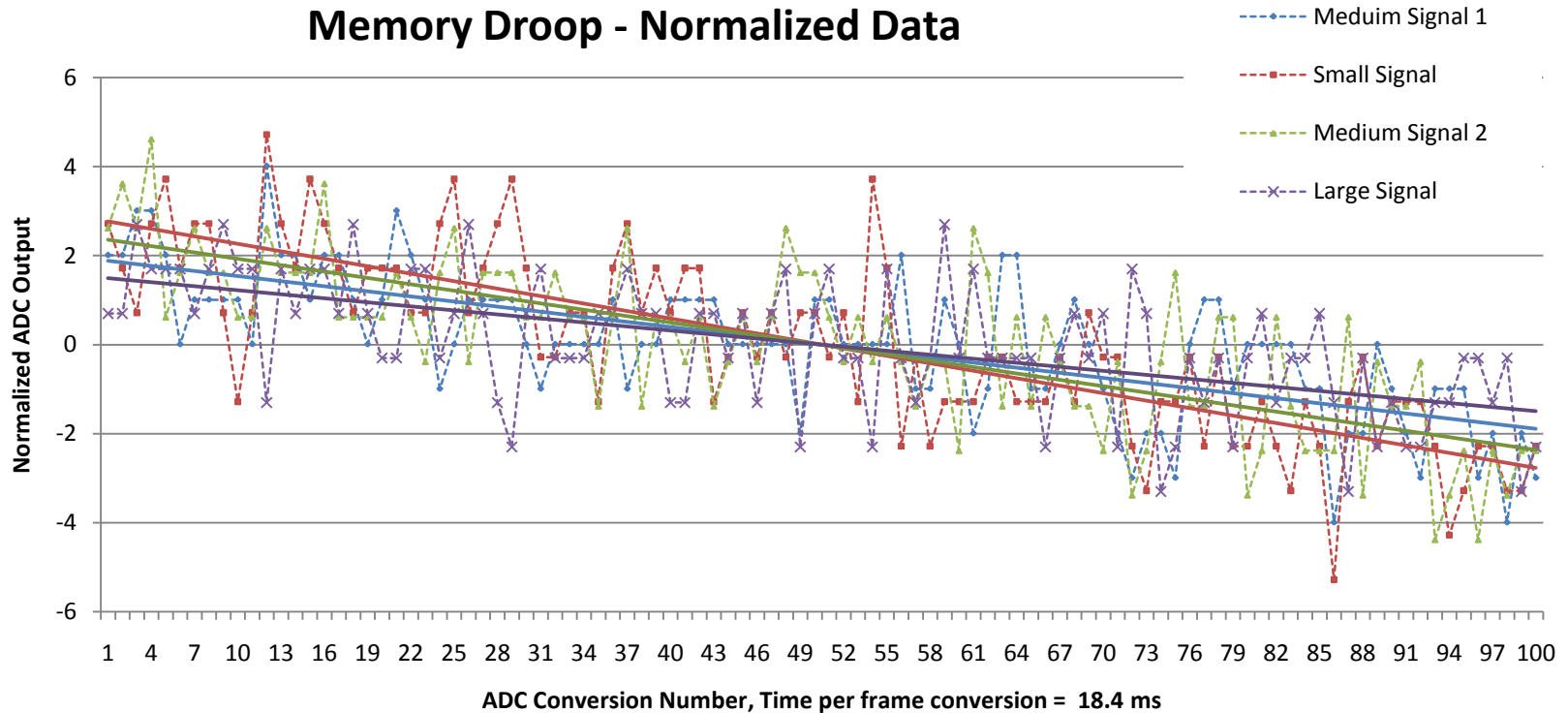
- INL and DNL measured using **16 bit ramp waveform generator** connected **direct to ADC1**
- 3 Million Conversions
- Increased counts seen in the upper ADC range as pad input switches start to cut off at higher voltages.
- DNL
  - Typical = +/- 0.1
  - Max = 1.05
  - Min = -0.71
- INL (excluding range beyond 3500)
  - Max=3
  - Min=-3



## Memory Droop for various Memory Input levels

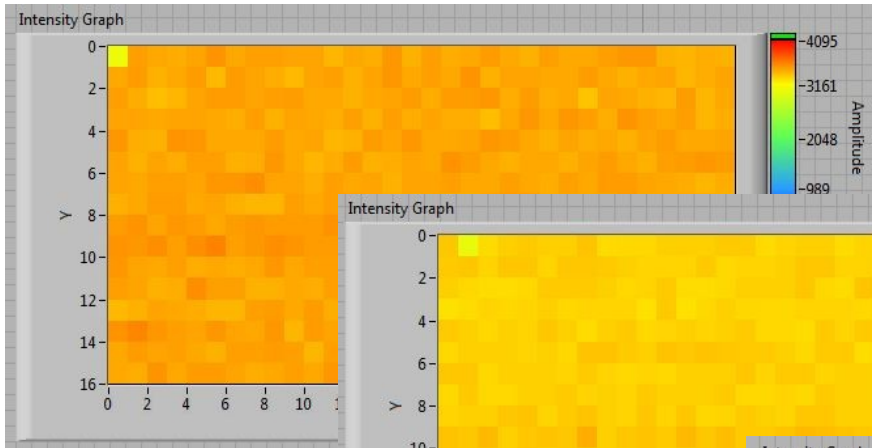


- Memory droop was measured by reading out the same memory frame 100 times. Using a slower master clock speed this readout period is almost 20 times longer than specification. (1.84 sec. cf 0.094 sec.)

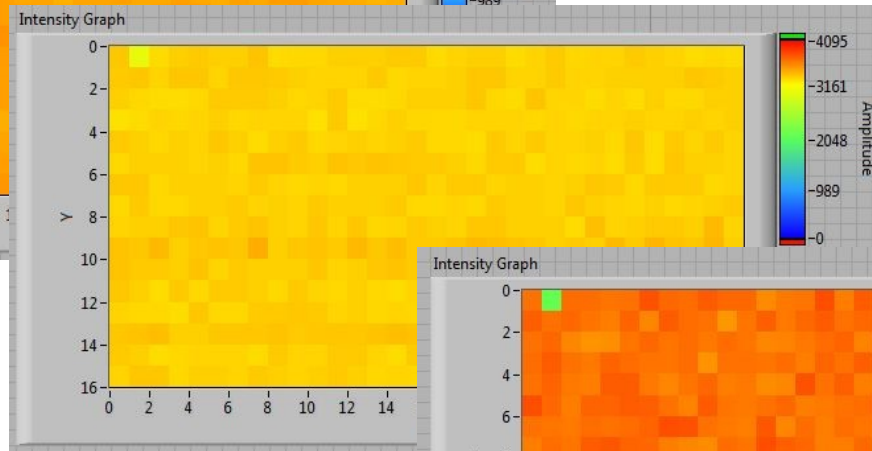


- Memory droop over 1.84s. Between 4-6 ADC bins depending on stored voltage level.

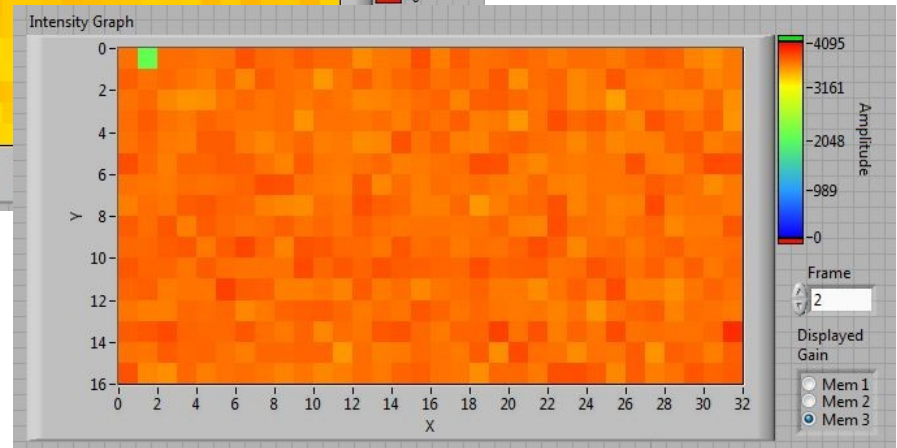
1x Channel



10x Channel



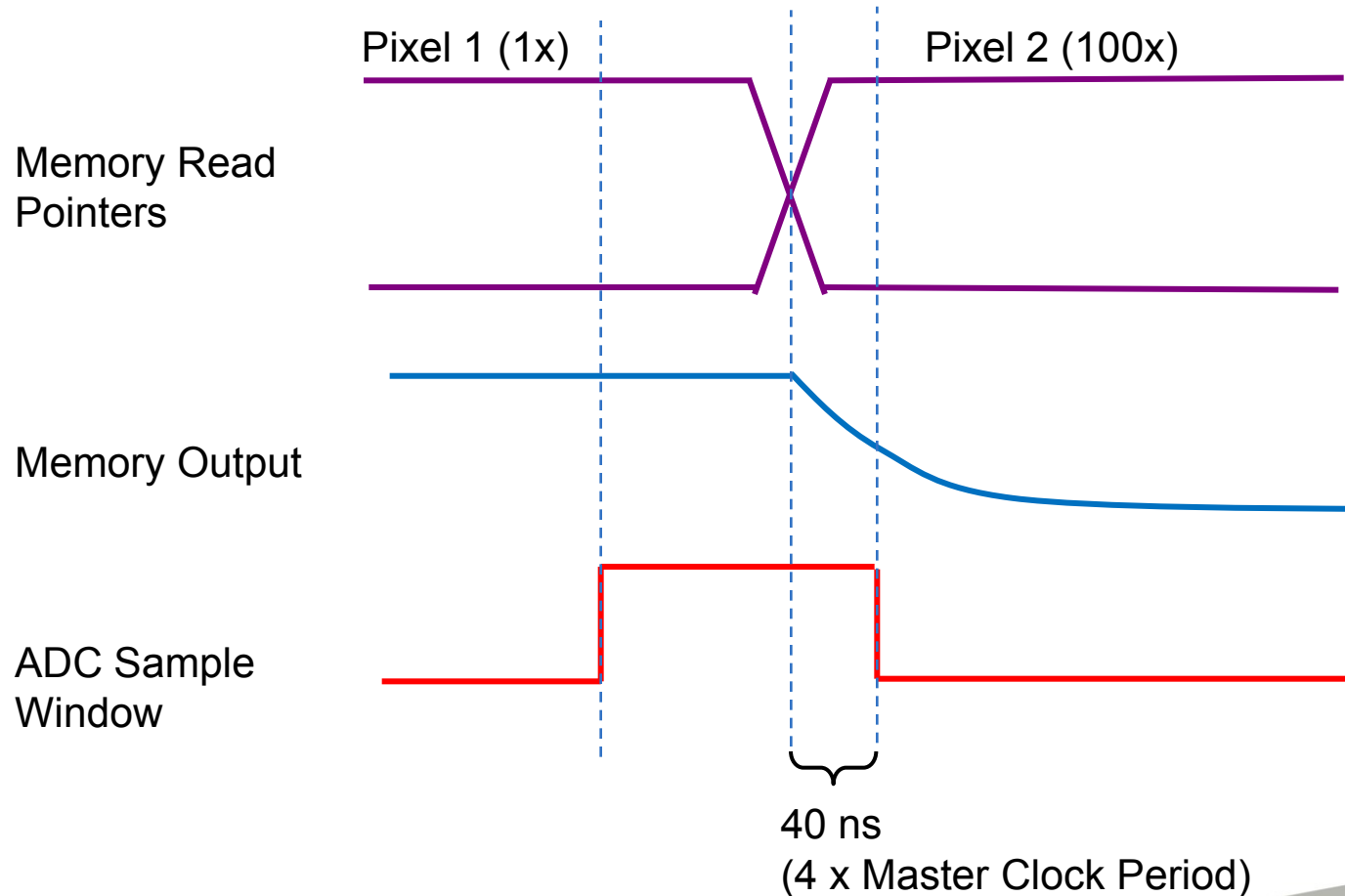
100x Channel



Apparent crosstalk  
between pixels?

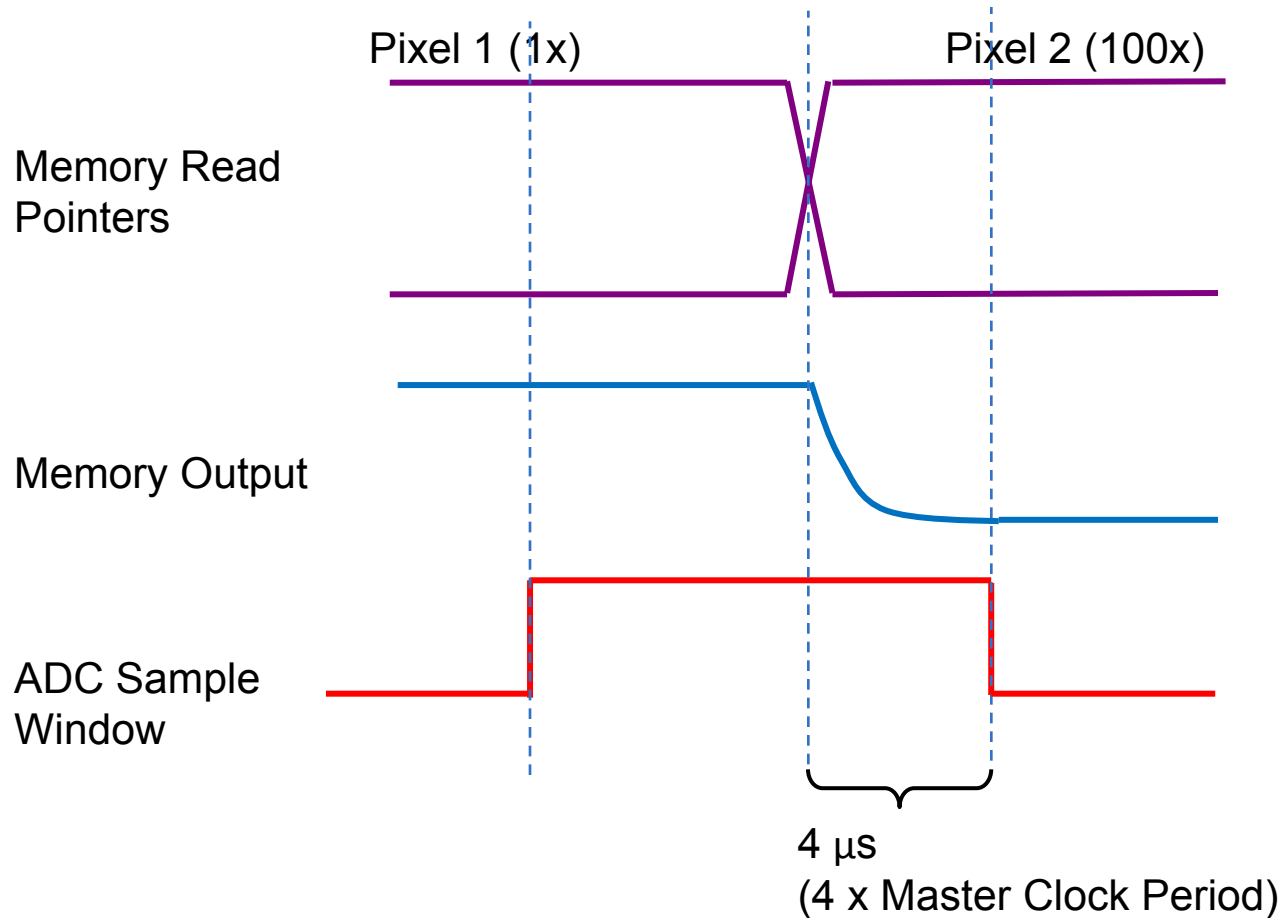
# ADC Sample Issue

Recap: ADC sample window overlaps with memory pointer so sample becomes mixed with next frame.



# ADC Sample Fix

Fix: Write Cycle operates at 100MHz, then Read cycle runs at 1MHz

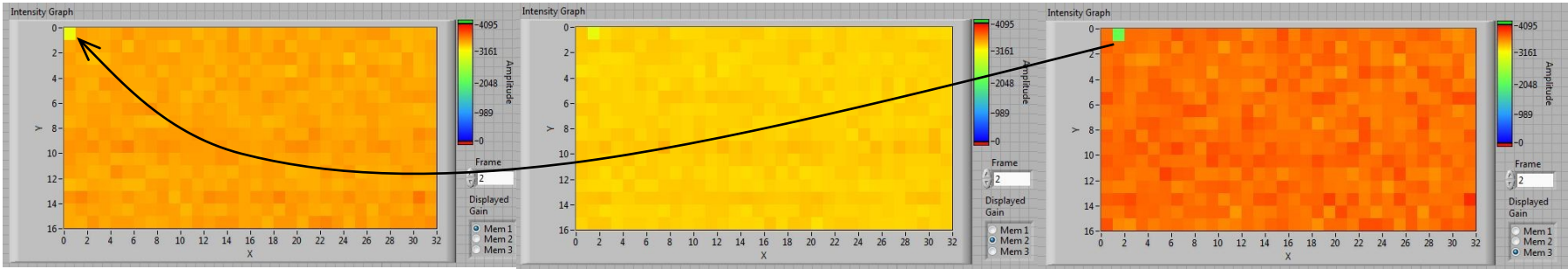


# ADC Sample Fix

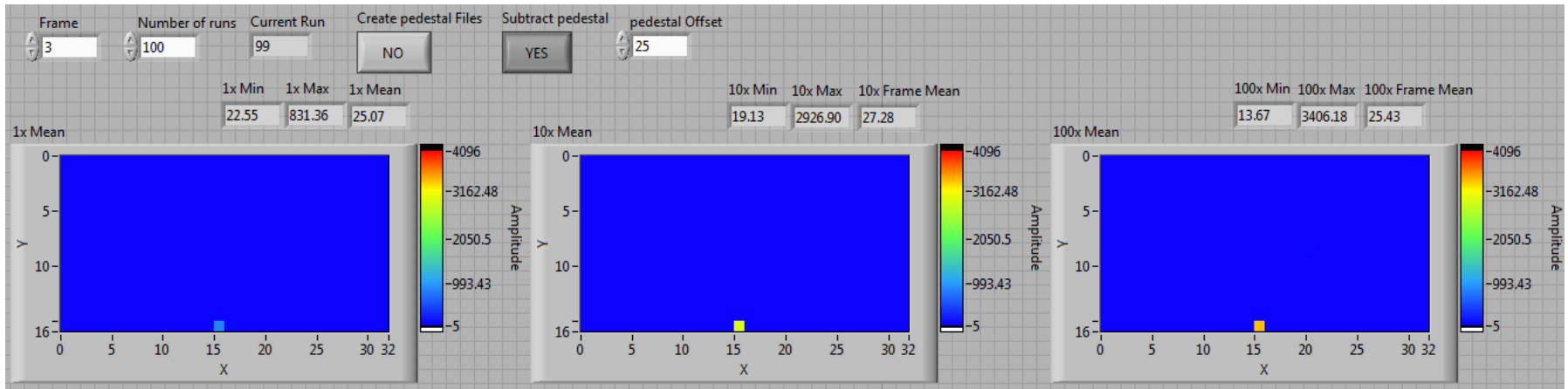
1 x Gain Stage

10 x Gain Stage

100 x Gain Stage

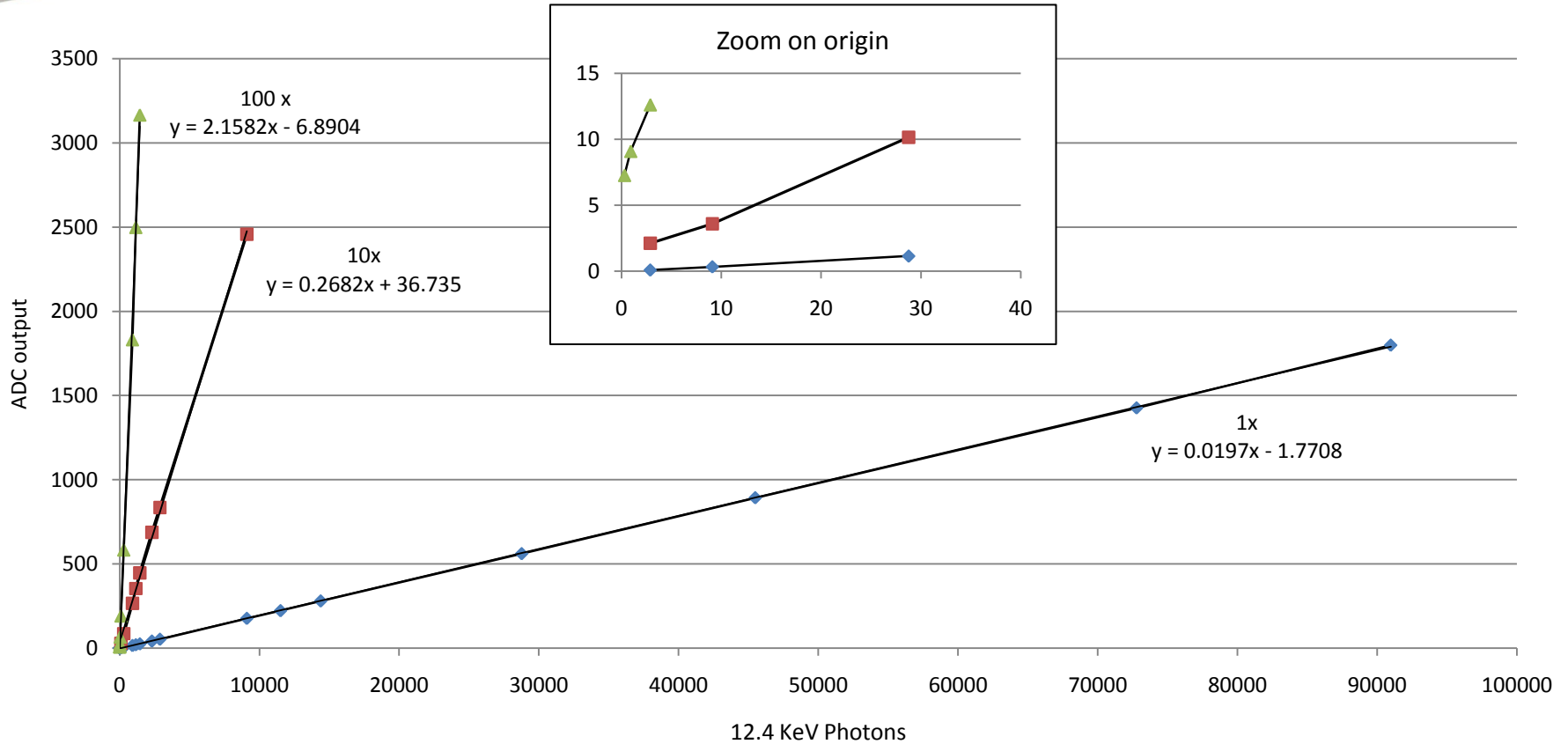


Prior to ADC fix 100x signal seen in previous pixels 1x output



With ADC running slowly cross talk of this type is not seen (note: pedestals subtracted from lower images)

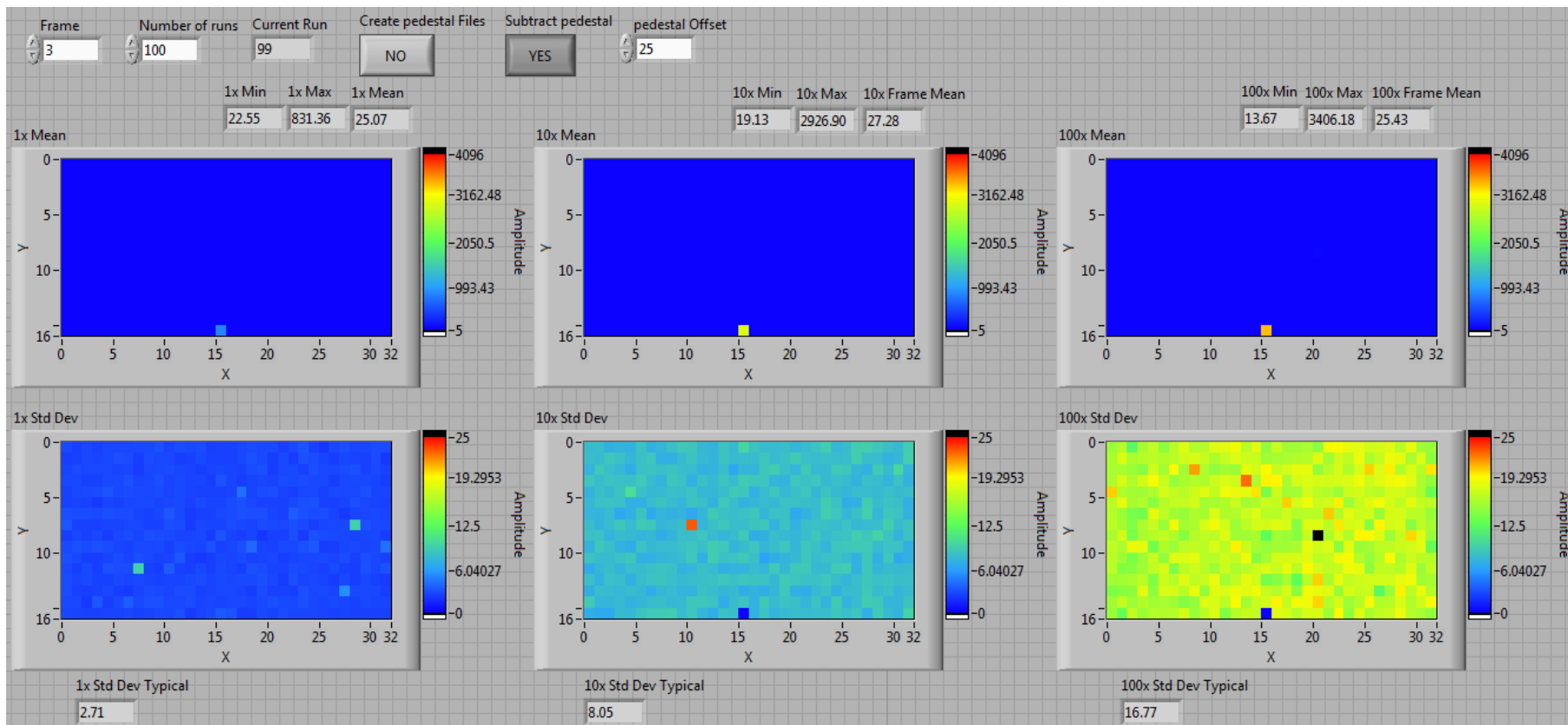
# Calibration



## Photon to ADC output

Gain Channel	1x	10x	100x
Fitted Gain	0.02	0.268	2.16
Effective Gain	1x	13.6x	109.6x

# Noise



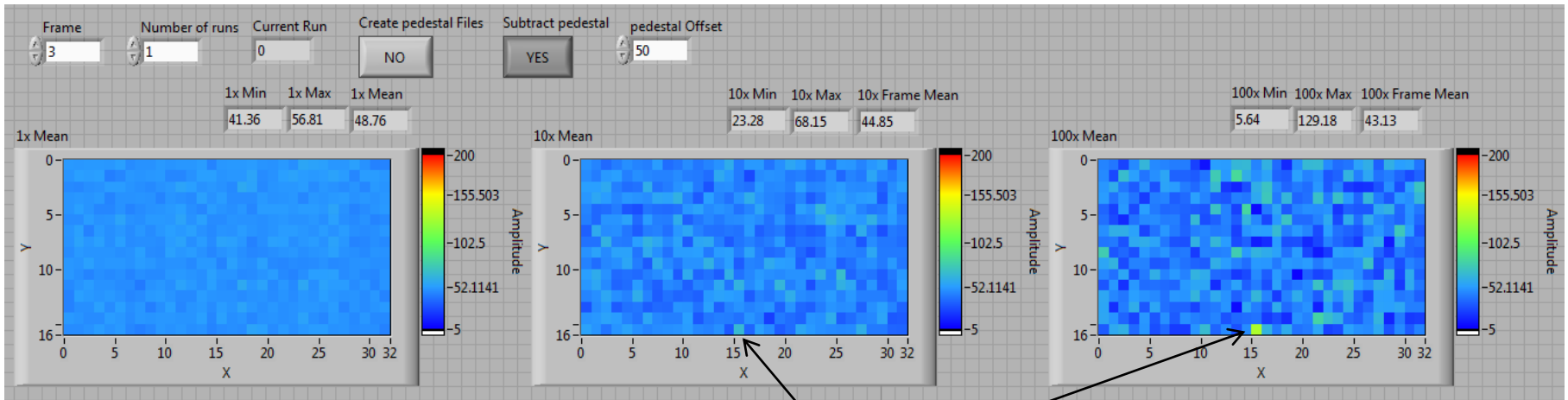
## Noise in LSBs to Noise in Photons

Gain Channel	1x	10x	100x
Typ. Noise (LSB)	2.7	8	16.7
LSB/Photons	0.02	0.268	2.16
<b>Noise in photons (<math>1\sigma</math>)</b>	<b>135</b>	<b>30</b>	<b>7.7</b>

# Investigation of Noise

## Noise in LSBs to Noise in Photons

Gain Channel	1x	10x	100x
<b>Noise in photons (<math>1\sigma</math>)</b>	<b>135</b>	<b>30</b>	<b>7.7</b>

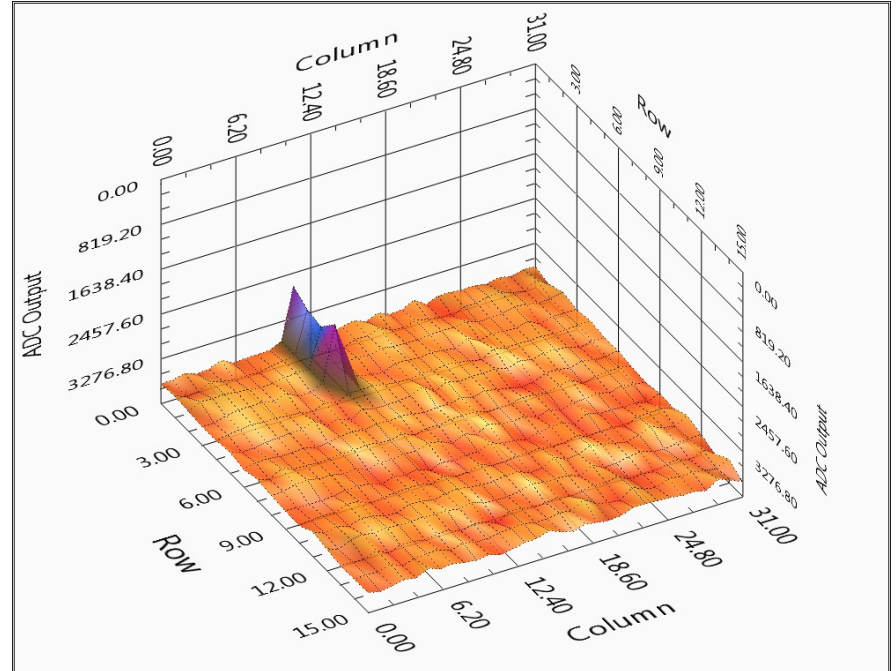


Signal equivalent to **28.7 Photons (12.4KeV)**

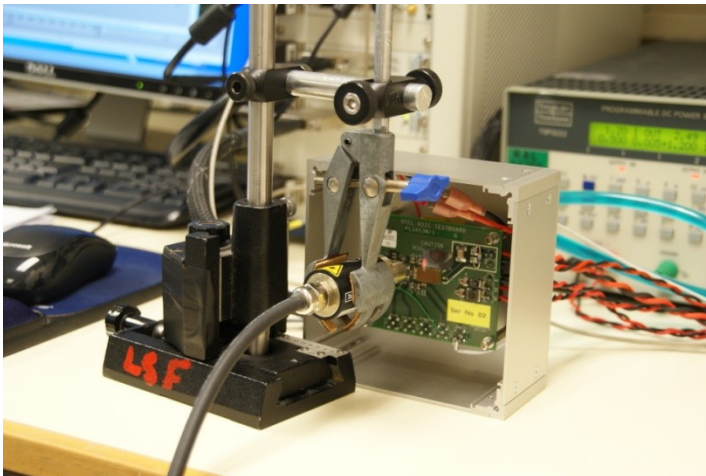
These frames have had pedestals subtracted so noise in the image is genuine.

Noise roughly a factor of 2 larger than simulation. Where is this from? Models, Power supplies, Reset Injection.

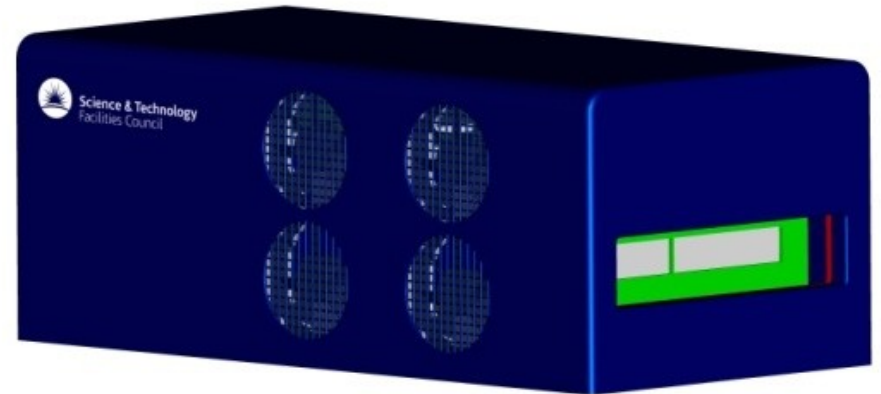
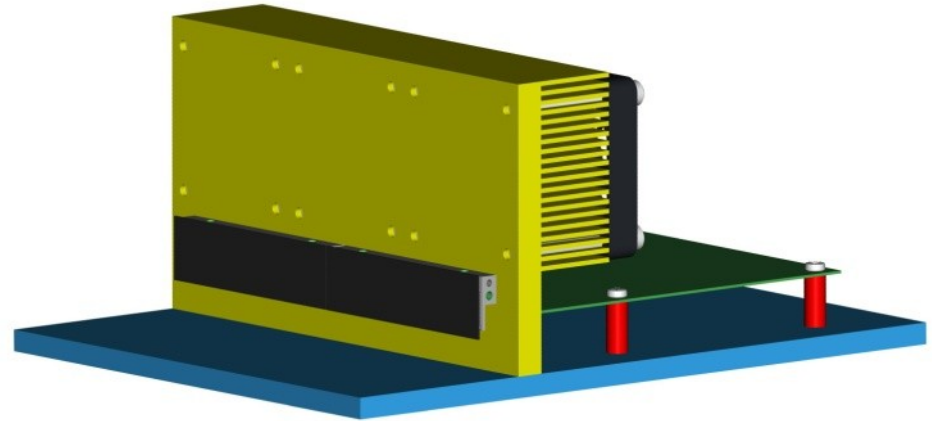
# Laser Test



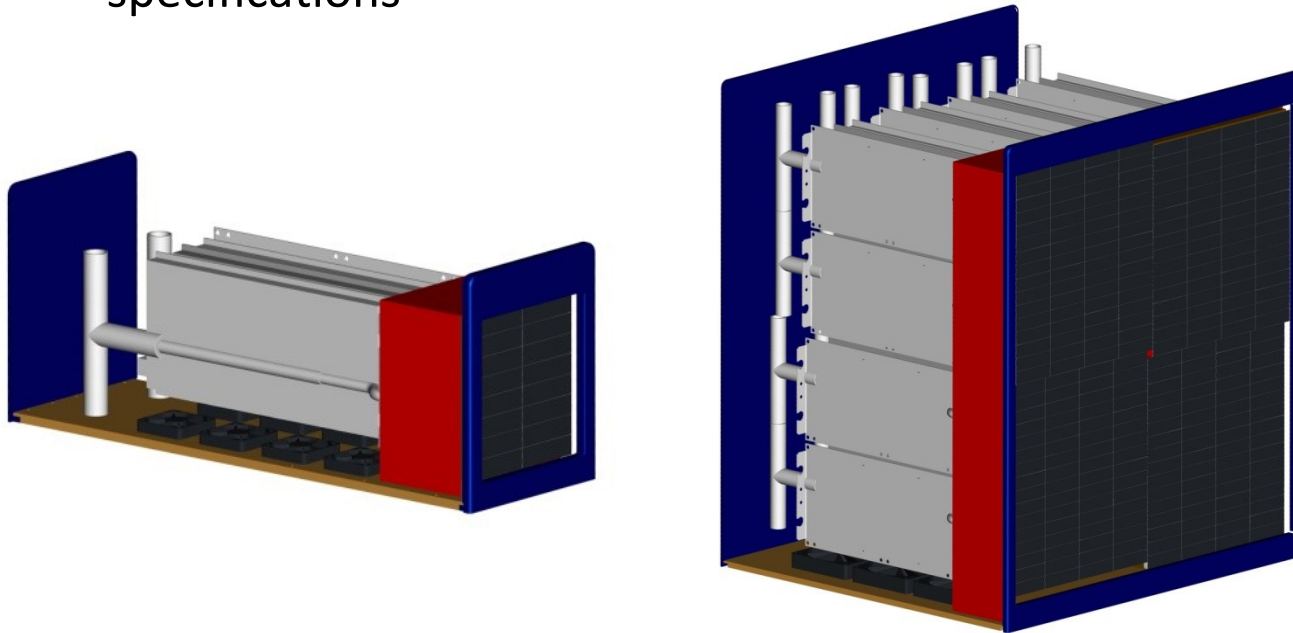
- Pico second laser used in single shot mode to deposit charge in the detector
- 30V Detector Bias



- ASIC Test
  - Noise investigation
  - Saturation Recovery
  - Signal in many pixels
- Module Test
  - Functionality
  - Radiation Hardness
- Reiterate ASIC with optimised dynamic range, Fix ADC sample timing.



- Construction of the first megapixel
- Finalising design with beam line scientists
  - Beam Hole requirements
  - Feedback on dynamic range requirements and other operating specifications



- The LPD system, from Detector Module to Megapixel
- Most system components manufactured and in test ready to construct super-modules
- ASIC functional and first tests show performance is in the right direction
- Future – Test of modules and development to get early systems to beam scientists.



# Acknowledgements

- Project
  - Marcus French
- ASIC
  - Matthew Hart
  - Mark Prydderch
  - Davide Braga
  - Michelle Key-Charriere
- Sensors
  - Paul Seller
- DAQ
  - John Coughlan and Rob Halsall
- Mechanics, Cooling, Power
  - Stephan Burge
- Software
  - Tim Nicholls

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