Monolithic sensors in high-voltage deep-submicron technology

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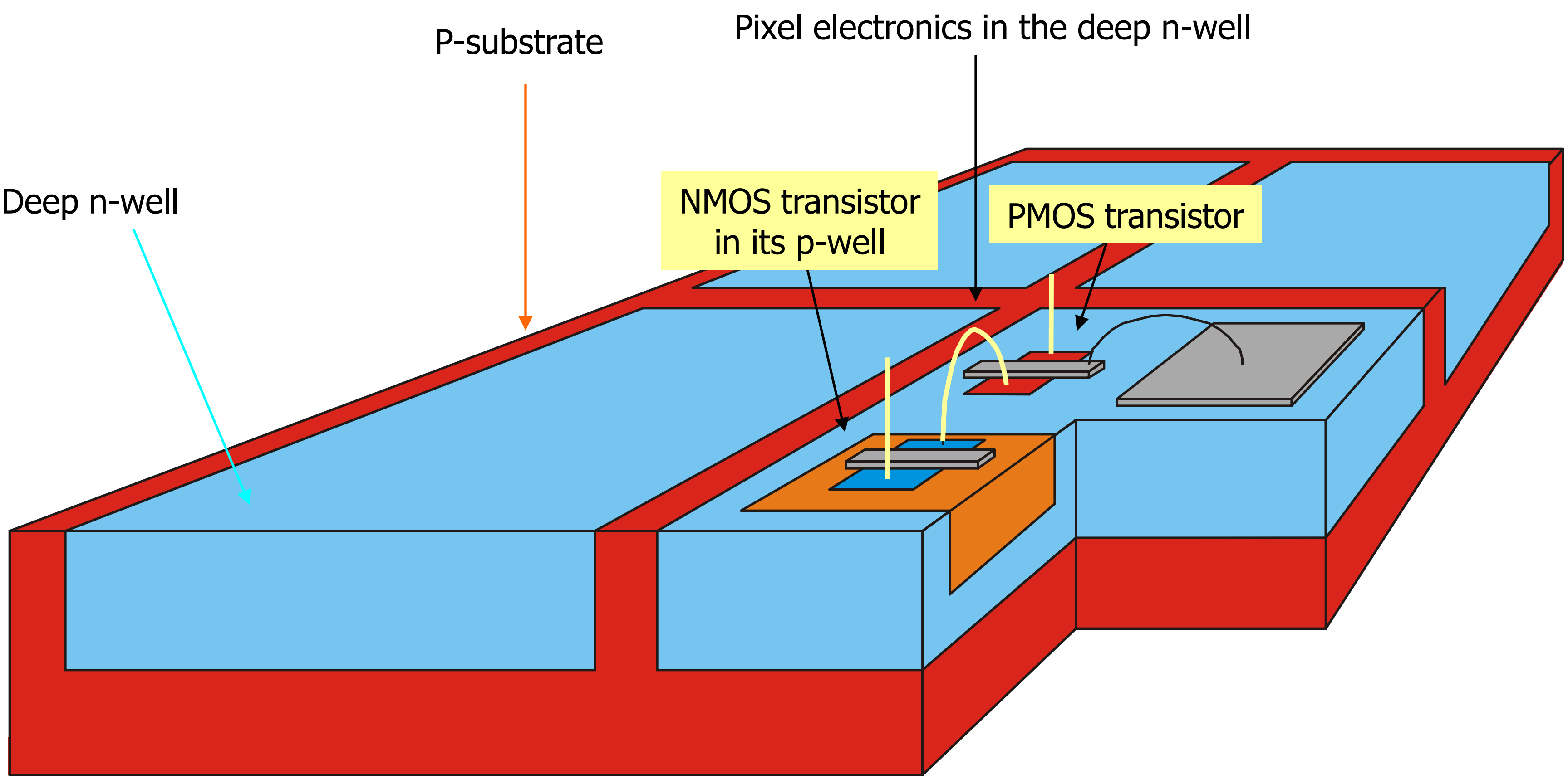
- Introduction to pixel sensors in high voltage CMOS technology
- Operation principle, advantages and disadvantages
- Summary of the project results
- Pixel types
- 1) Particle sensitive pixels with complex CMOS electronics
  - Test chip in 180nm technology
- 2) Integrating pixels with simple “4T” electronics
  - 4PMOST source follower pixels
  - 4PMOST pixels with voltage amplification
  - >4T CDS pixels
- Test beam and lab measurements

Pixel detector in HV CMOS technology

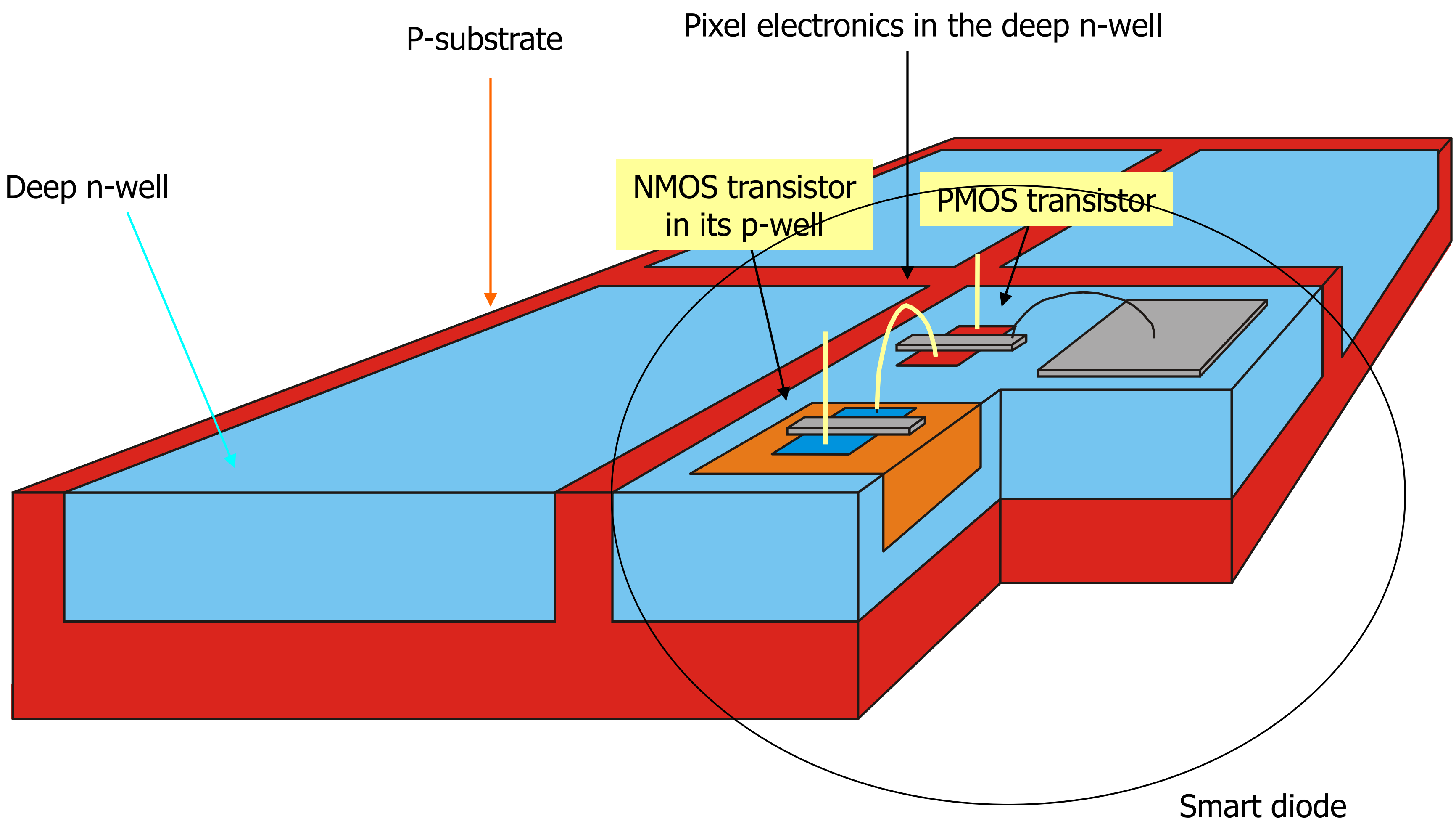
- Monolithic pixel sensor
- 100% fill-factor
- In-pixel CMOS signal processing
- Good timing properties (theoretically 40 ps signal collection time)
- Radiation hard (tested to 50 MRad (x-rays) and 10^{15} n_{eq} (protons))
- Not expensive (monolithic sensor, no bumping, standard technology used)
- 350nm technology: 8 inch wafer run: 90k€ (350nm)
- 180nm technology: 120k€ and 1.5k€/wafer (1 wafer ~ 200 cm^2)
- Allows thinning

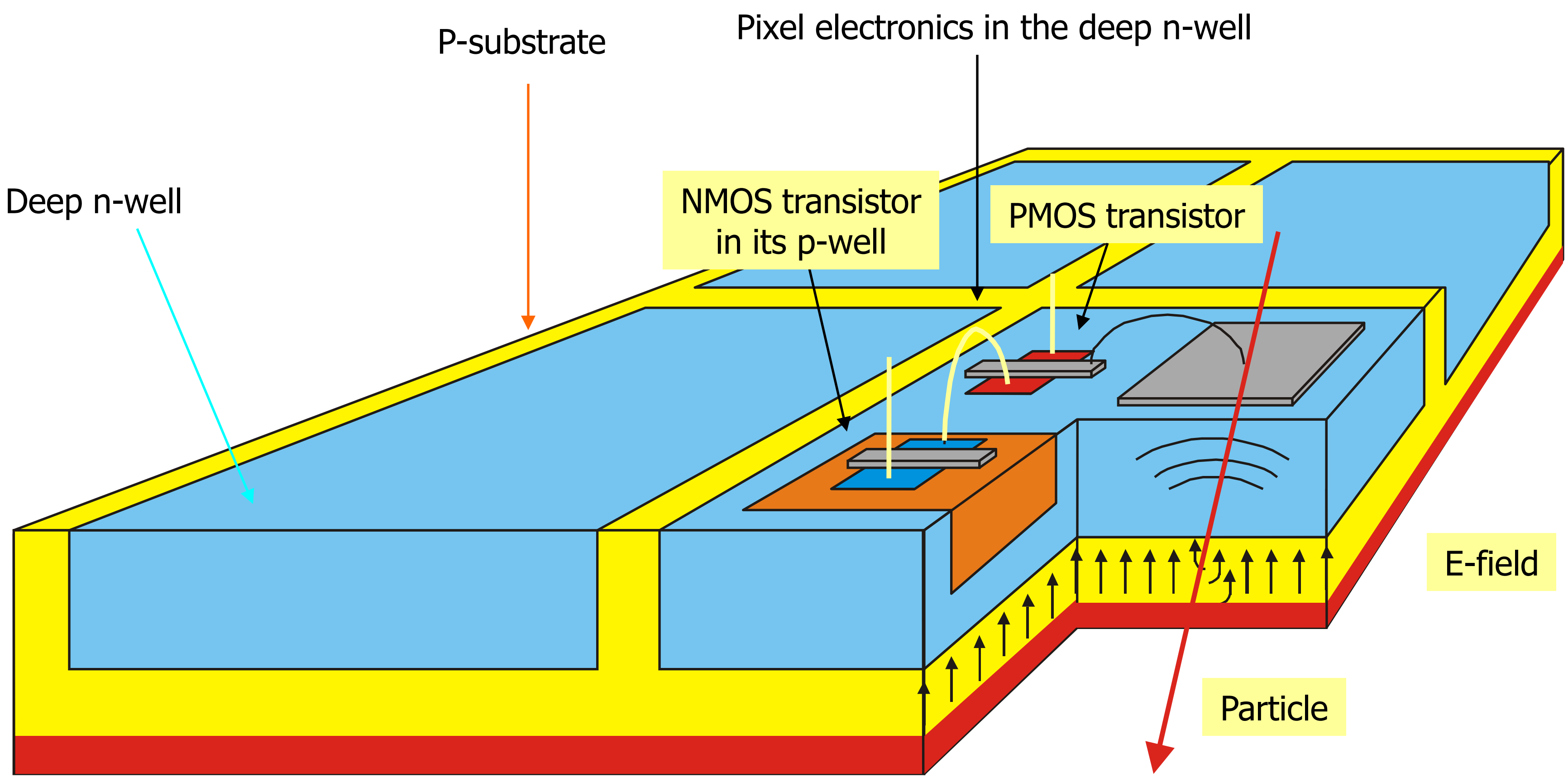
Detector structure

- The sensor is based on the “deep” n-well in a p-substrate
- Main properties:
- 1) Charge collection is based on drift
- 2) **CMOS** signal processing electronics



The CMOS signal processing electronics are placed inside the deep-n-well. PMOS are placed **directly inside n-well**, NMOS transistors are situated in their **p-wells** that are embedded in the n-well as well.


P-substrate
Pixel electronics in the deep n-well
Deep n-well
NMOS transistor in its p-well
PMOS transistor
Smart diode


P-substrate
Pixel electronics in the deep n-well
Deep n-well
NMOS transistor in its p-well
PMOS transistor
E-field
Particle

SDA in high voltage CMOS technology

- Although this structure can be implemented in any CMOS technology (see 65nm pixel), the best results are achieved when a standard *high voltage* CMOS technology with twin well is used.
- A lowly-doped deep n-well can be then used. Such an n-well can be reversely biased with a high voltage.
- In the process we used, we expect a depleted area thickness of 14 µm (20Ωcm substrate resistance -> acceptor density ~ 10^{15} cm^{-3})
- We measure a MIP signal of ~ 2000e, ~ 50% probably originates from undepleted bulk.
- The charge generated by ionizing particles in the depleted area is collected by drift. Due to high electric field and small drift path, charge collection is very fast. We estimate ~ 40ps.
- Due to drift based charge collection we have high radiation tolerance

Strong points

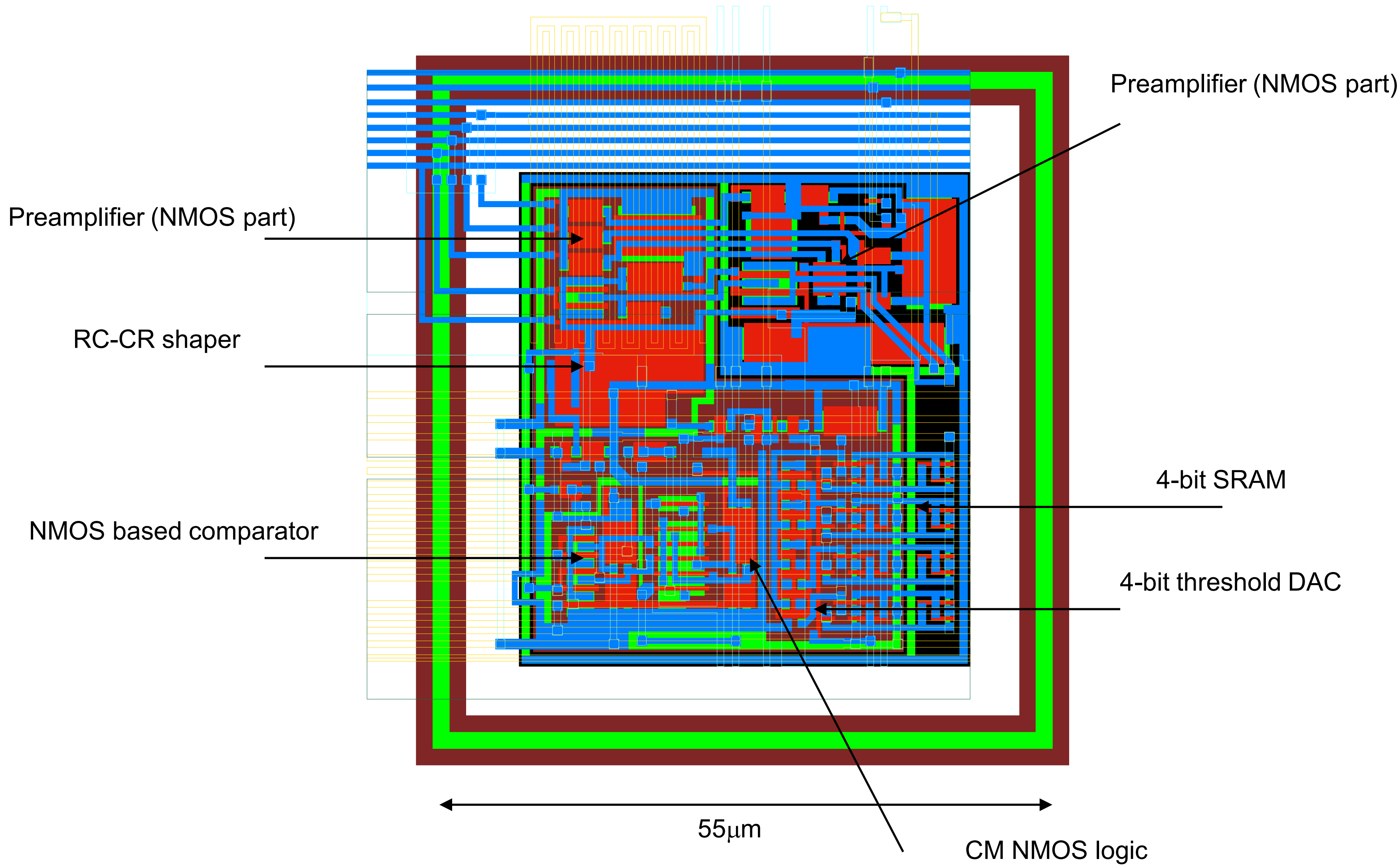
- 1) Monolithic sensor
- 2) CMOS in-pixel electronics
- 3) Fast signal collection
  - Theoretically 40ps
- 4) Thinning possible
  - Since the charge **collection is limited to the chip surface**, the **sensors can be thinned**
- 5) Price and technology availability
  - Standard technology without any adjustment is used
  - Many industry relevant applications of HV CMOS technologies assure their long tern availability
  - 350nm technology: 8 inch wafer run: 90k€ (350nm)
  - 180nm technology: 120k€ and 1.5k€/wafer (1 wafer ~ 200 cm^2)
- 6) High tolerance to non-ionizing radiation damage
  - High drift speed
  - Short drift path
- 7) High tolerance to ionizing radiation
  - Deep submicron technology
  - Radiation tolerant design can be used
  - PMOS transistors, that are more tolerant to radiation, can be used (in contrast to MAPS with high-resistance substrate)

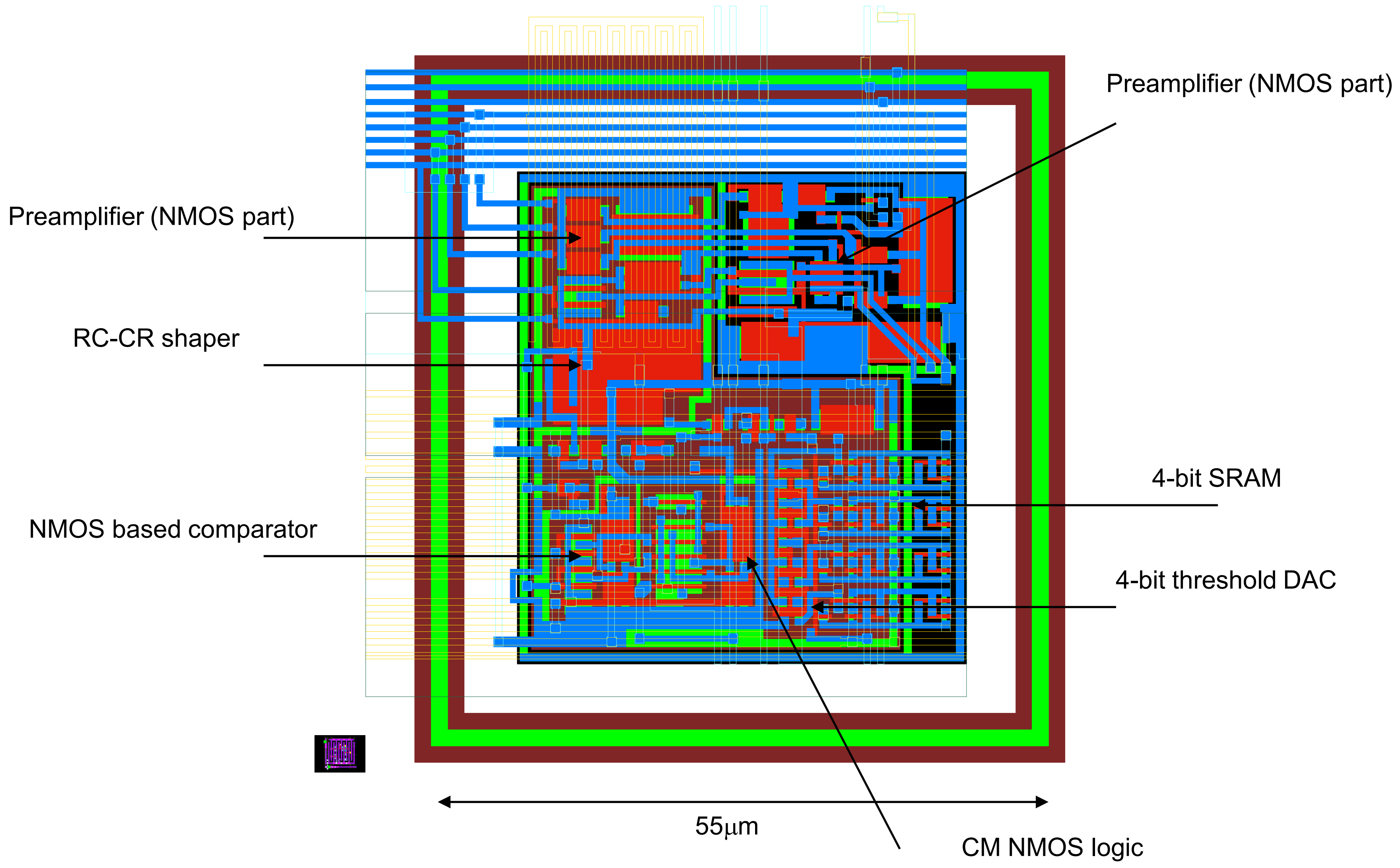
Drawbacks

- 1) Capacitive feedback
  - We can implement the majority of important pixel circuits in CMOS, like the charge sensitive amplifier, shaper, tune DAC, SRAM but…
  - "Digitally active" CMOS logic gates in pixels should be avoided
  - Possibility 1: Current mode logic can be used instead CMOS (drawback – current consumption ~ 1 μA / digital gate)
  - Possibility 2: Separate digital and analog circuits (drawback – a few per cent of inactive area at the chip edge)
- 2) Relatively large size of the collecting electrode
  - Typical values for the total n-well capacitance are
  - 10fF - small 21x21 μm^2 pixels and simple pixel electronics (already tested)
  - 200fF 55x55 μm^2 CMOS pixels (already tested)
  - 700fF 80x400 μm^2 CMOS pixels (proposed long pixels for SLHC)
- 3) Lower signals than in the case of fully depleted sensors
  - The signals do not decrease significantly after irradiation to 10^{15} n_{eq} cm^2

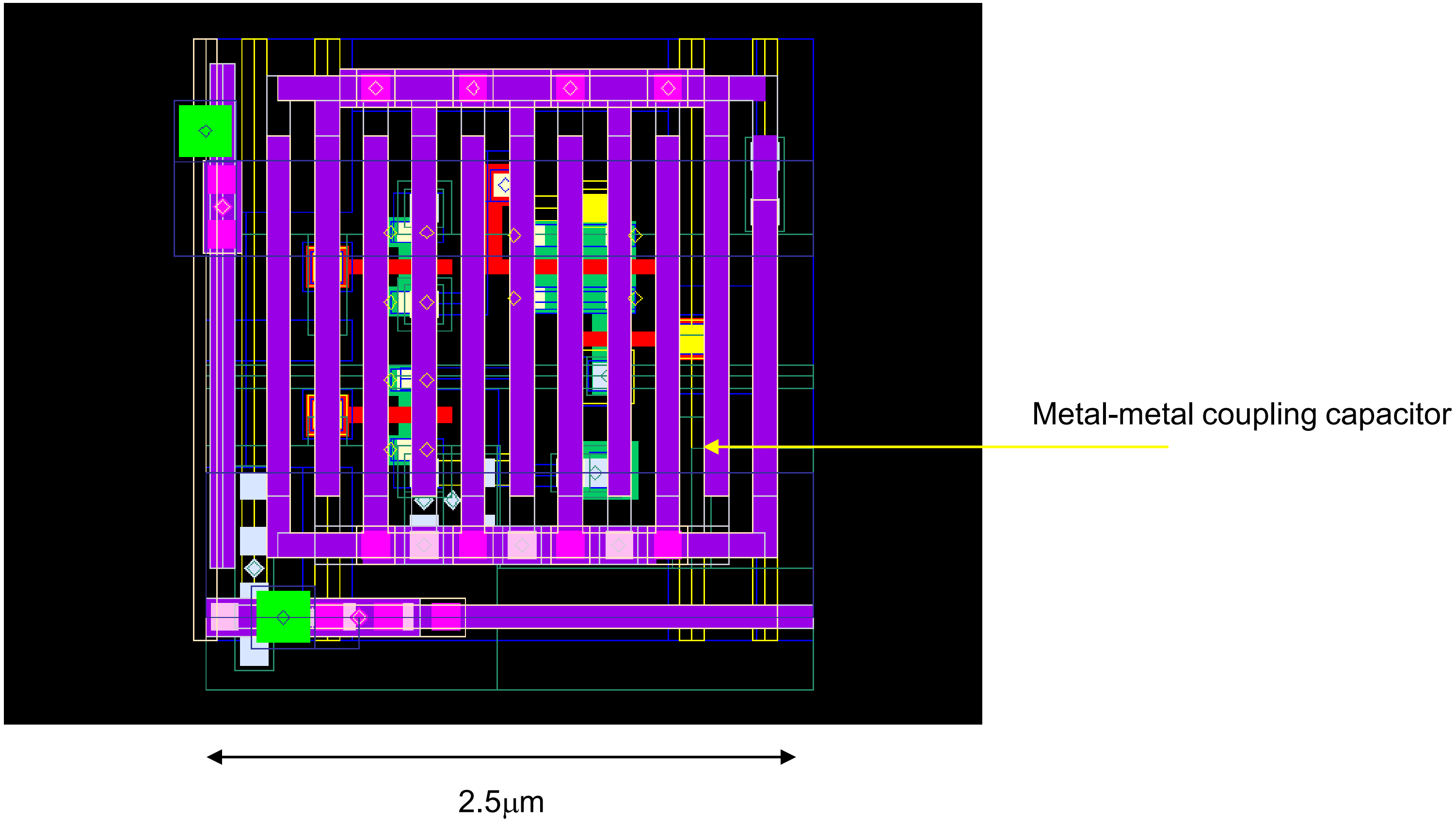
Results of the Project

- The SDAs have been developed within a small project whose aim was the proof of principle
- CMOS particle sensitive (“intelligent”) pixels in 350nm technology
- In pixel hit-detection and binary trigger based readout (similar to ATLAS pixels). Pixel size is 55x55μm^2
- Noise of 60e
- Direct hit signal - 1800e, leading to a seed pixel SNR of 30
- Signal delay time ~ time resolution of the detector ~ 120ns
- Part of the signal originates from the un-depleted bulk and is collected by diffusion – impact on timing will be investigated on a test chip, probably not an issue
- 4-transistor pixels (PM Chip) in 350nm technology
- Test beam:
- Efficiency 97.5%
- MIP cluster signal is 2000e and seed pixel signal 1200e
- The noise is about 44e that is twice as large as in lab tests – non-ideal setup
- Seed pixel SNR is 27, Cluster Signal/Seed Noise = 47
- We measure spatial resolution < 3.8µm


Preamplifier (NMOS part)
Preamplifier (NMOS part)
RC-CR shaper
4-bit SRAM
NMOS based comparator
4-bit threshold DAC
55µm
CM NMOS logic


Preamplifier (NMOS part)
Preamplifier (NMOS part)
RC-CR shaper
4-bit SRAM
NMOS based comparator
4-bit threshold DAC
55µm
CM NMOS logic

4T pixel in 65nm technology



Here only the standard N-Well has been used, only PMOS electronics
Lower signals expected (small depleted volume)
We hope to compensate this by lower detector capacitance

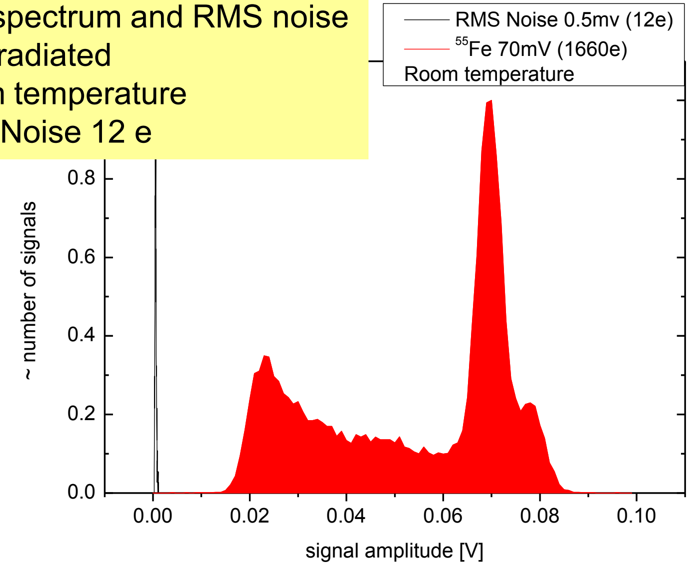
- In order to test the radiation tolerance we have performed a few irradiations

Proton irradiation

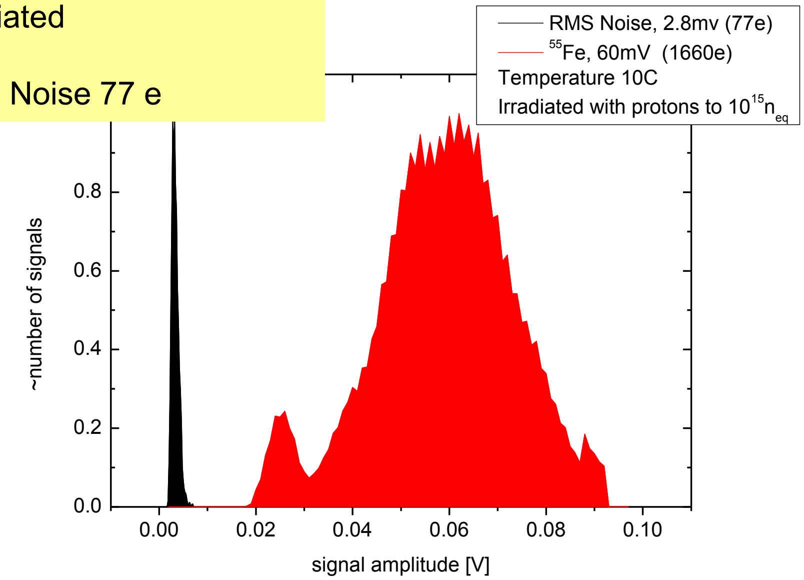
- Proton irradiation of continuous readout pixels up to 10^{15} n_{eq}/cm^2, which corresponds to a dose of ~300MRad in SiO_2.
- As expected, we measure an increased noise. For example, at 20C we measure 270e. (We had 12e before irradiation.) However, only a light cooling leads to significant noise improvement, a sign that the noise is caused by leakage current. At 10C we have a noise of 77e and at -10 only 40e.
- We have measured the response to ^{22}Na beta particles. SNR at -10C is 93.

Irradiation with protons (10^{15} n_{eq}/cm^2, 300 MRad)

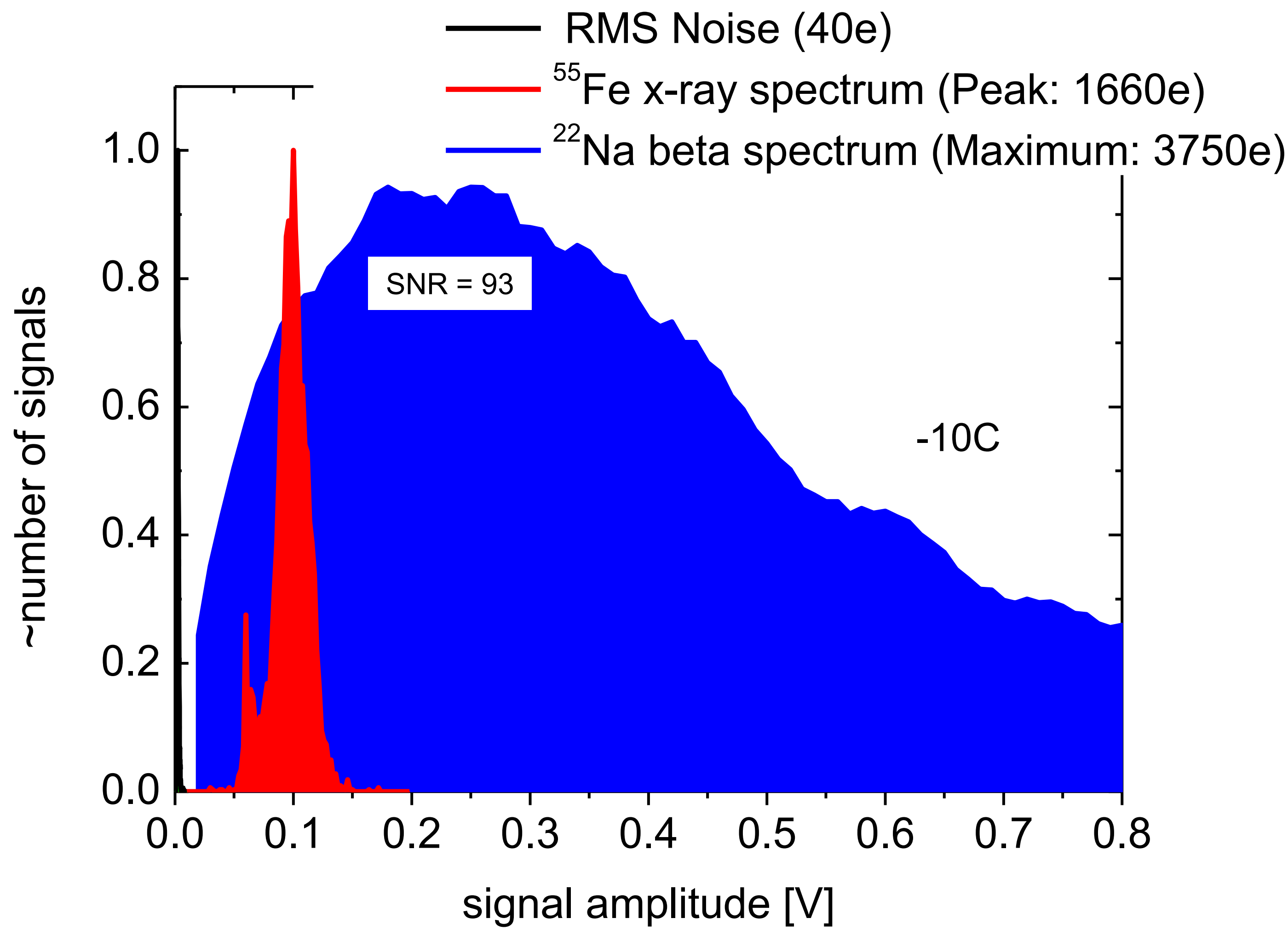
^{55}Fe spectrum and RMS noise
Not irradiated
Room temperature
RMS Noise 12 e



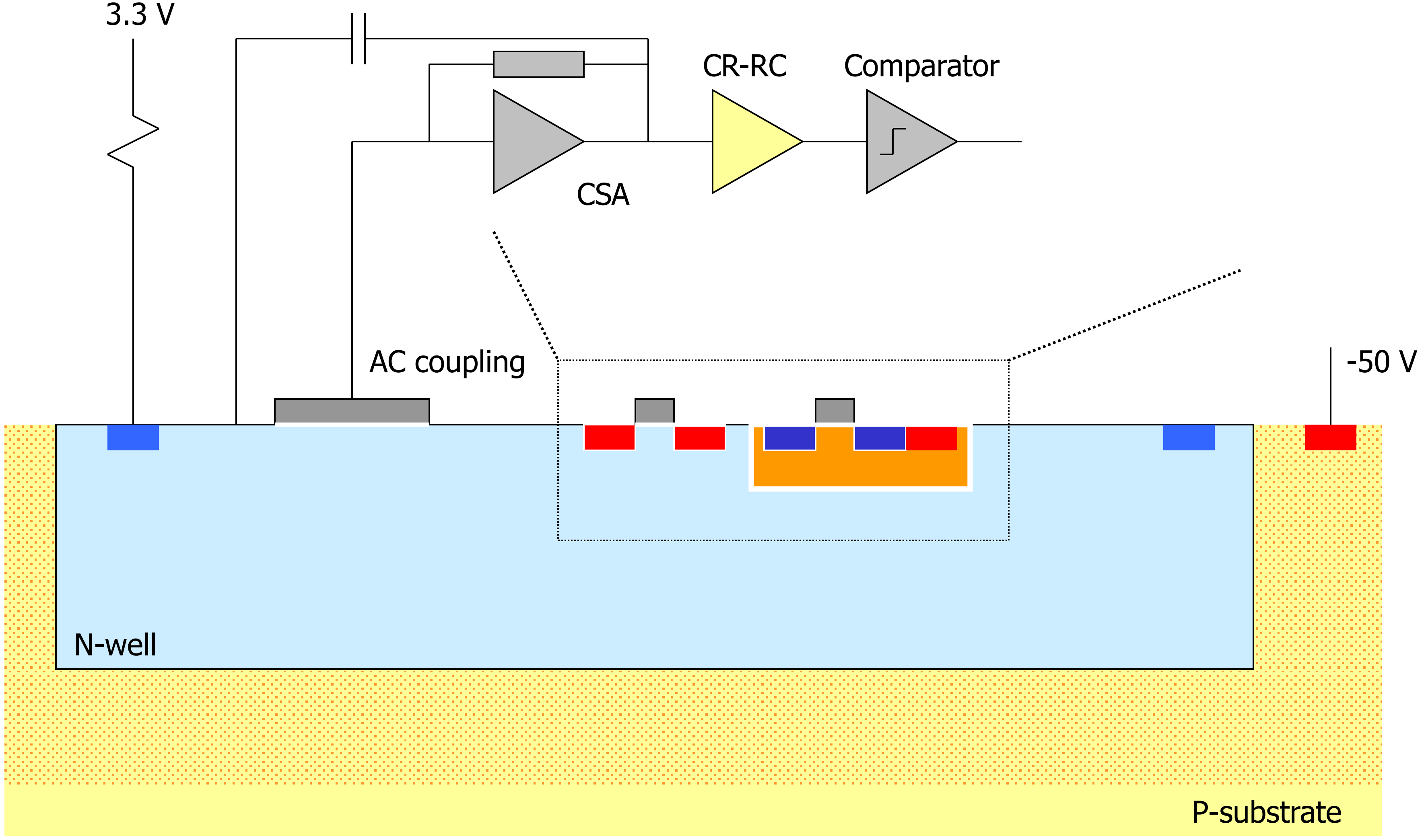
^{55}Fe spectrum, RMS noise
Irradiated
10C
RMS Noise 77 e

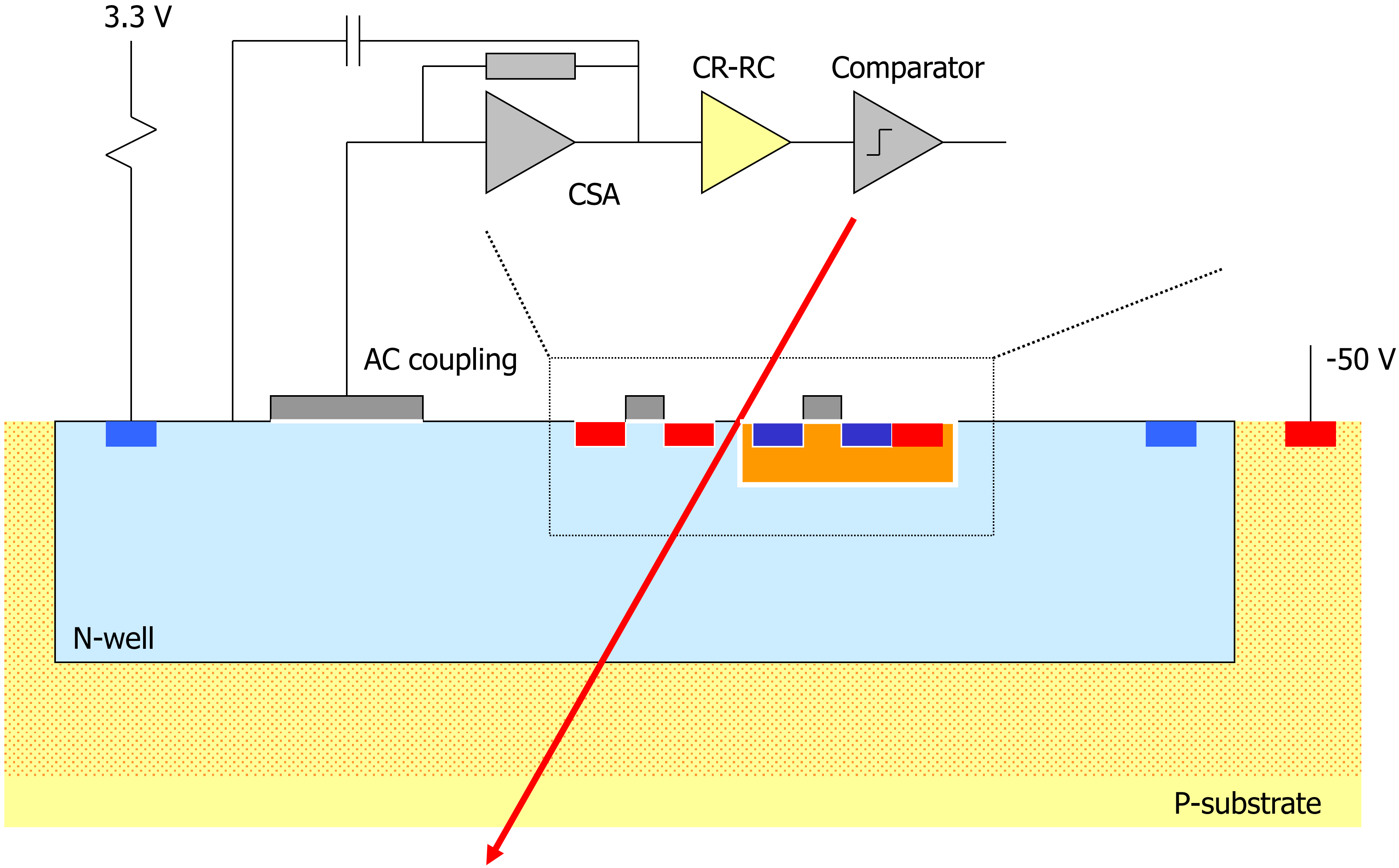


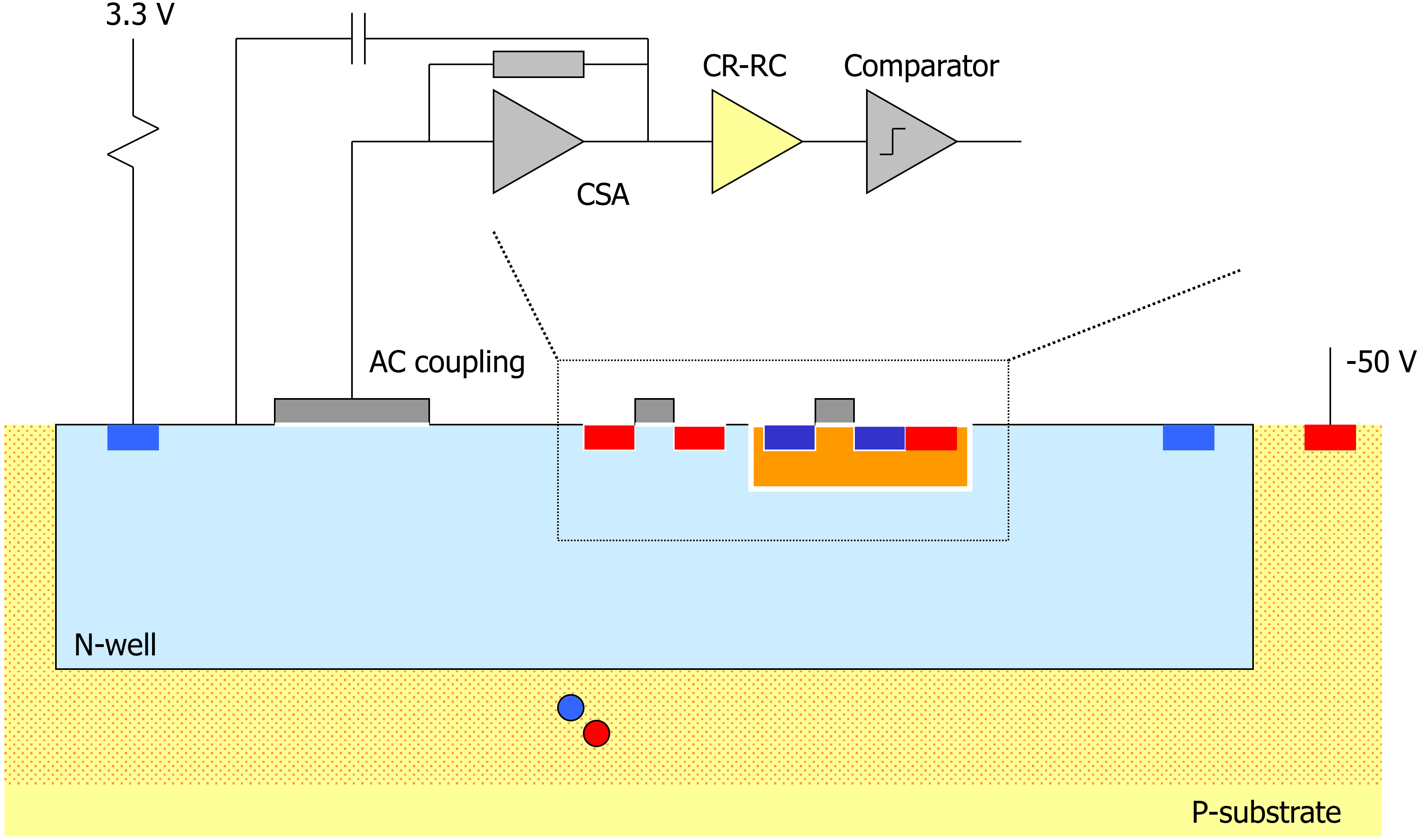
Irradiation with protons (10^{15} n_{eq}/cm^2, 300 MRad)

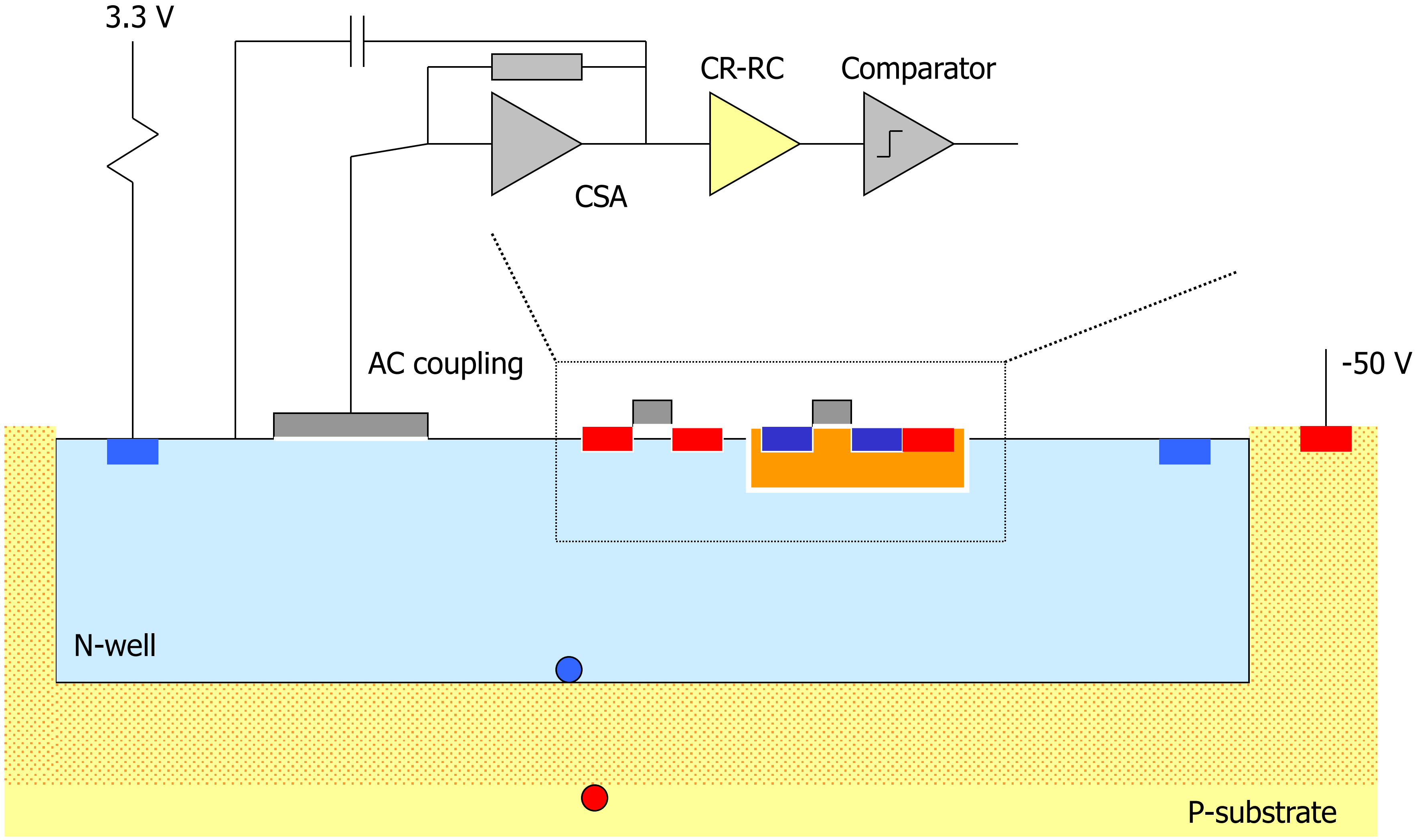


Particle sensitive pixels with CMOS electronics and continuous readout

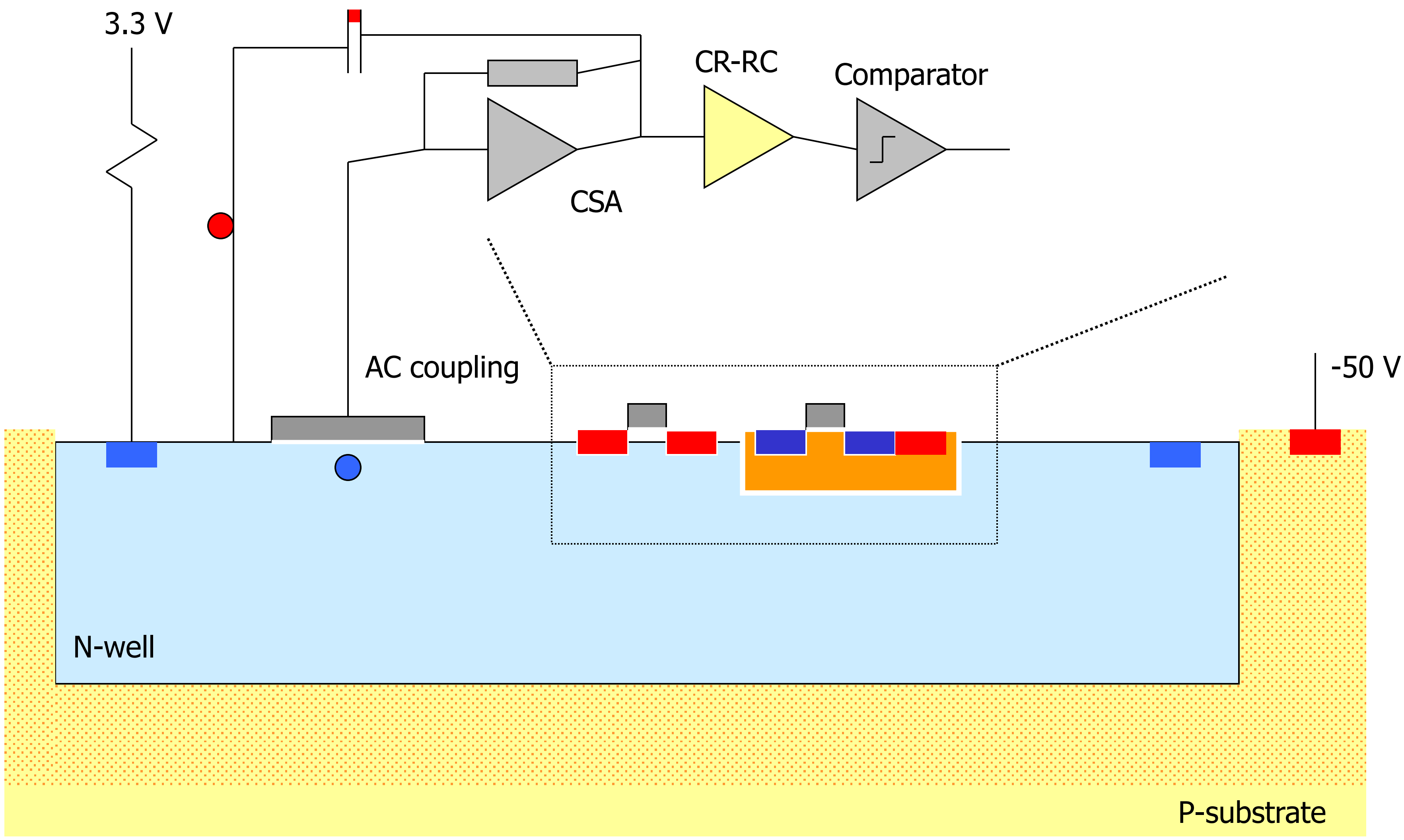

3.3 V
CR-RC
Comparator
CSA
AC coupling
-50 V
N-well
P-substrate

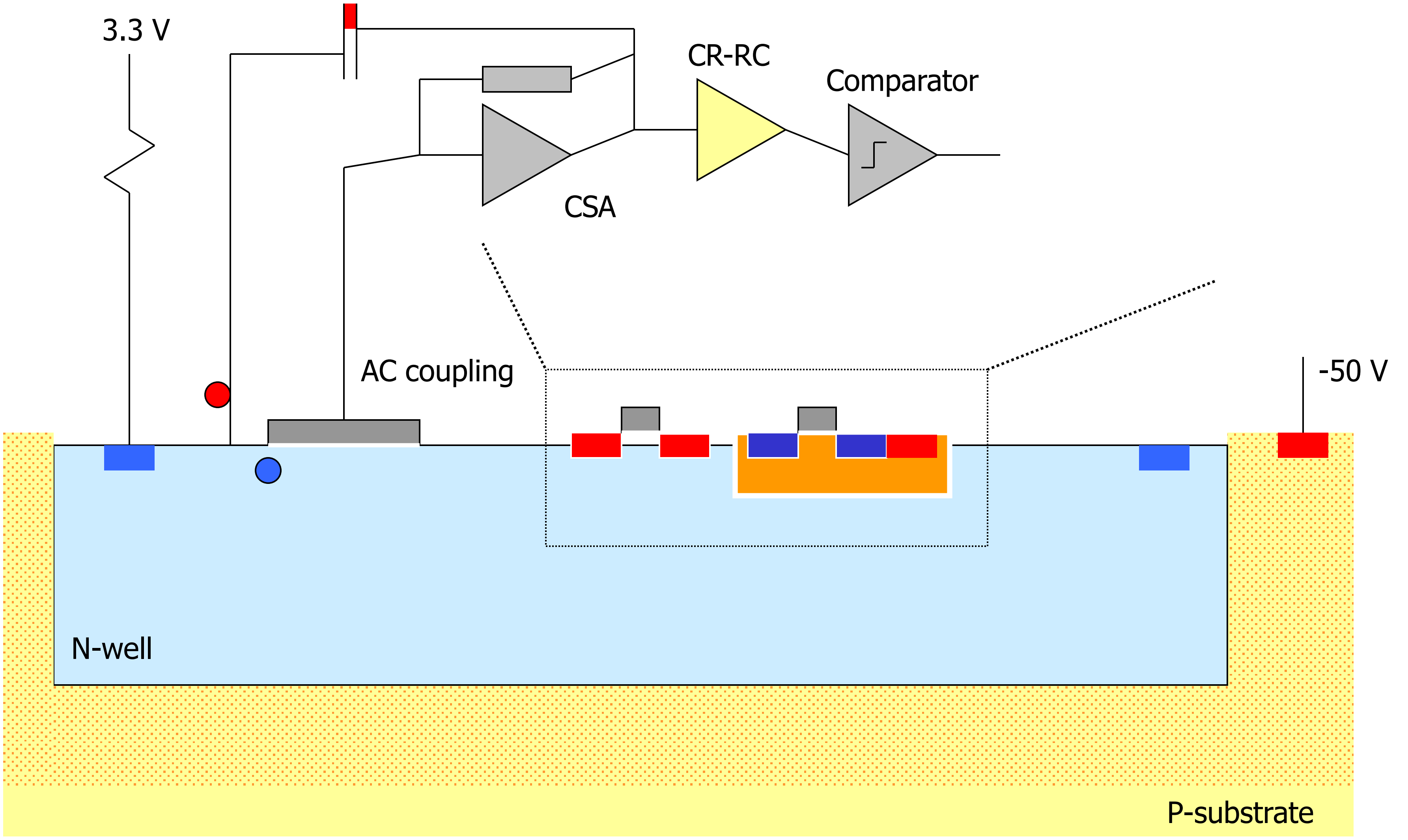

3.3 V
CR-RC
Comparator
CSA
AC coupling
-50 V
N-well
P-substrate

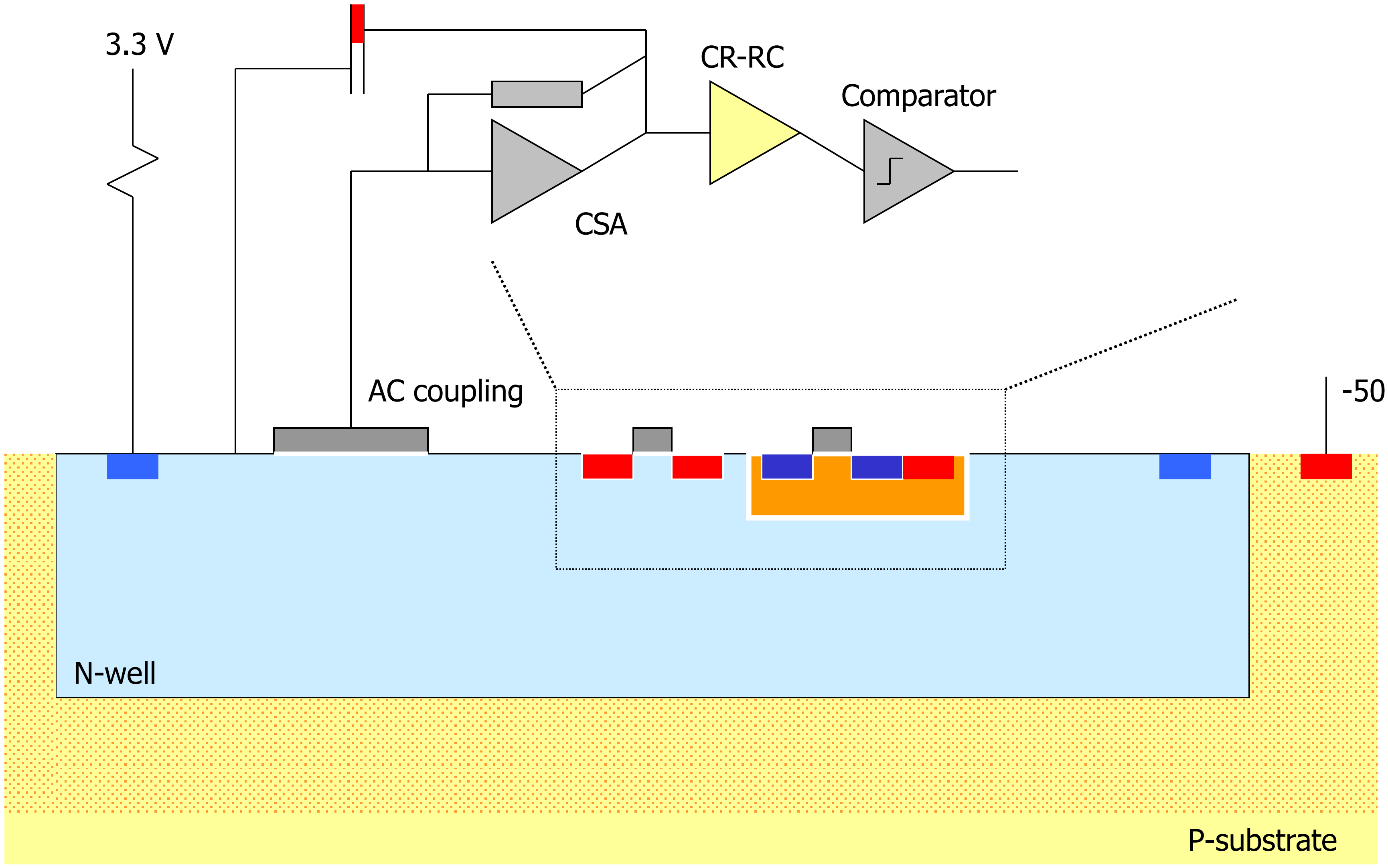

3.3 V
CR-RC
Comparator
CSA
AC coupling
-50 V
N-well
P-substrate

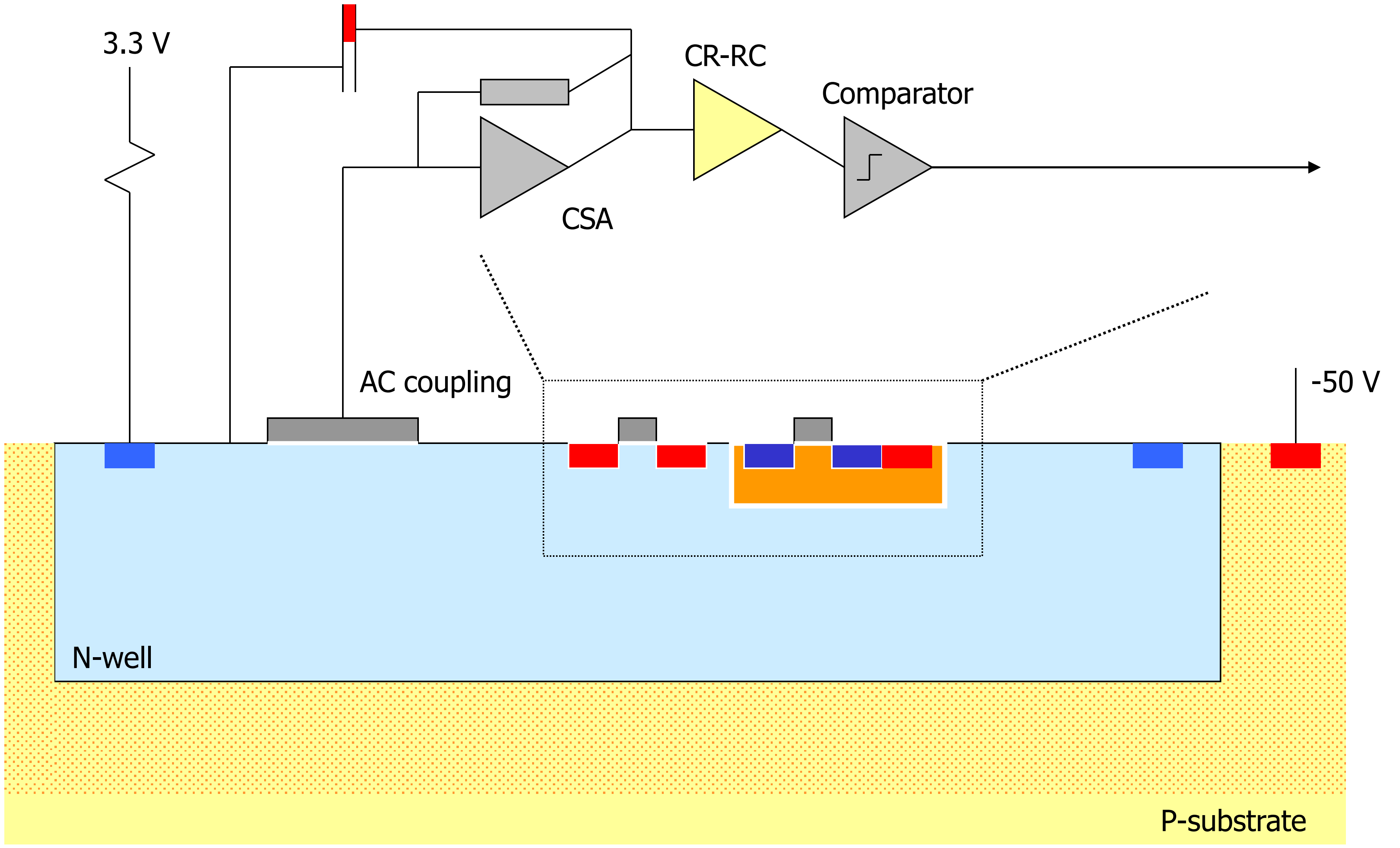

3.3 V
CR-RC
Comparator
CSA
AC coupling
-50 V
N-well
P-substrate

Signal detection

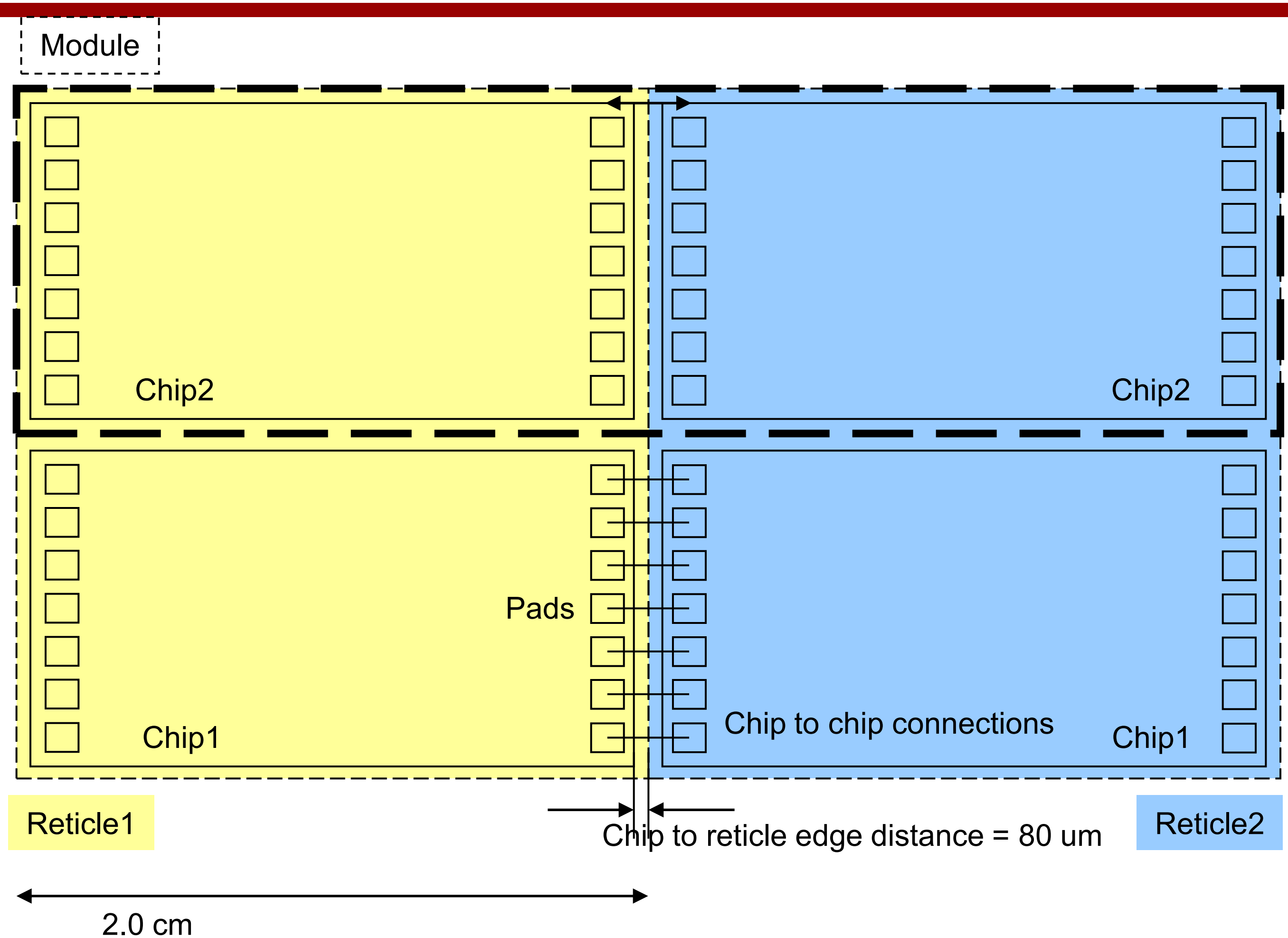



3.3 V
CR-RC
Comparator
CSA
AC coupling
-50 V
N-well
P-substrate

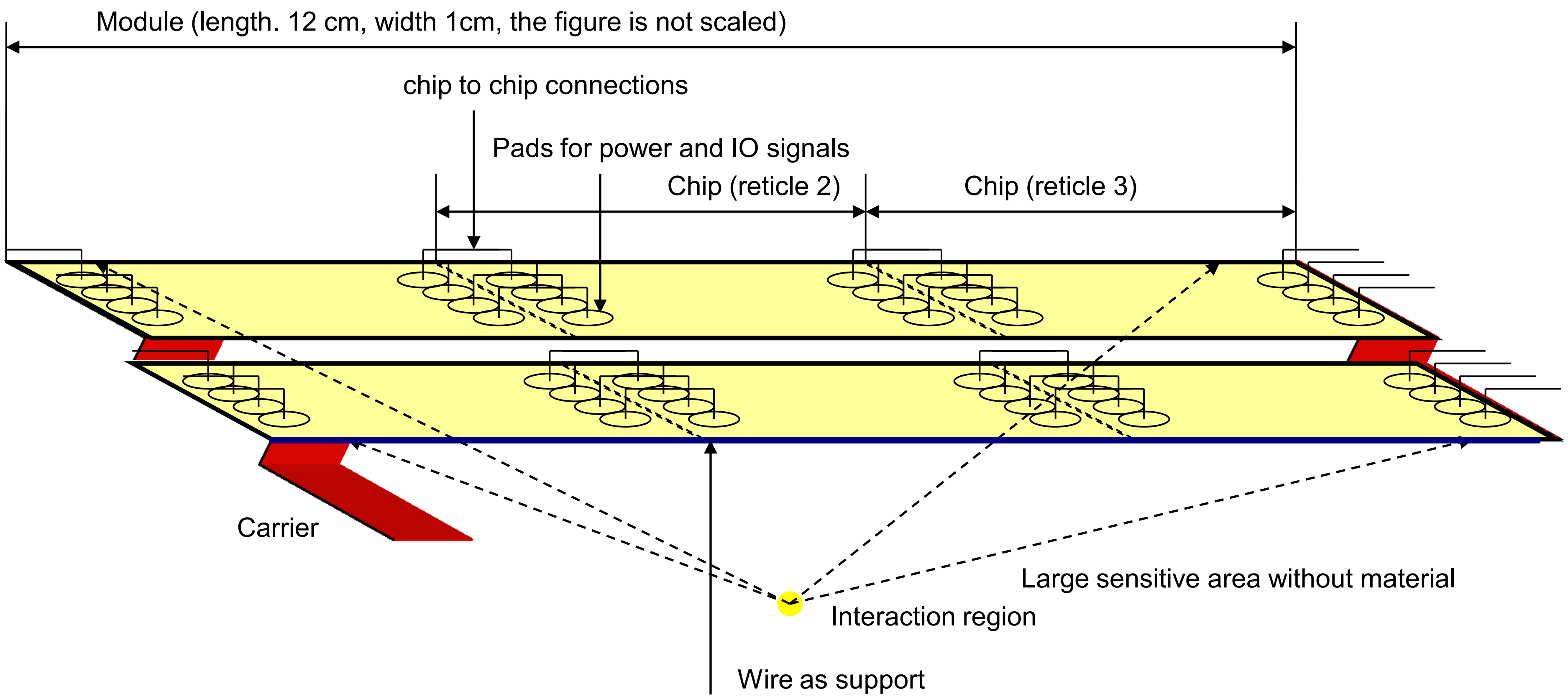

3.3 V
CR-RC
Comparator
CSA
AC coupling
-50 V
N-well
P-substrate


3.3 V
CR-RC
Comparator
CSA
AC coupling
-50 V
N-well
P-substrate

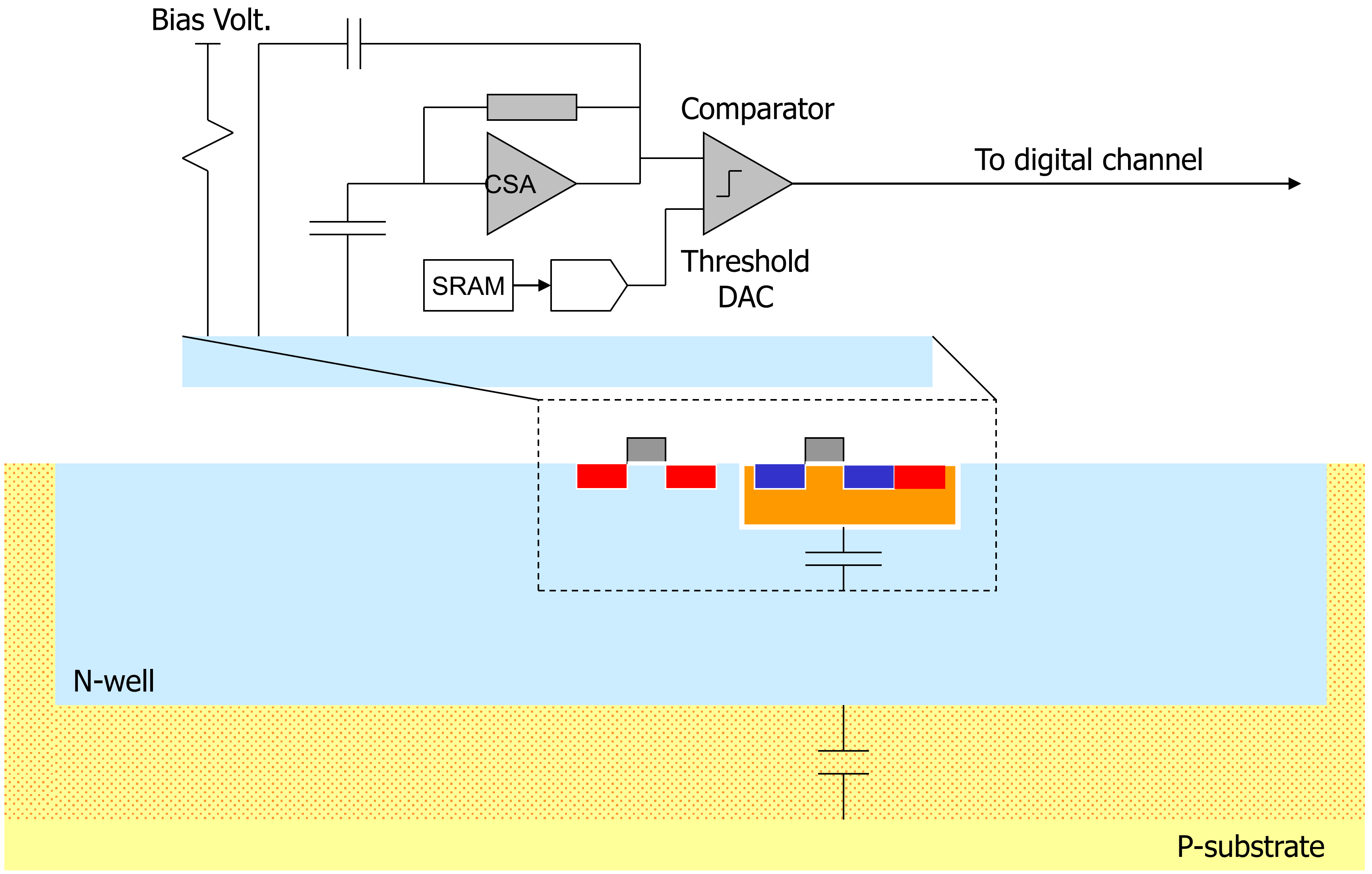
- Vertex detector for the novel experiment. Goal: search for lepton flavor violating decay μ -> eee
- Four layers of pixels ~ 80x80μm^2 size
- Continuous muon beam stopped at target – 10^9 muon stops/s –> requires time stamping with ~ 100ns resolution
- Energy range of interest: 15-50MeV –> multiple scattering dominates momentum measurement –> ~50 μm thin detector

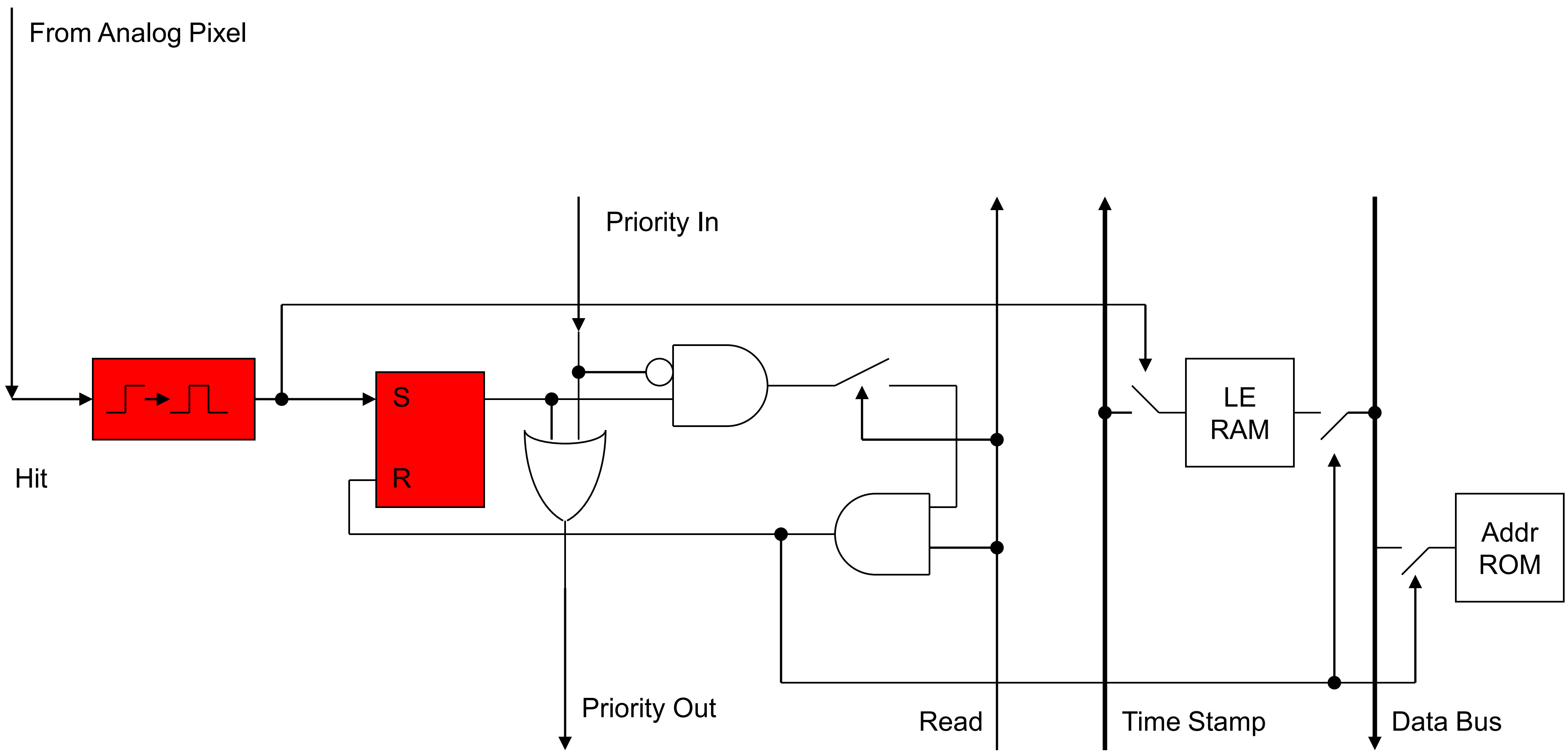


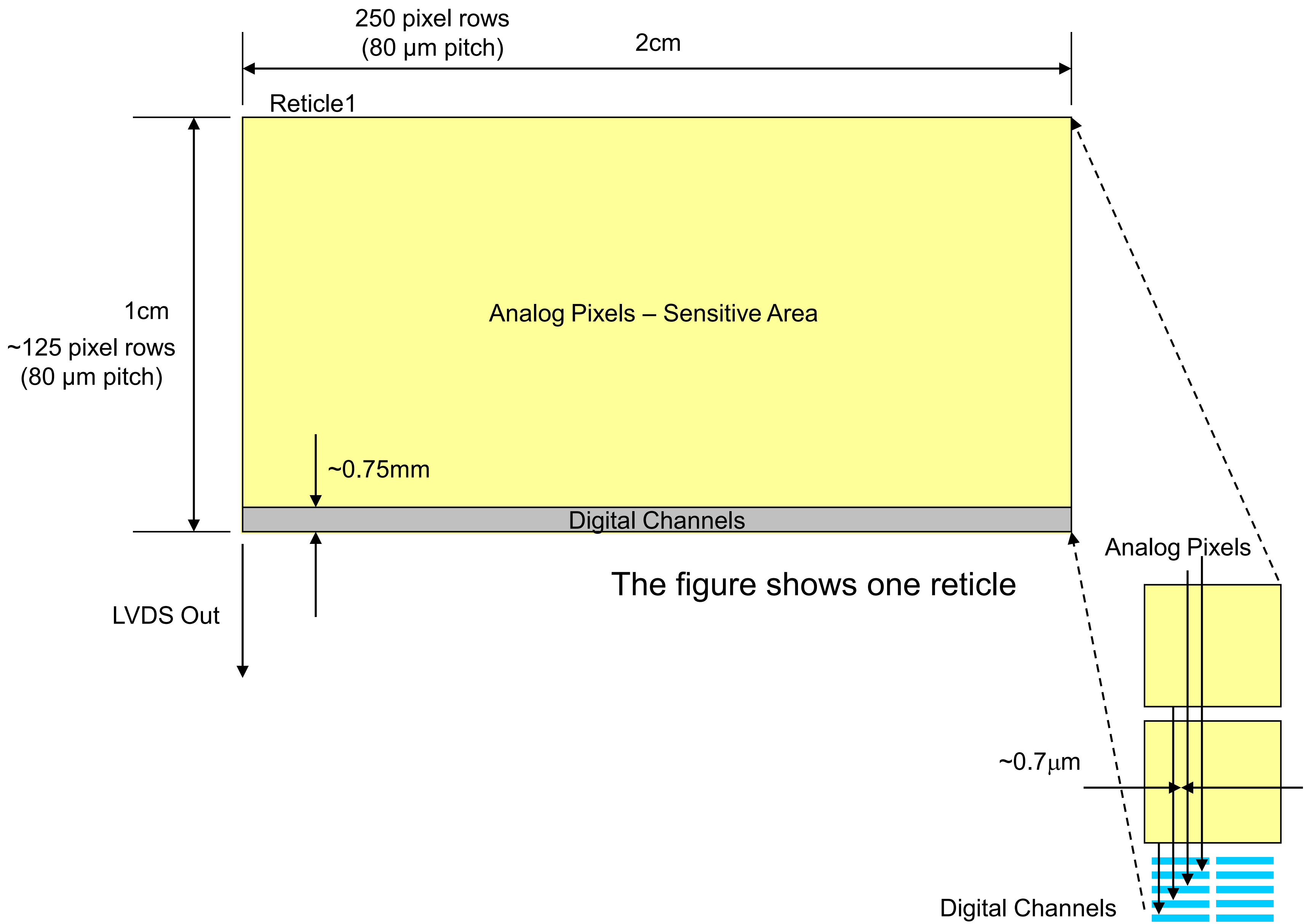
Pixel modules with (almost) no insensitive area can be produced
Reticle-reticle connections can be made easily by wire bonding
Instead of wire-bonding, an extra metal layer can be used as well



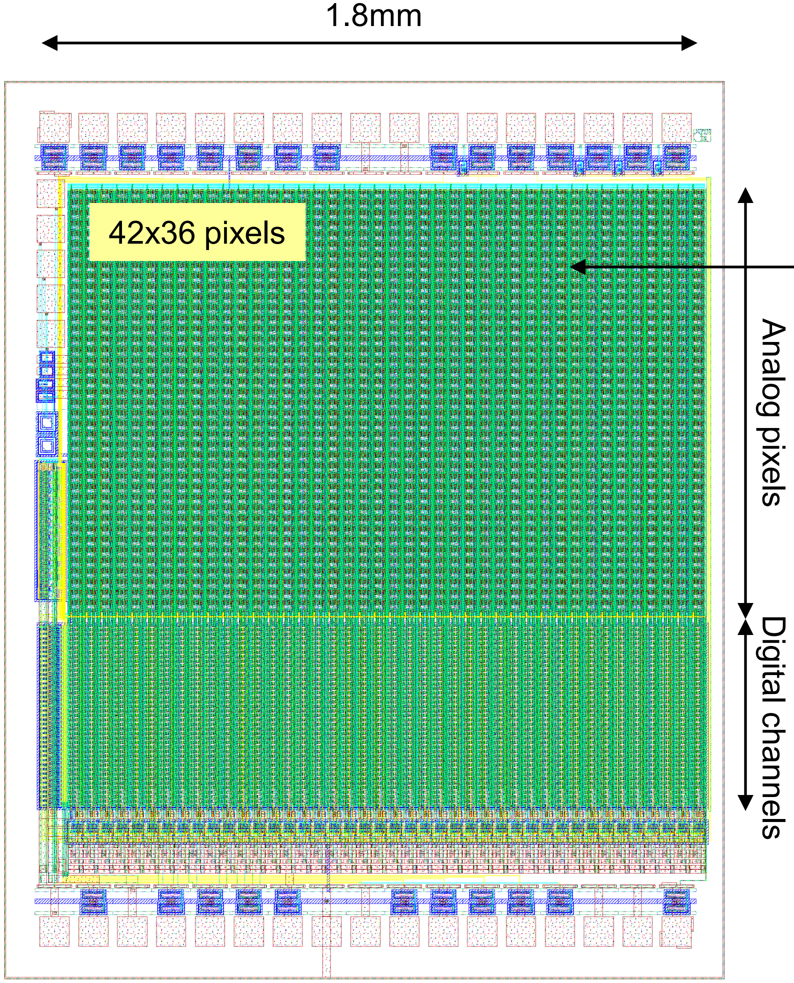
Very low-mass only silicon module

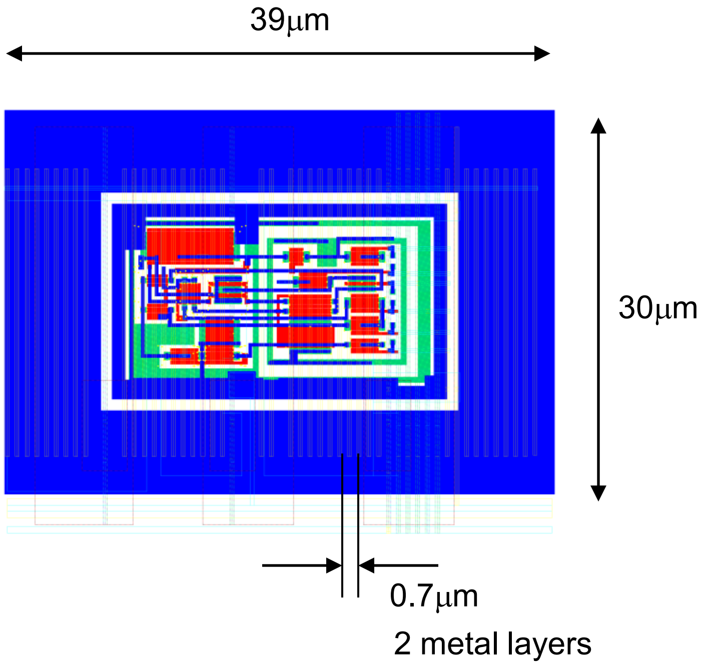

Bias Volt.
Comparator
To digital channel
CSA
SRAM
Threshold
DAC
N-well
P-substrate


From Analog Pixel
Priority In
Hit
S
R
LE
RAM
Addr
ROM
Priority Out
Read
Time Stamp
Data Bus



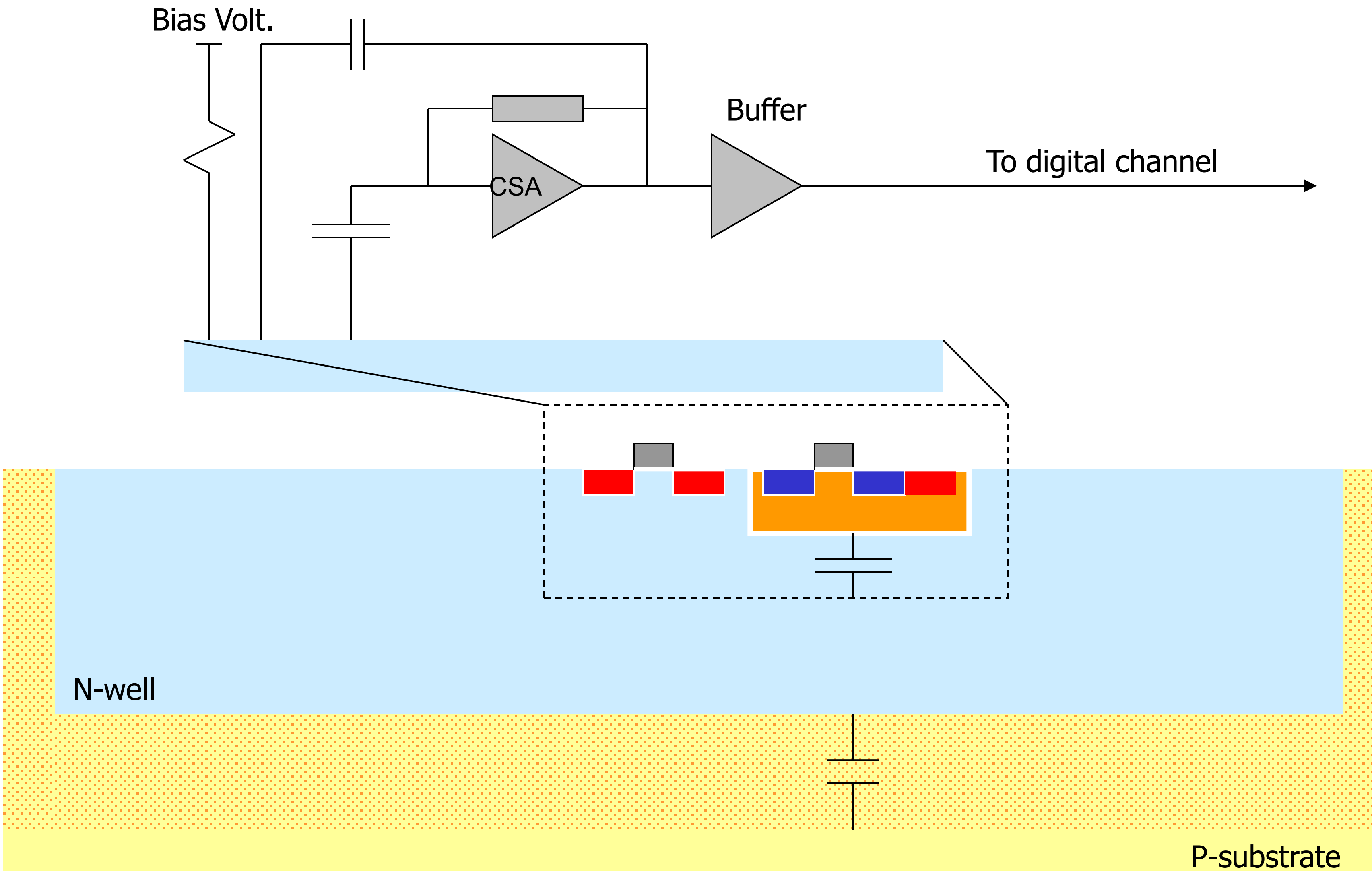
The figure shows one reticle



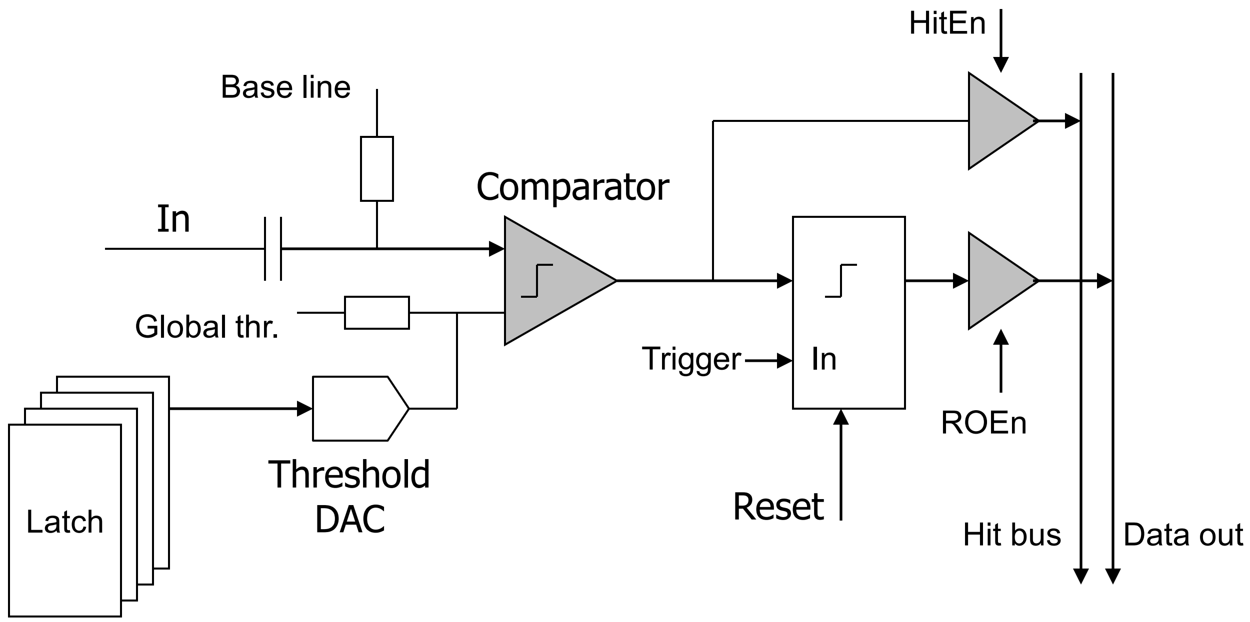


Analog pixel layout

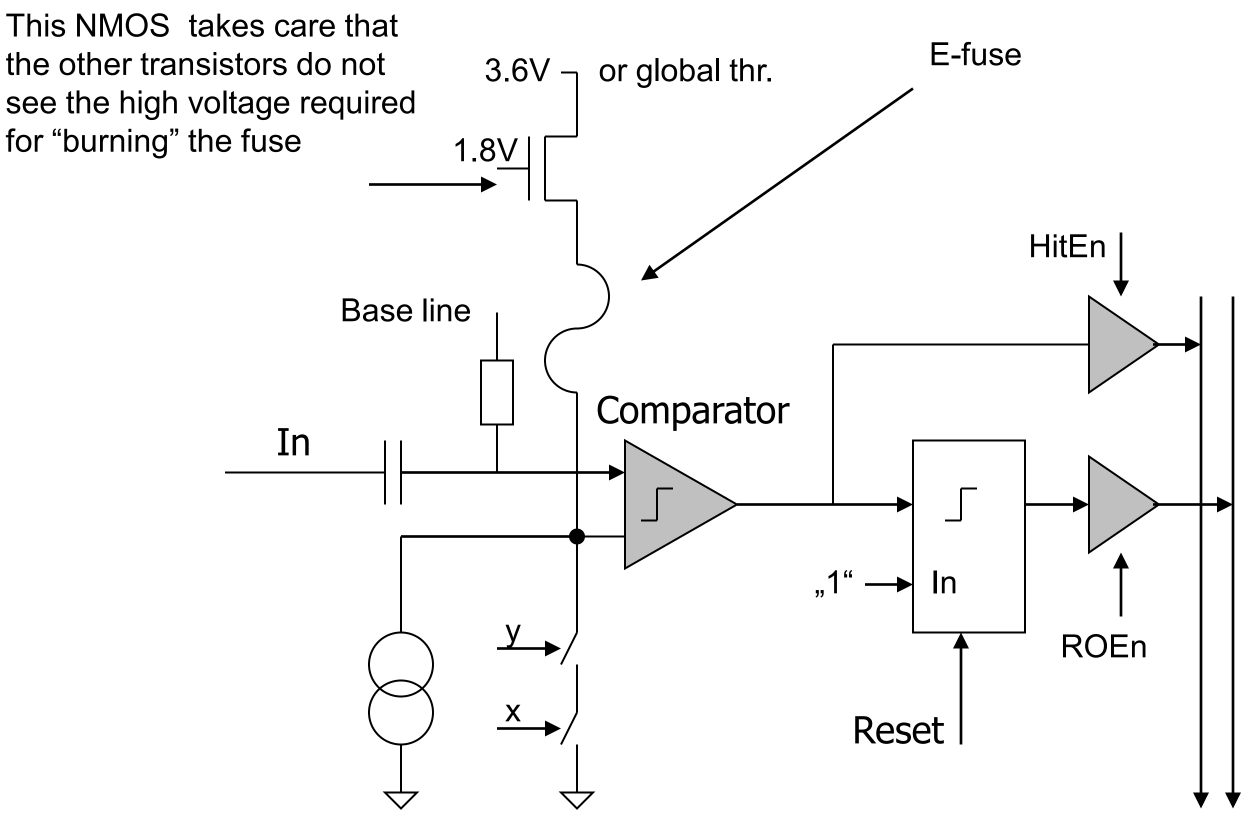
Pixel is made smaller than needed
This has positive impact on detector capacitance



The analog pixel is slightly different than required for the final design
Comparator, tune DAC and SRAM are missing (placed in the digital channel)



The digital channel is slightly different than required for the final design
Similar number of transistors

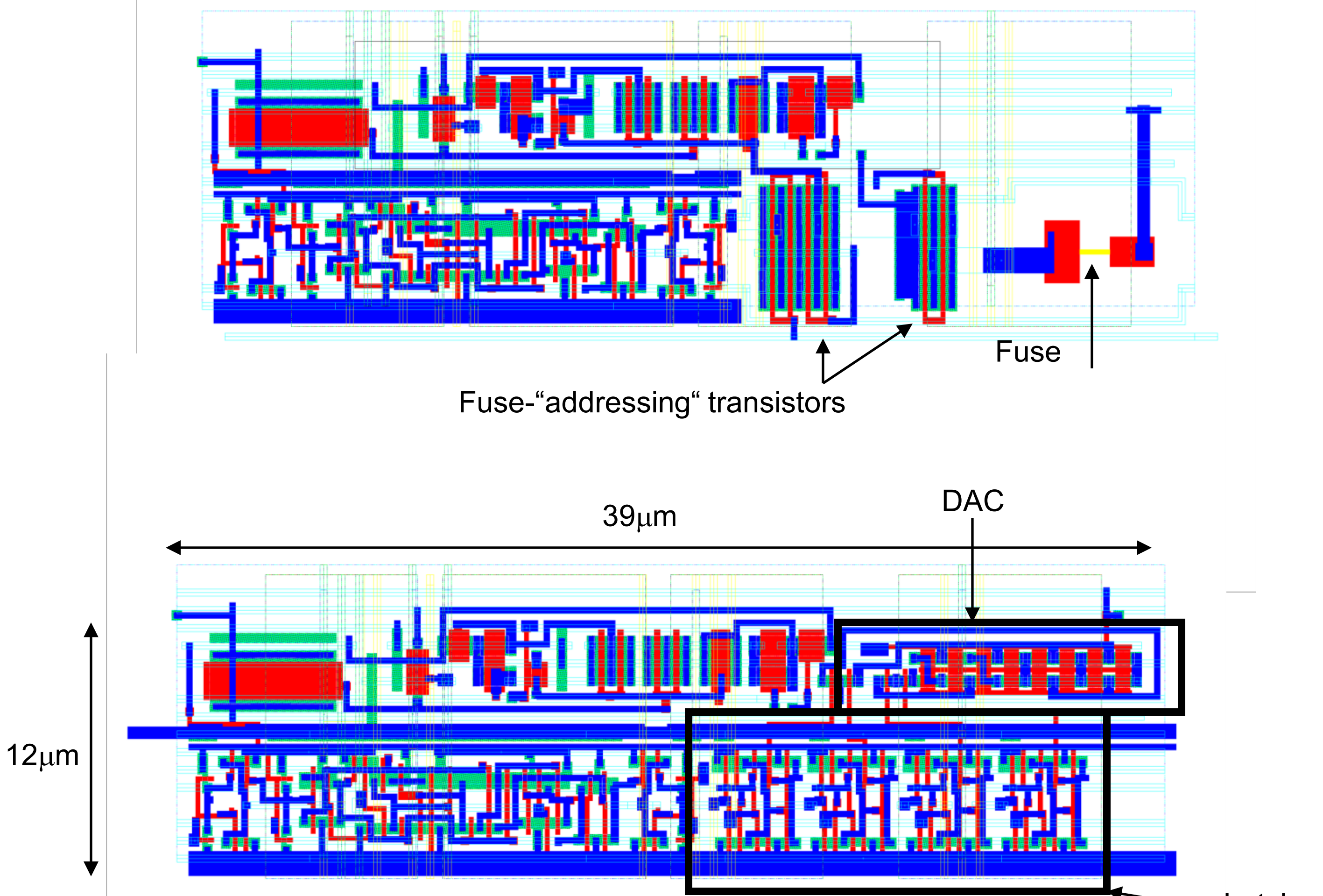


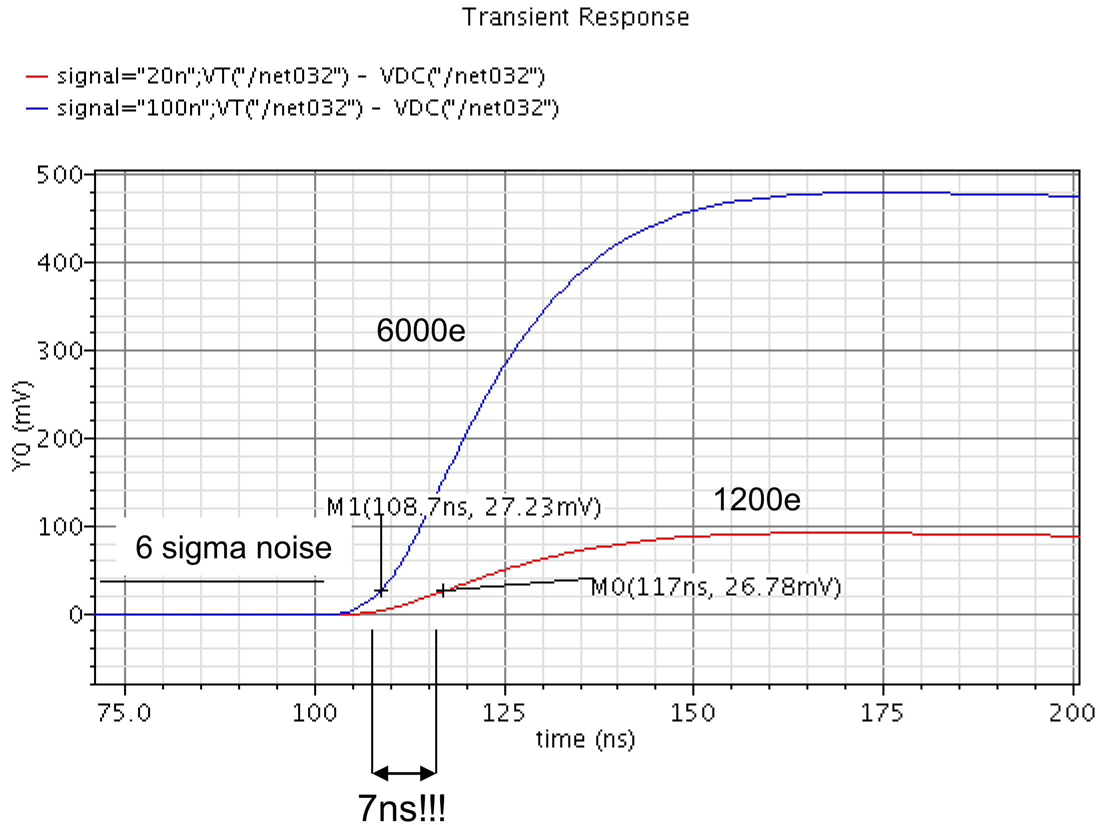
E-fuse substitutes threshold tune DAC -> smaller layout

Idea: Strasbourg "MAPS" group (A. Dorokhov)

E-fuse requires high voltage to be "burned"

Digital Channels

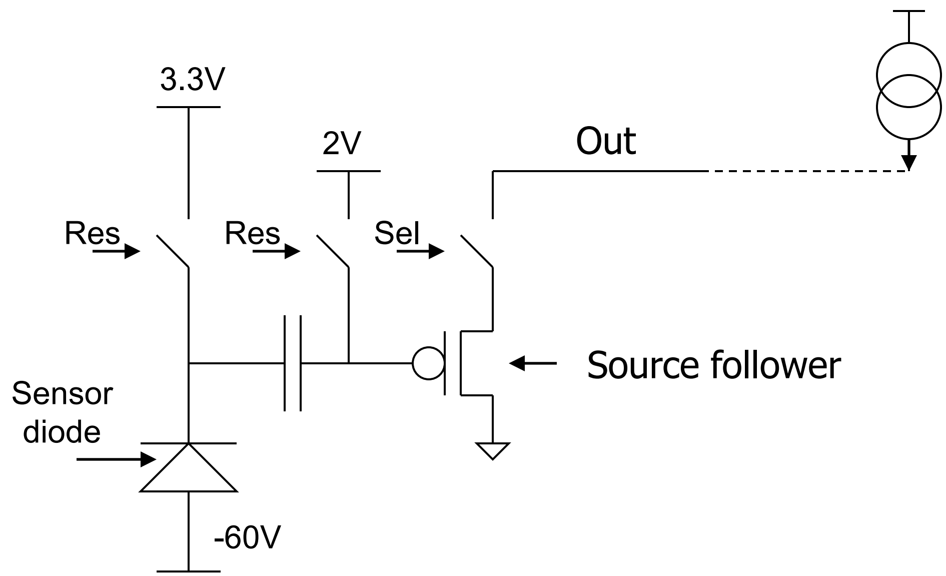




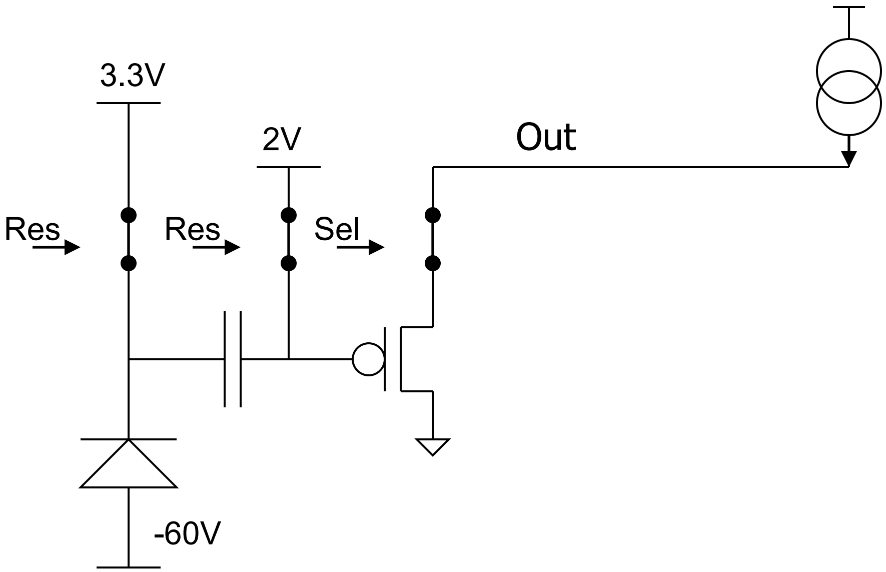
Power in analog pixel ~ only 8μW

Integrating pixels

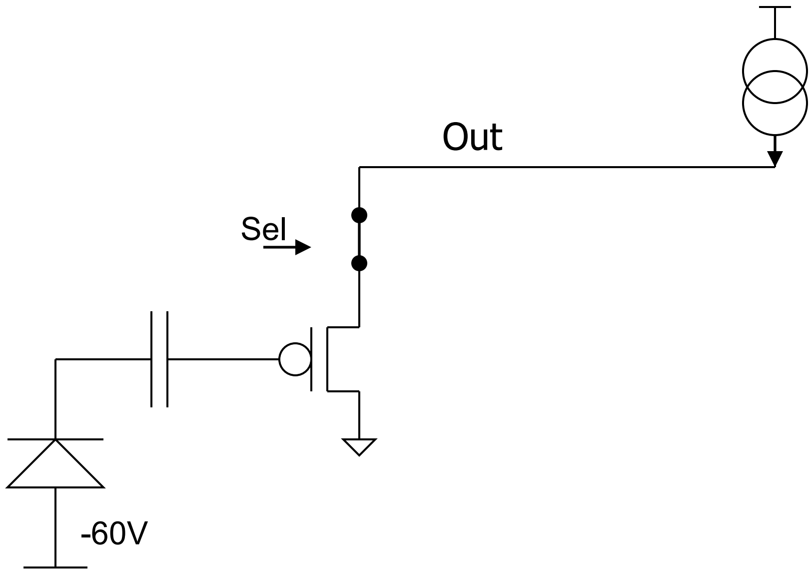
Integrating pixels with source follower readout



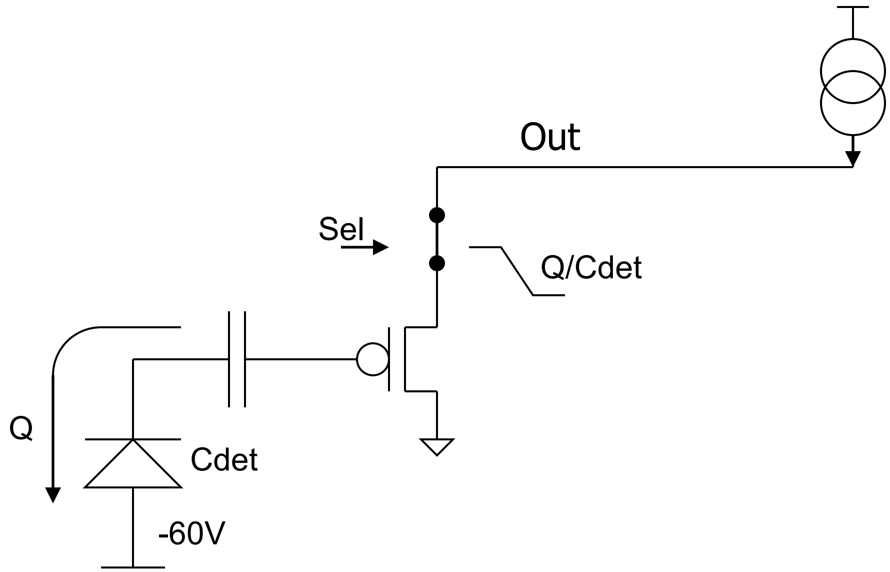
Only PMOS transistors -> no need for P-Well



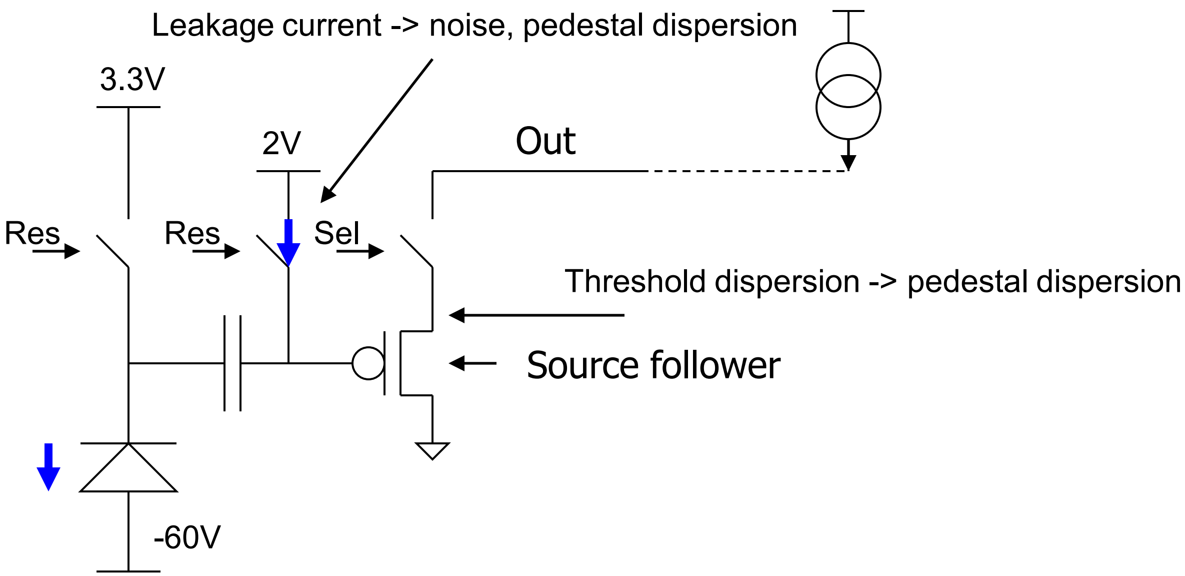
Reset phase



Signal detection phase

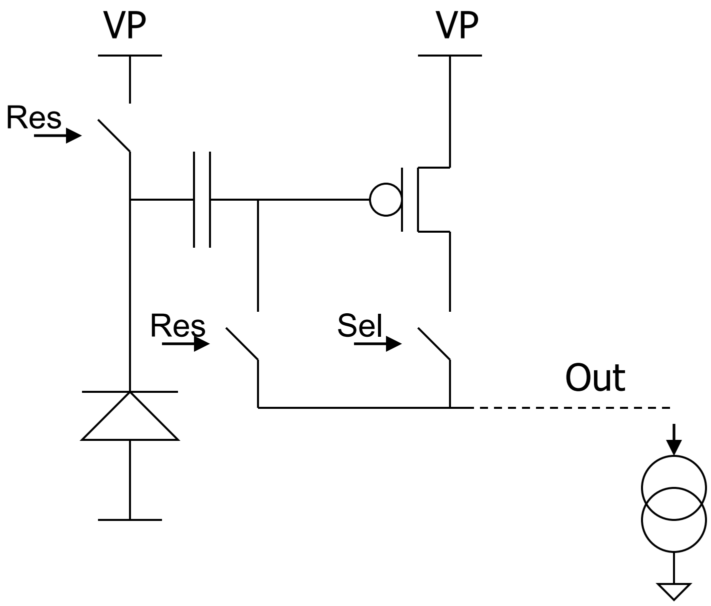


Signal detection phase

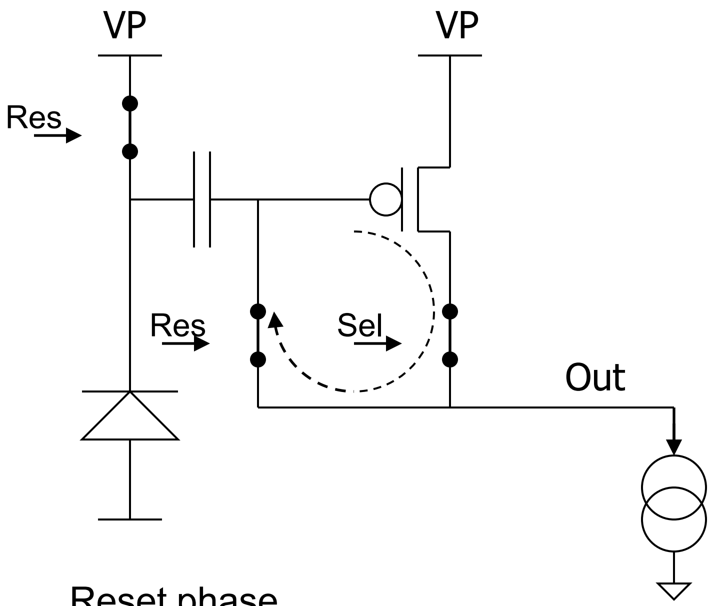


The main problems:
KTC noise -> requires CDS
Leakage current (leakage of PMOS switches probably dominates)
Leakage current causes noise and pedestal dispersion
Threshold dispersion

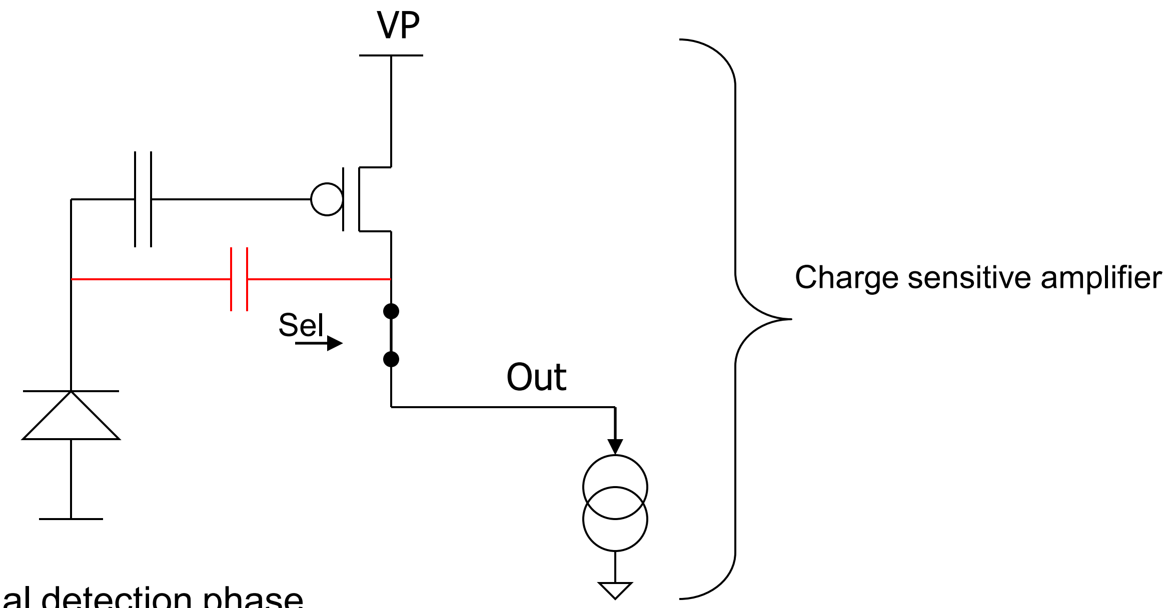
Integrating pixels with voltage amplification



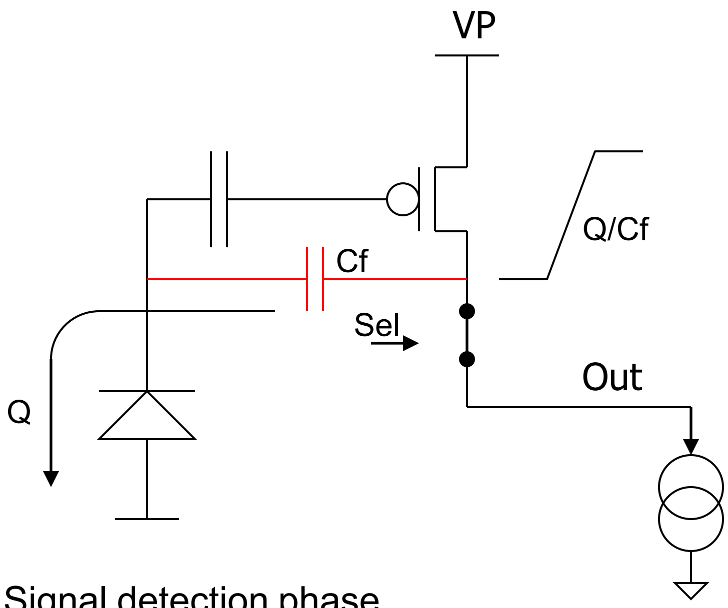
Integrating pixels with voltage amplification



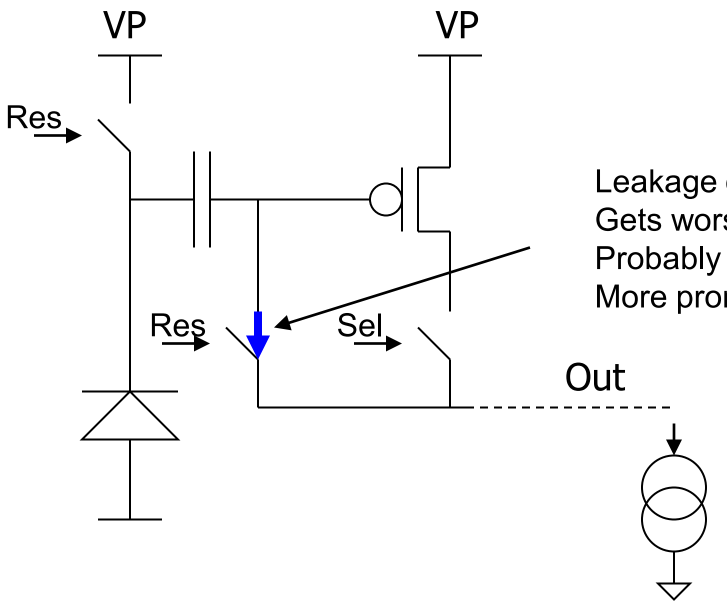
Reset phase



Signal detection phase

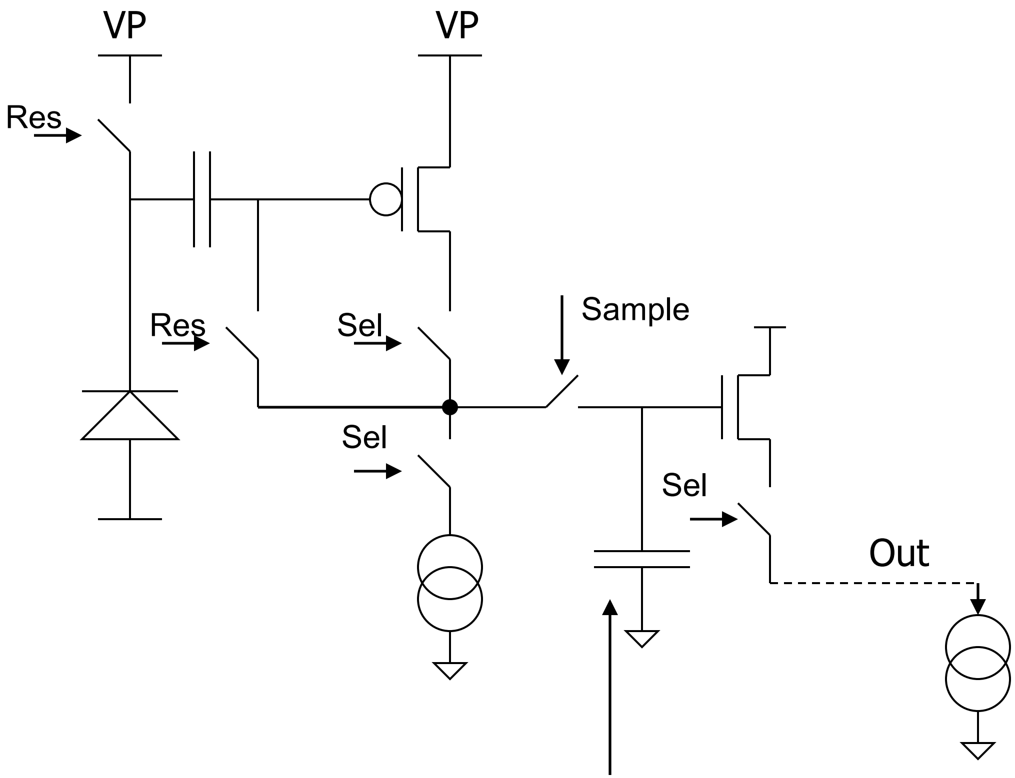


Signal detection phase



Leakage current -> noise, pedestal dispersion
Gets worse with higher reverse bias
Probably a kind of back gate effect
More pronounced than in source follower pixels

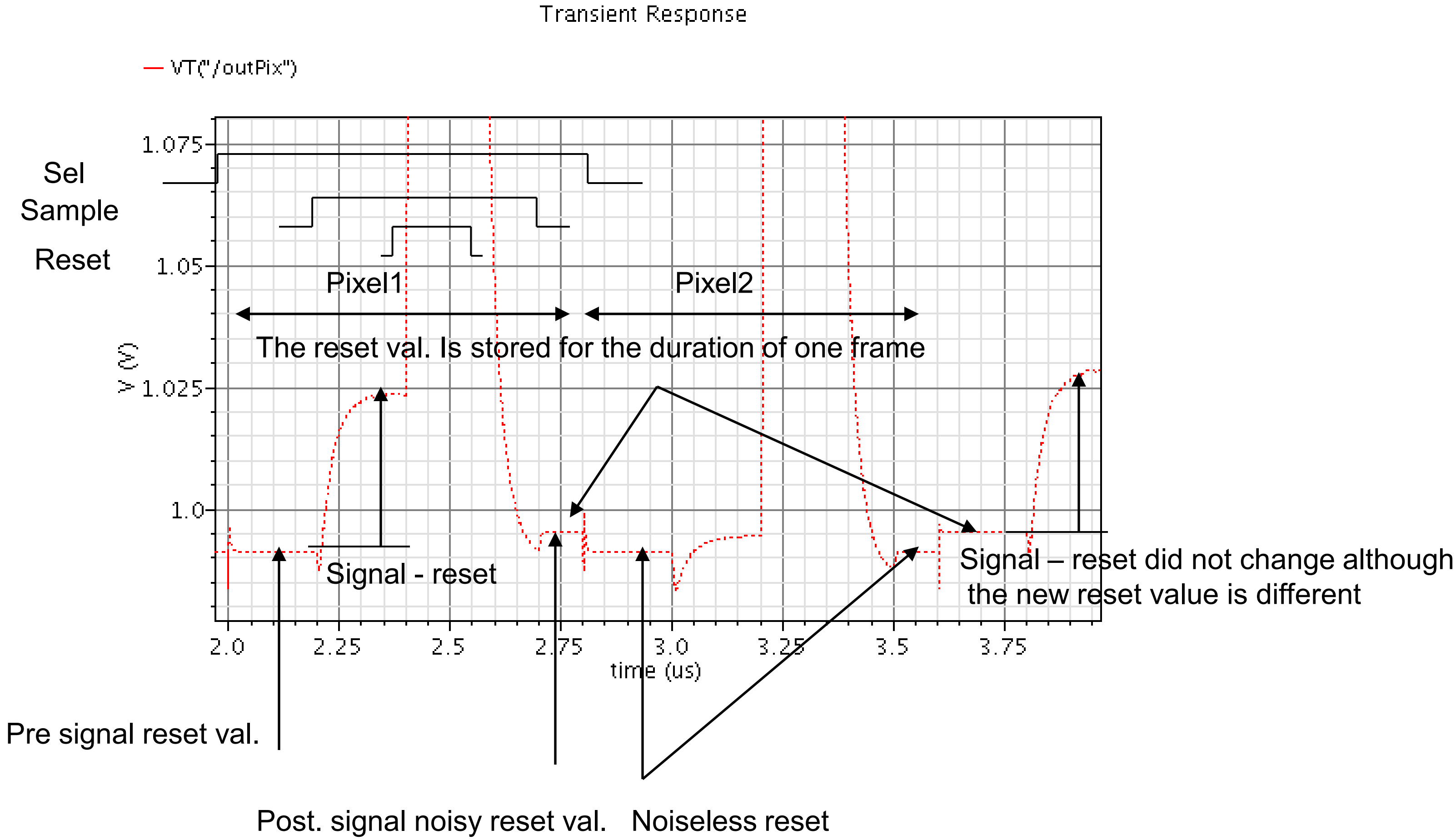
The main problems:
KTC noise -> requires CDS
PMOS leakage current
Threshold dispersion is not the issue since its effect is reduced by applied gain



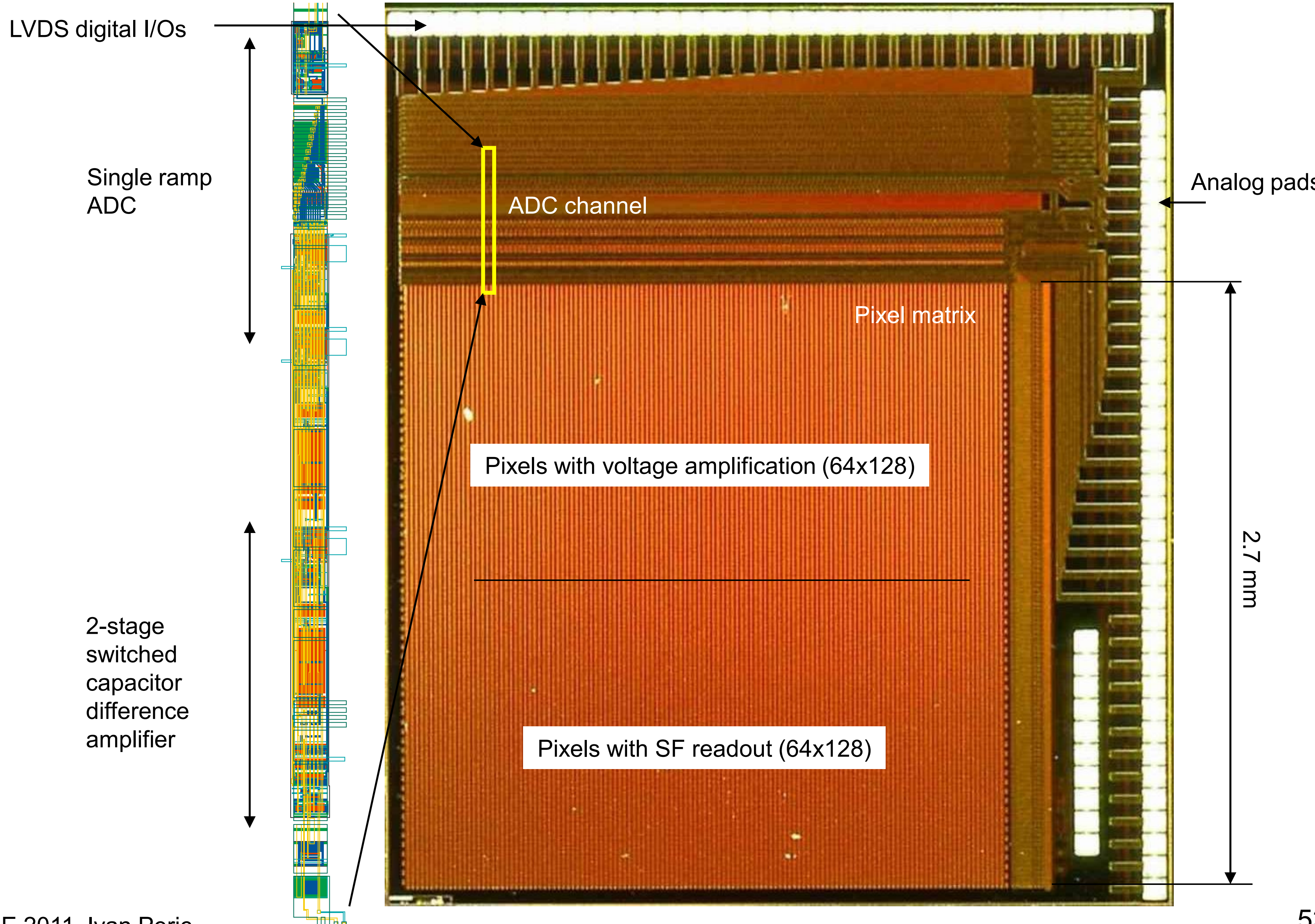
~100fF sampling capacitor to store the reset value for duration of one frame

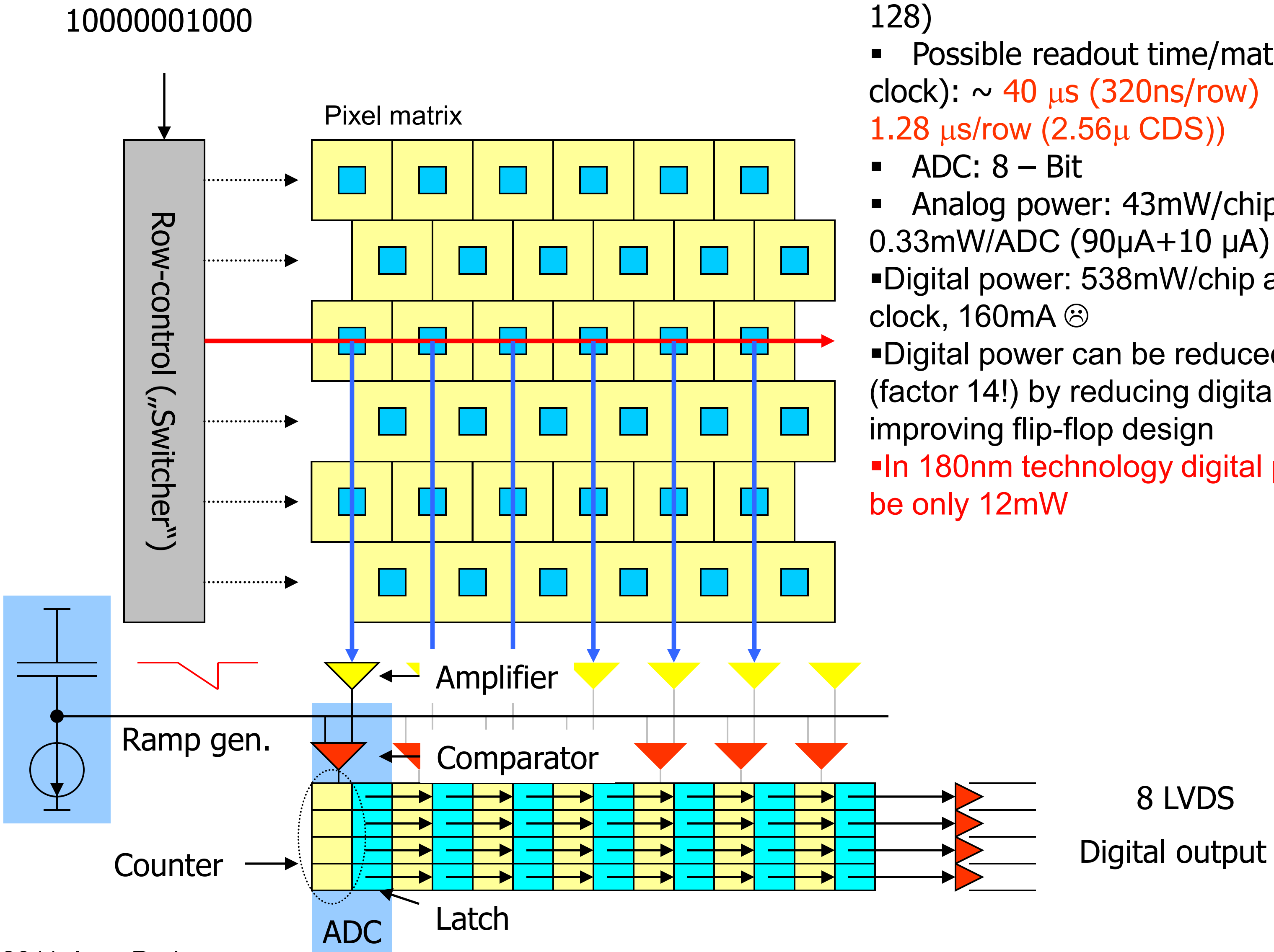
A few NMOS transistors in pixel required -> P-Well is mandatory

Transient noise simulation



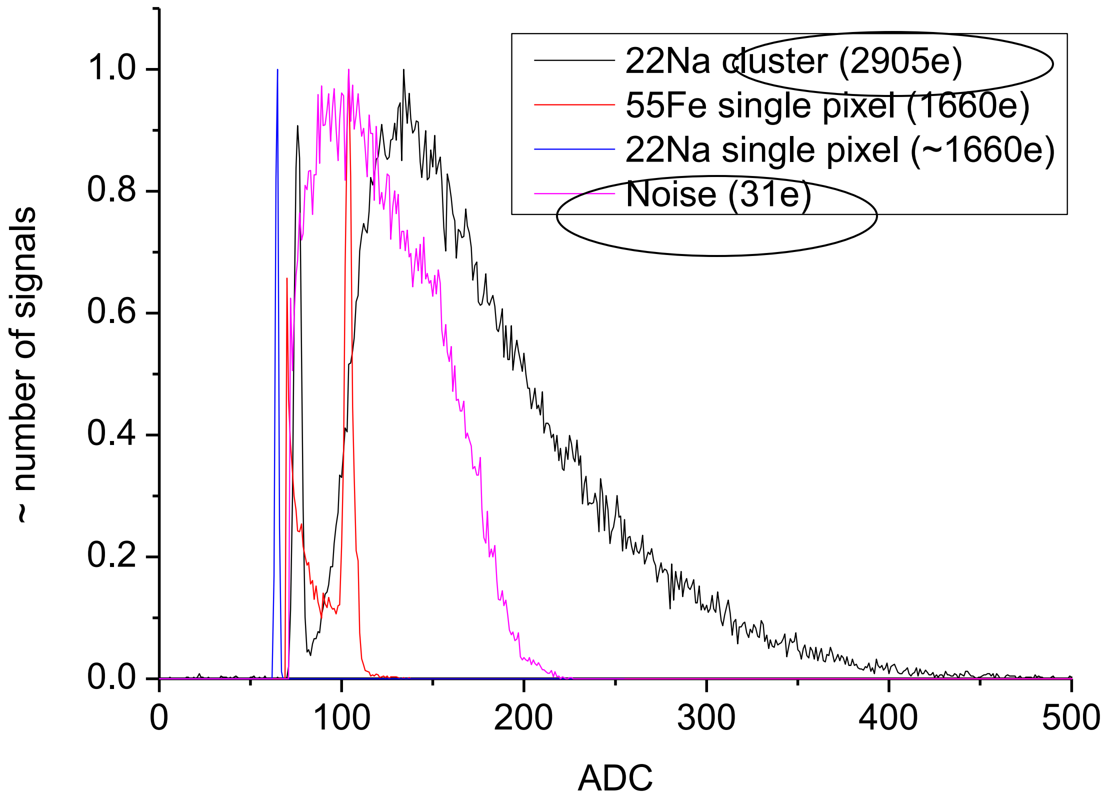
PM2 chip (known in Eudet community as „Taki“)





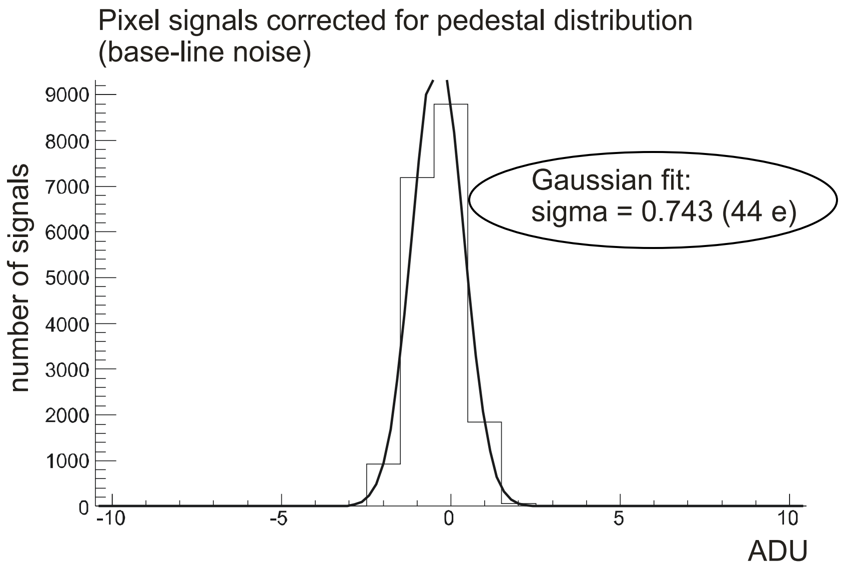
- Pixel size: 21 X 21 μm
- Matrix size: 2.69 X 2.69 mm (128 X 128)
- Possible readout time/matrix (400MHz clock): ~ 40 μs (320ns/row) (tested so far 1.28 μs/row (2.56μ CDS))
- ADC: 8 – Bit
- Analog power: 43mW/chip, 0.33mW/ADC (90μA+10 μA)
- Digital power: 538mW/chip at 400MHz clock, 160mA ☹
- Digital power can be reduced to 40mW ☺ (factor 14!) by reducing digital supply and improving flip-flop design
- In 180nm technology digital power would be only 12mW

Integrating pixels with SF readout – experimental results

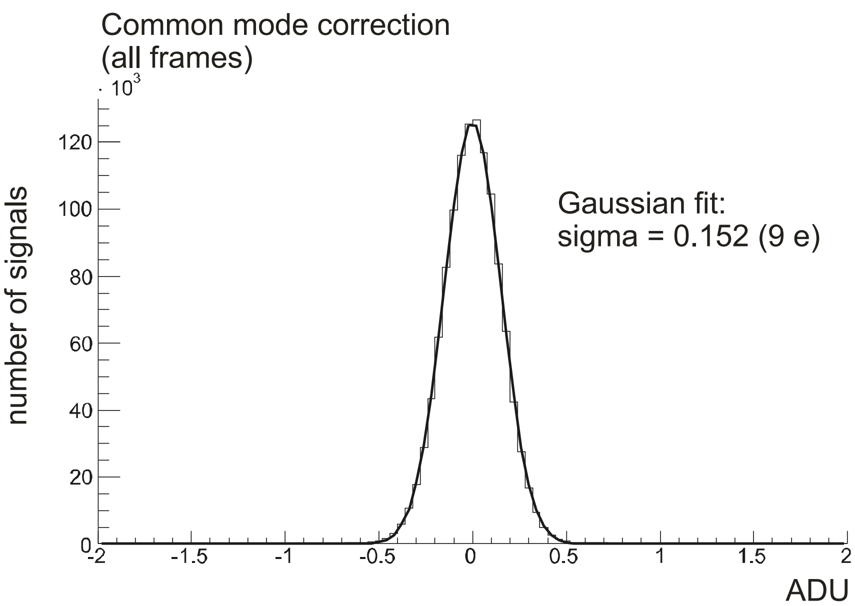


The spectrum has been measured with ^{22}Na beta source at room temperature
Most probable cluster signal: 2905e
Most probable single pixel signal ~1660 e
Noise: 31e
SNR single pixel = 54
SNR cluster signal to single pixel noise = 94
Integration time 160 µs

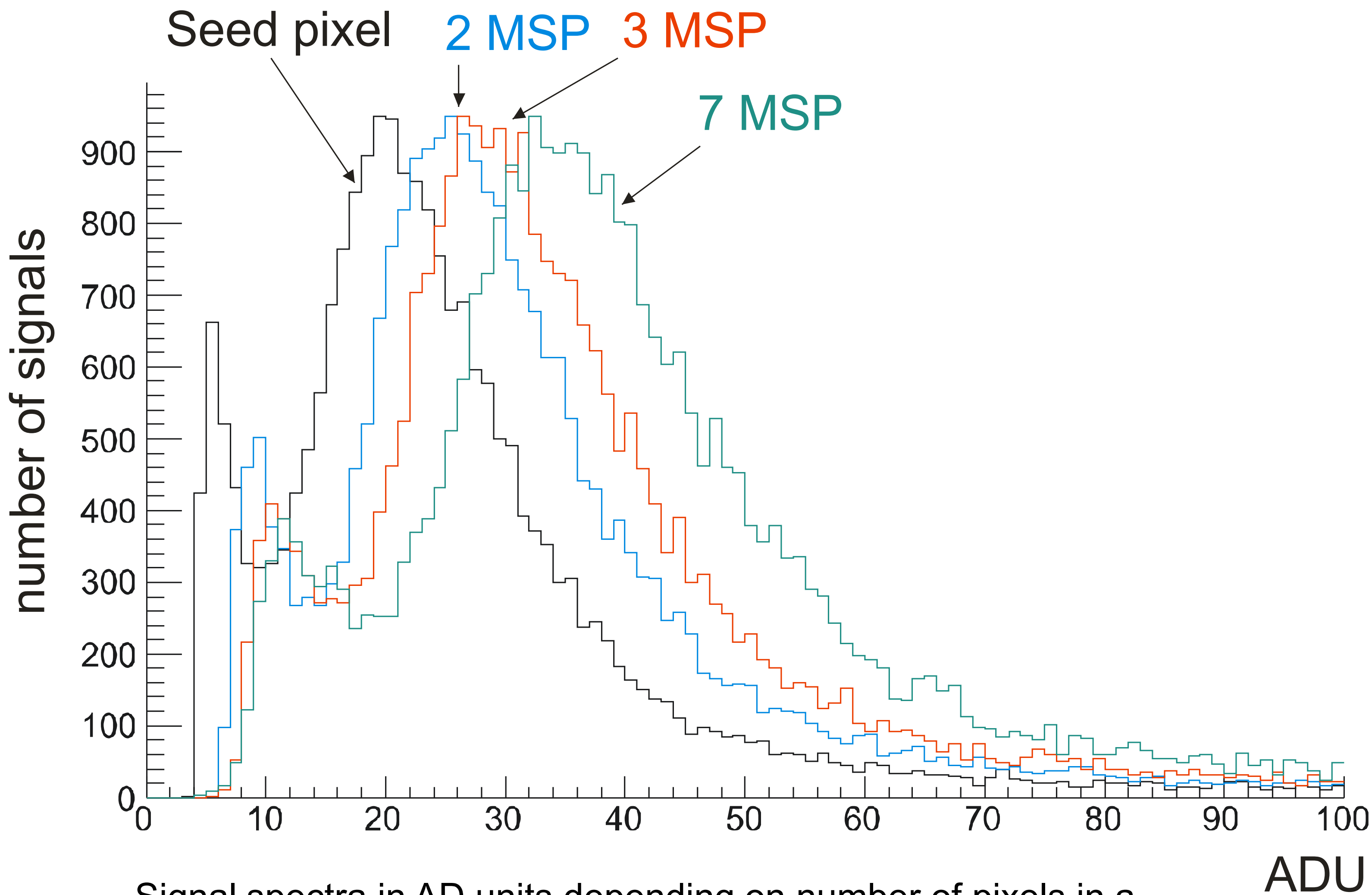
Noise measurement



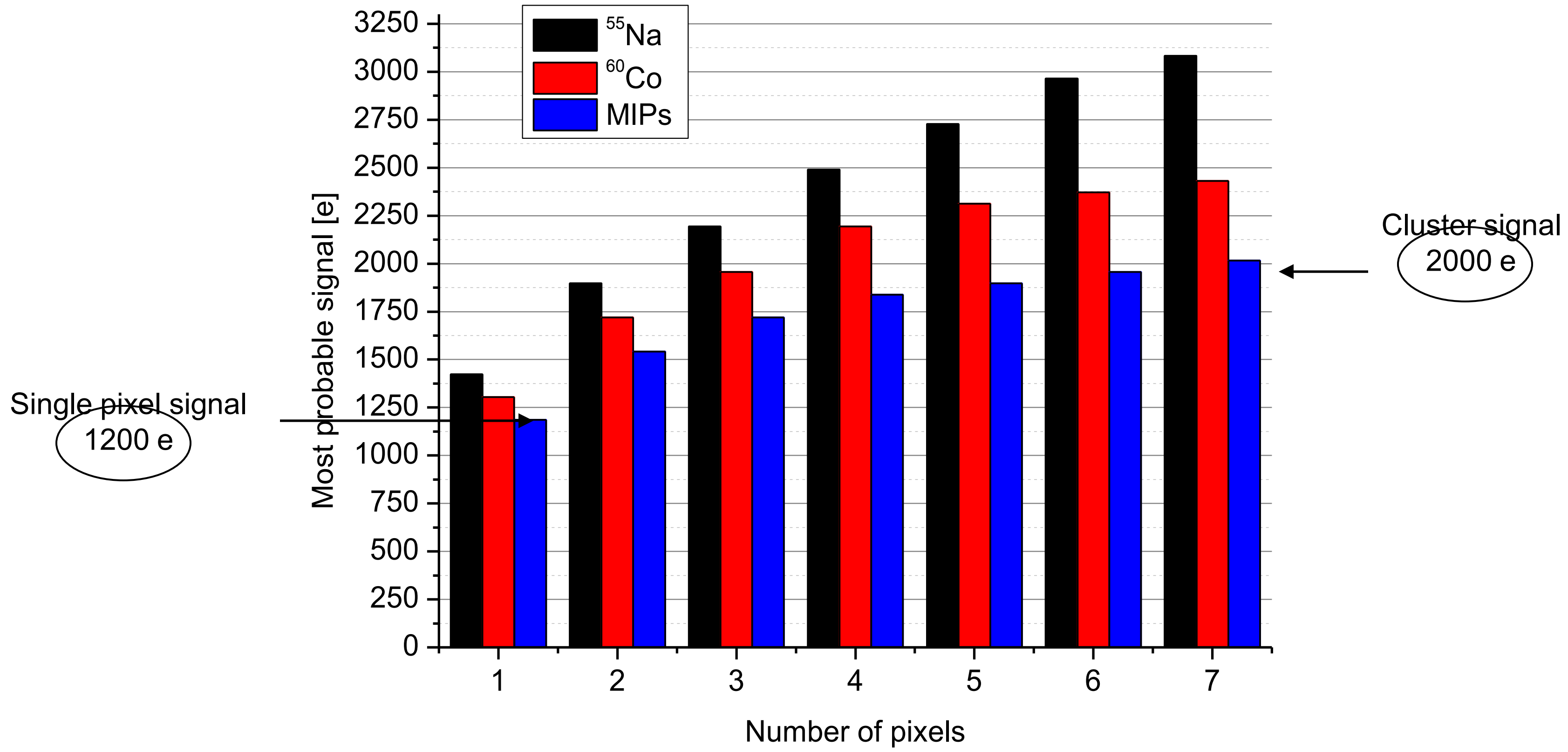
Base line noise – the pixel signals corrected for pedestal distribution,
all pixel in one frame are shown



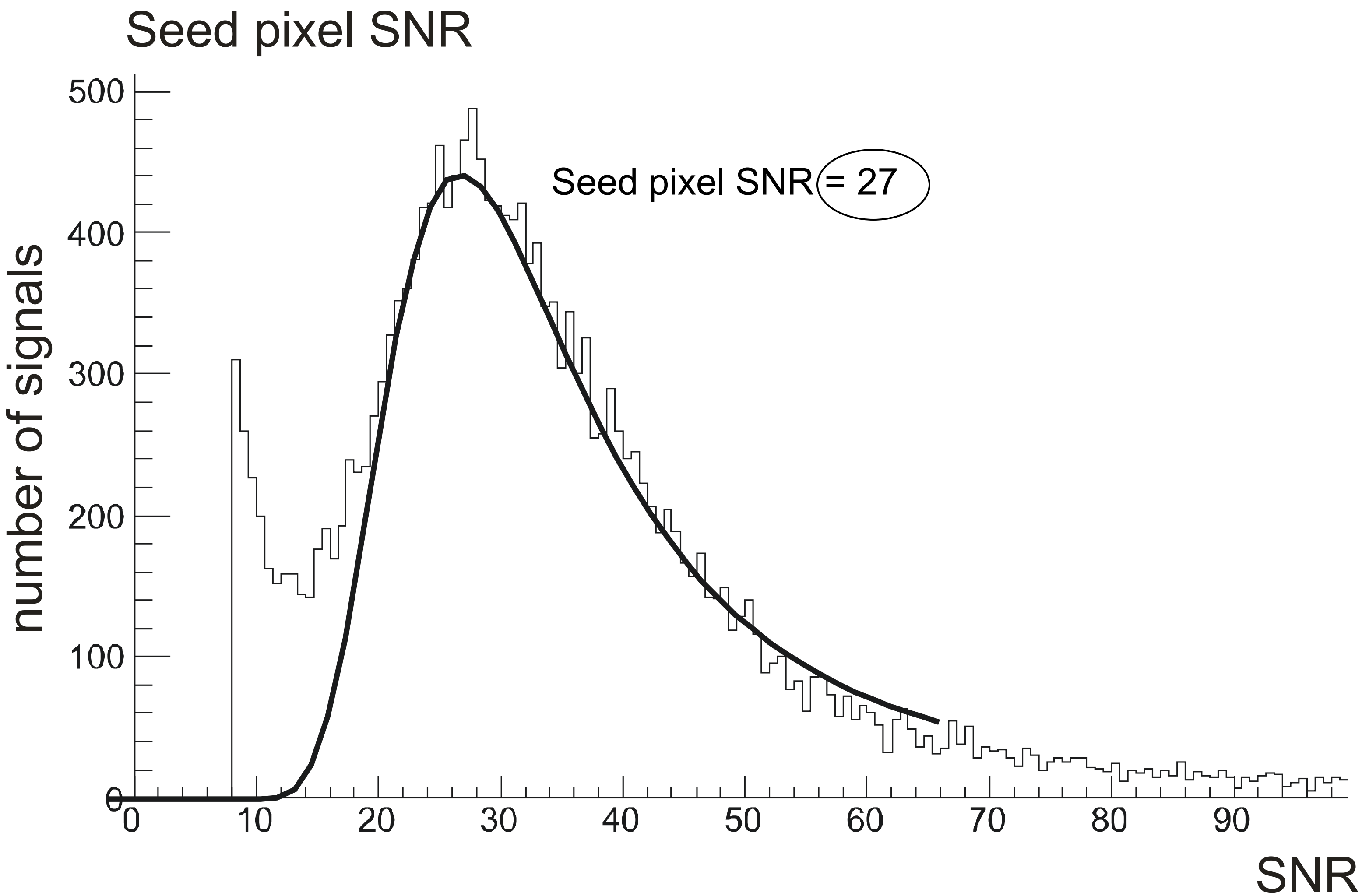
Common mode noise –
common mode correction values for all frames and rows

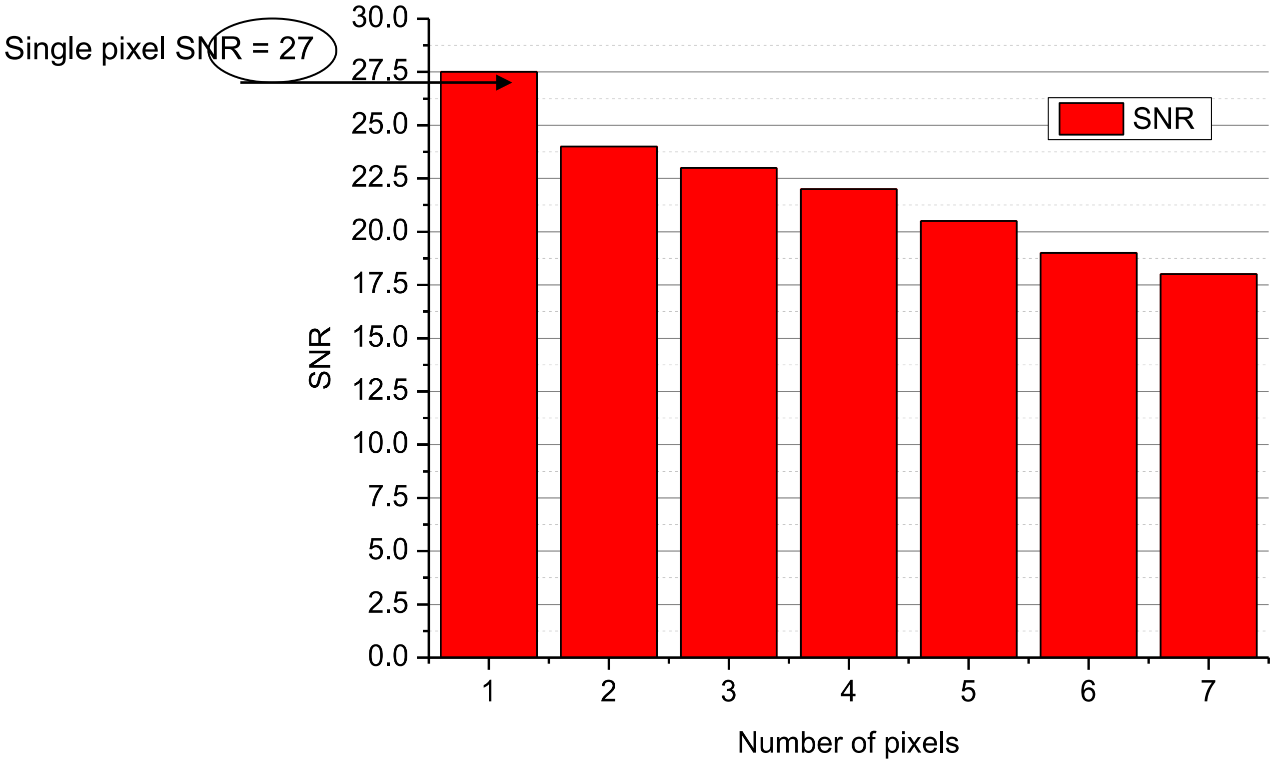


Signal spectra in AD units depending on number of pixels in a cluster



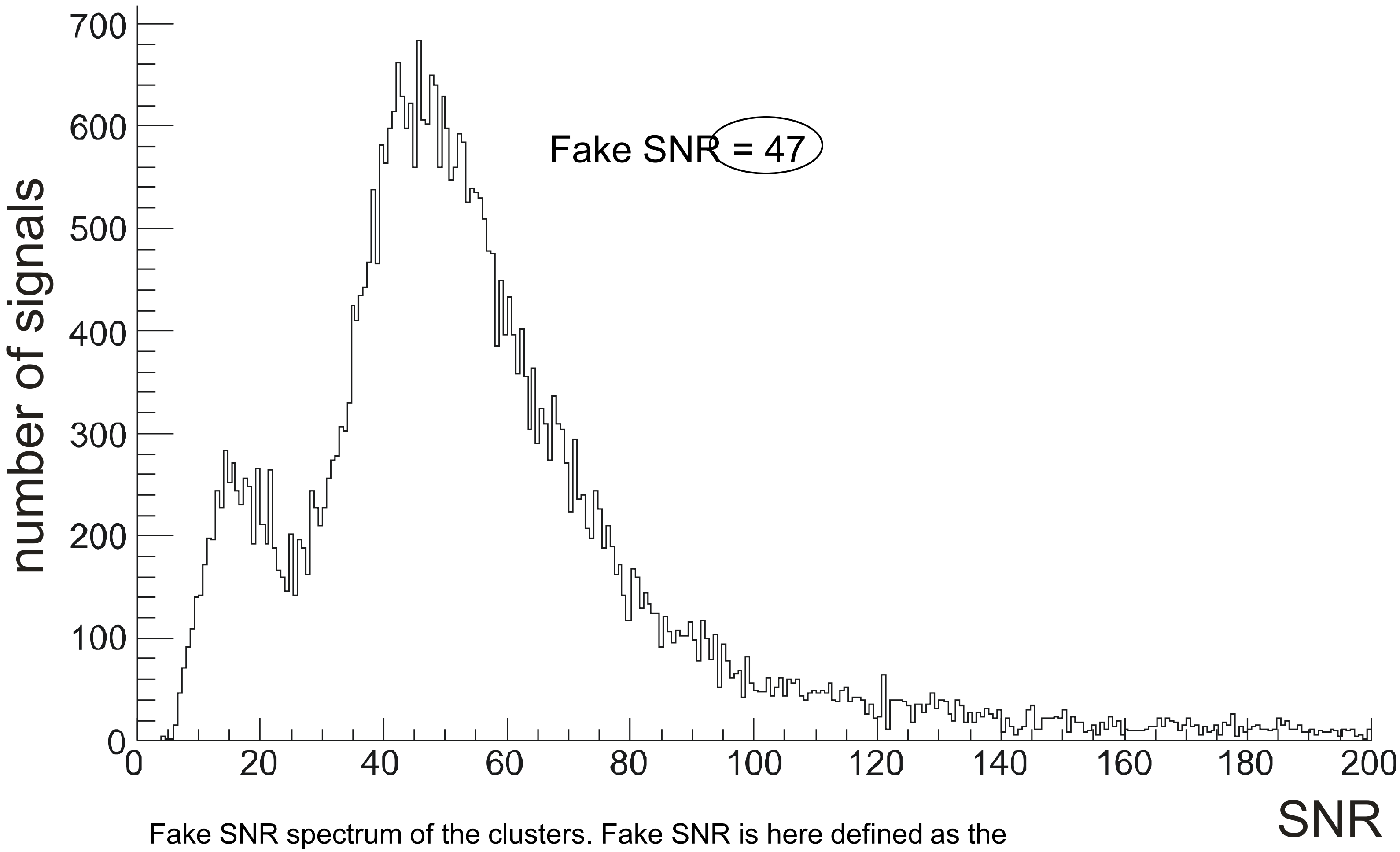
High energy particle signals depending on number of pixels in cluster


Seed pixel SNR
number of signals
500
400
300
200
100
0
Seed pixel SNR = 27
0
10
20
30
40
50
60
70
80
90
SNR



Cluster signal to noise ratio (MPX) vs. number of pixels in cluster

SNR as cluster signal over seed pixel noise



Fake SNR spectrum of the clusters. Fake SNR is here defined as the total cluster charge divided by the seed pixel noise.

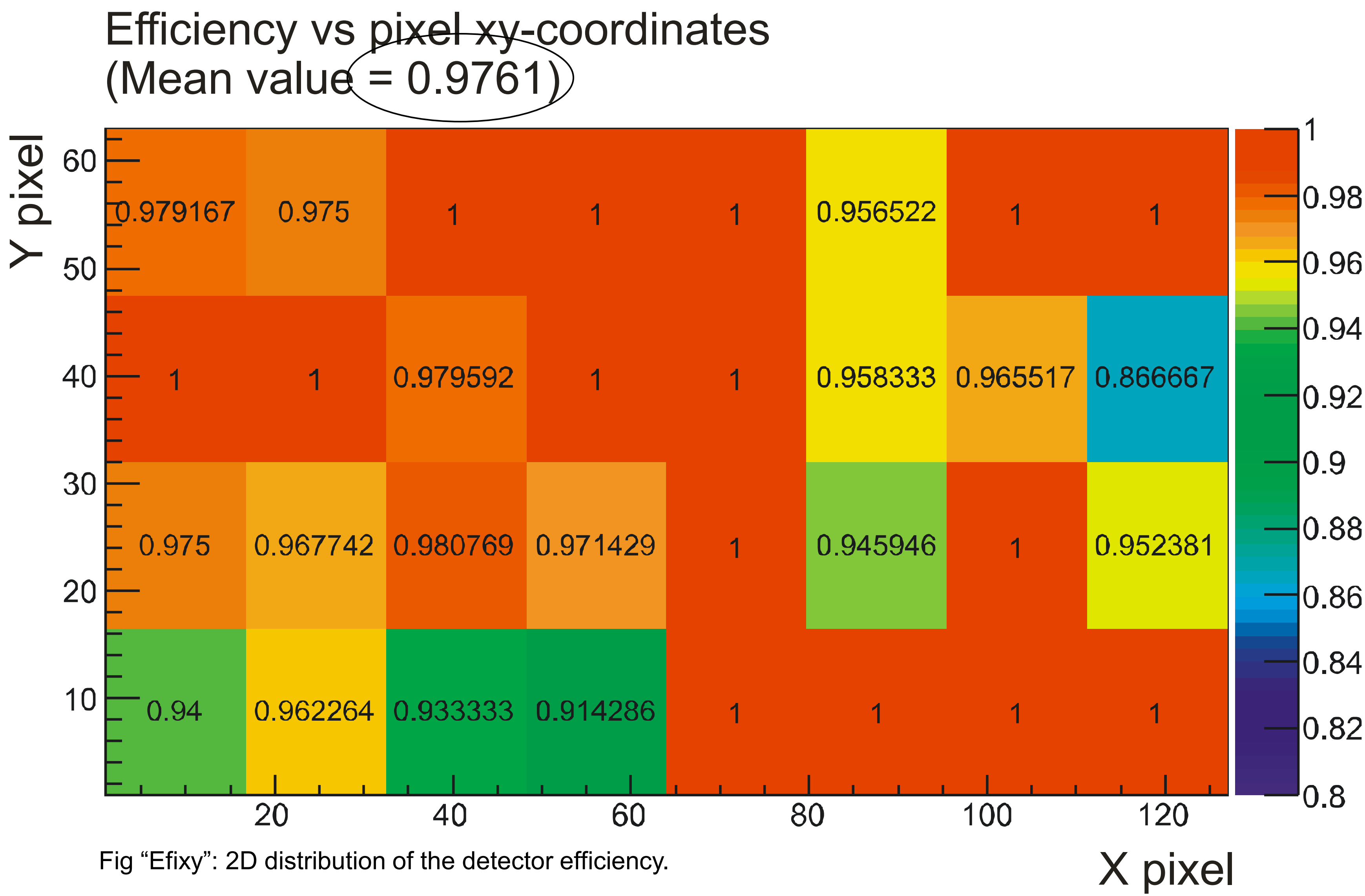
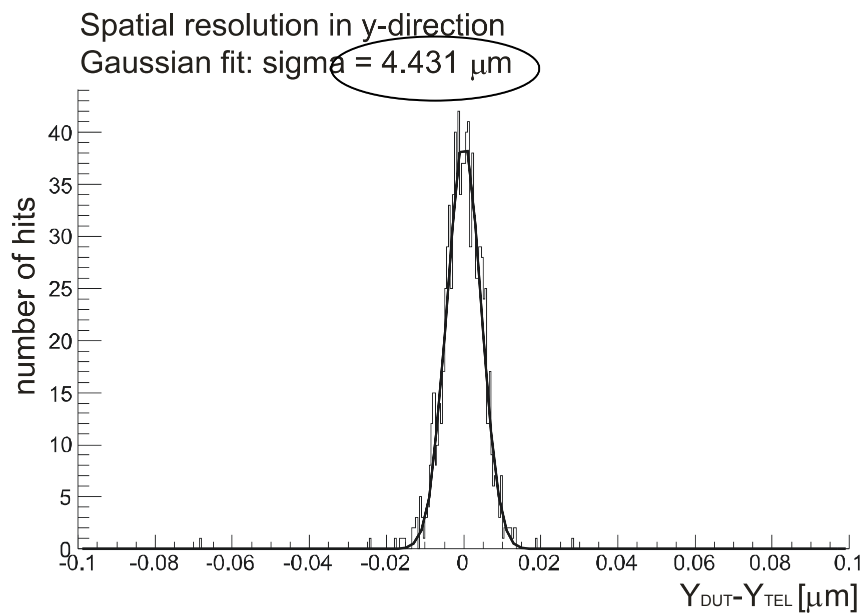
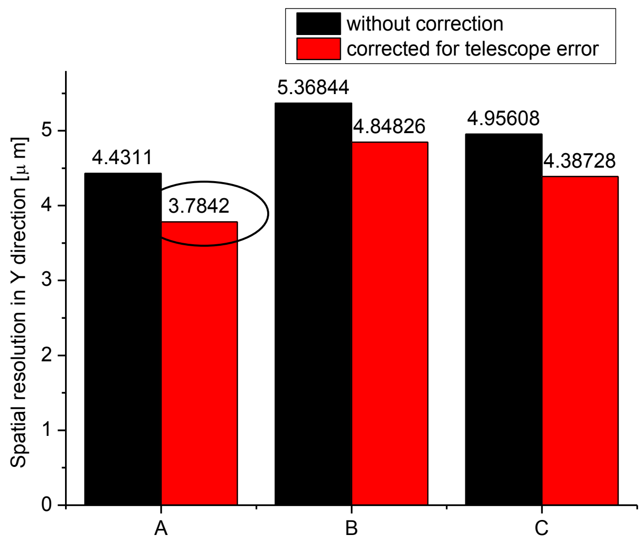


Fig "Efixy": 2D distribution of the detector efficiency.



Distribution of the differences between the measured and the fitted y hit-coordinate.



Spatial resolution of the DUT in y direction. The black rectangles show the measured and red rectangles the exact spatial resolutions of the DUT corrected for the telescope error. In the cases A and B we used the eta-corrected CoG, and in the case C only the raw CoG corrections. The corrections were calculated only with 3 most significant pixels of a cluster in the case B.

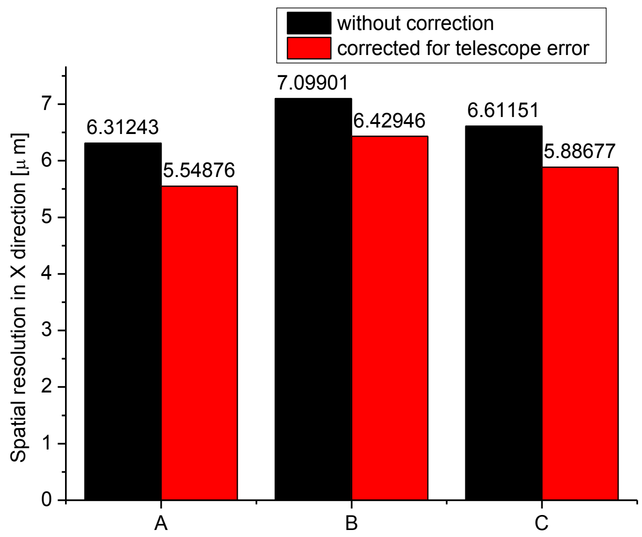
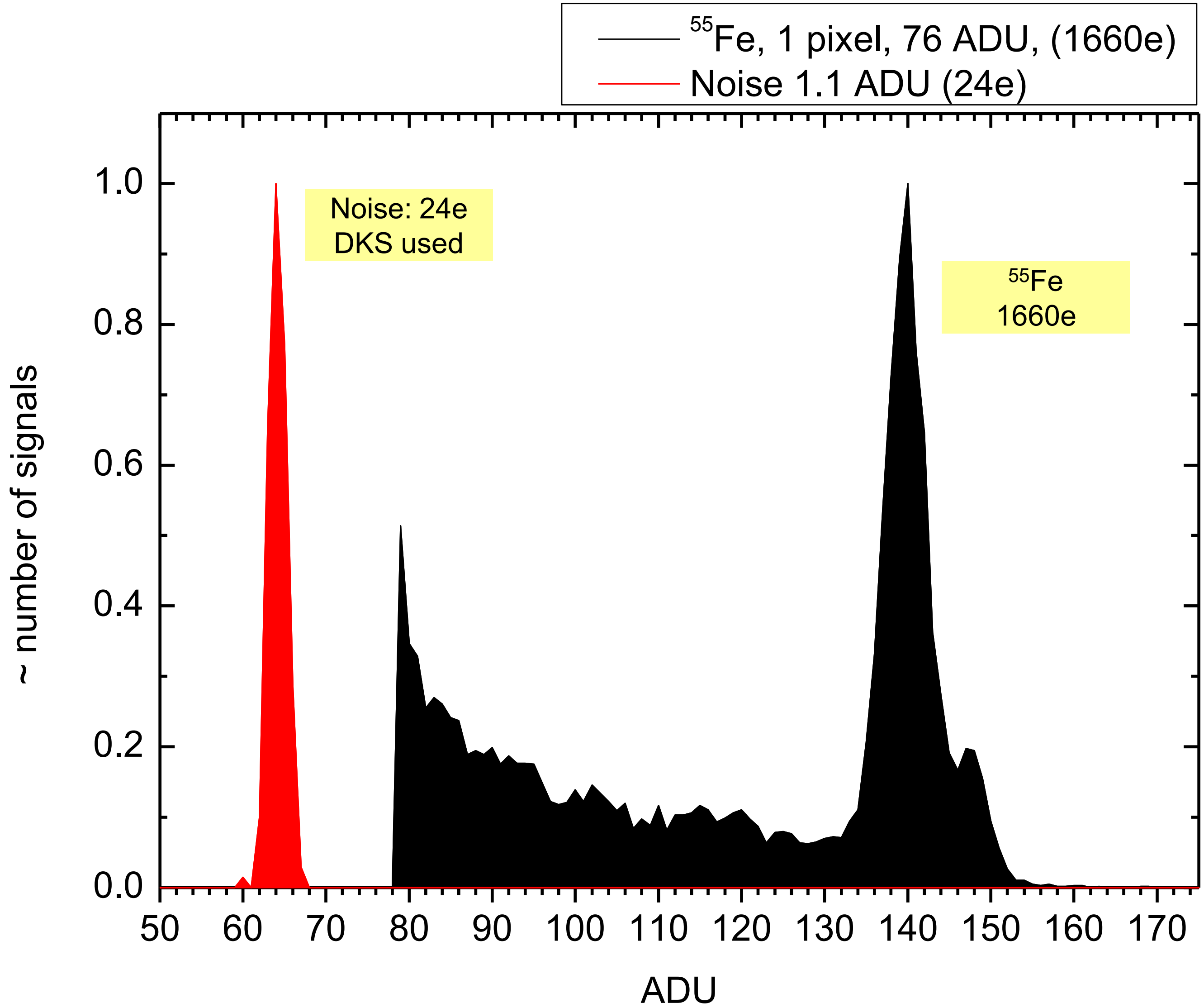


Figure „ResAllx“: Spatial resolution of the DUT in x direction.

Integrating pixels with voltage amplification – experimental results

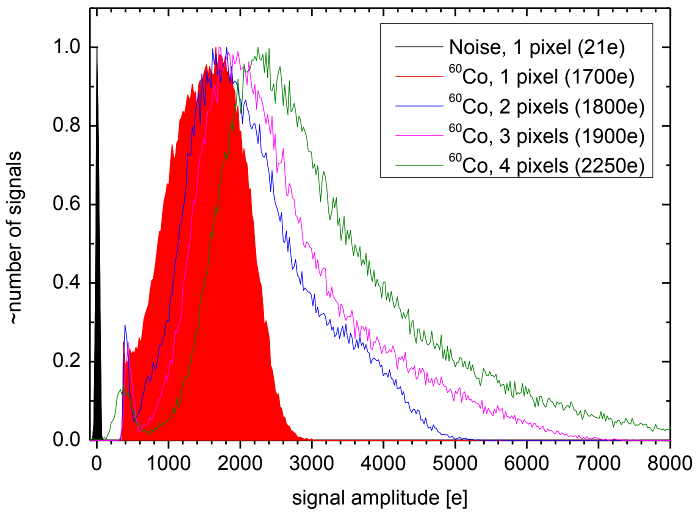


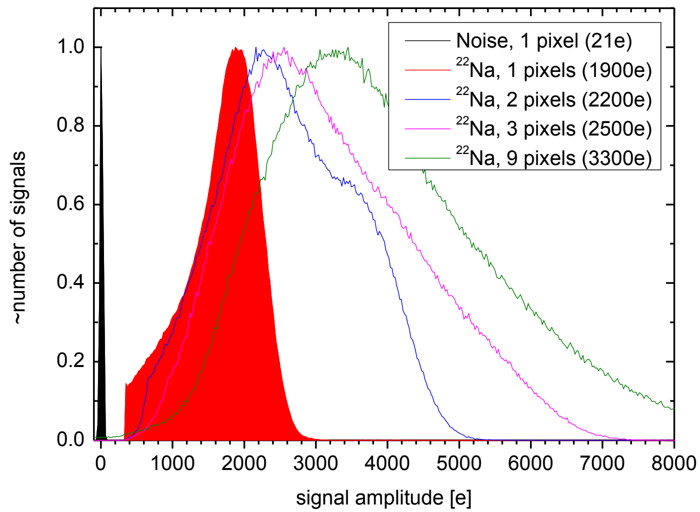
Sensor has been cooled with a small Peltier cooler: T ~ (?) 10C

High-energy beta spectra

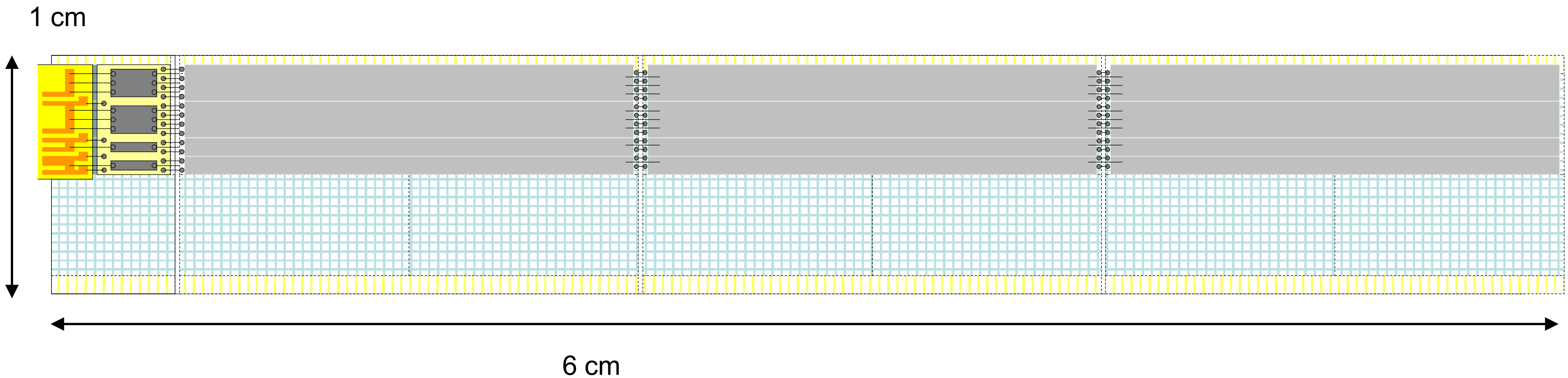
^{60}Co betas (about 10% higher signals than MIPs)
Seed signal: 1700e
Cluster signal: 2250e
Noise: 21e
Seed SNR: 81
Cluster signal/seed noise: 107

^{55}Na betas
Seed signal: 1900e
Cluster signal: 3300e
Noise: 21e
Seed SNR: 90
Cluster signal/seed noise: 157





Estimated MIP seed pixel SNR: 57
Cluster signal/seed noise: 95



Half module size 1x6cm
Pixel size 40x40µm
Pixels 250x1500
RO time 80µs/matrix
Resolution 7(!) bit/pixel (count up to 125) – if CDS pixels are used, we need probably only 6 bits
Power 960mW/module (150mW/cm2 (80 analog + 70 digital))
Data output width 7x12 = 84 bits @ 400Mbit
180nm Technology:
Power 210mW/module (35mW/cm2 (14 analog + 21 digital))
20µs/matrix possible – power 140mW/cm^2

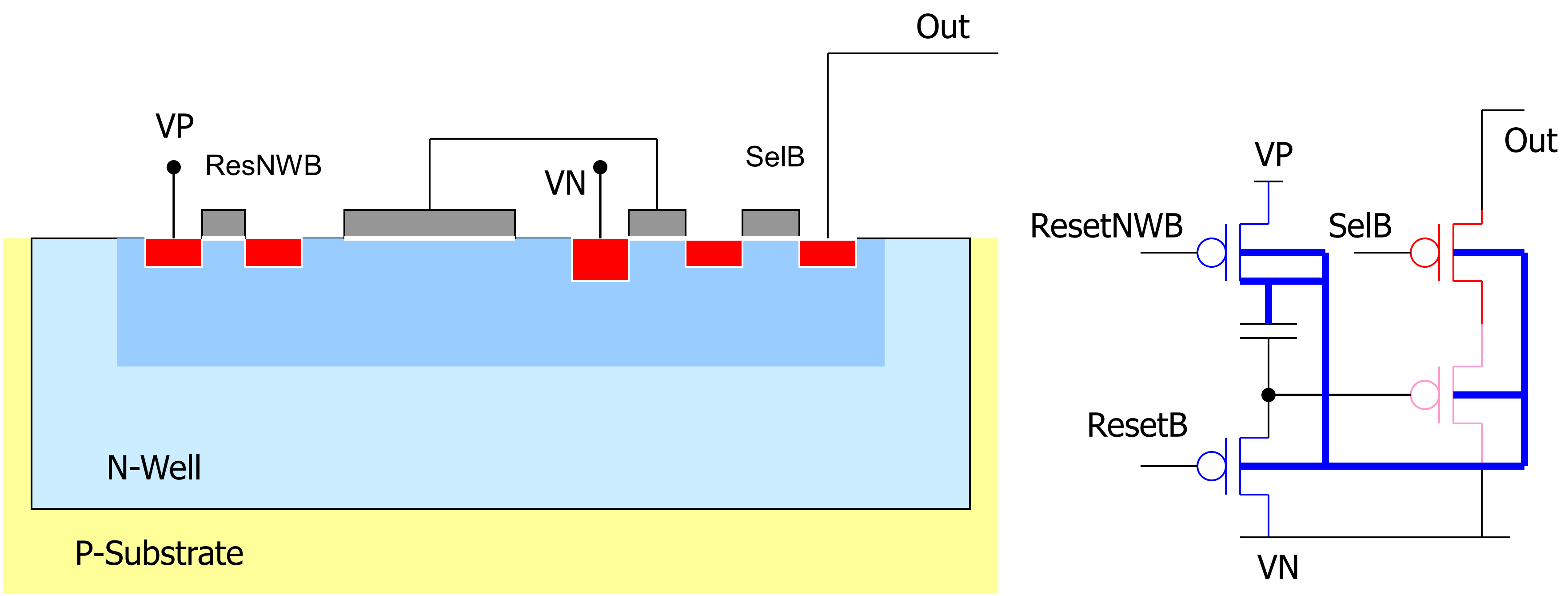
- We have developed a new pixel sensor structure (smart diode array) for high energy physics that can be implemented in a high voltage CMOS technology.
- The sensor has 100% fill-factor and can have in-pixel electronics implemented with p- and n-channel transistors.
- We have tested the sensor structure in various variants:
- 1) Sensor with in-pixel hit detection and sparse readout,
- 2) Sensor with fast rolling-shutter readout and simple pixel electronics
- We have done three test-beam measurements with good results.
  - Detection efficiency 98%
  - Seed Pixel SNR ~ 27
  - Cluster Signal/Seed Pixel Noise ~ 47
  - Spatial resolution ~ 3.8 μm
- We have irradiated the chips with neutrons, protons and x-rays to test radiation tolerance.
- After irradiation with protons up to very high fluence 10^{15} n_{eq}/cm^2 and dose 300MRad, we have still very large SNR (>40) for high energy beta particles at nearly room temperatures (10C).
- We have submitted a new test-chip in 180nm technology
- We are planning an engineering run either in 350nm or in 180nm technology, probably with two detectors, one for muon experiment (CMOS pixels) and one for electron microscopy (integrating pixels)

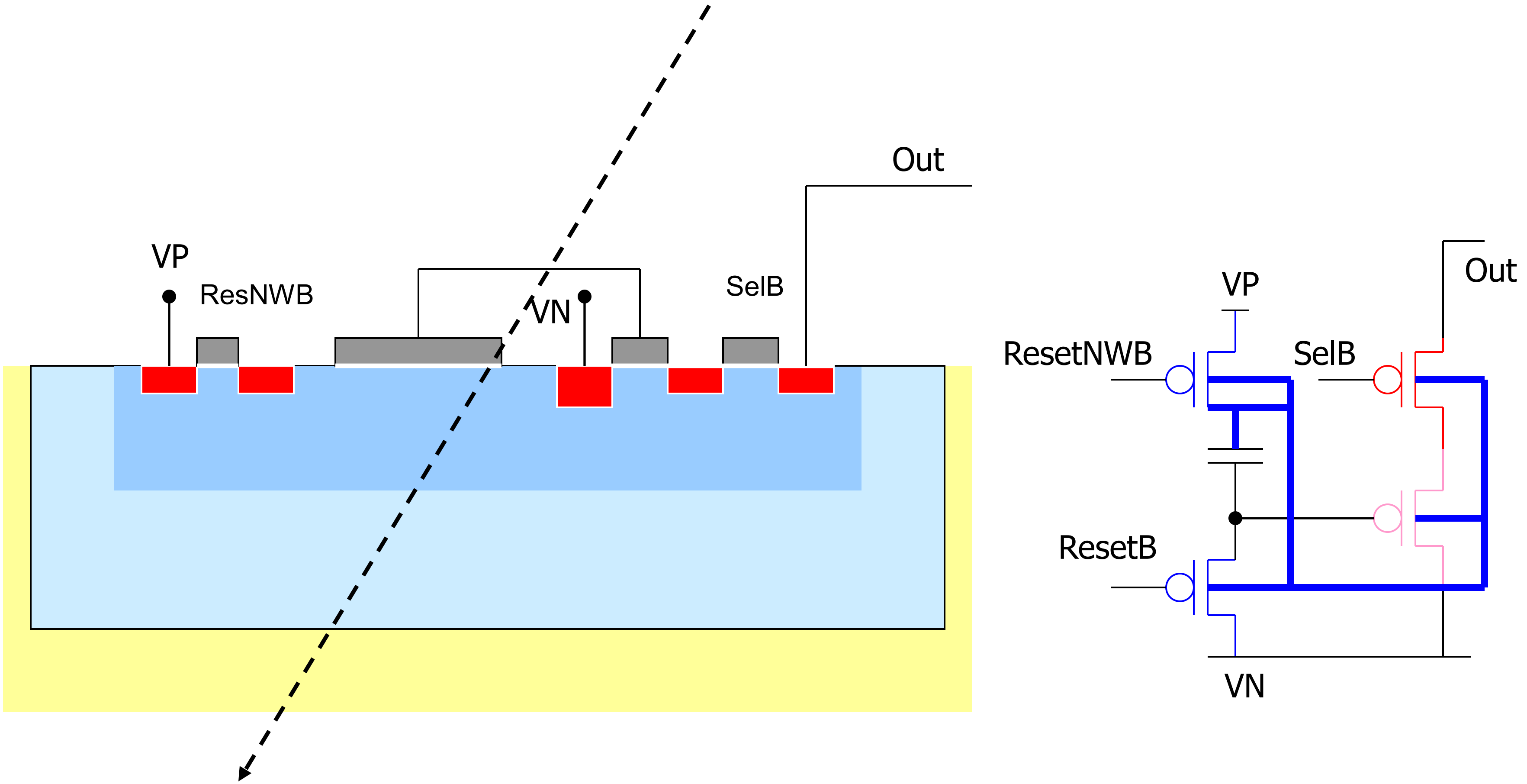
- Thank you!

- Backup slides

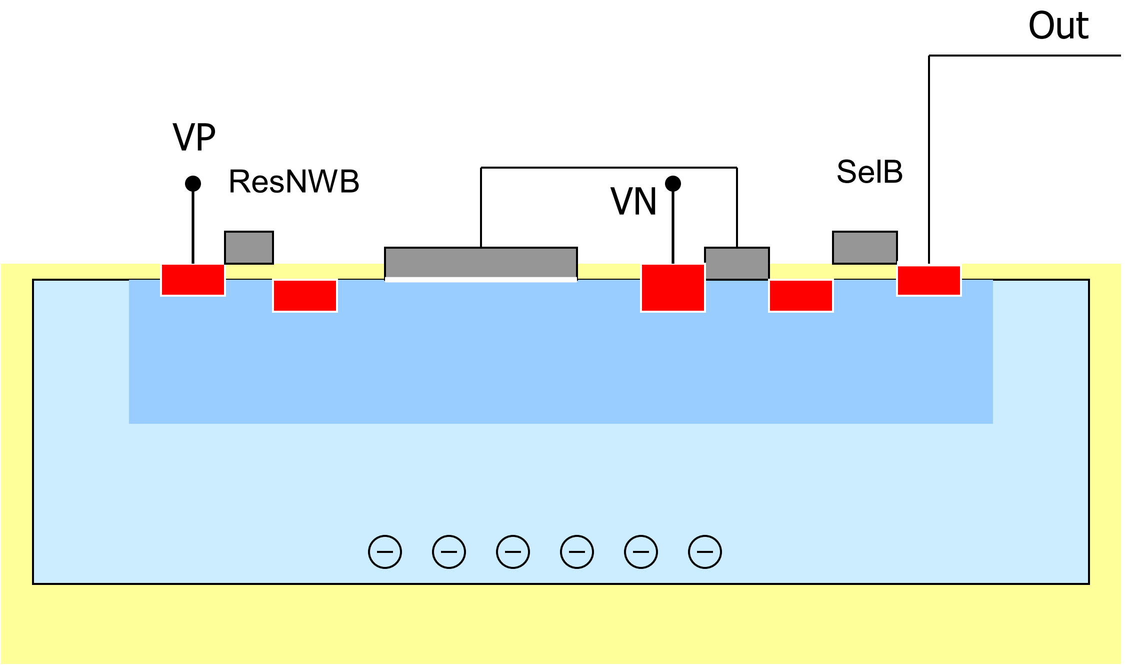
Integrating pixels with source follower readout

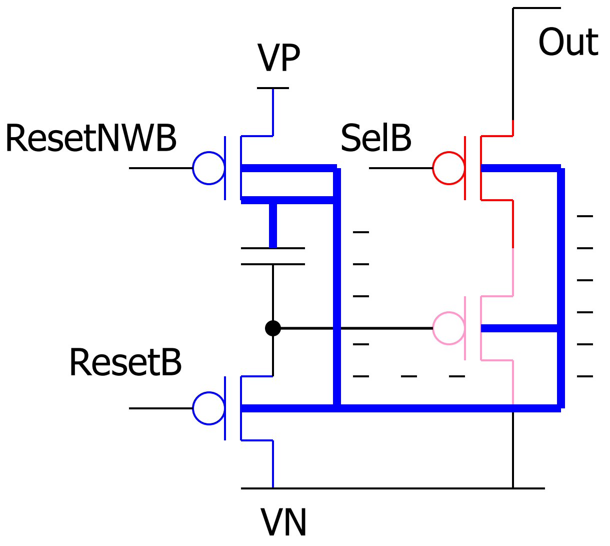
Pixels with SF RO – signal detection phase



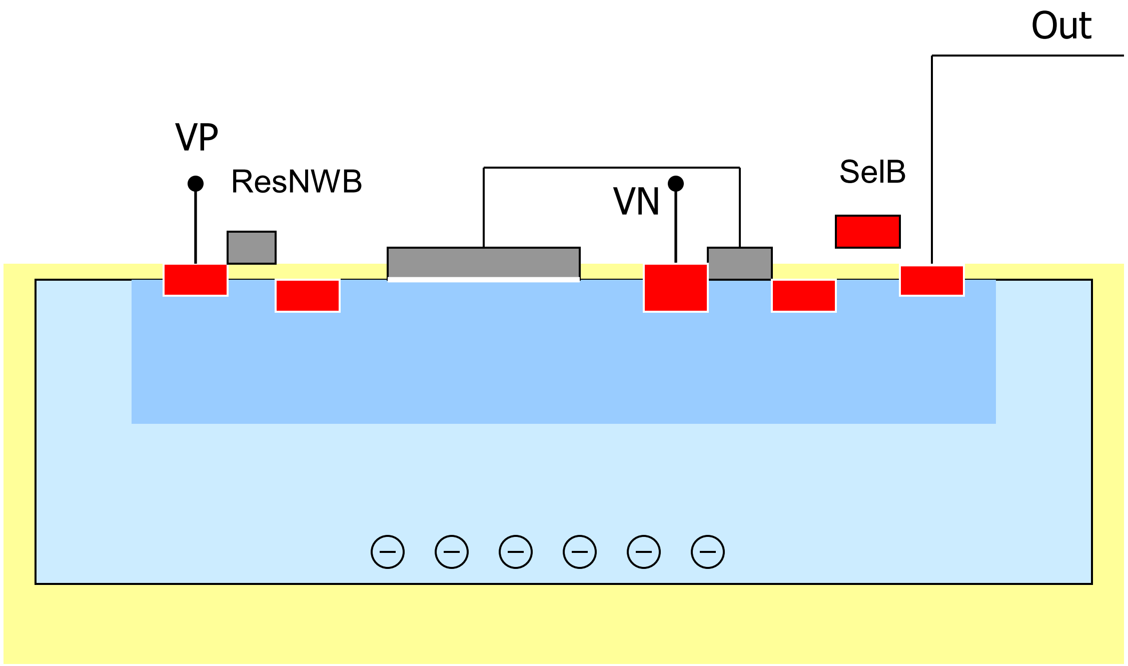

Out
VP
ResNWB
VN
SelB
VP
Out
ResetNWB
SelB
ResetB
VN

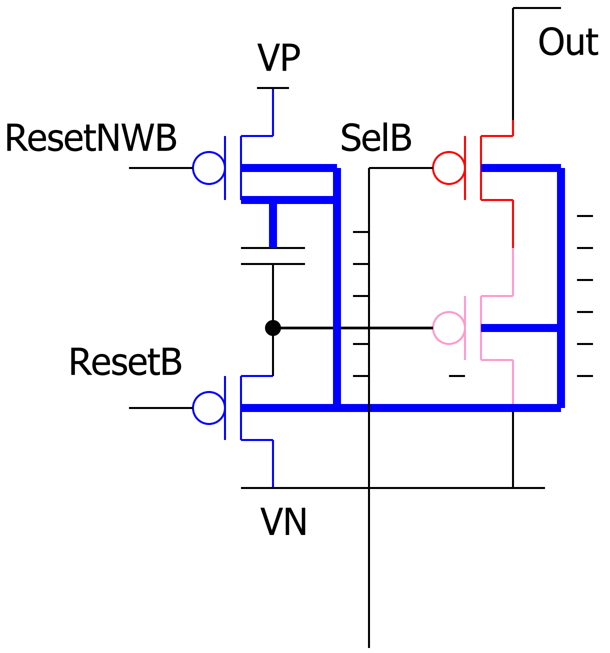
Charge collection

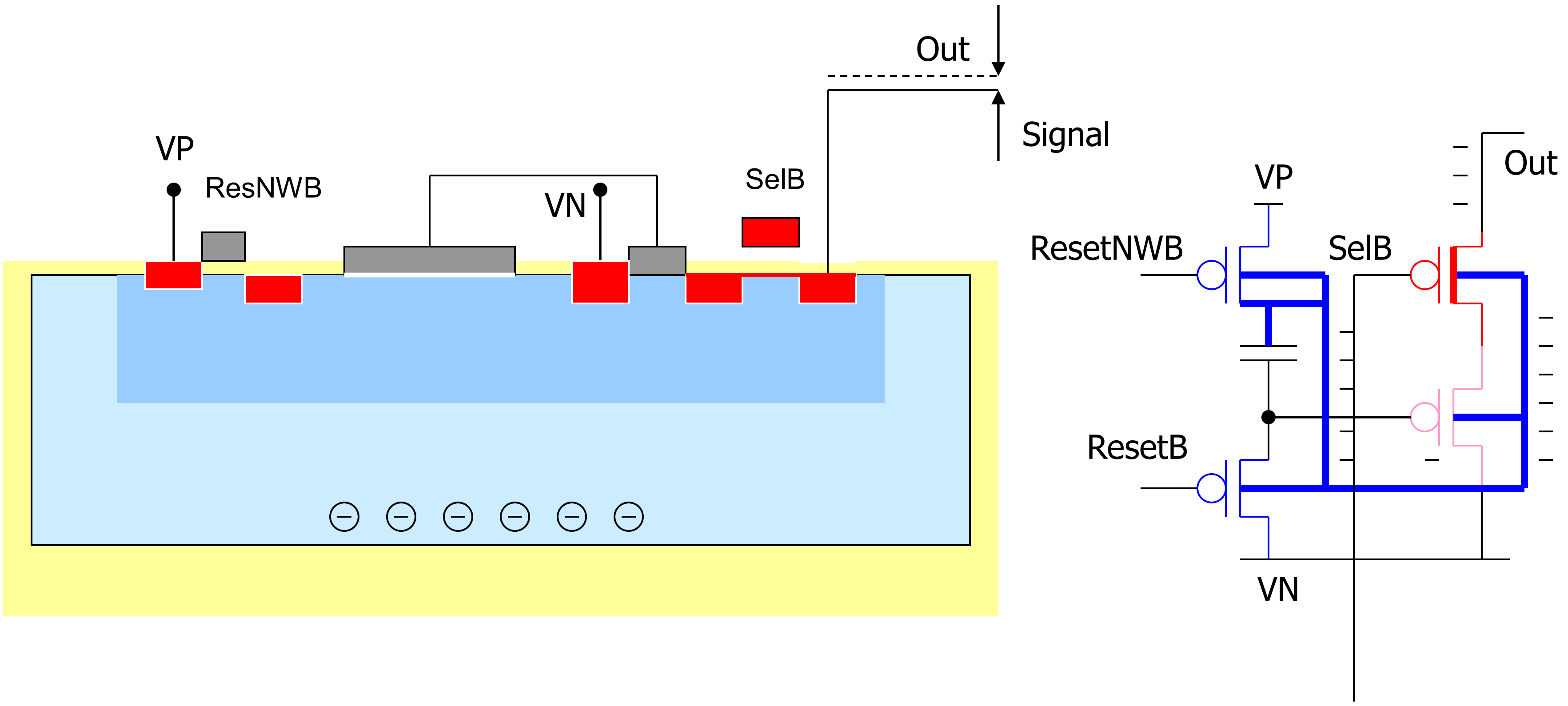




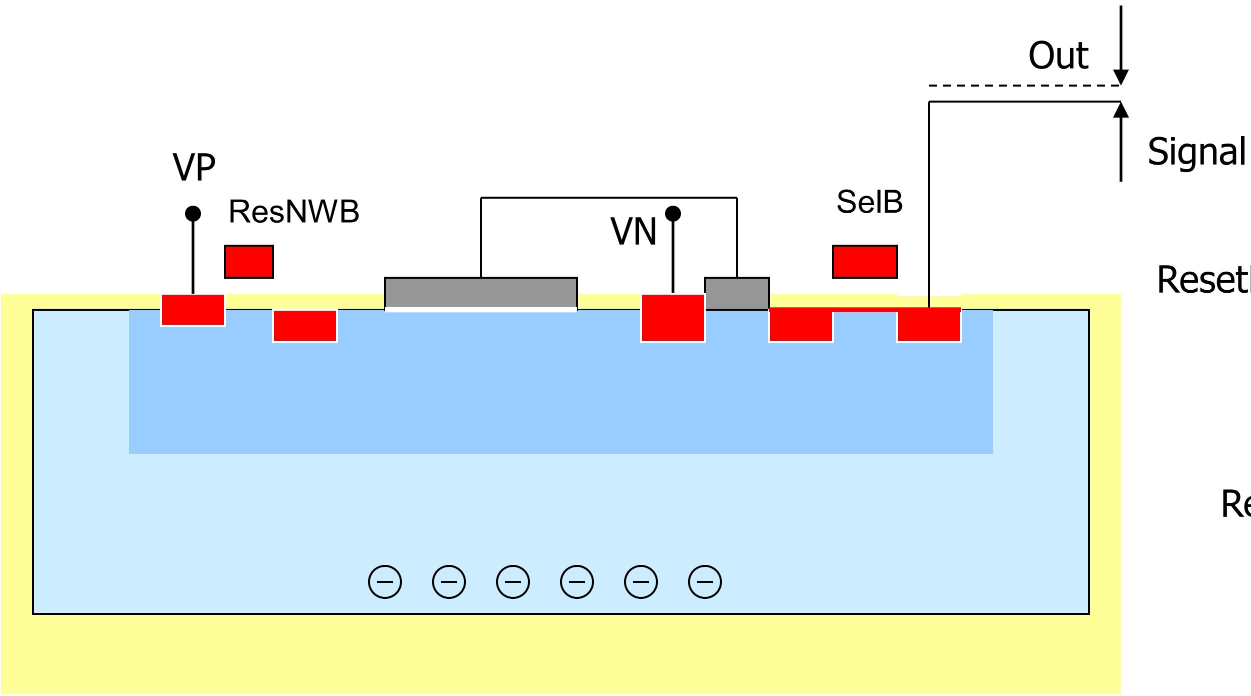
Readout phase

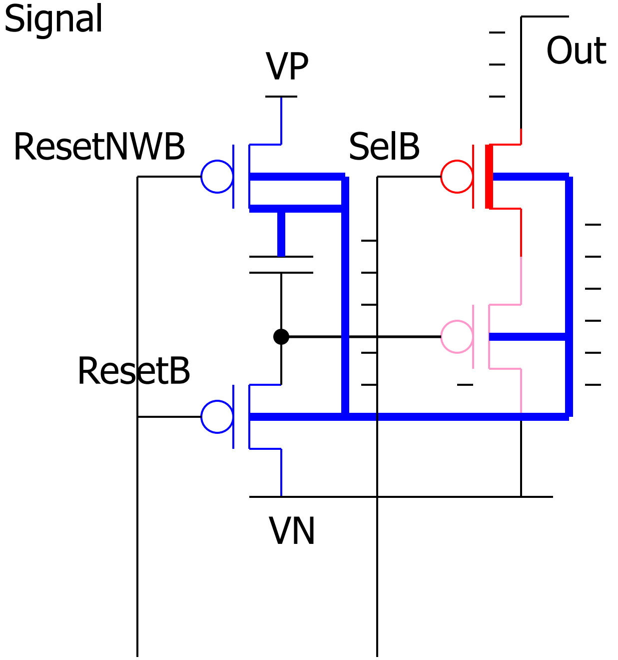




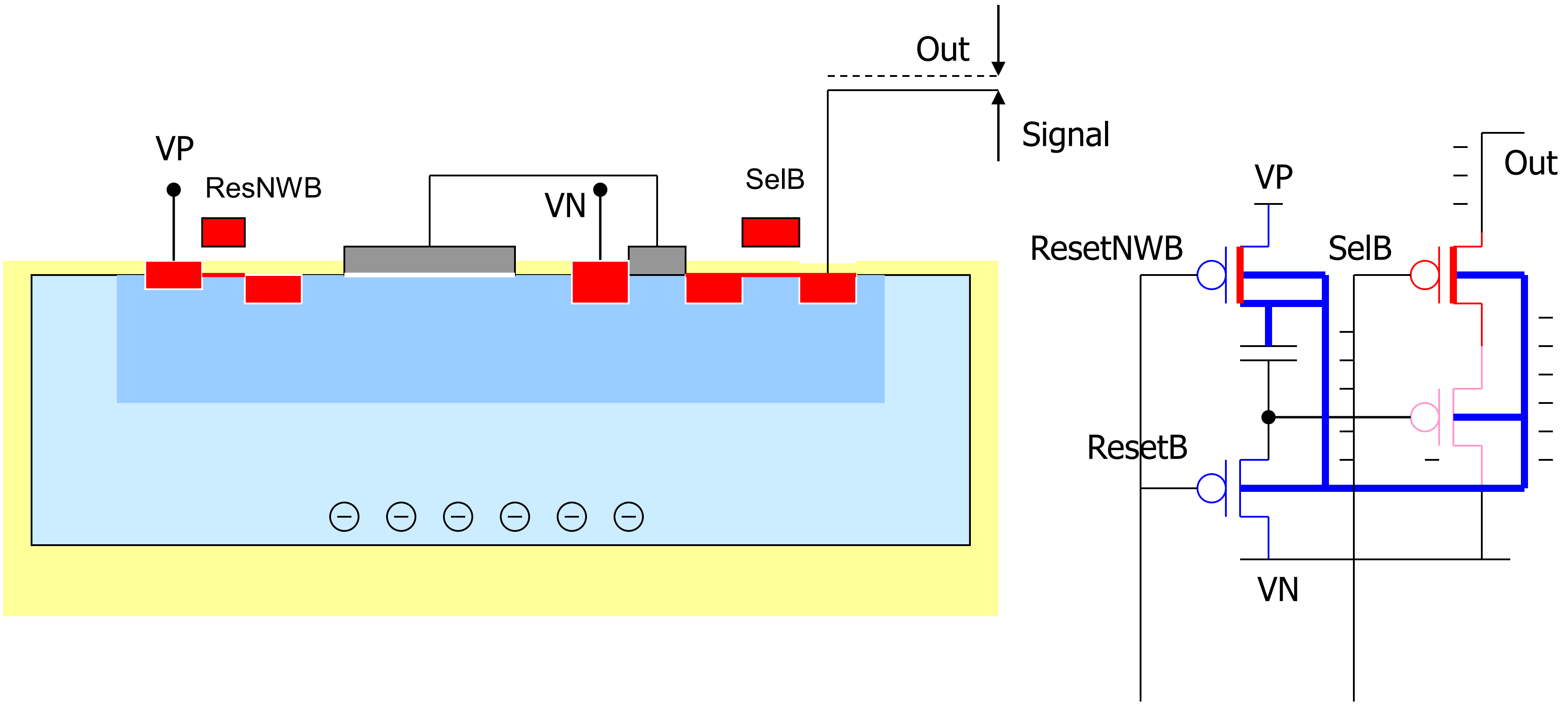

Out
Signal
VP
ResNWB
VN
SelB
VP
Out
ResetNWB
SelB
ResetB
VN

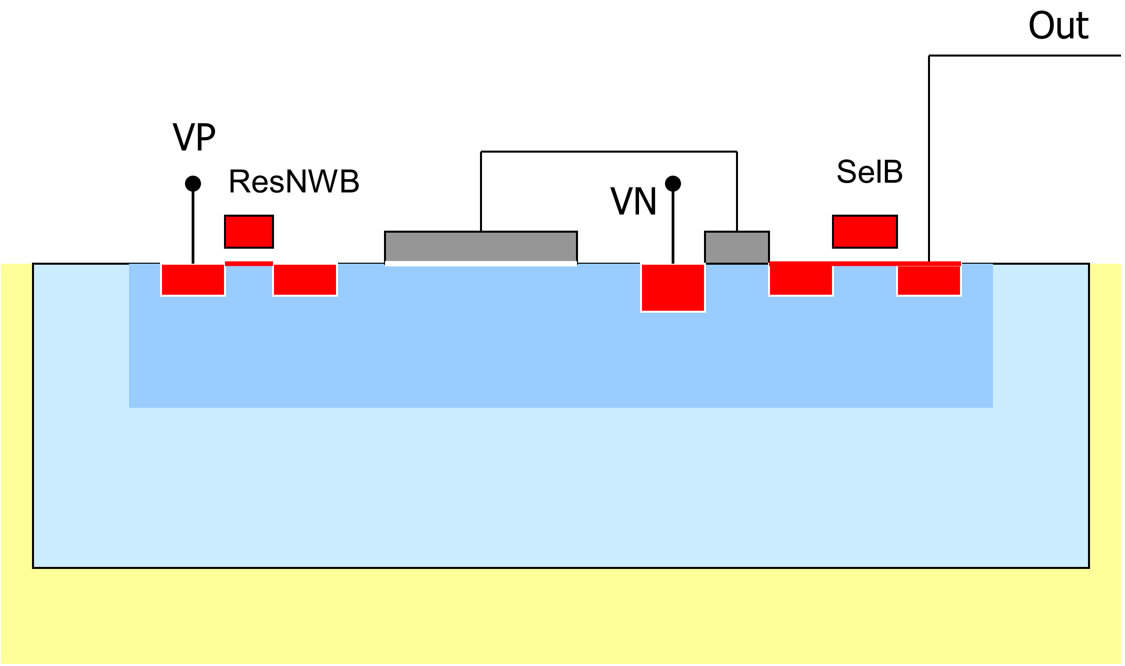
Reset

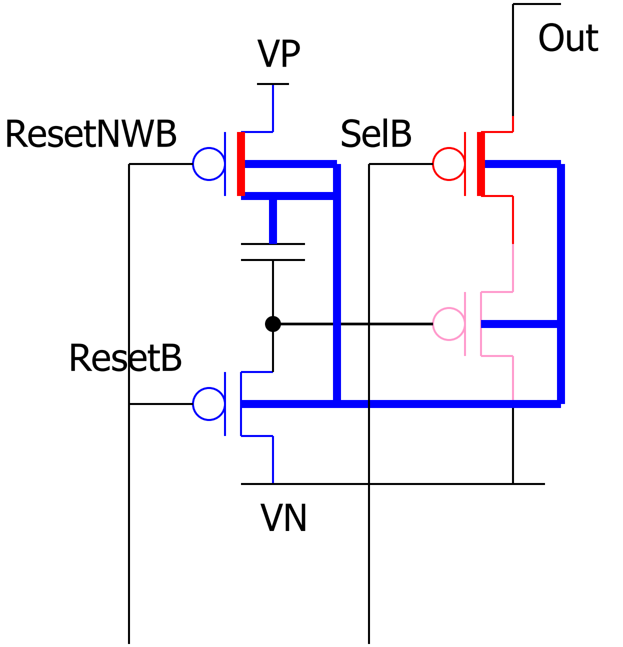

Out
Signal
VP
ResNWB
VN
SelB
ResetNWB
ResetB

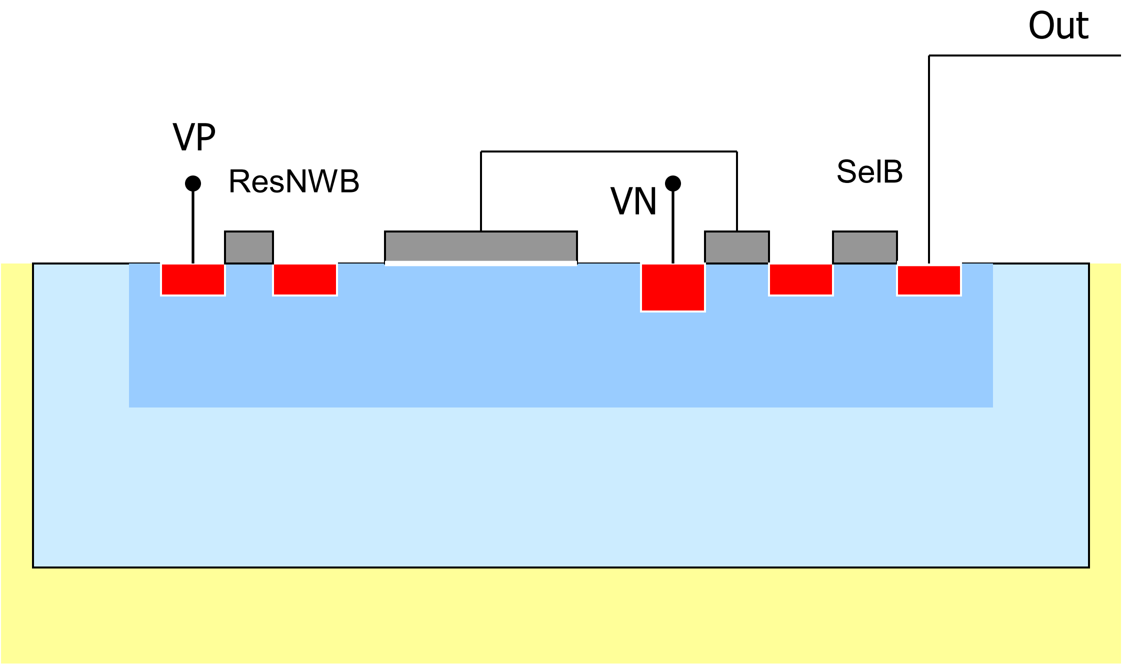

VP
Out
ResetNWB
SelB
ResetB
VN

Reset

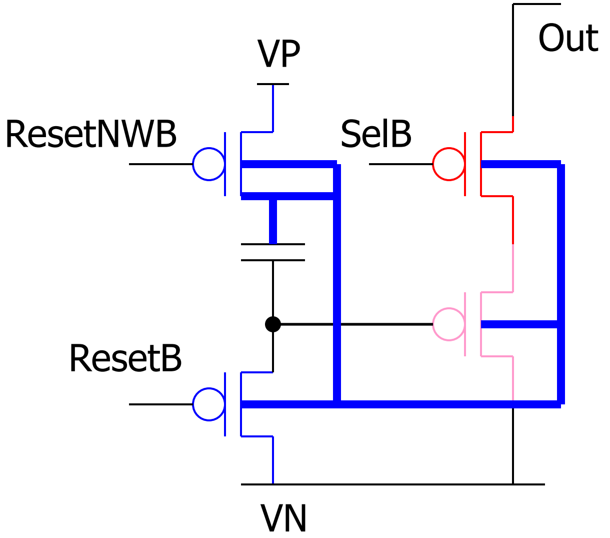



Out
VP
ResNWB
SelB
VN


Out
VP
ResetNWB
SelB
ResetB
VN



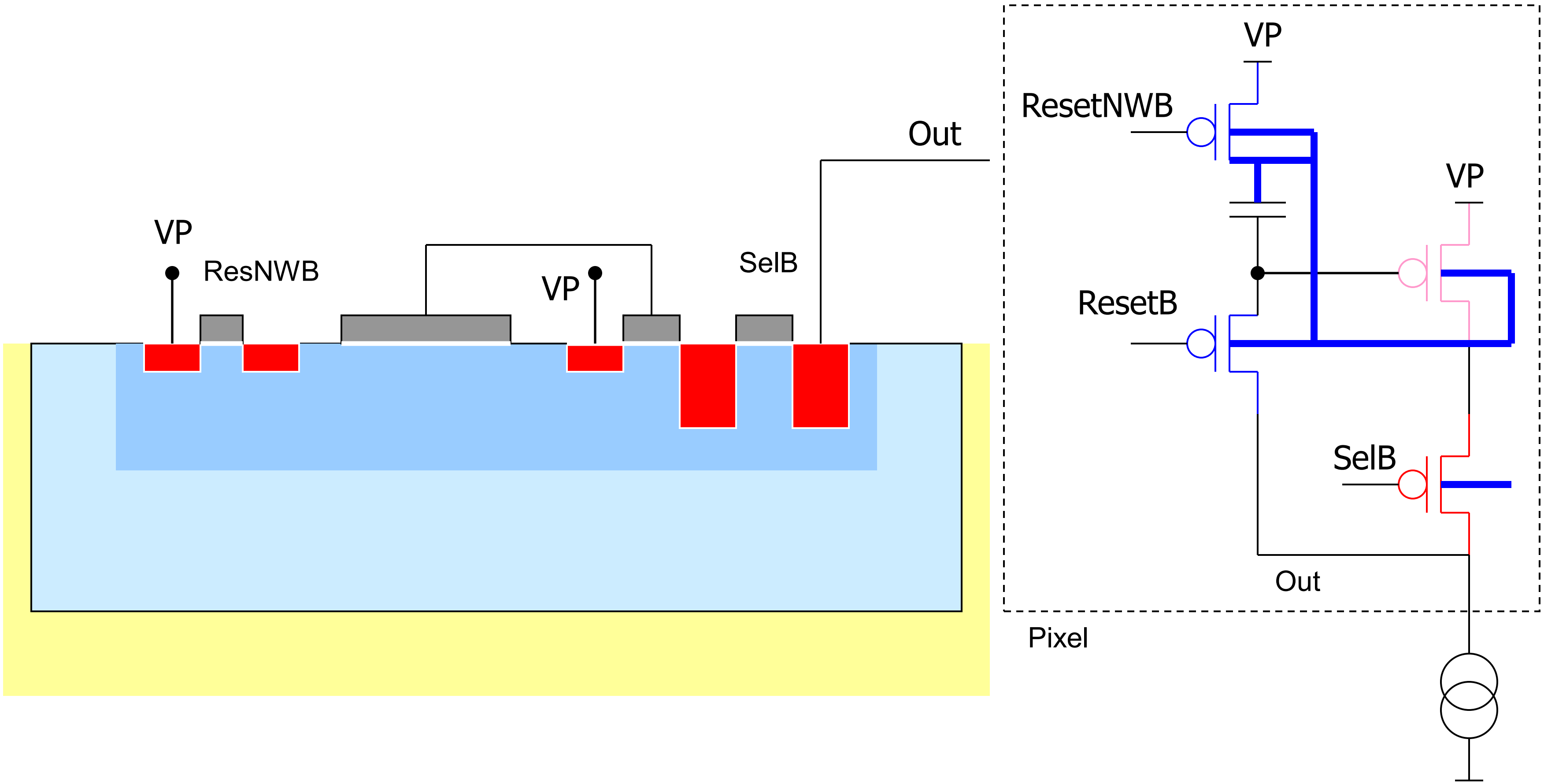
Out
VP
ResNWB
VN
SelB

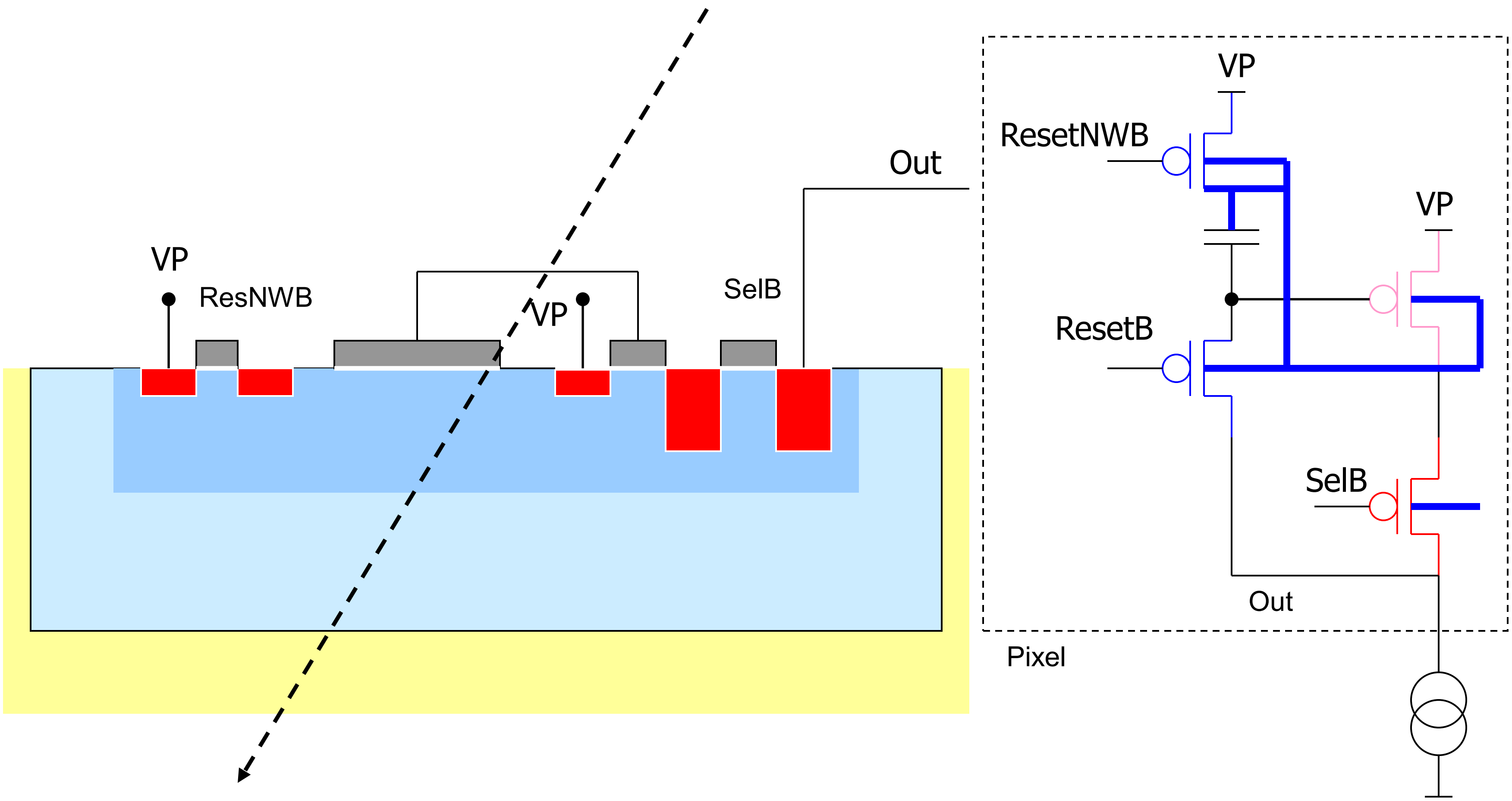


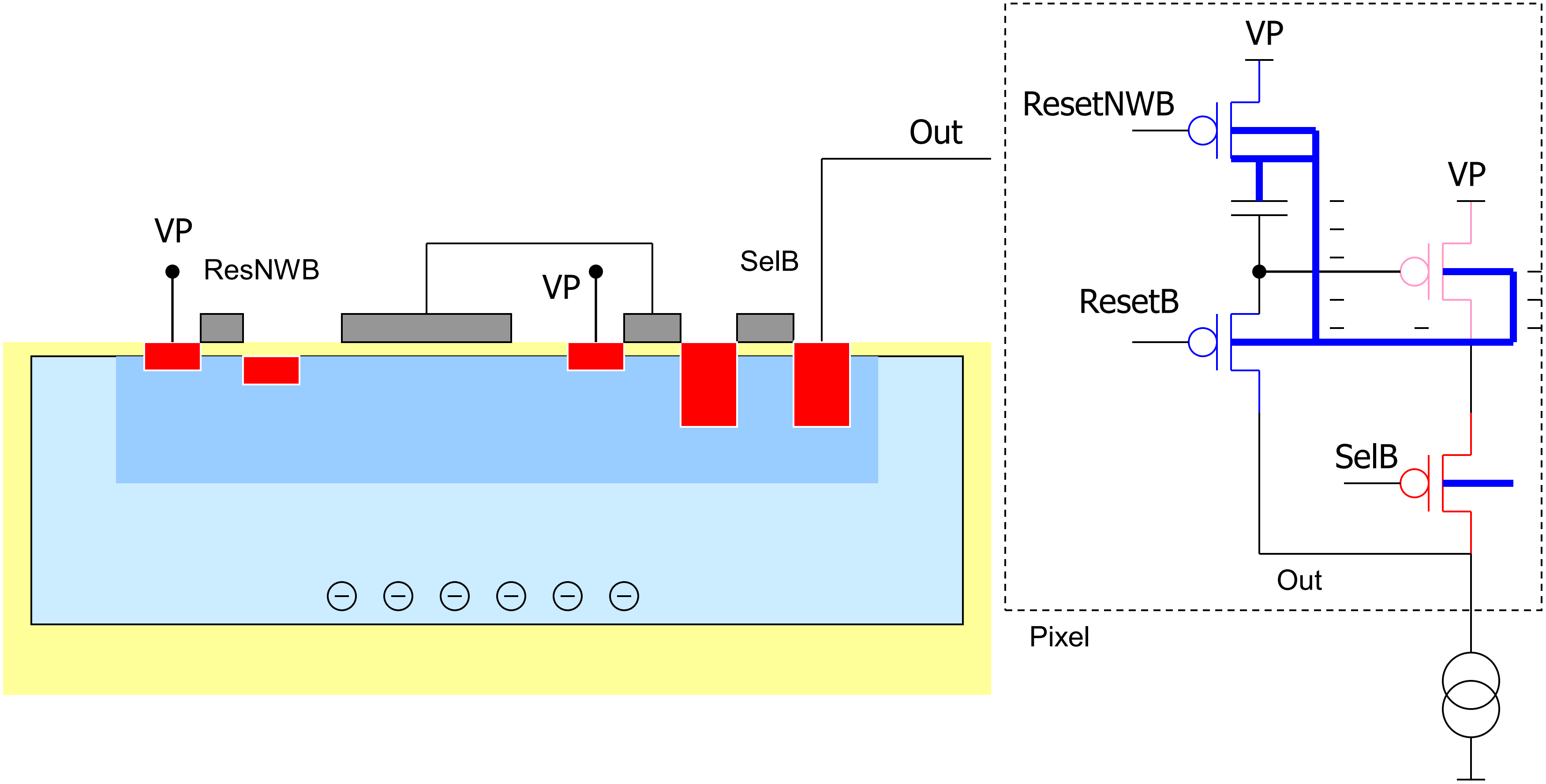
Out
VP
ResetNWB
SelB
ResetB
VN

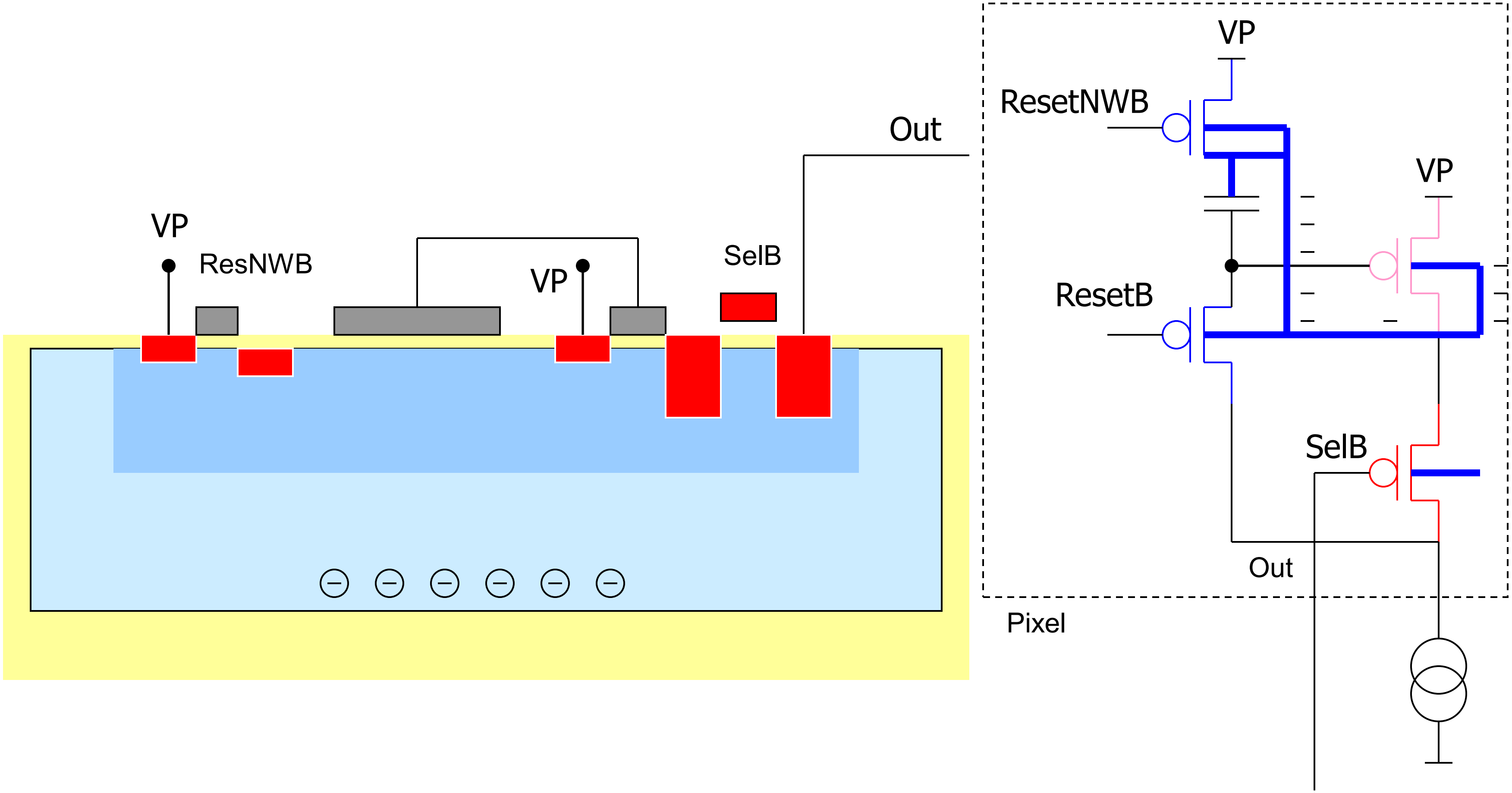
Integrating pixels with voltage amplification

Pixel with volt. amplification – signal detection phase

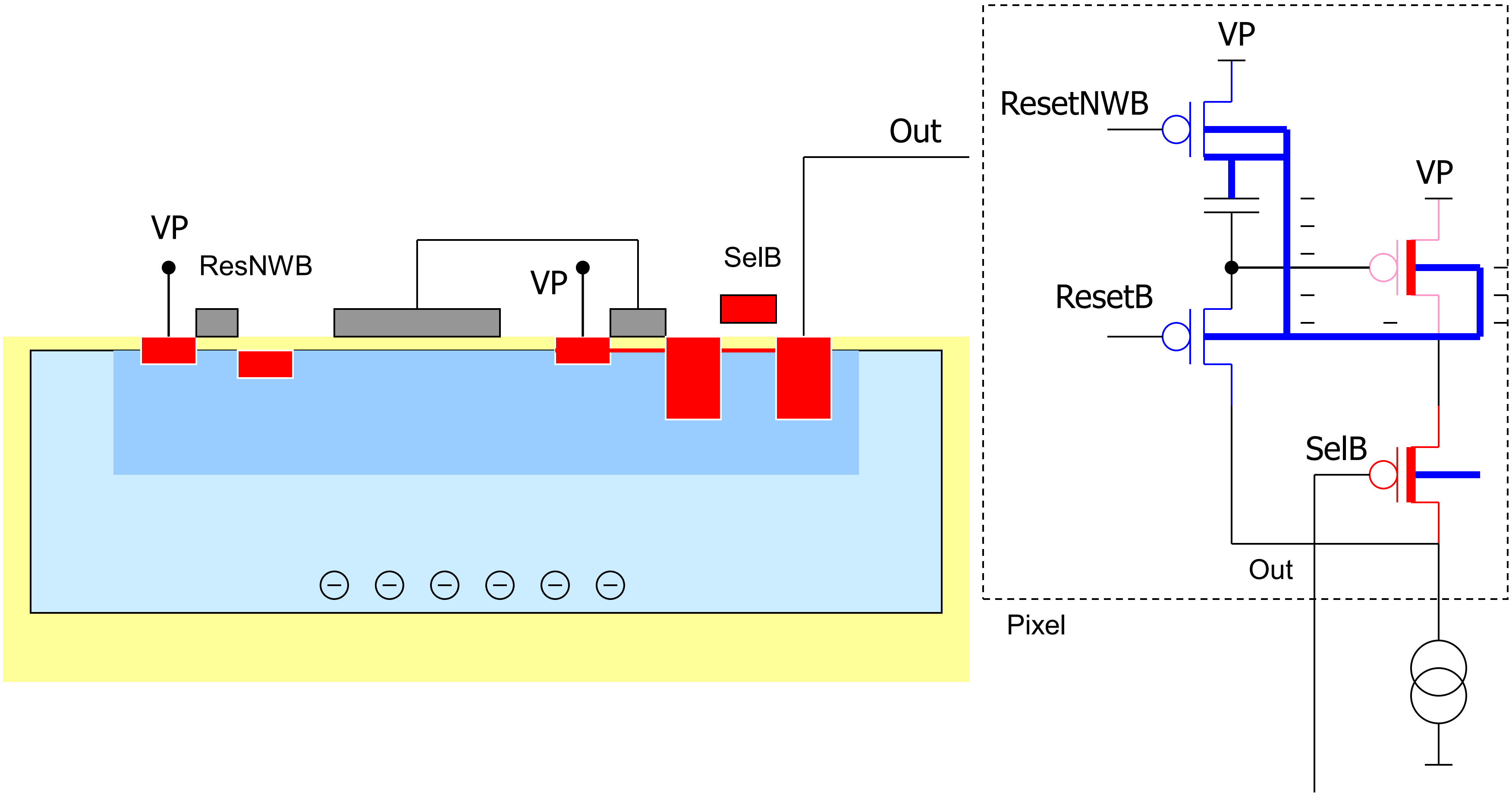


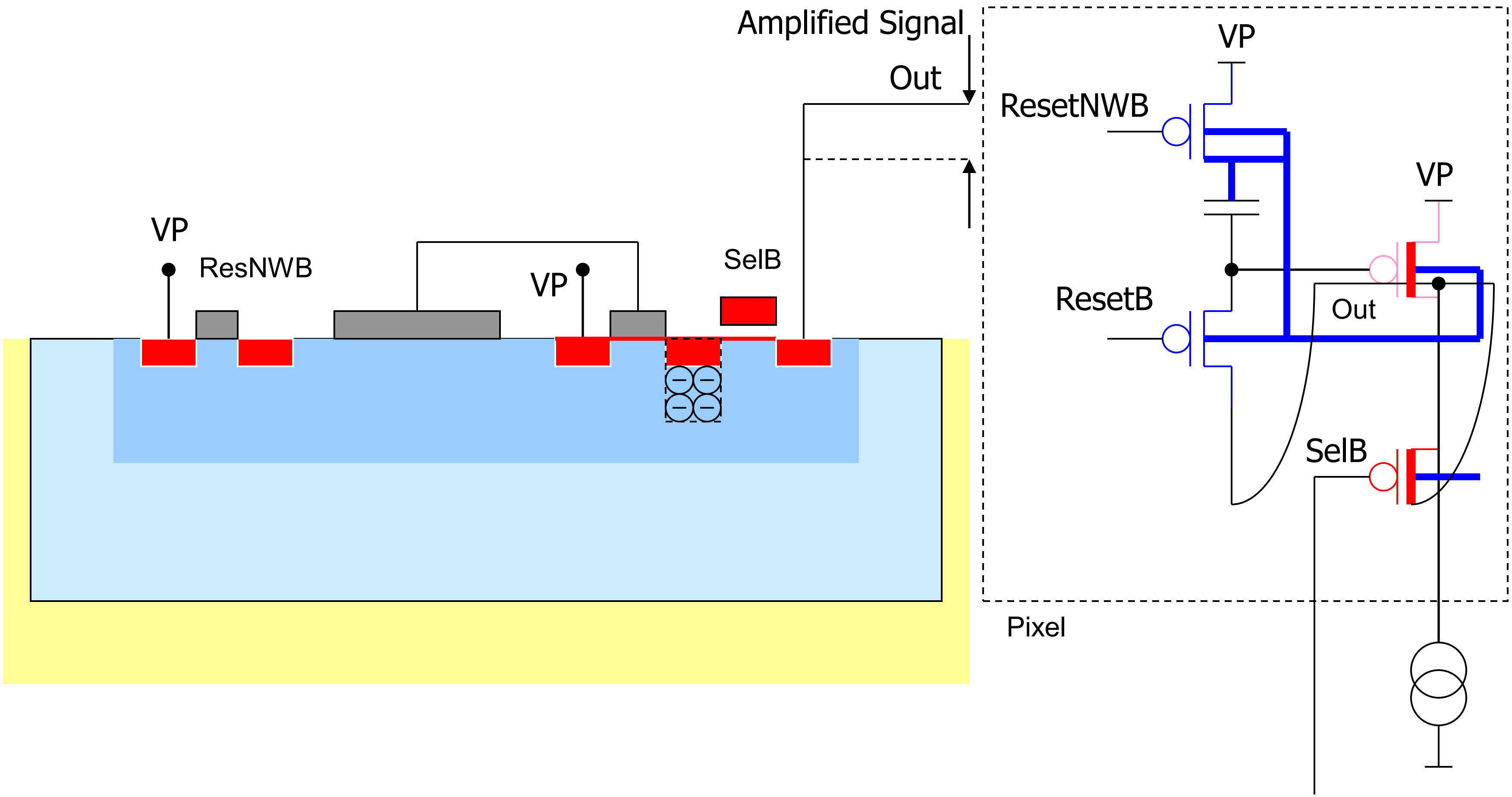

VP
ResNWB
VP
SelB
Out
VP
ResetNWB
VP
ResetB
SelB
Out
Pixel


VP
ResNWB
VP
SelB
Out
Pixel
VP
ResetNWB
VP
ResetB
SelB
Out

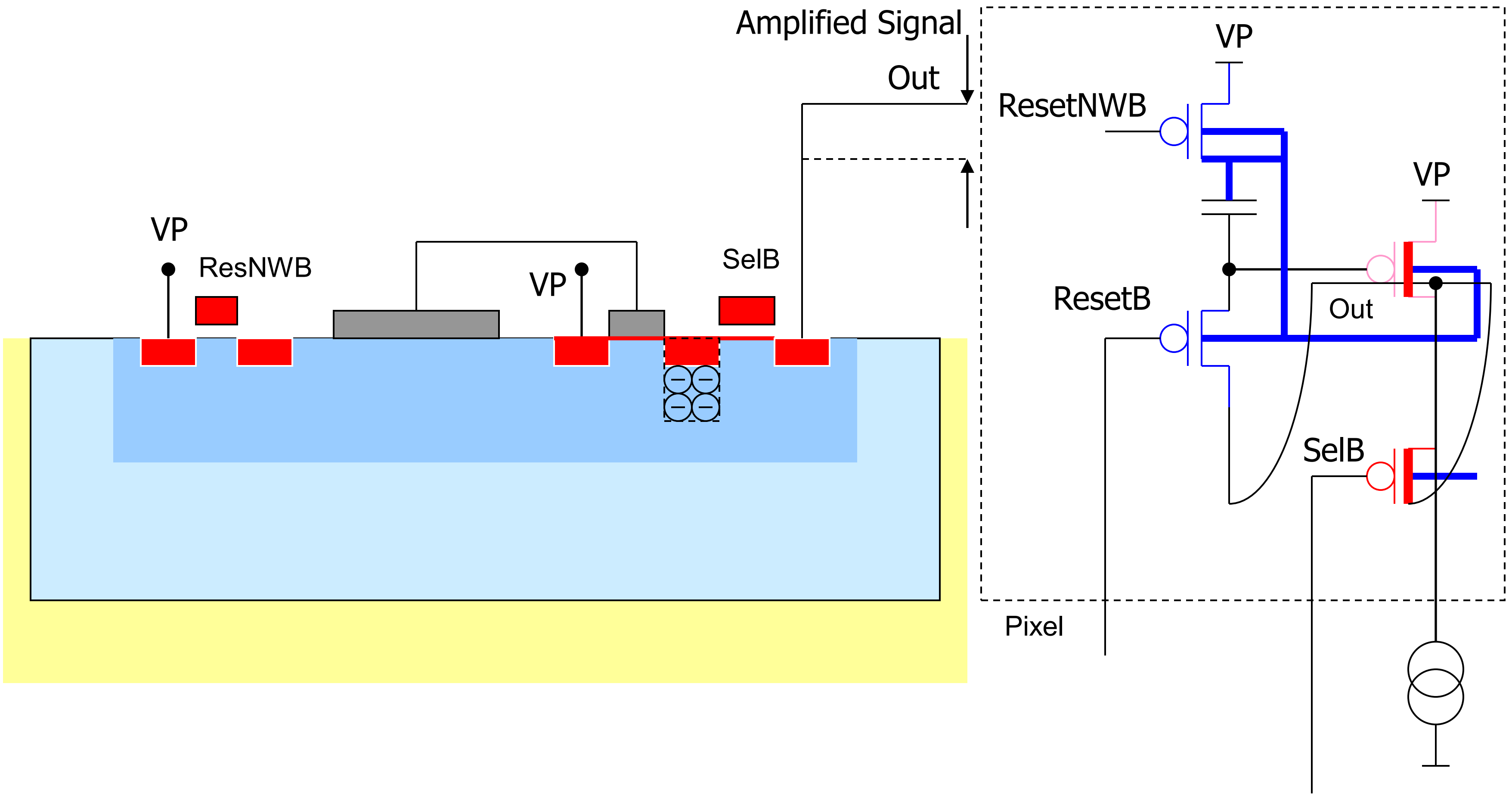


VP
ResNWB
VP
SelB
Out
VP
ResetNWB
VP
ResetB
SelB
Out
Pixel

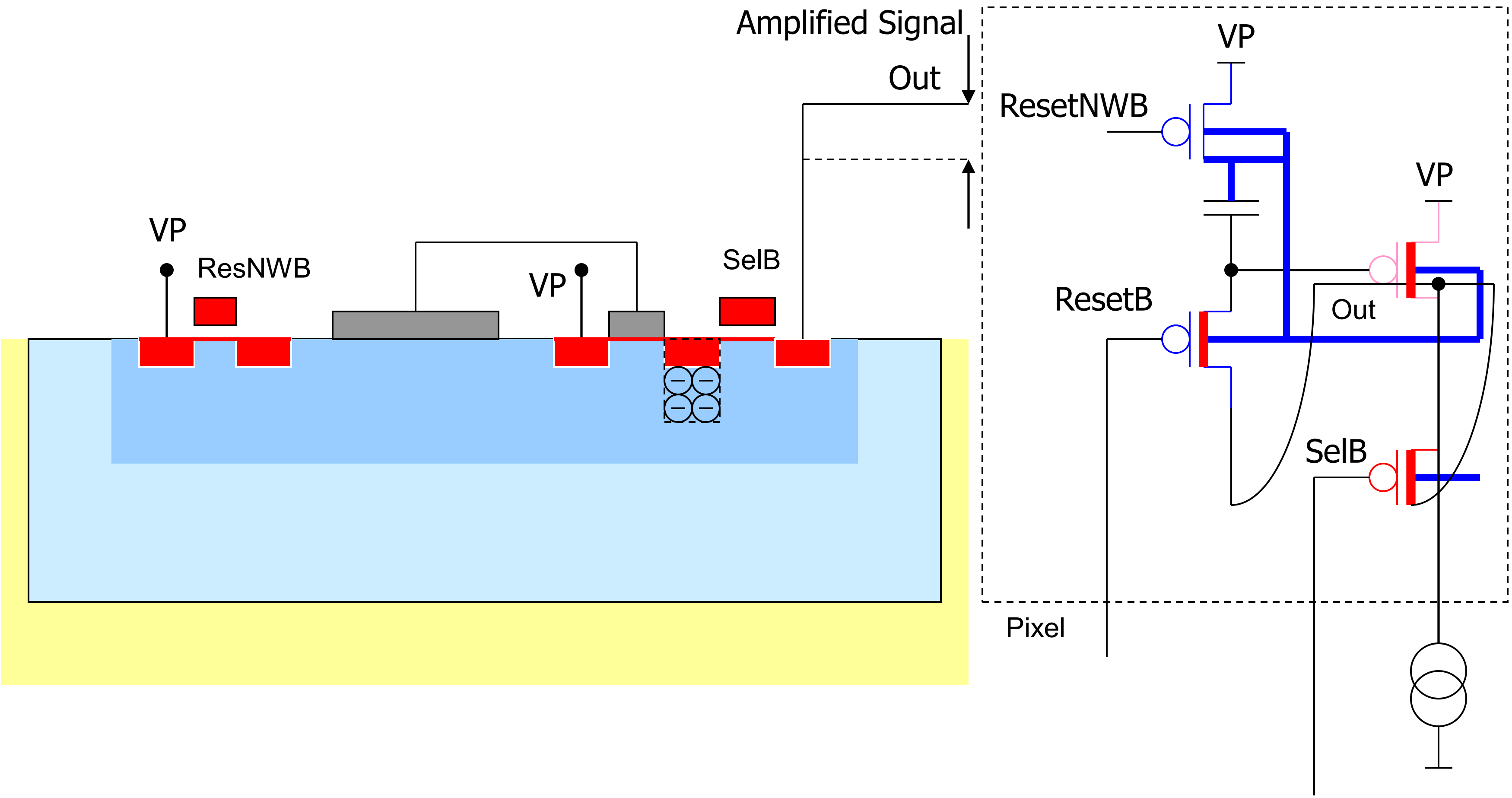

VP
ResNWB
VP
SelB
Out
VP
ResetNWB
VP
ResetB
SelB
Out
Pixel


Amplified Signal
Out
VP
ResetNWB
VP
ResetB
Out
SelB
Pixel
VP
ResNWB
VP
SelB

Readout – voltage amplification

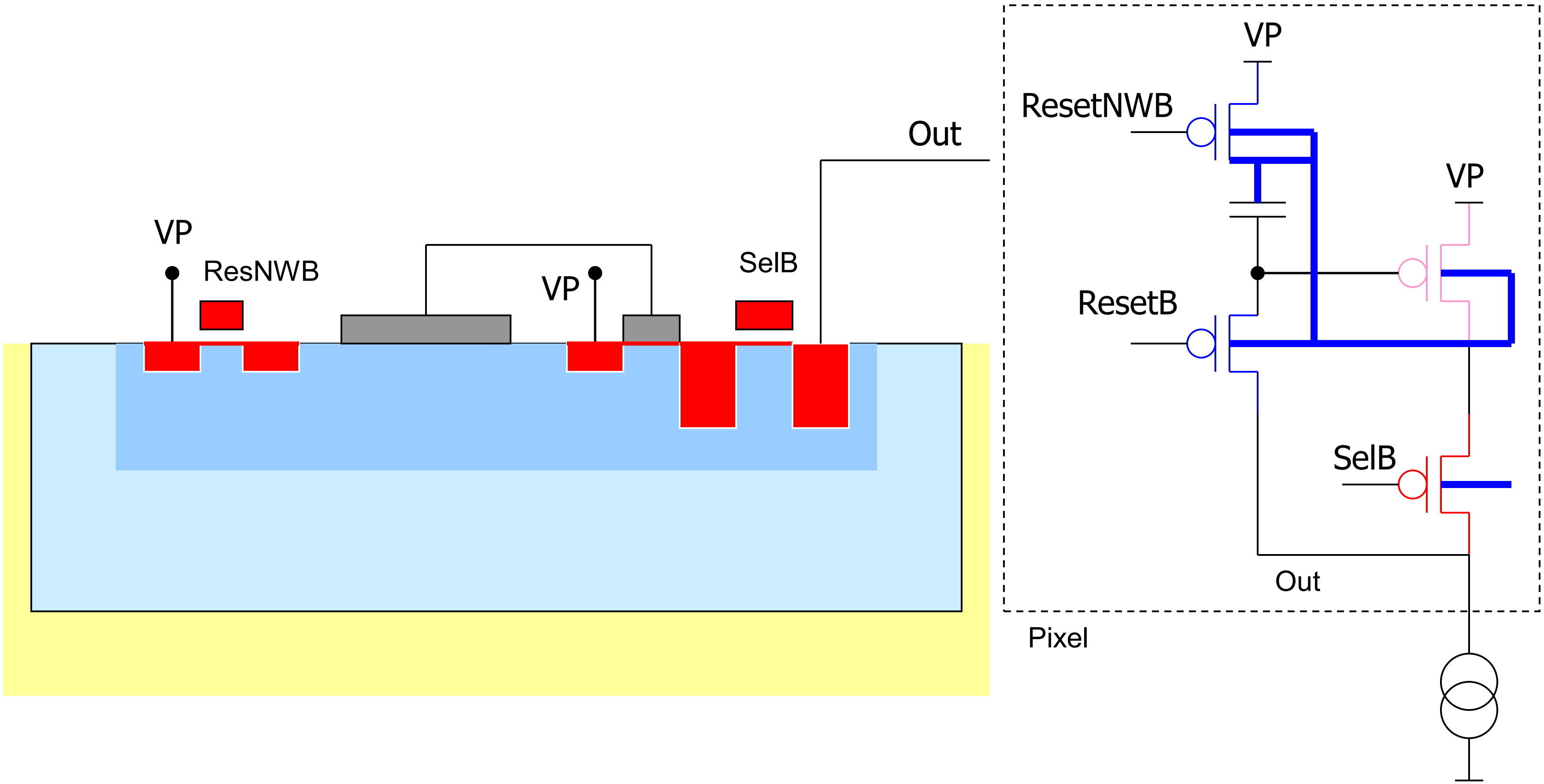


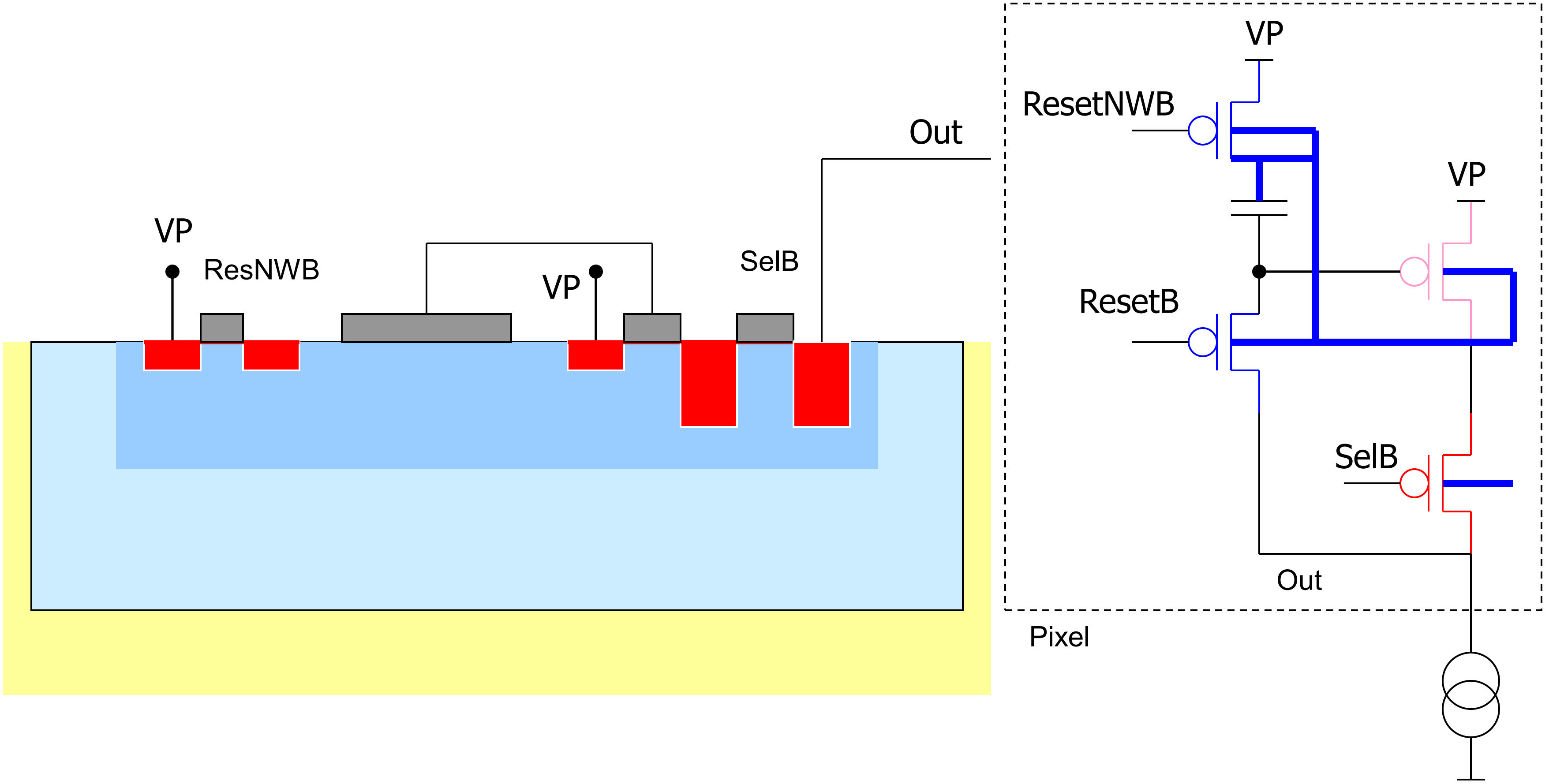
Reset



Amplified Signal
Out
VP
ResNWB
VP
SelB
VP
ResetNWB
VP
ResetB
Out
SelB
Pixel

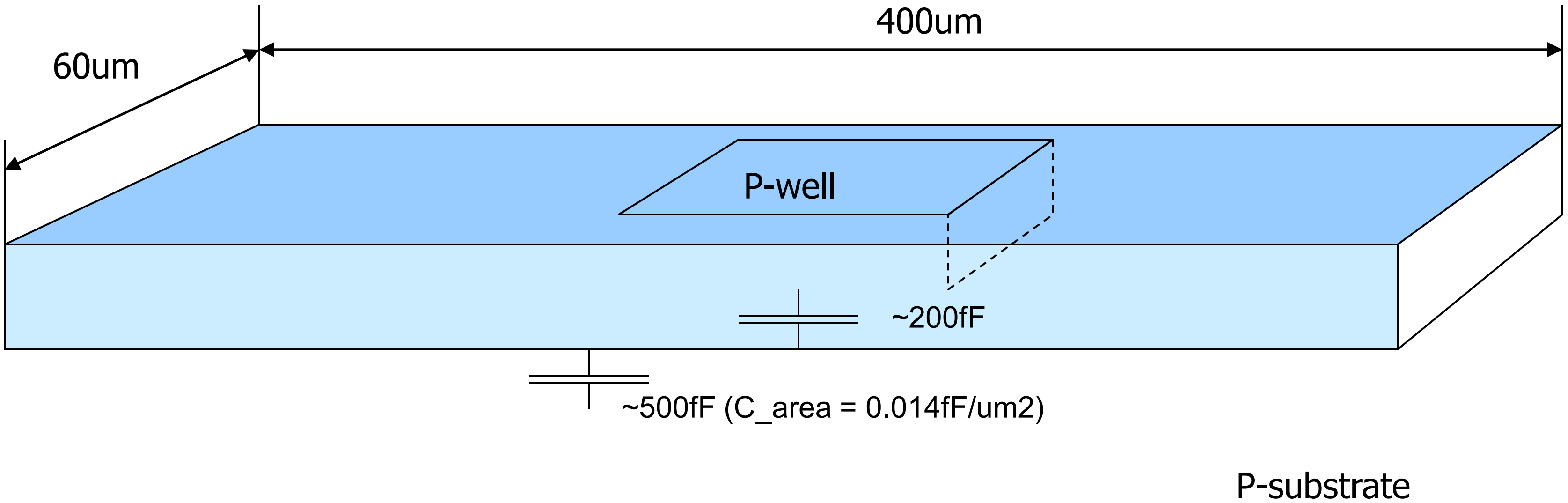
Reset + offset readout

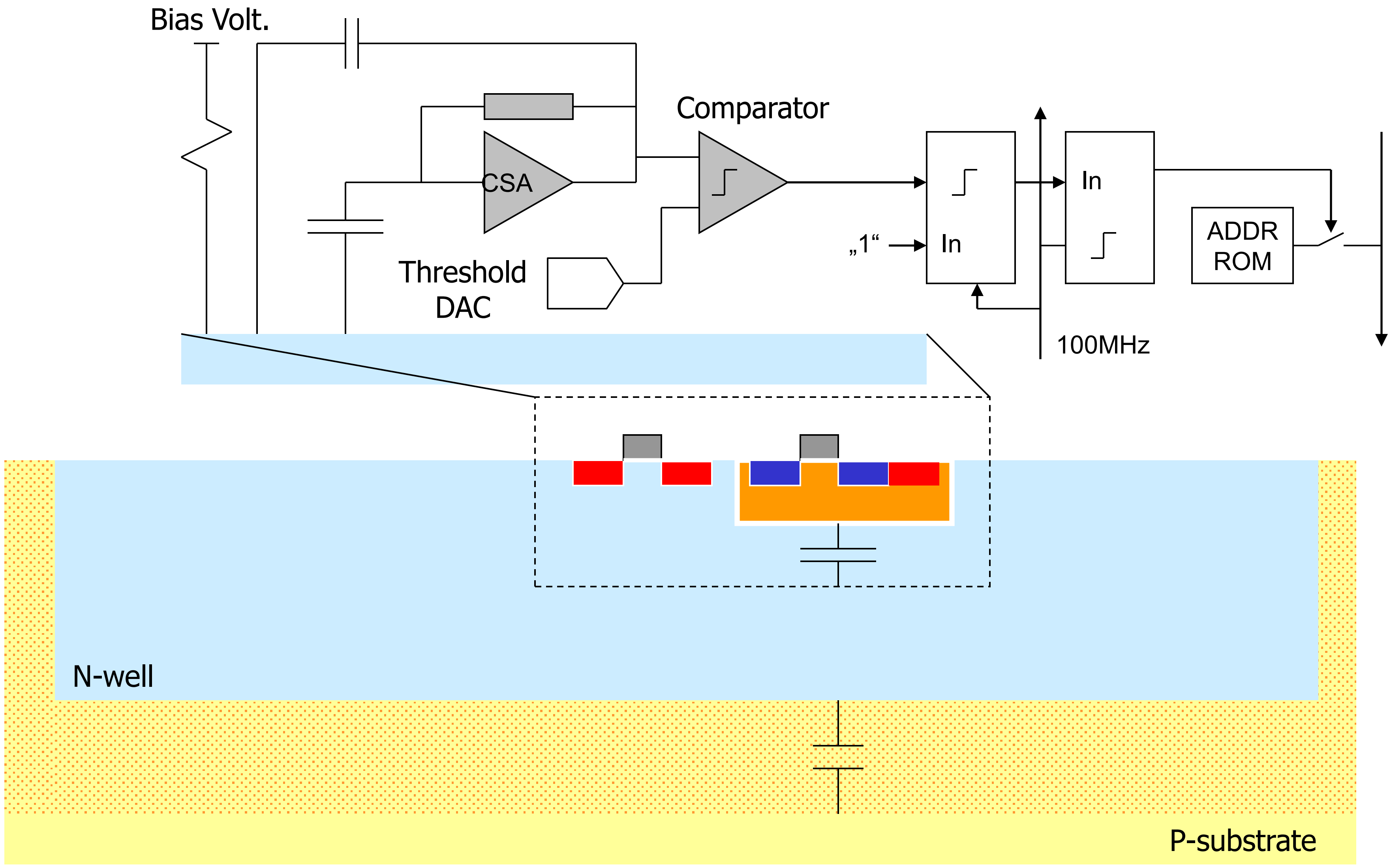


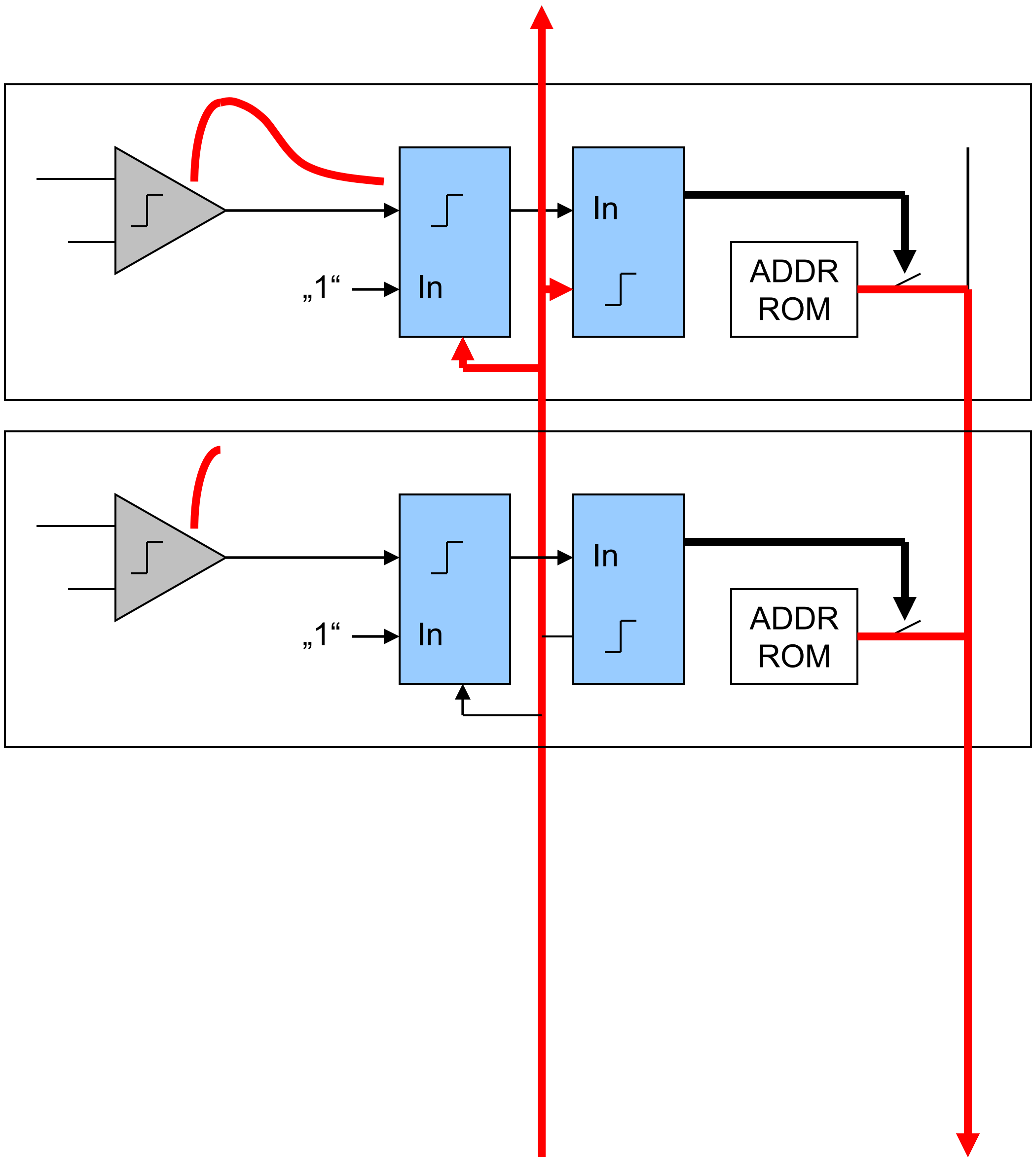

VP
ResNWB
VP
SelB
Out
VP
ResetNWB
VP
ResetB
SelB
Out
Pixel

- The pixel electronics could include a charge sensitive amplifier (CSA), leakage current compensation, continuous feedback, comparator and threshold tune DAC.
- The digital circuits inside pixel should be as simple as possible
- The idea:
- The addresses of *all* hit pixels are transmitted out of the sensor within next bunch crossing
- No hit buffering
- No trigger data reduction
- Assumption: occupancy is low enough so that we do not have not more than one hit per pixel column in one bunch crossing. This holds for R ~ 30 - 50cm

Total 700fF




Bias Volt.
Comparator
CSA
Threshold DAC
„1“
In
In
ADDR ROM
100MHz
N-well
P-substrate



Hit in Pixel A

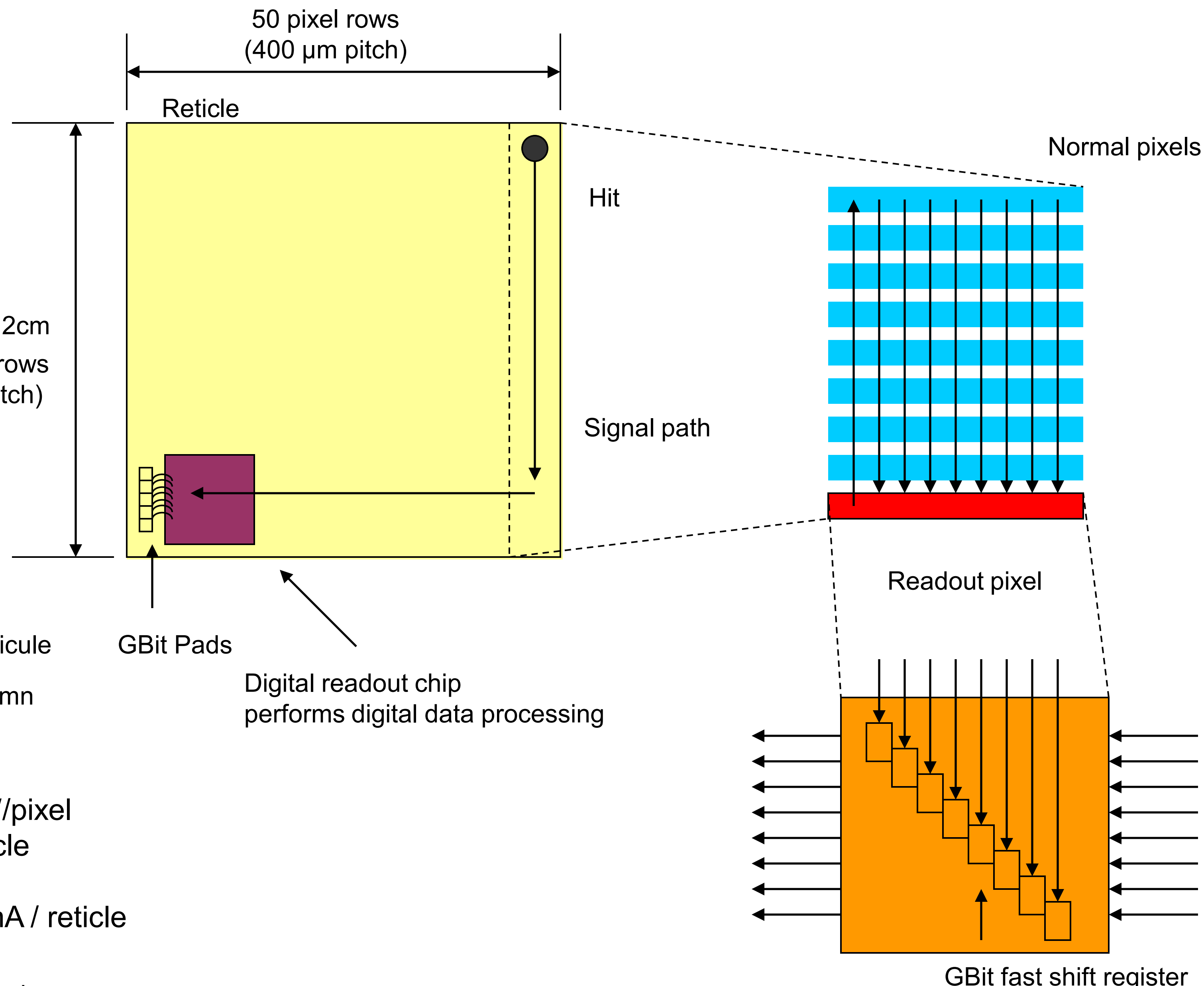
Time signal 1

Address „A“ on the data line

Hit in Pixel B

Time signal 2

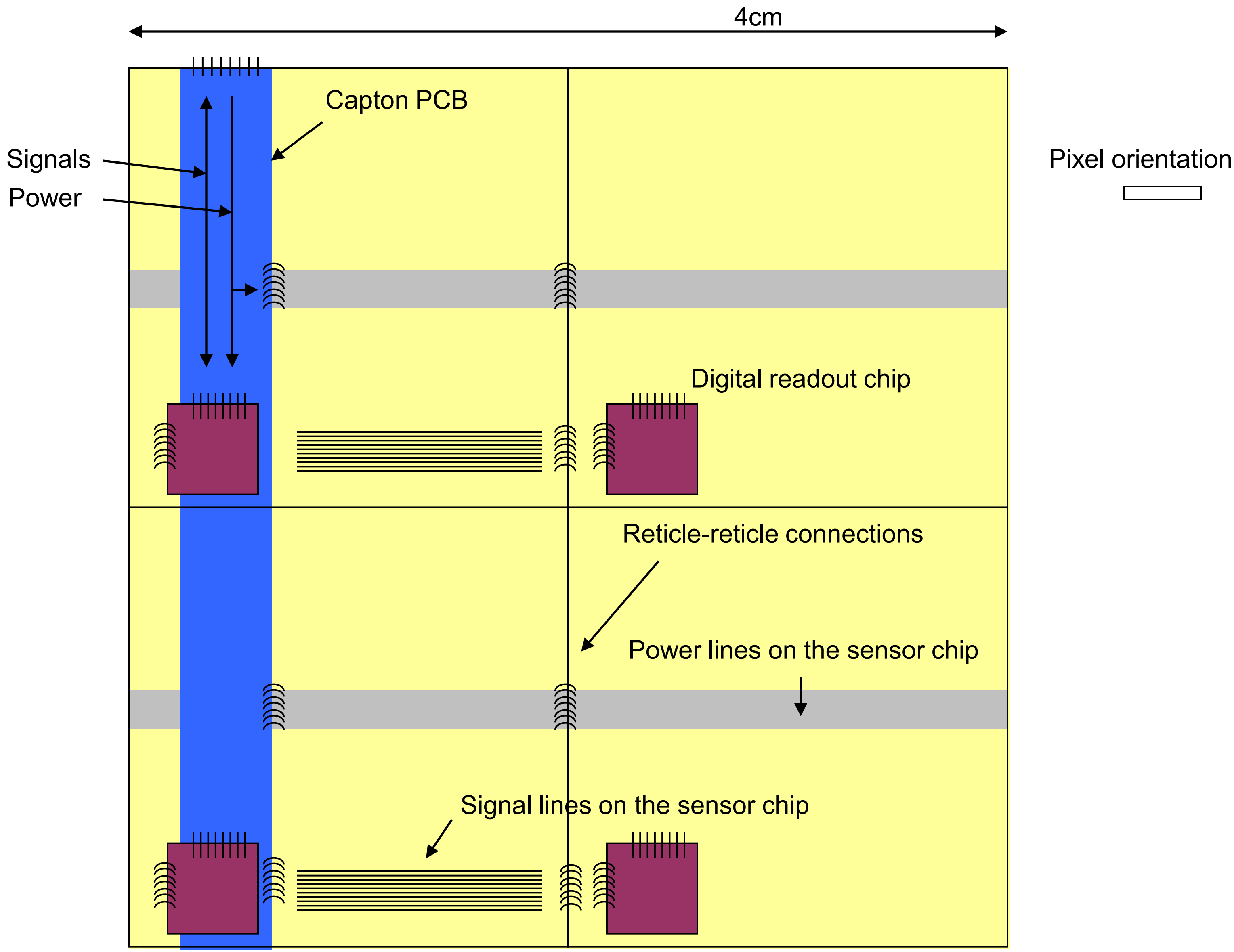
Address „B“ on the data line

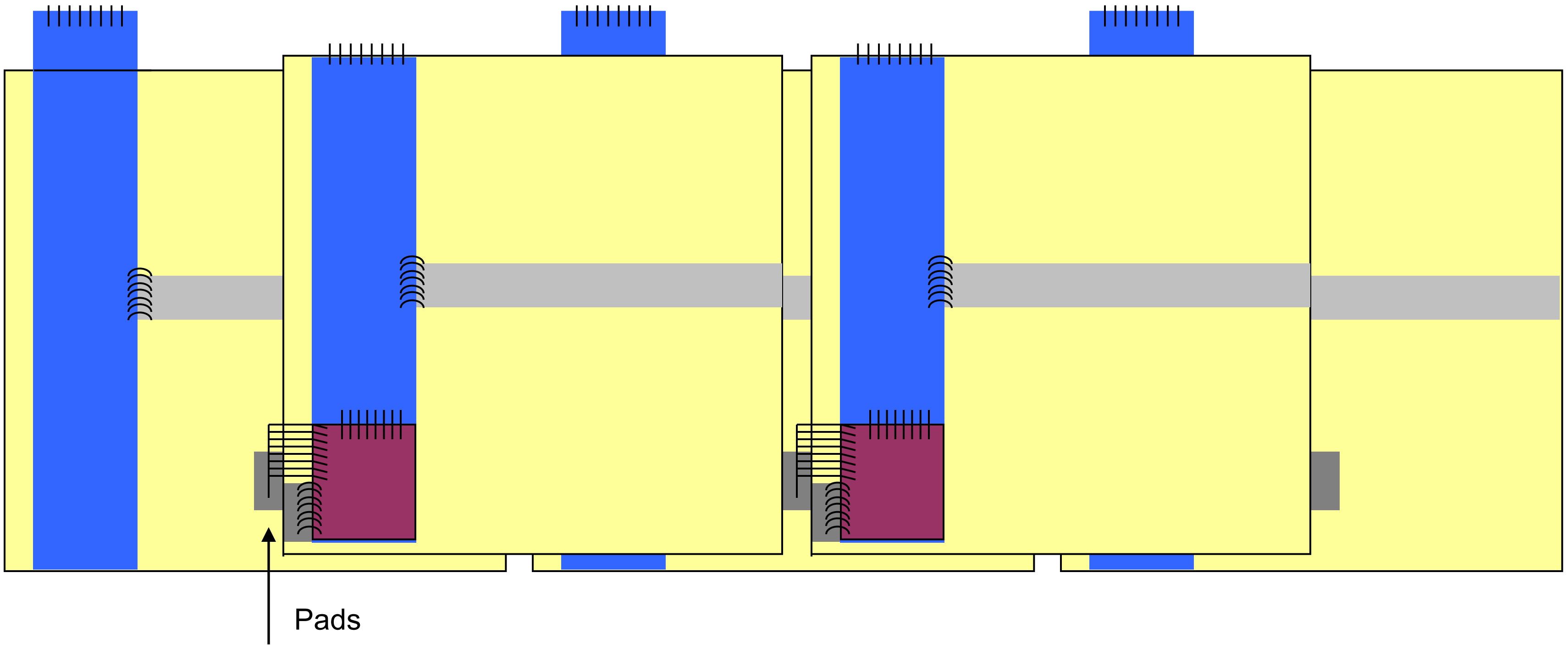


1. Sensor reticule

2. Pixel column

Power 30 µW/pixel
375mW / reticle
94mW / cm^2
Current 288mA / reticle

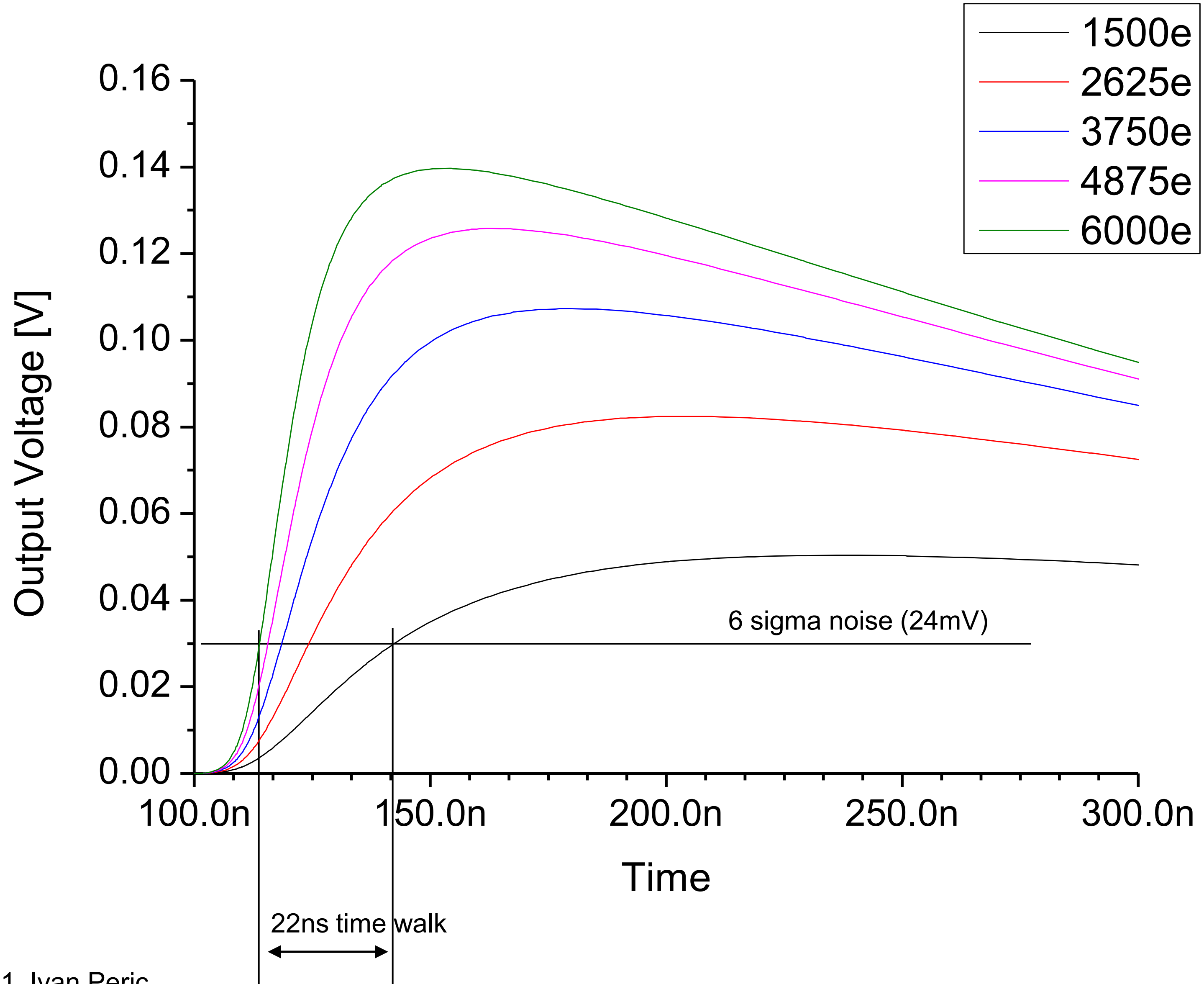

4cm
Capton PCB
Signals
Power
Pixel orientation
Digital readout chip
Reticle-reticle connections
Power lines on the sensor chip
Signal lines on the sensor chip



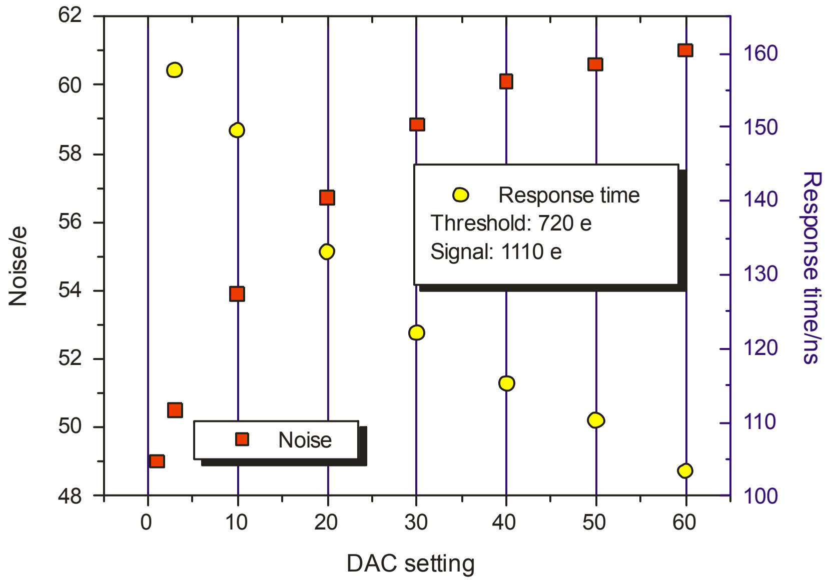
Digital readout chips receive the hits from both detector layers
Generation of trigger possible?

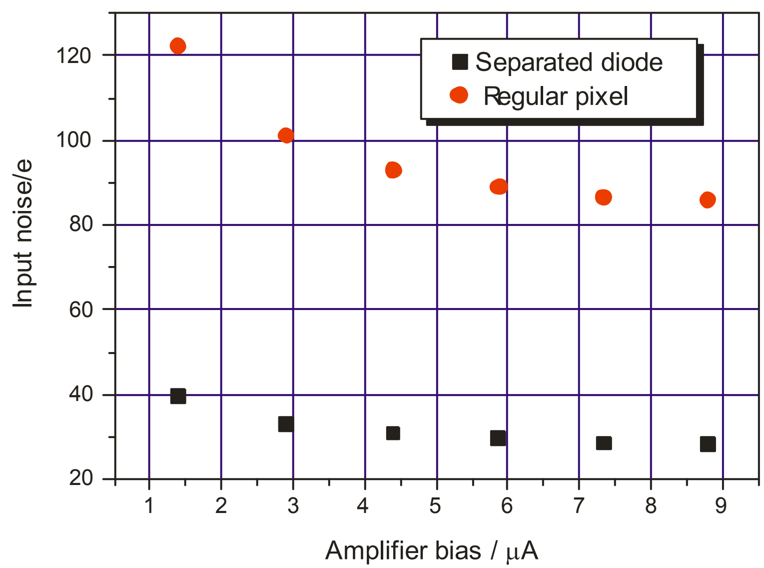
Time Resolution

- Time resolution is limited by time walk (can be improved by ToT correction!)
- Time resolution is proportional to preamplifier bias current and power consumption
- Time resolution is inversely proportional to detector capacitance


1500e
2625e
3750e
4875e
6000e
0.16
0.14
0.12
0.10
0.08
0.06
0.04
0.02
0.00
Output Voltage [V]
6 sigma noise (24mV)
100.0n
150.0n
200.0n
250.0n
300.0n
Time
22ns time walk

Time Resolution with HV1

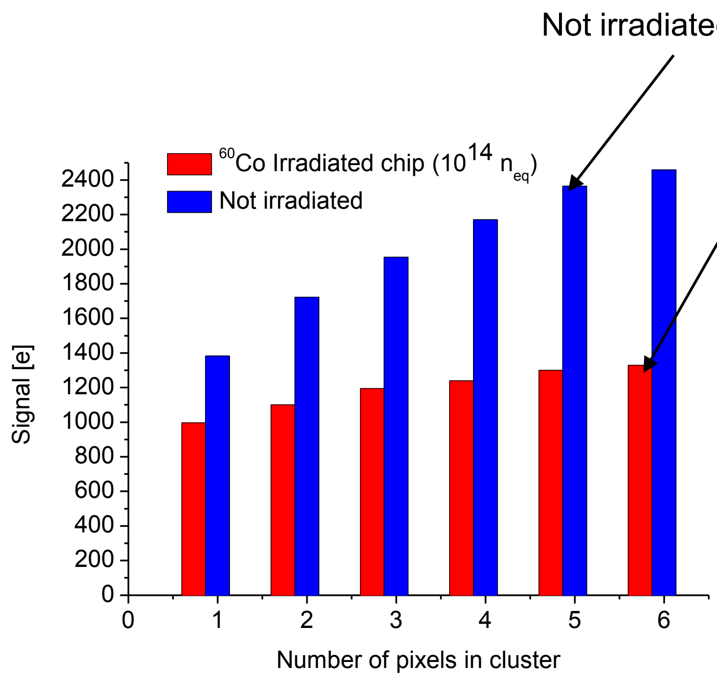


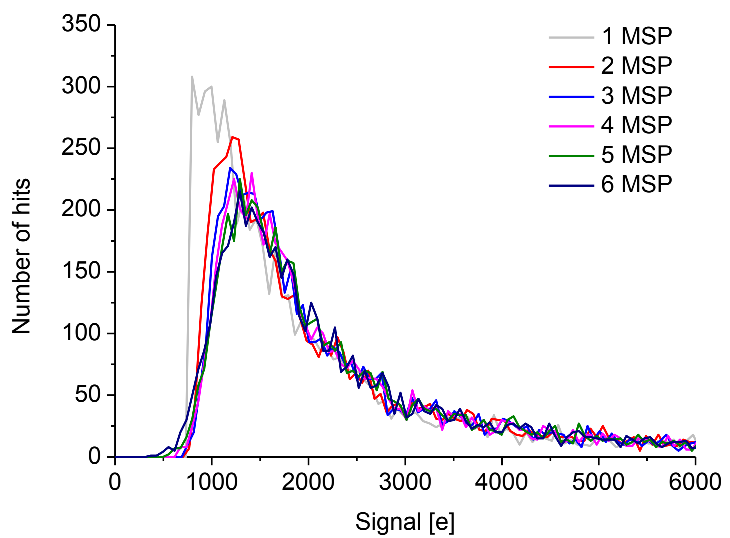


Response time ~ time resolution

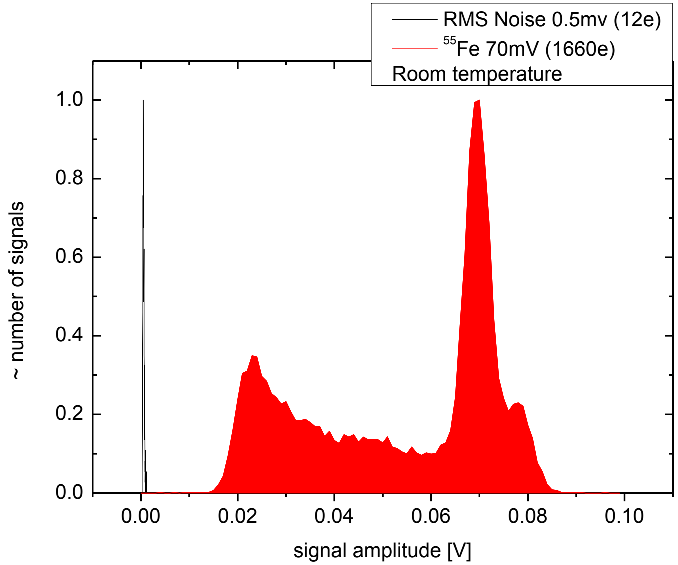
Irradiation with neutrons (10^{14} n_{eq}/cm^2) – signal

Increase of the detector leakage current from 350fA to 130pA per pixel
Seed pixel signal decrease from 1300e to 1000e.
The measurement has been performed at 0C

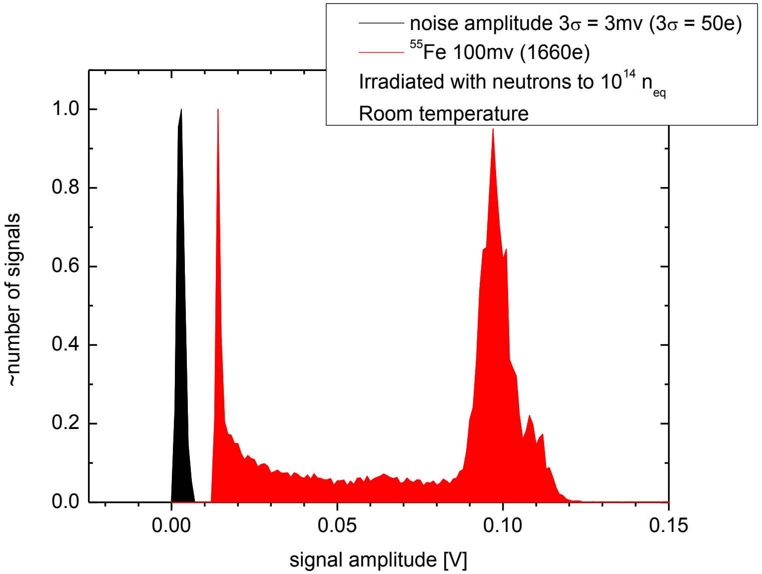




^{55}Fe spectrum and RMS noise
Not irradiated
Room temperature
RMS Noise 12 e

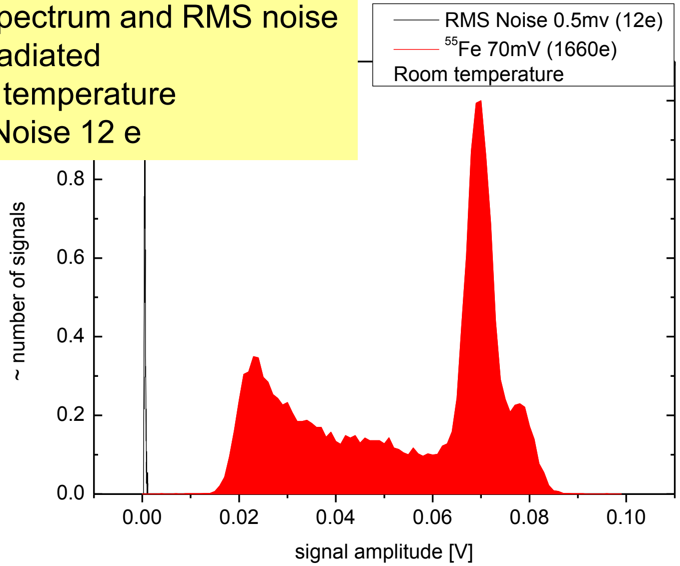


^{55}Fe spectrum and noise amplitude
Irradiated with neutrons (10^{14} n_{eq})
Room temperature
Noise amplitude (~3 sigma) ~ 50 e

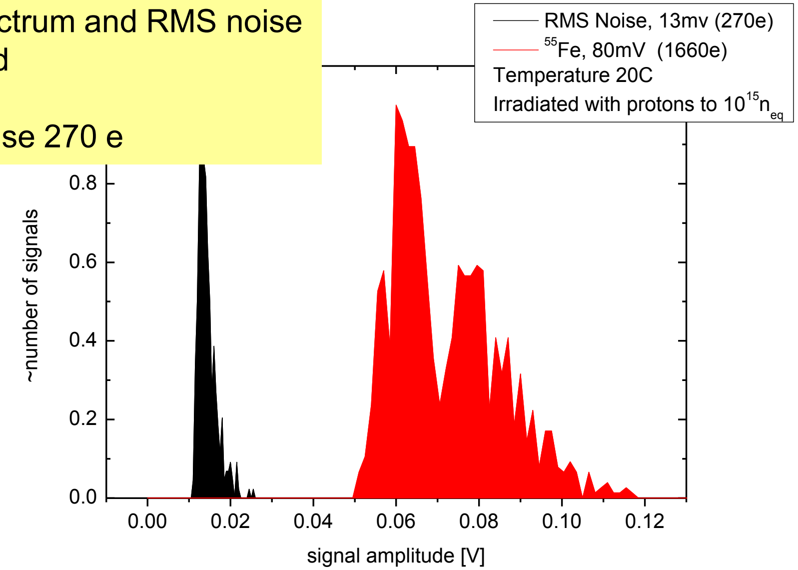


Irradiation with protons (10^{15} n_{eq}/cm^2, 300 MRad)

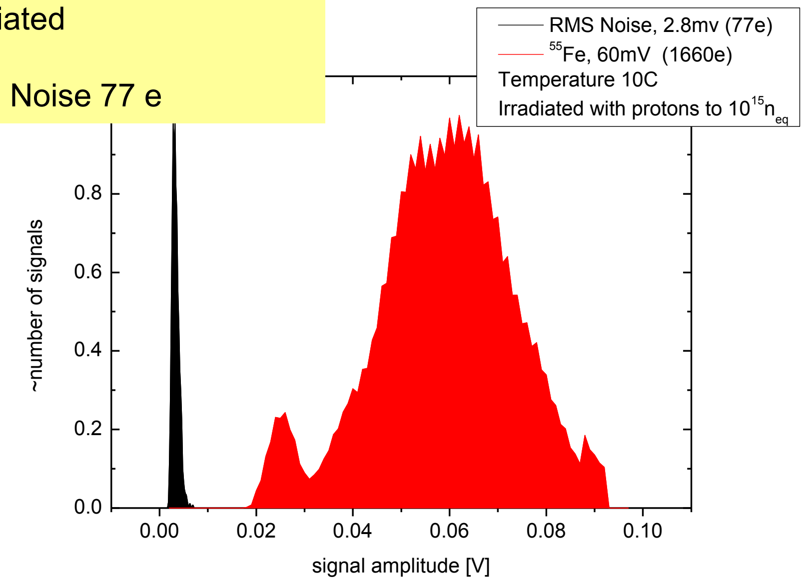
^{55}Fe spectrum and RMS noise
Not irradiated
Room temperature
RMS Noise 12 e



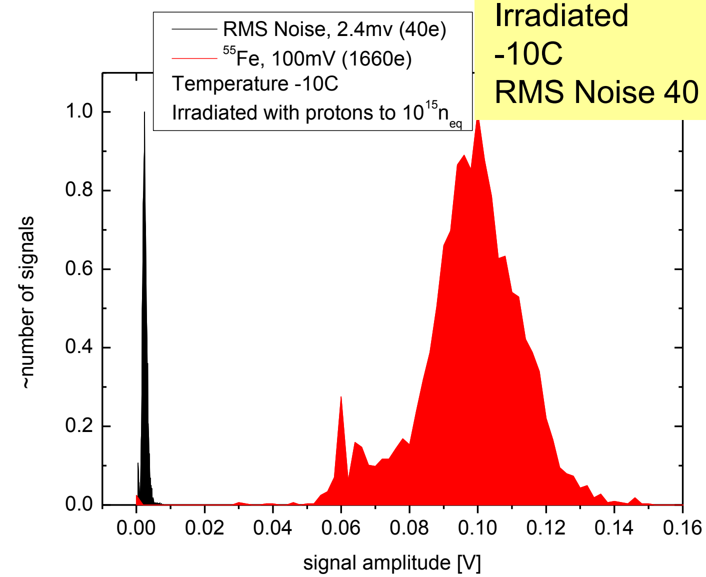
^{55}Fe spectrum and RMS noise
Irradiated
20C
RMS Noise 270 e



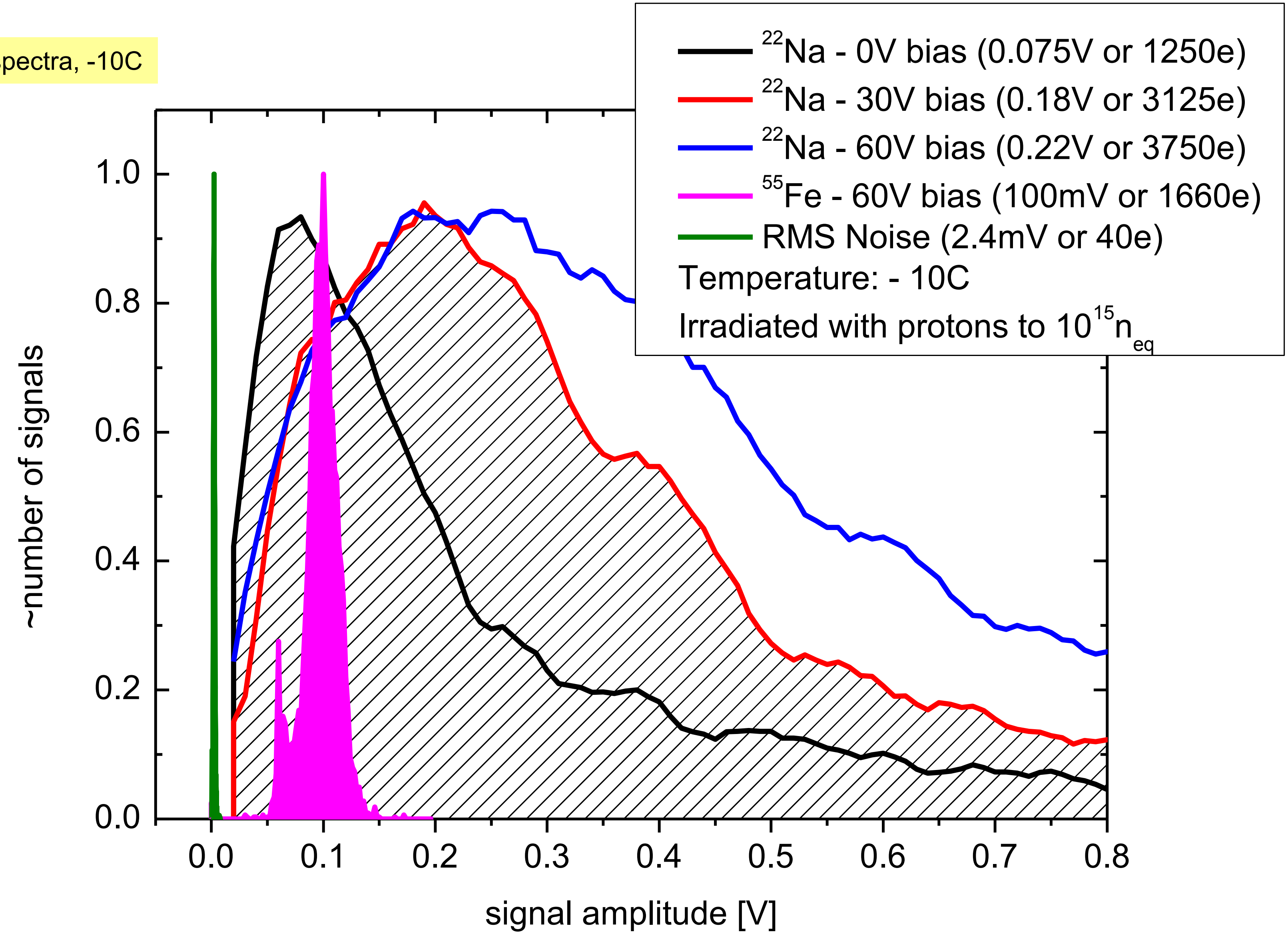
^{55}Fe spectrum, RMS noise
Irradiated
10C
RMS Noise 77 e

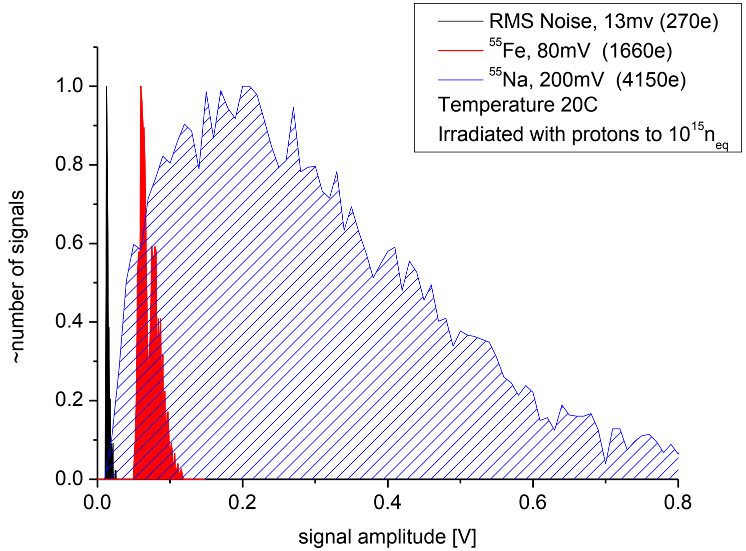


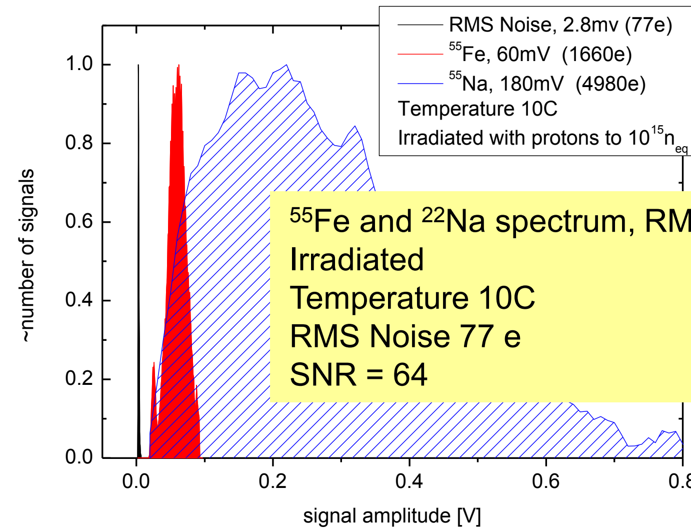
^{55}Fe spectrum, RMS noise
Irradiated
-10C
RMS Noise 40 e



^{55}Na spectra, -10C

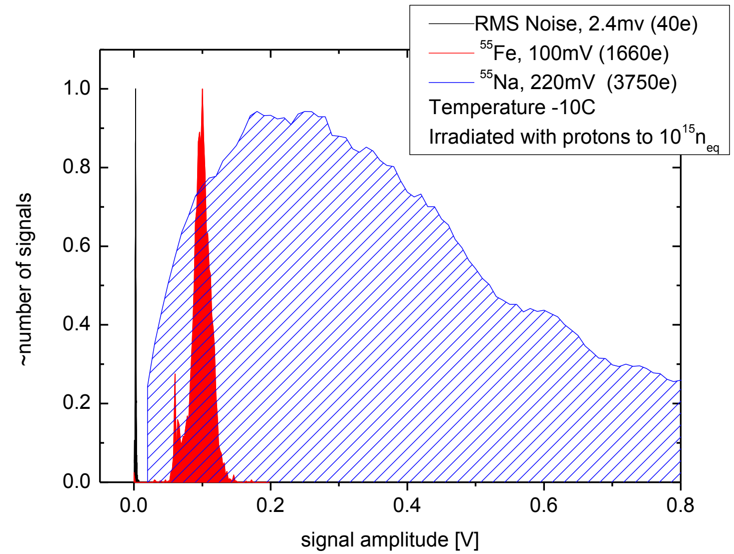






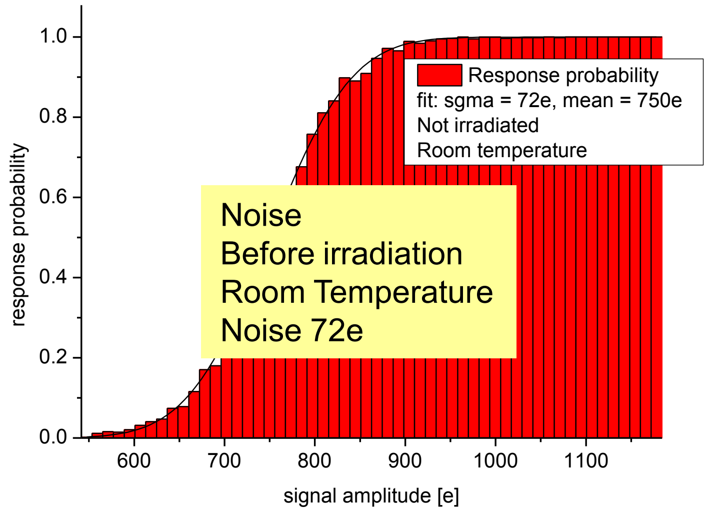
^{55}Fe and ^{22}Na spectrum, RMS noise
Irradiated
Temperature 10C
RMS Noise 77 e
SNR = 64

^{55}Fe and ^{22}Na spectrum, RMS noise
Irradiated
Temperature 20C
RMS Noise 270 e
SNR = 15

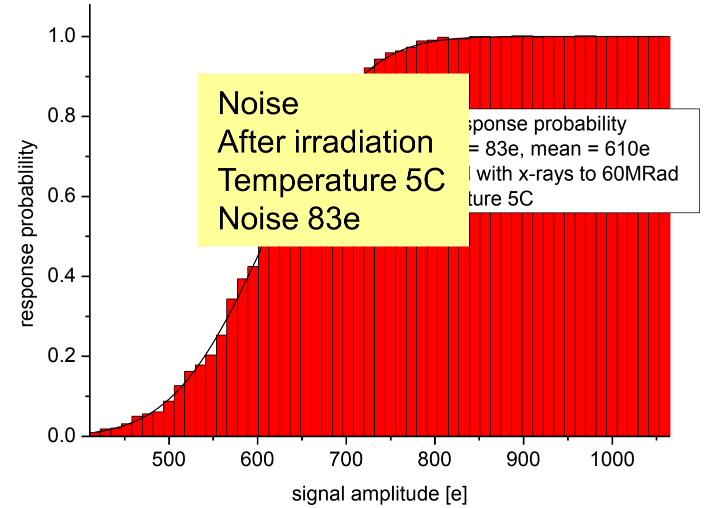


^{55}Fe and ^{22}Na spectrum, RMS noise
Irradiated
Temperature -10C
RMS Noise 40 e
SNR = 93

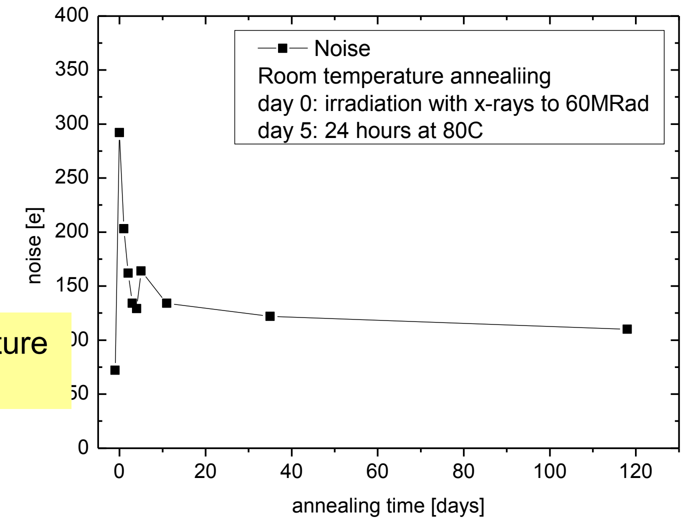
Irradiation x-rays (50 MRad)



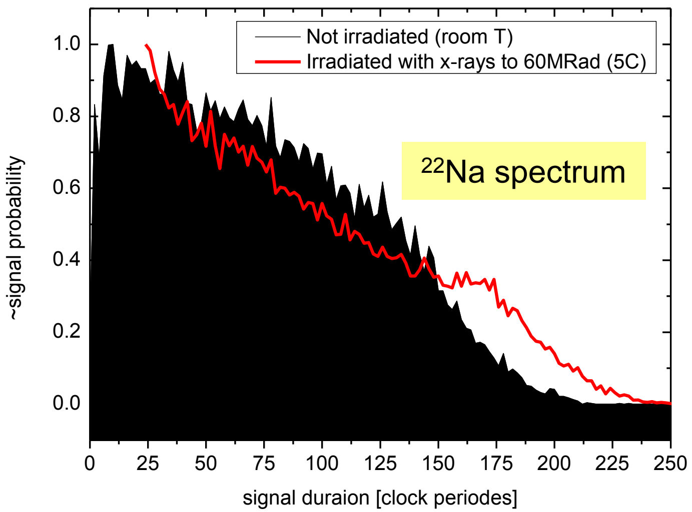
Noise
Before irradiation
Room Temperature
Noise 72e

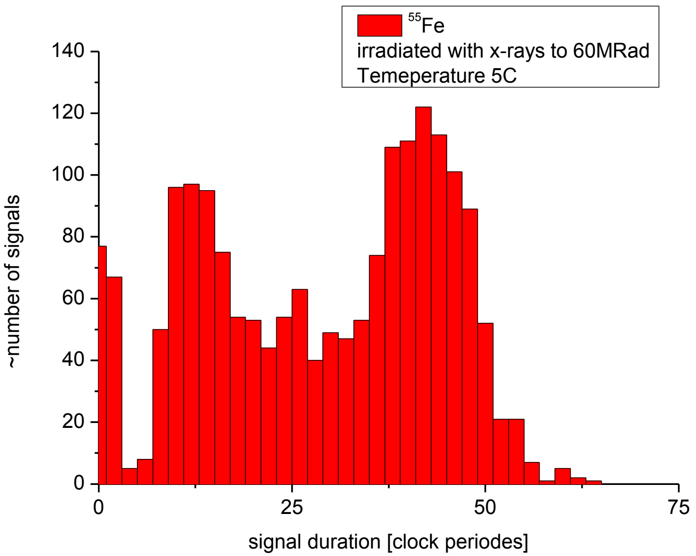


Noise
After irradiation
Temperature 5C
Noise 83e

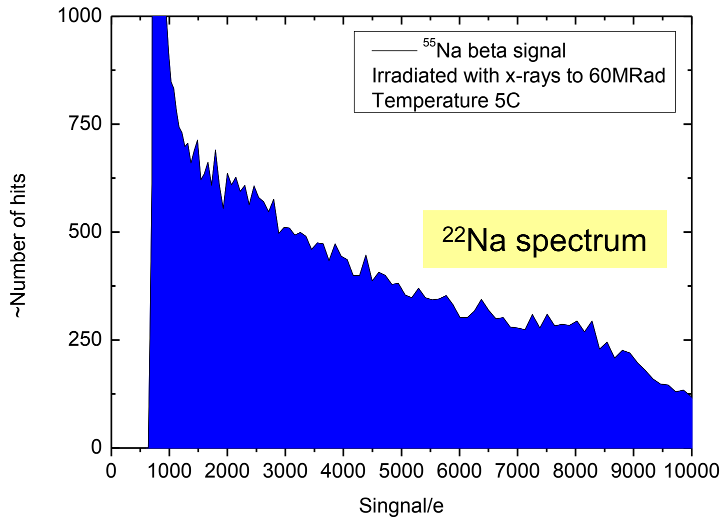


Noise at room Temperature
Vs. annealing time

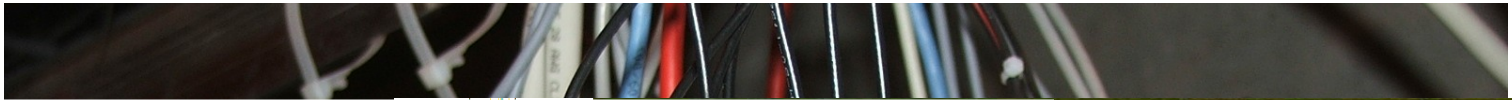


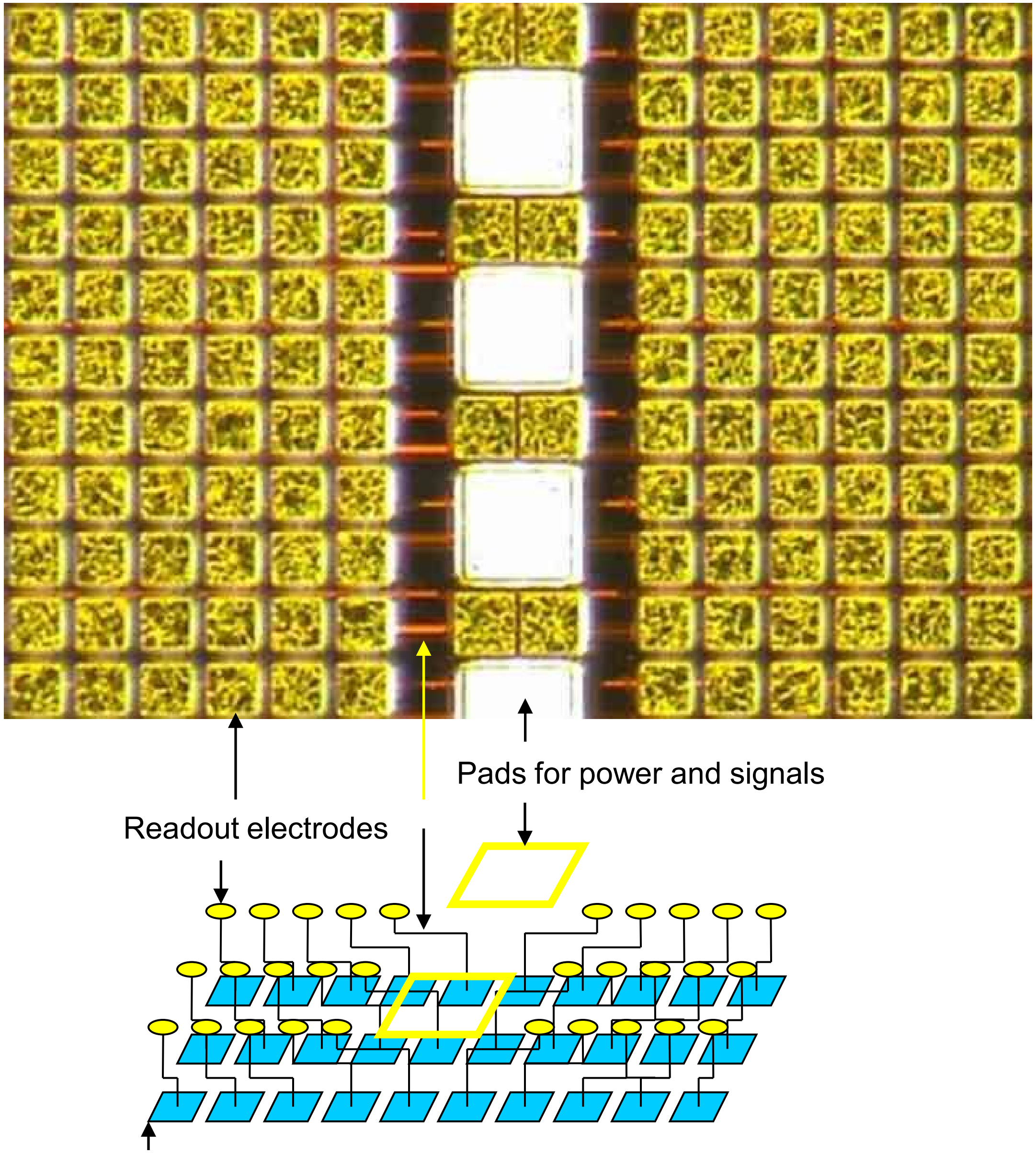


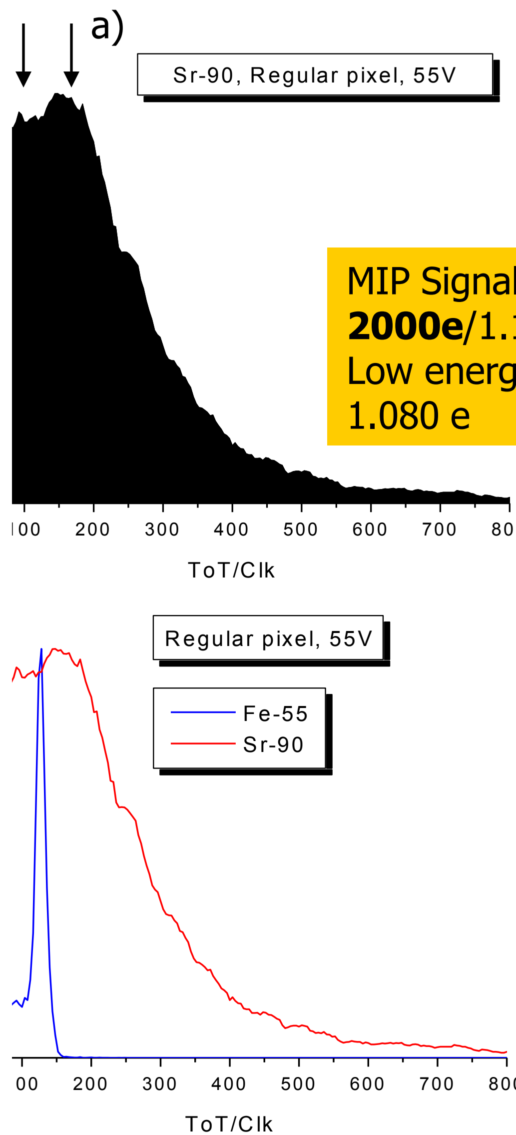
^{22}Fe spectrum



Tes







MIP Signal:
2000e/1.17 = **1710 e**
Low energy peak:
1.080 e