Evaluation of 65nm technology for front-end electronics in HEP

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Introduction

- The microelectronics group at CERN is investigating the possibility to use downscaled technologies for future projects
- A test chip was submitted on March, 23rd to test radiation hardness and the functionality of some test structures (both analog and digital)
- This research is mainly focused on the design of future vertex detectors for high energy physics experiments.

Why 65nm Technology?

Scaling is necessary to improve the performances of pixellated detectors:

- Smaller pixel sizes (pitch)
- More “intelligence” in each pixel

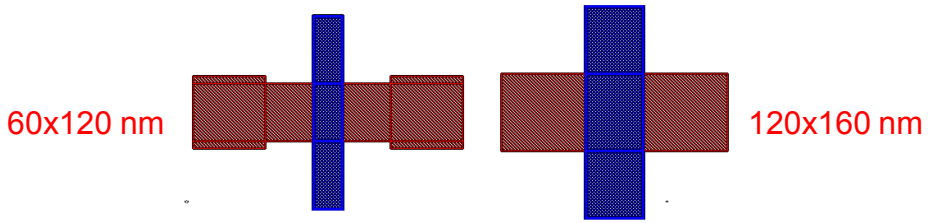
On the other hand, deep submicron technologies are not designed primarily for analog designs!

Also, studies on radiation hardness of the selected technology are needed.

Expected advantages

The expected advantages in porting a front-end circuit to a more downscaled technology include:

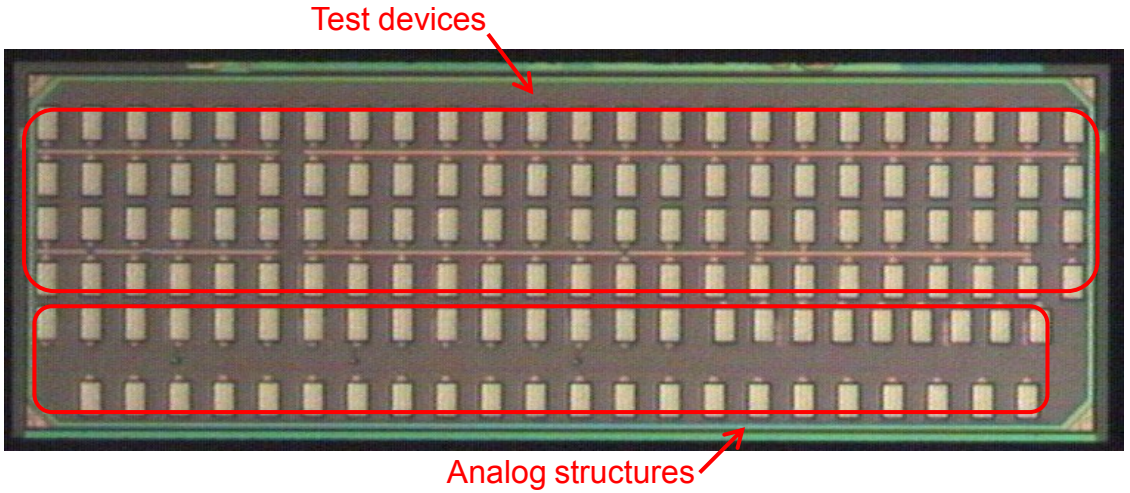
- A much more compact digital part (the scaling would allow for a reduction in area close to 60% compared to 130nm technology)



- A reduction in size of the analog part, even if not as much as the digital part (usually between 10% and 30%, with higher benefits for very regular structures such as DACs)
- Lower noise equivalent charge, due to the reduced capacitances associated with smaller pixels

The test chip

- Radiation and functional tests
- Total size: 3x4 mm
- Divided in three sub-chips:
- 1 chip for analog structures and test devices
  - 1 pad per multiple gates
  - Analog structures
- 1 chip w/ test structure/devices
  - 1 pad per gate
  - 142 total pins
- 1 chip for digital logic
  - Shift-register
  - Ring oscillator
  - Memory

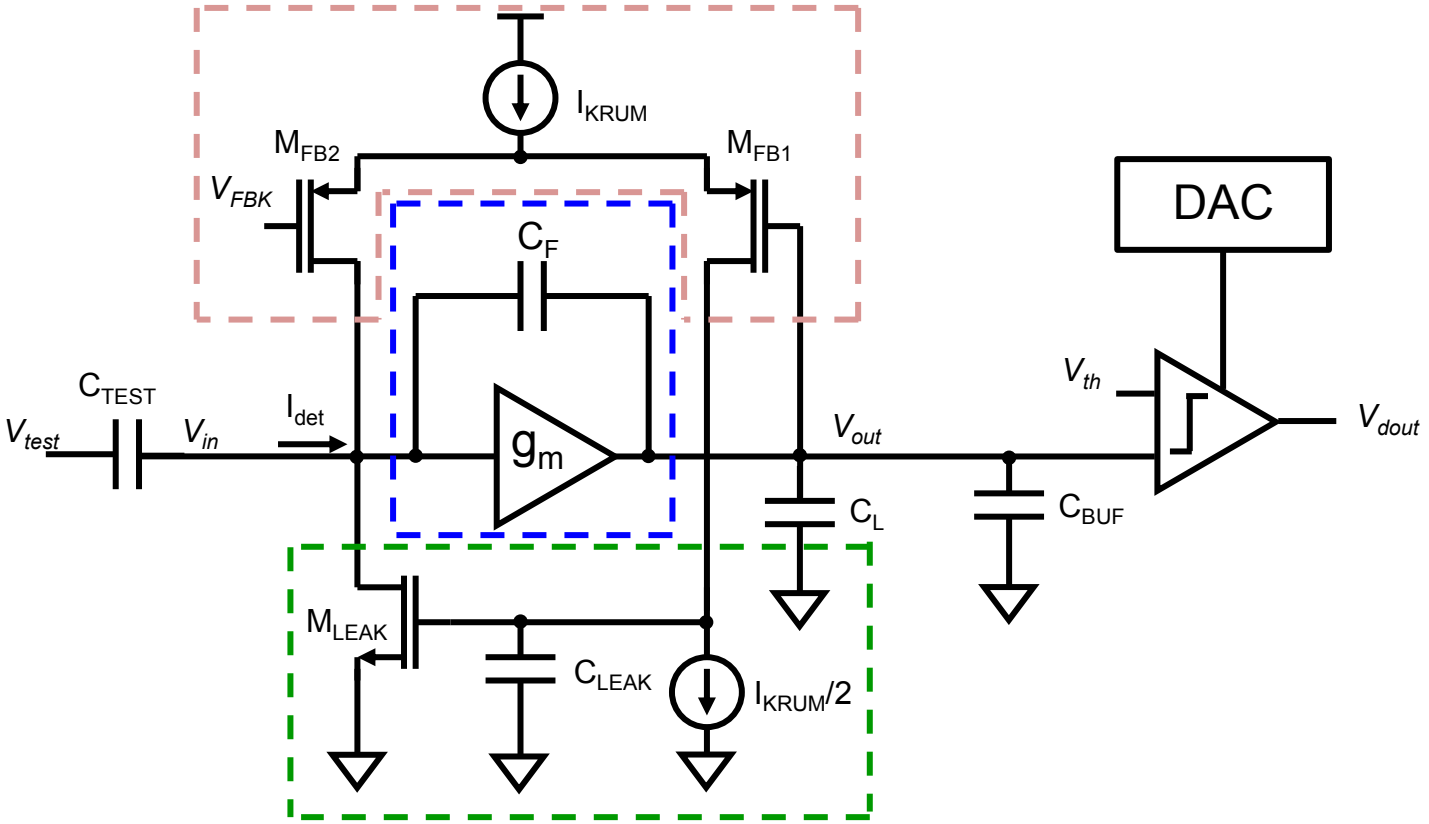


Analog structures

- Four structures are included:
  - A preamplifier with Krummenacher[1] feedback network
  - Discriminator
  - Binary weighted DAC
  - Sub-binary radix DAC
- Chosen in order to test the viability of developing future pixellated detectors with this technology

[1] F. Krummenacher, “Pixel detectors with local intelligence: an IC designer point of view”, *Nucl. Instr. and Meth. A*, Vol 305, Issue 3, Aug. 1991

Pixel block diagram

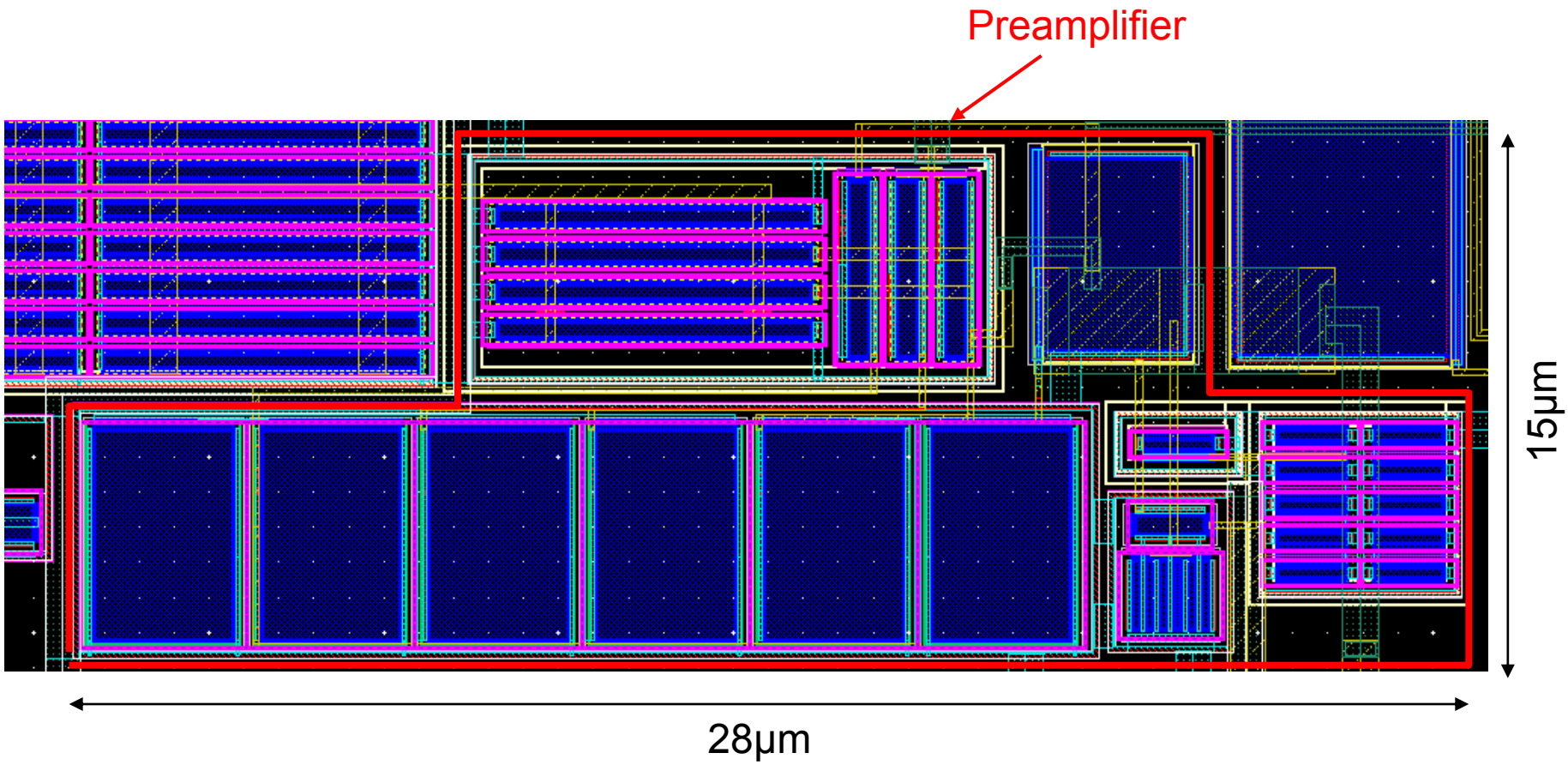


- The output of each block is buffered and accessible from I/O pads
- The biasing of the test structures is entirely configurable from outside the chip

Preamplifier versions

- Three different versions are included:
  - Standard transistors
  - ELT for the NMOS part
  - Segmented transistors for feedback current (Ikrum) mirror
- Performances according to simulations are very similar
- Layout size is approx. 15x28µm

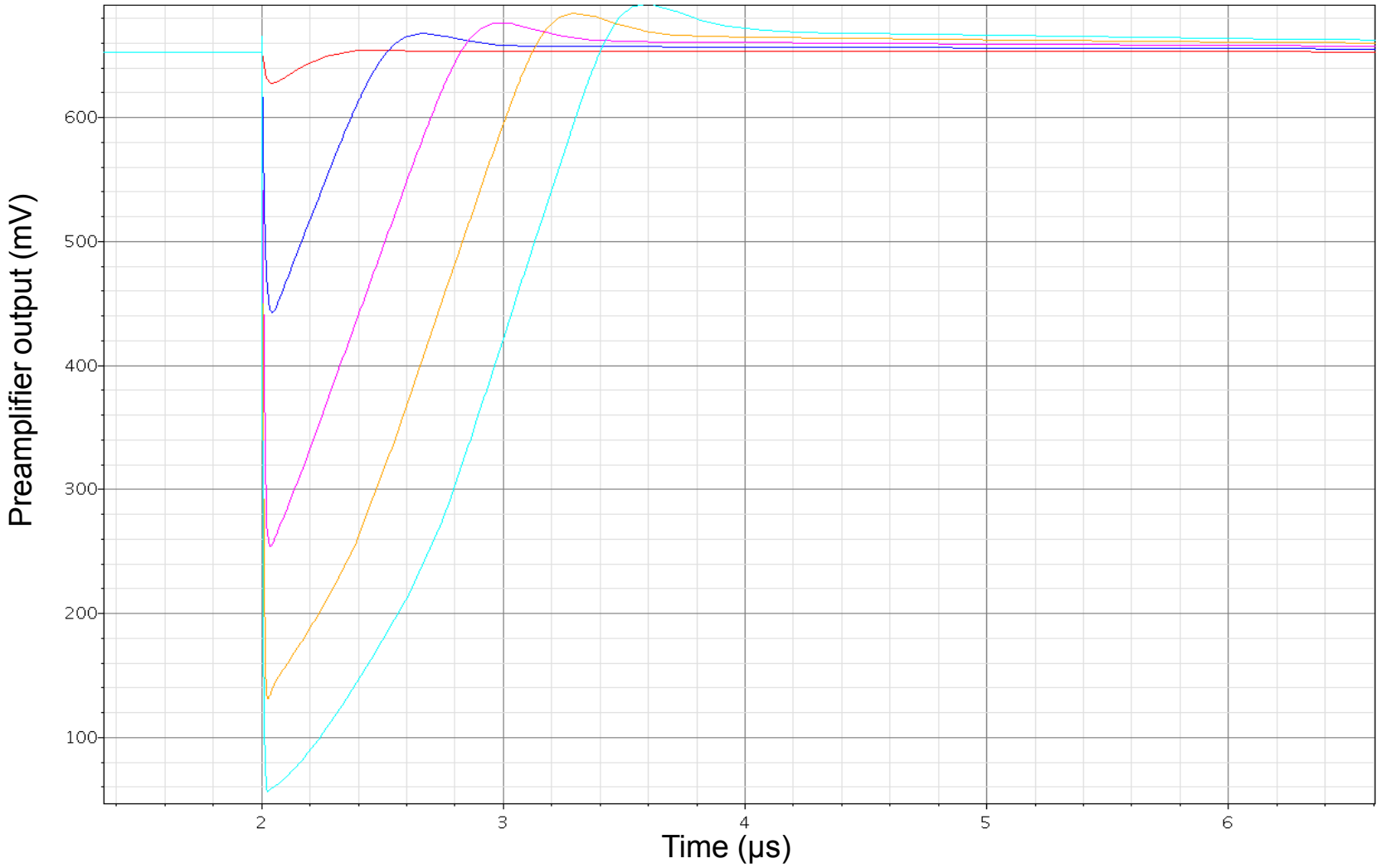
Preamplifier Layout



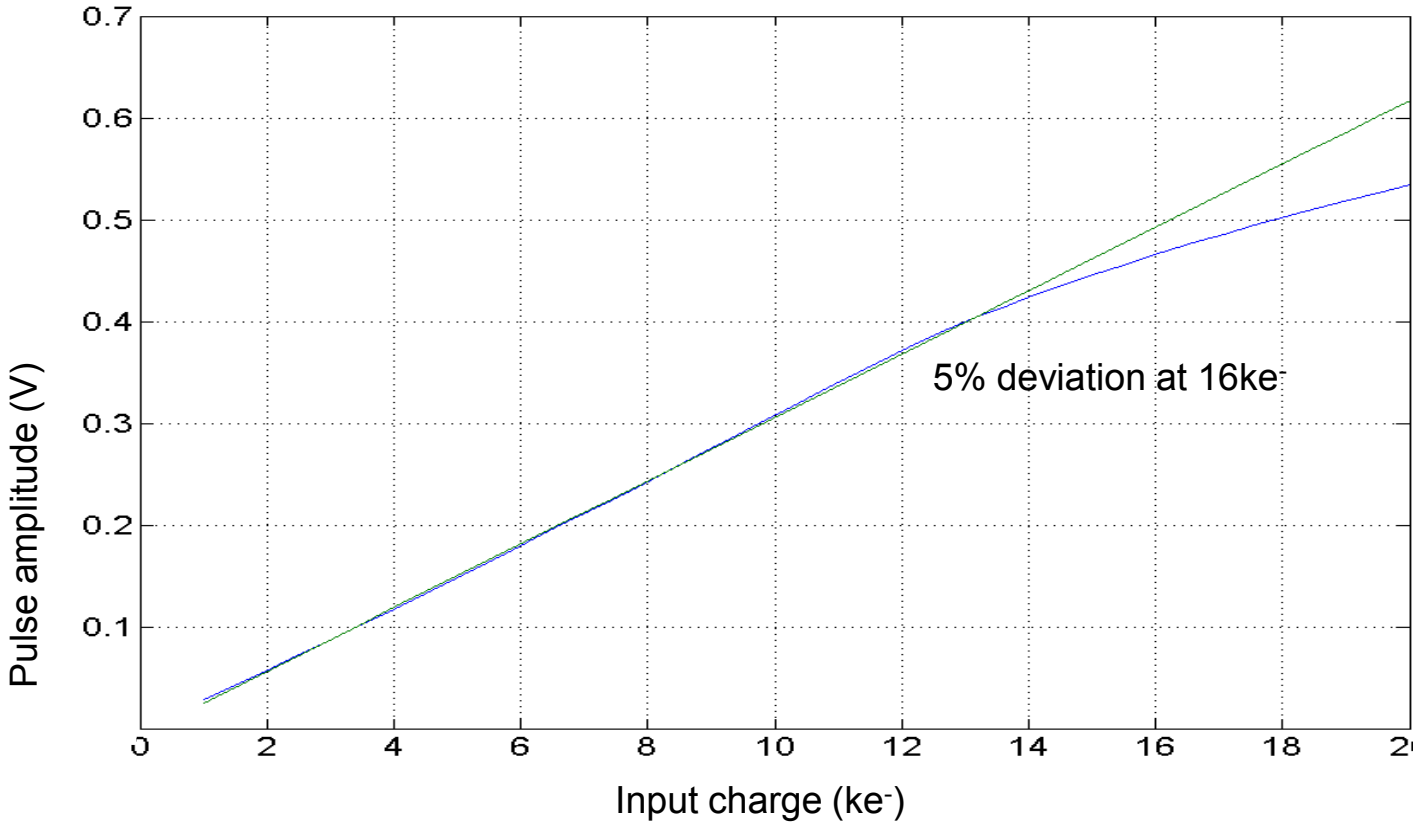
Specifications of the preamps

- Nominal values don't change with the different implementations:
- Feedback capacitance is 4fF, which corresponds to a gain of 31.5mV/ke$^-$
- Ikrum (feedback current) nominal value is 5nA, but it can be tuned from 1nA to 15nA
- Preamplifier bias current is 1.5µA
- The biasing can be modified to work with electrons or holes collection

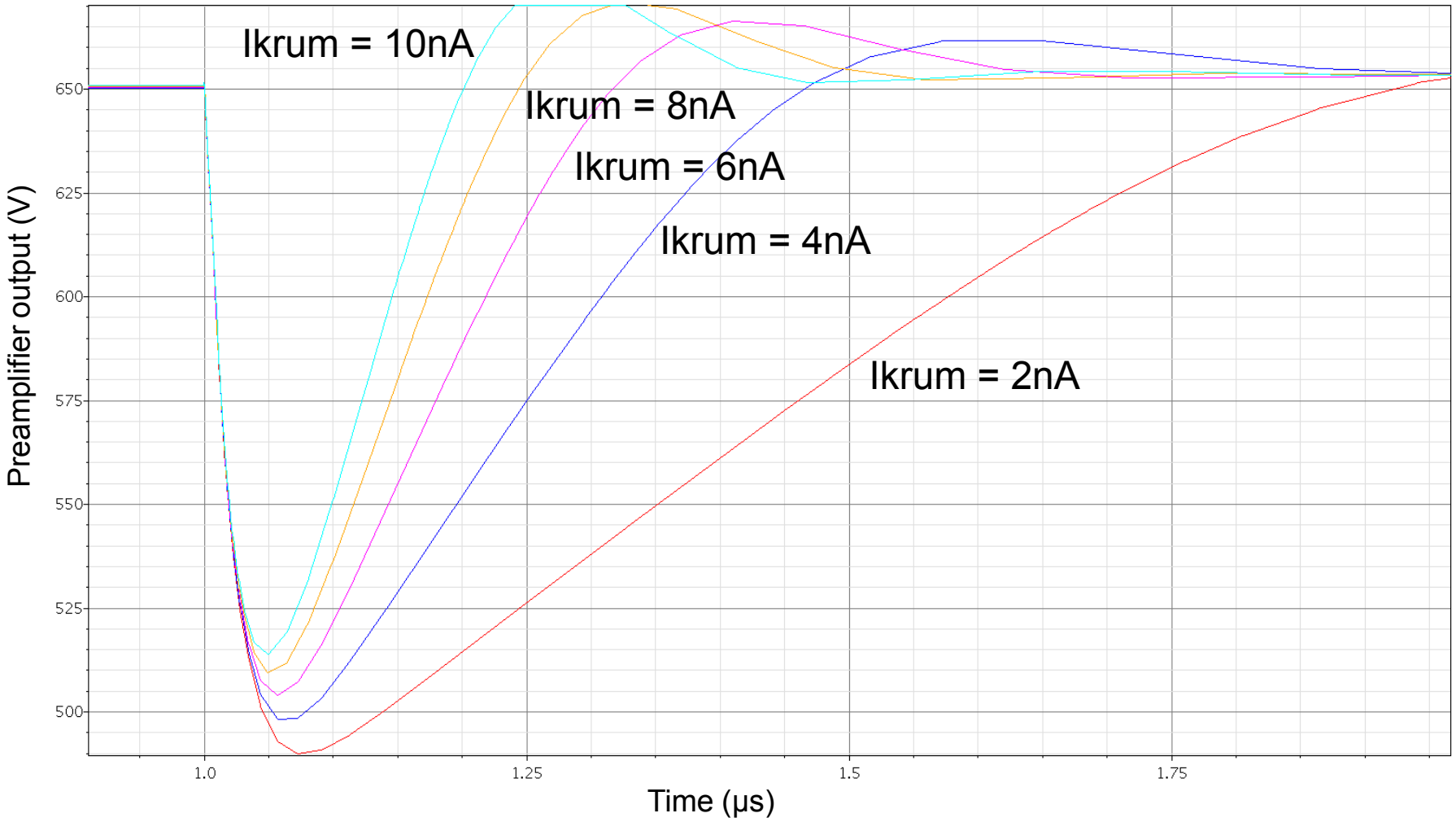
Sample test pulses (1ke$^-$ to 20ke$^-$)



Linearity of the preamplifier



Effect of change in feedback current



Other Specifications

- Peaking time: 40ns (from post-layout simulations)
- 5% non-linearity up to 16ke^-
- Speed of response can be adjusted by tuning Ikrum (but modifying the feedback current has an impact on the gain up to ±10% compared to the nominal value)

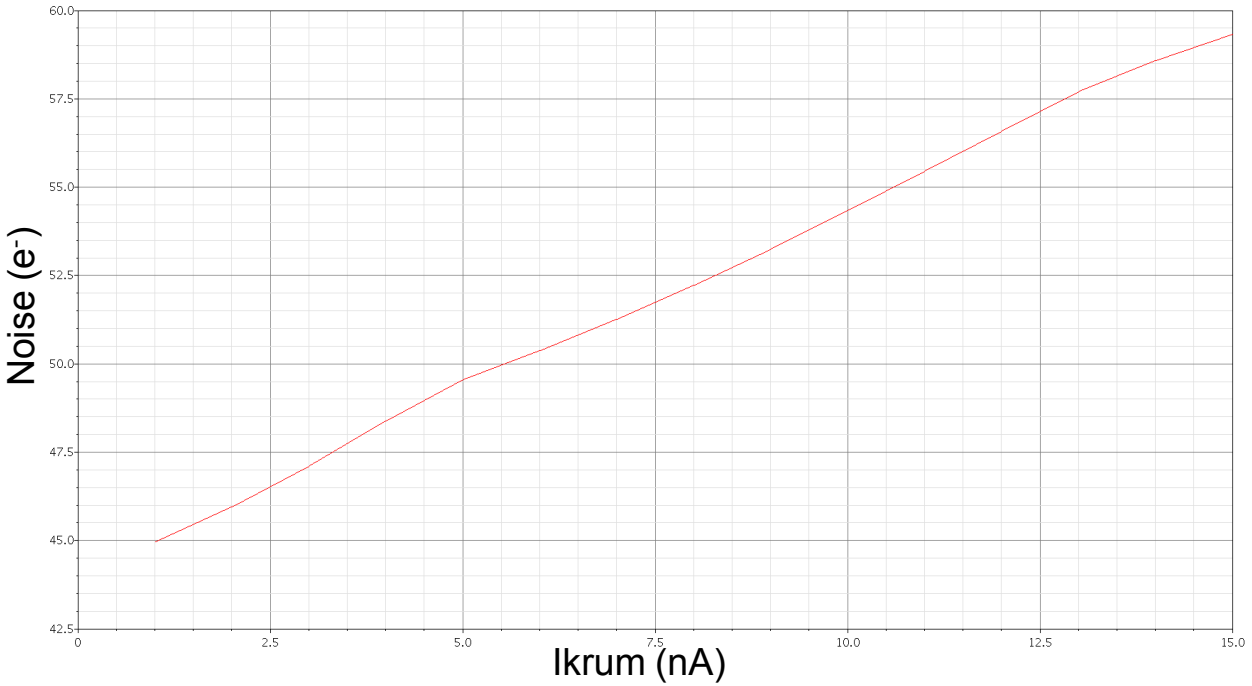
- A circuit to generate known test pulses is included for testing purposes
- Power consumption is practically due only to the single-ended OTA (nominally 1.5 µA)

Mismatch and energy resolution

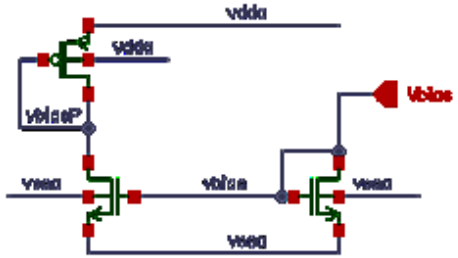
- The DC output voltage changes because of device mismatch
- Uncalibrated mismatch due to the preamplifier: 4.6mV r.m.s. (~130e^- r.m.s.)
- The front-end is not connected to the calibration DACs in this chip (to test the different subsystems one at a time)

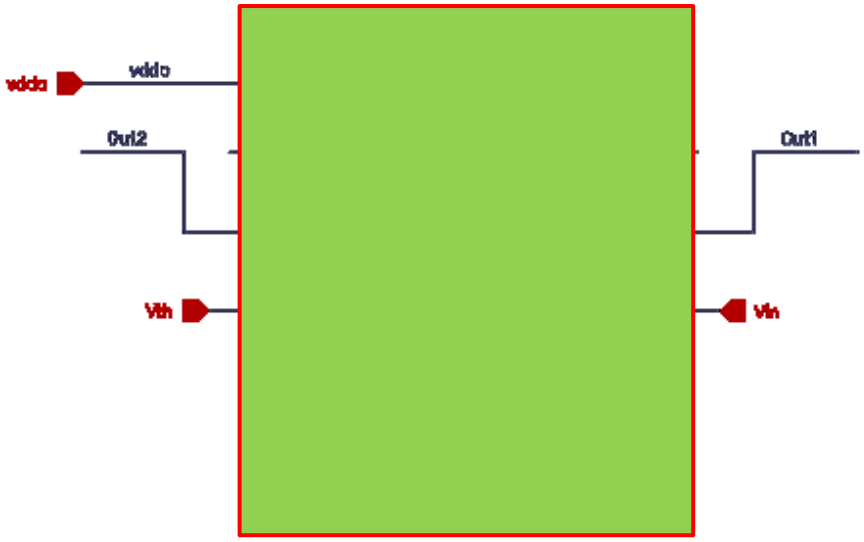
Post-layout noise simulations

- Equivalent noise charge at the output of the preamplifier was ~50e^- r.m.s. according to post-layout simulations
- Simulations included the test pulse circuit and a fake bondpad to emulate all parasitic capacitances
- Noise has a dependency on Ikrum, so it can be reduced by varying the biasing point

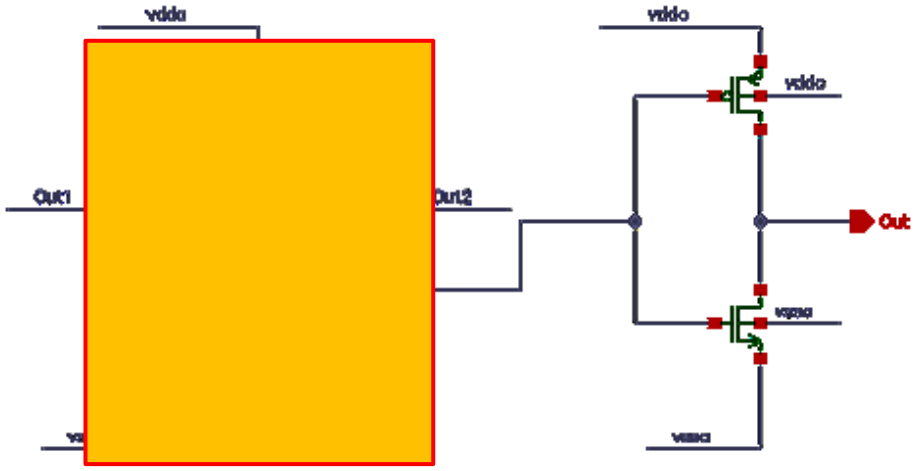


Discriminator (schematic)





First stage

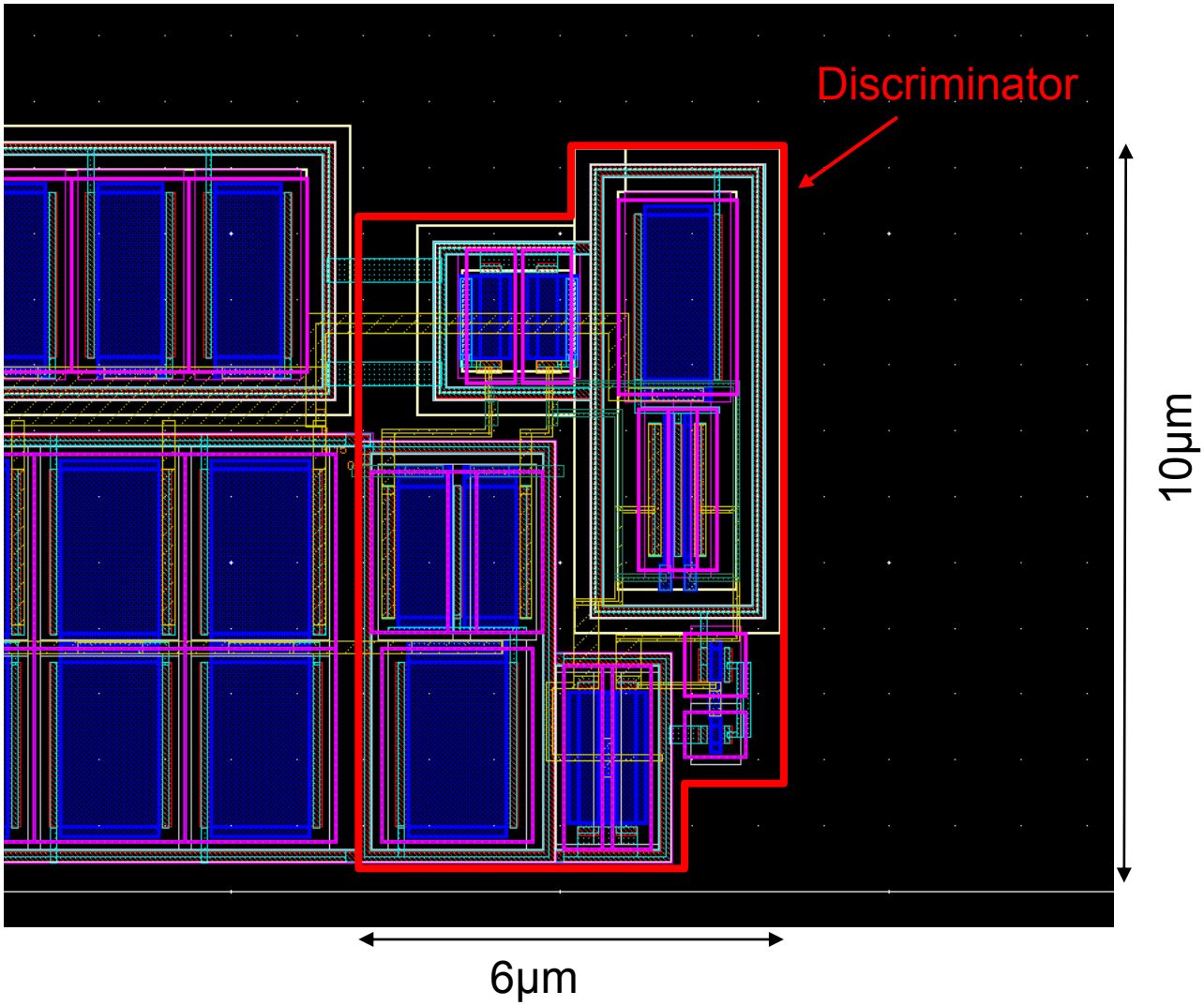


Second stage

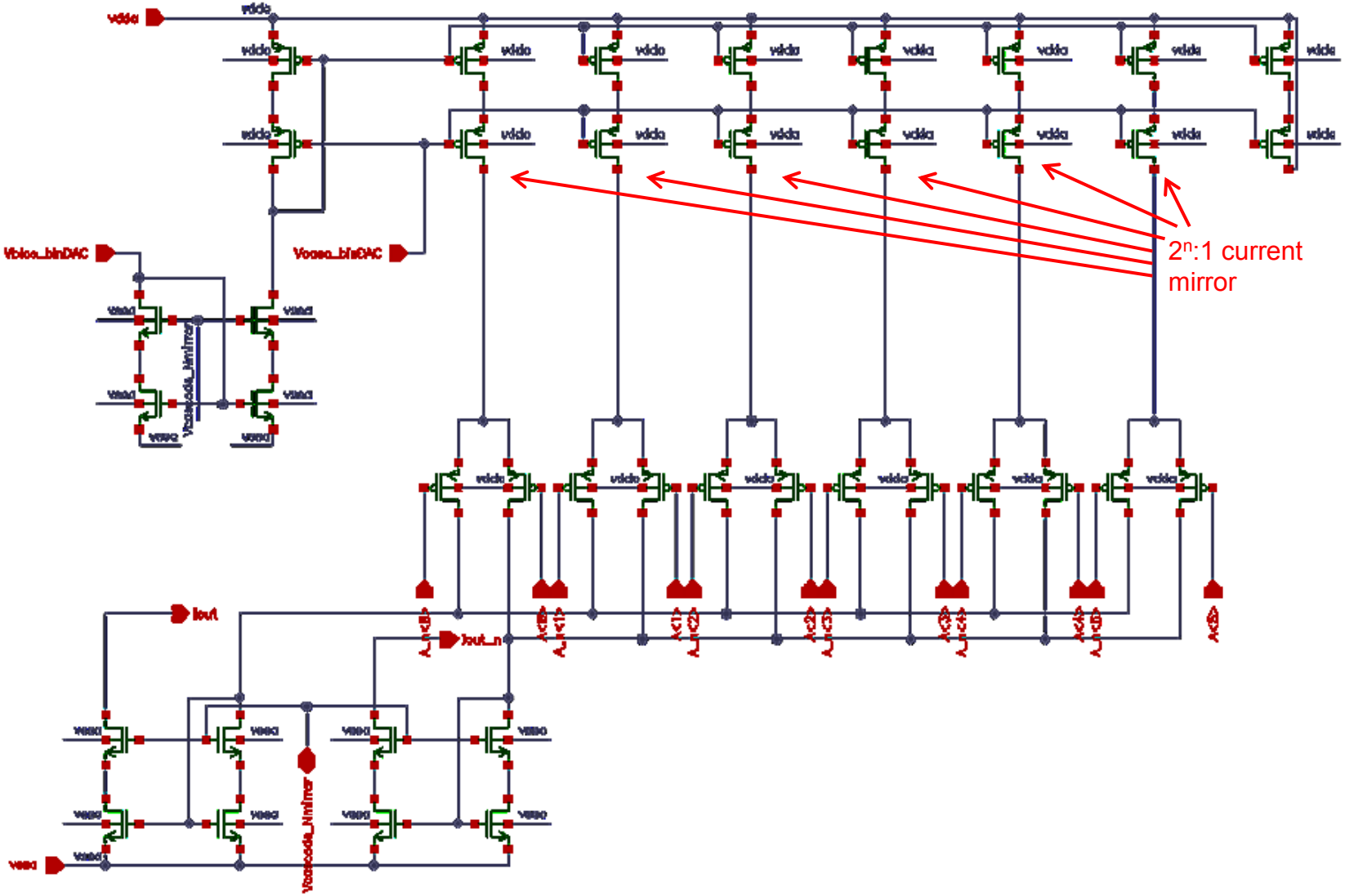
Discriminator

- Discriminator has a delay of 3.3ns
- The offset voltage due to mismatch is 3mV r.m.s. (for a total of 156e^- r.m.s.)
- Voltage input difference for the output to switch (0.2V to 1V) is 0.6mV (it is adequate for a 6 bits equalization DAC)
- Current consumption is 4μA
- Different biasing currents are possible
- Circuit size is 6x10μm

Discriminator Layout

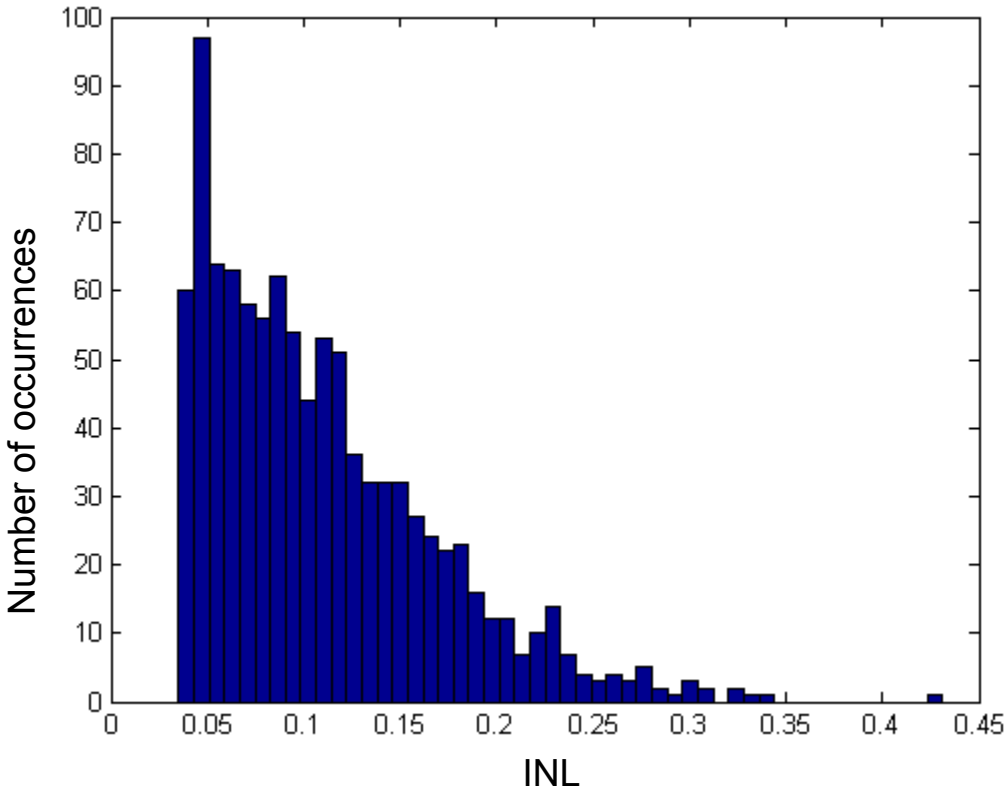


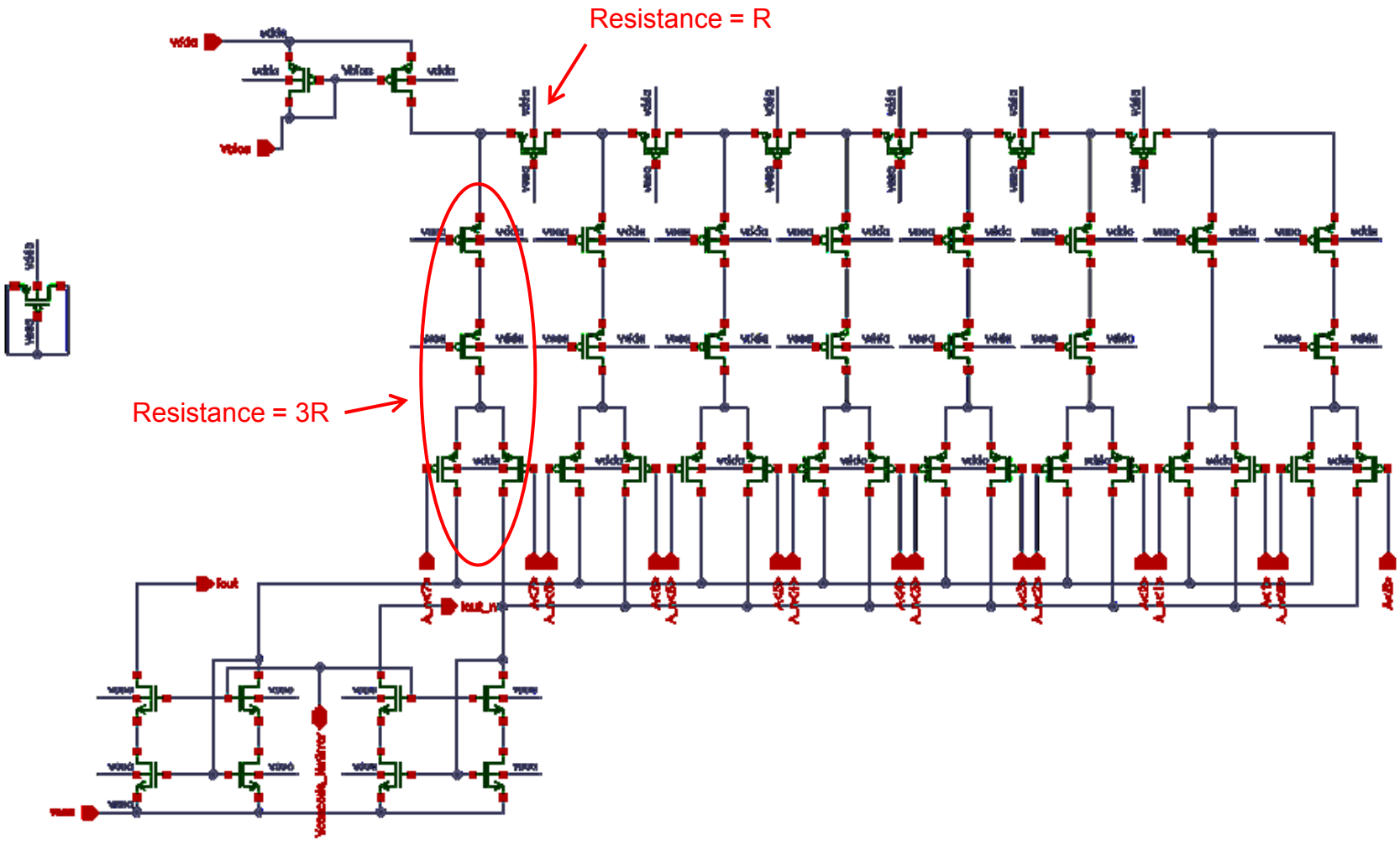
Binary weighted DAC (schematic)



Binary weighted DAC

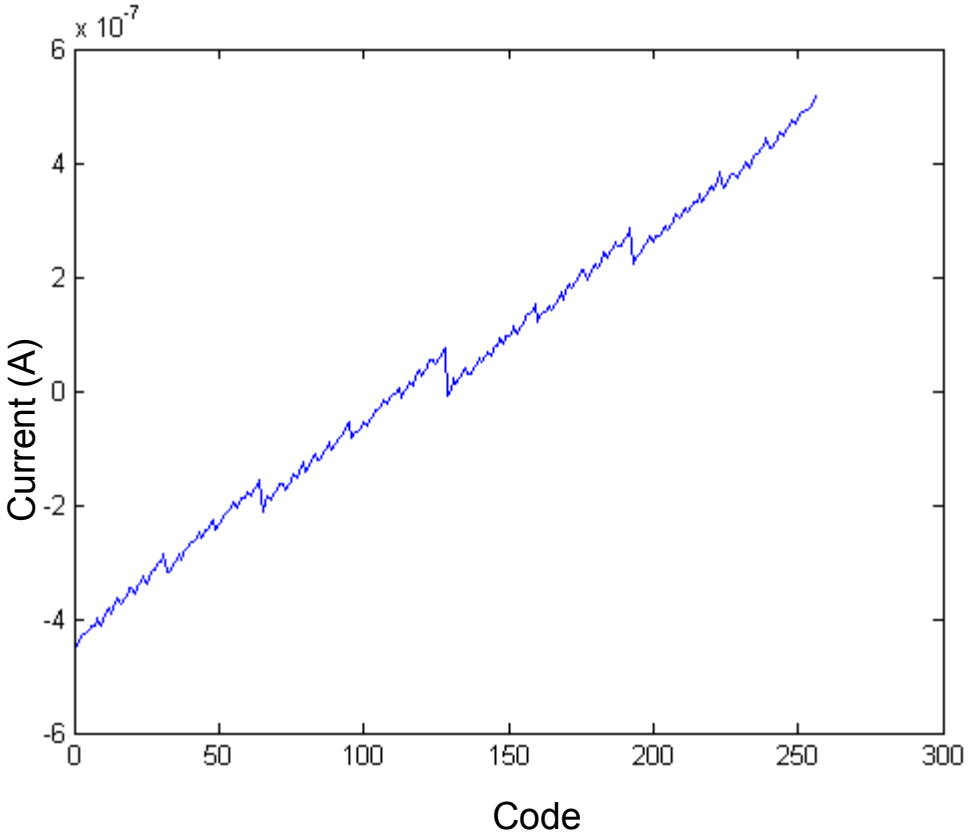
- Transistors size: 10x1µm (mismatch σ/μ_{LSB} ~2.5%)
- INL calculated in 1000 points Montecarlo simulation
- Total circuit size: 105x15µm!




Resistance = R
Resistance = 3R

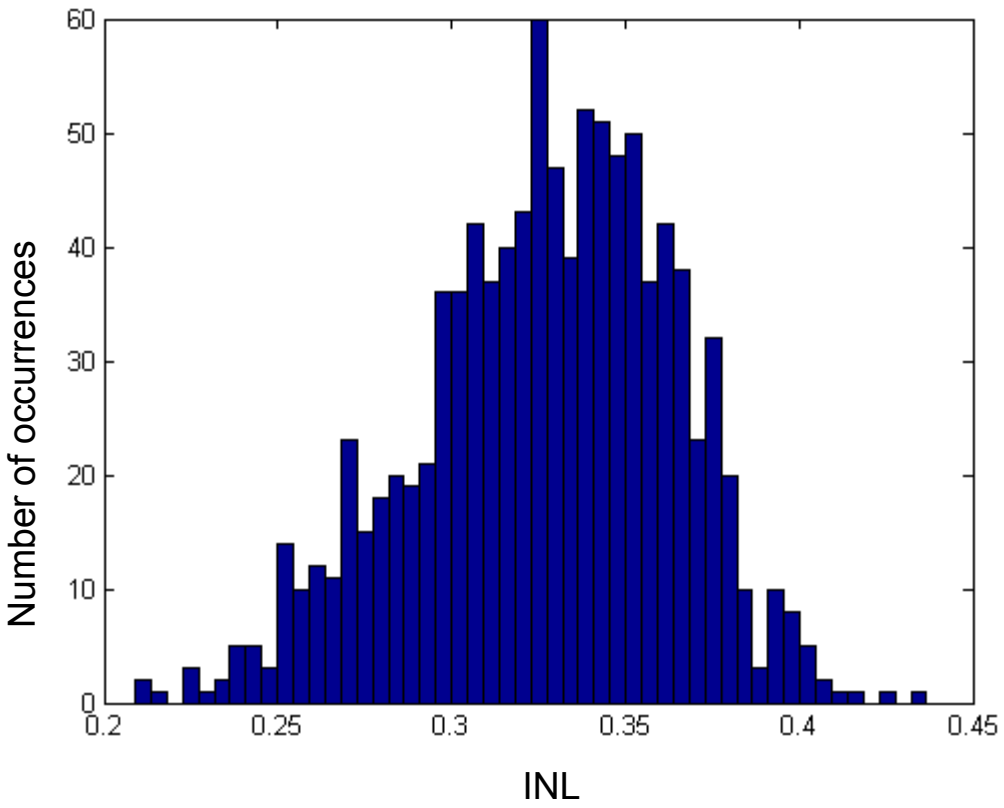
Sub-binary radix DAC characteristic

- Caracteristic is non linear and non monotonic (having a level of redundancy)
- More bits are used to recover the lost dynamic range

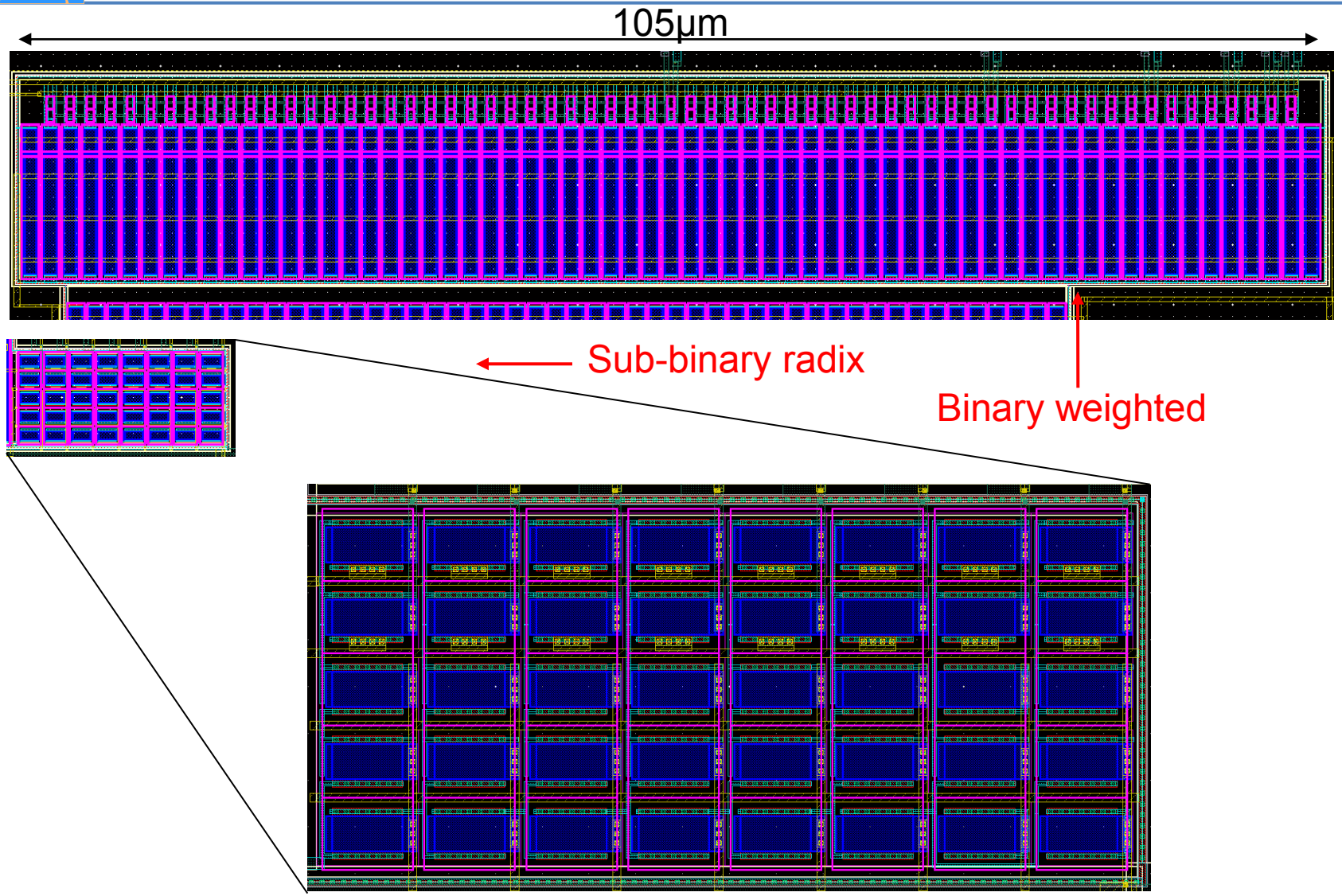


Sub-binary radix DAC non-linearity

- Transistors size: 1x0.75µm (mismatch σ/μ_{LSB} ~12%)
- INL calculated in 1000 points Montecarlo simulation
- Total circuit size: 17x8µm



DAC layout comparison



Main issues of the new technology…

- Much higher gate leakage current and higher subthreshold conduction. It is negligible for a test pixel, but it must be considered for large arrays, mainly to provide a stable biasing. Buffers for biasing voltages will be needed.
- More stringent design rules: ELT transistors for example are not allowed (a DRC waiver was necessary). It is more difficult to achieve an optimal layout.

Main issues of the new technology…

- Smaller dynamic range due to the lower power supply reduced the possibilities to use some structures (such as cascoded stages). Multiple stages, with possible stability issues, are needed to achieve a high gain.
- This problem is moreover worsened by the lower output resistance of the MOSFETs which lowers the gain of the single stages.
- Higher cost of tape-out compared to older technologies

… and its main advantages

- The main advantage is the smaller area.
- Compared to the Medipix3 chip (designed in a 130nm technology) the preamplifier is ~10% smaller.
- The sub-binary radix DAC is also very small (it is the same size as Medipix3 calibration DAC, but has a 4-bit accuracy, compared to 6-bits implemented with 8 real bits).

… and its main advantages

- Lower equivalent noise charge, due to the possibility of designing smaller pixels.
- More metal layers are available for routing, making some parts of the layout easier.
- Much better digital circuitry integration. Digital standard cells are approx. 60% smaller than corresponding 130nm cells, so it is possible to achieve a smaller pixel size or put more “intelligence” in each pixel.

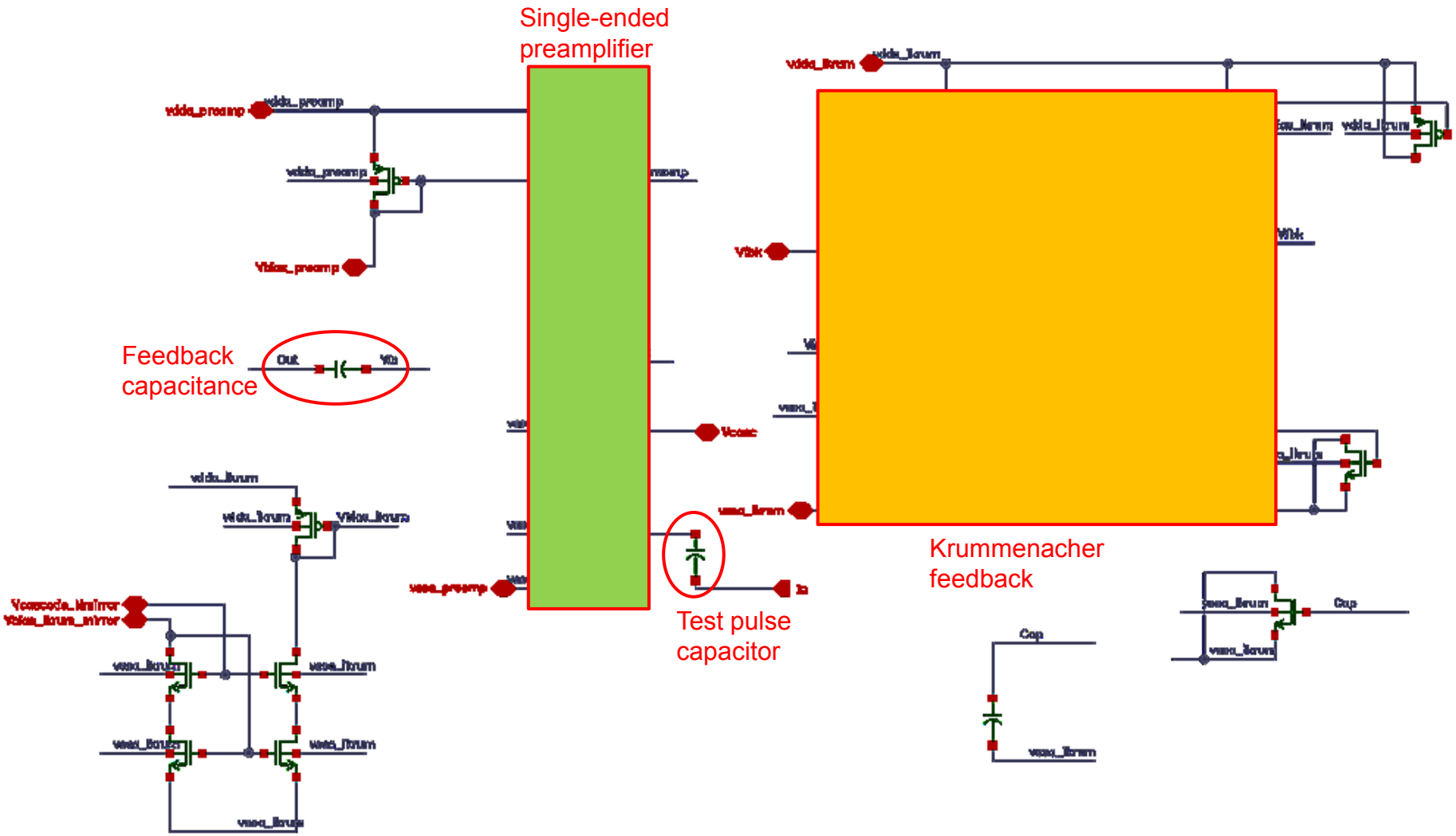
Conclusions

- The main advantages and disadvantages of moving to a downscaled technology for front-end electronics for HEP applications have been analyzed
- The reduction in size, especially for the digital part (up to 60%), is needed if smaller pixel pitches are to be achieved. Noise reduction is also an important benefit of new technologies
- Lower dynamic range and higher leakage currents must be taken into account (low-voltage architectures and buffers for global signals can be used)
- A test chip containing both analog front-end circuitry and test structures for radiation testing has been developed and will be tested in the next months

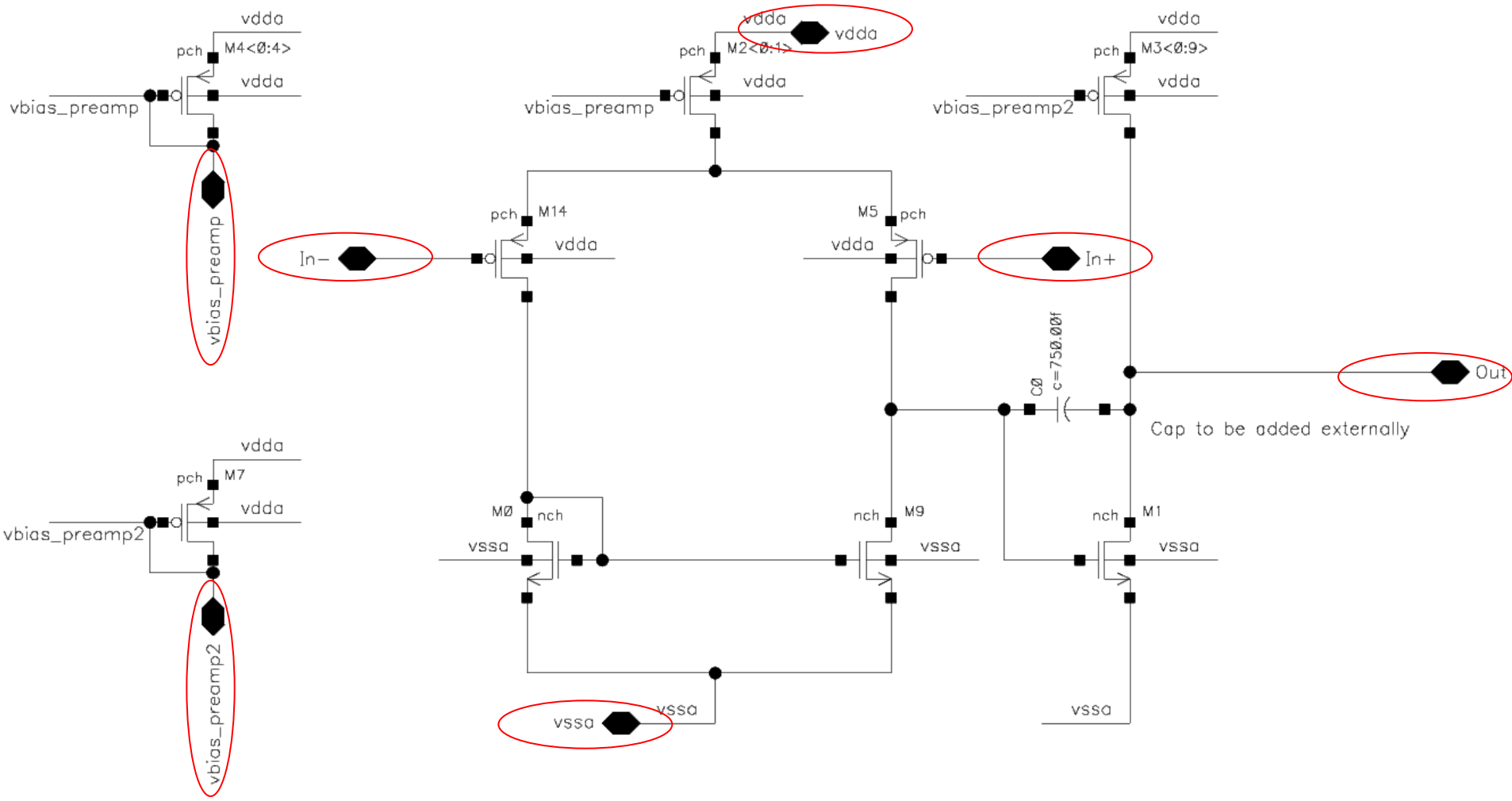
Thanks for your attention

Backup Slides

Preamplifier (schematic)



Output buffer (schematic)



Other Test Structures

- Other than analog structures, on chip 1 and 2 a number of single transistors are connected to pads, in order to test their characteristics during/after radiation exposure
- On chip 1 a high number of devices share the same gate and source connections and have separate drains
- On chip 2 a lower number of devices is present, but they have all unique connections for both gates and drains

Test Devices

Test devices include:

- NFETs/PFETs of different sizes
- Native, high Vt and high voltage devices
- Triple well and dual gate devices
- Enclosed layout transistors
- Diodes, resistors, FOXFETs…

Digital Circuits

Chip 3 has three digital structures for testing purposes:

- Shift register
- Ring oscillator
- SRAM

The circuits were designed using libraries provided by the foundry (for both the digital cells and the memory)