

Design and measurements of readout ICs for hybrid pixel detectors in 90 nm CMOS technology

R. Szczygiel, **P. Grybos**, P. Maj
Department of Measurement and Instrumentation,
AGH UST, Cracow, Poland

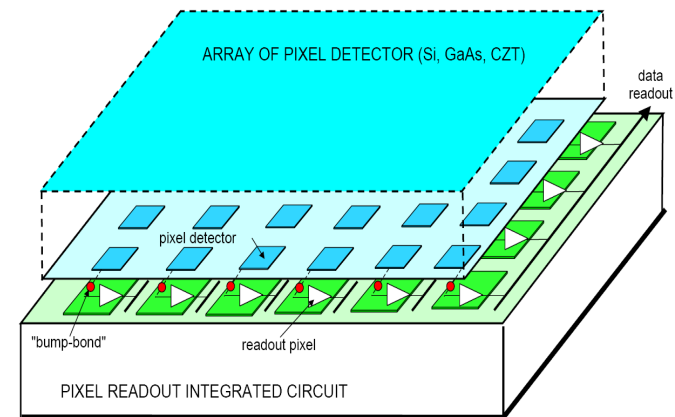
Outline



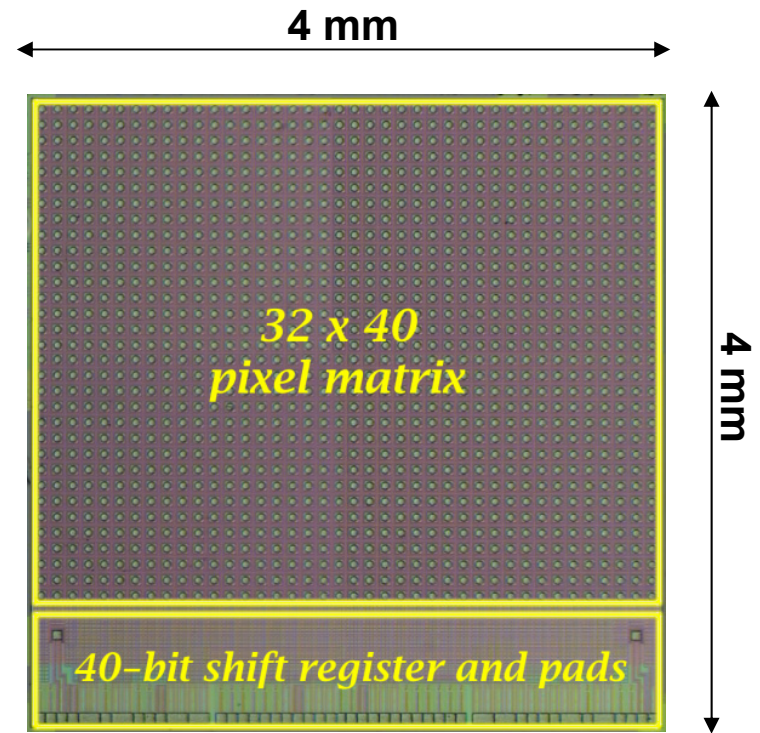
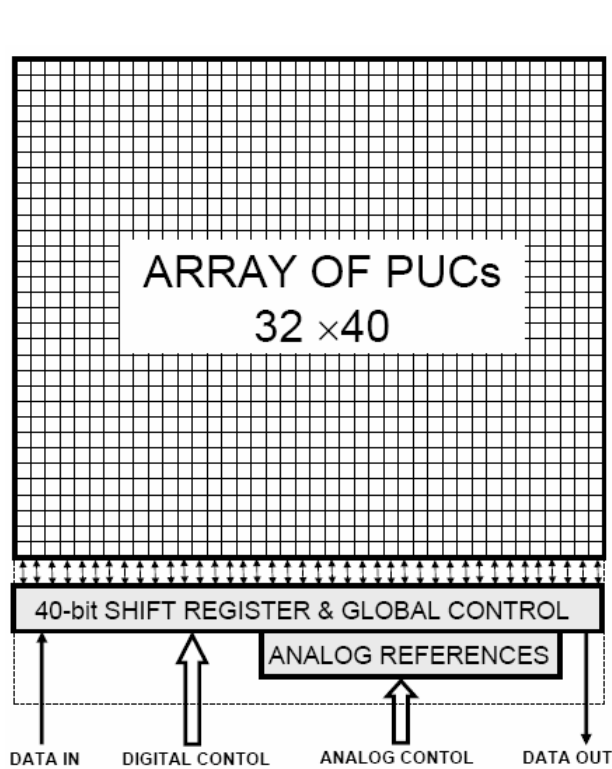
1. Motivation:
imaging with single photon counting
2. Readout chip architecture
3. Measured parameters
(matching, ENC, high count rate performance)
4. Conclusions

Motivation: project in DSM technology

- Prototype readout chip for hybrid pixel detector working in SFC mode (X-ray imaging applications: 8 keV)
- Functionality:
 - single photon counting,
 - energy window,
 - continuous readout
- Critical parameters:
 - pixel size $100 \times 100 \text{ } \mu\text{m}^2$,
 - noise - matching – high count rate
- Submicron technology (CMOS 90 nm)



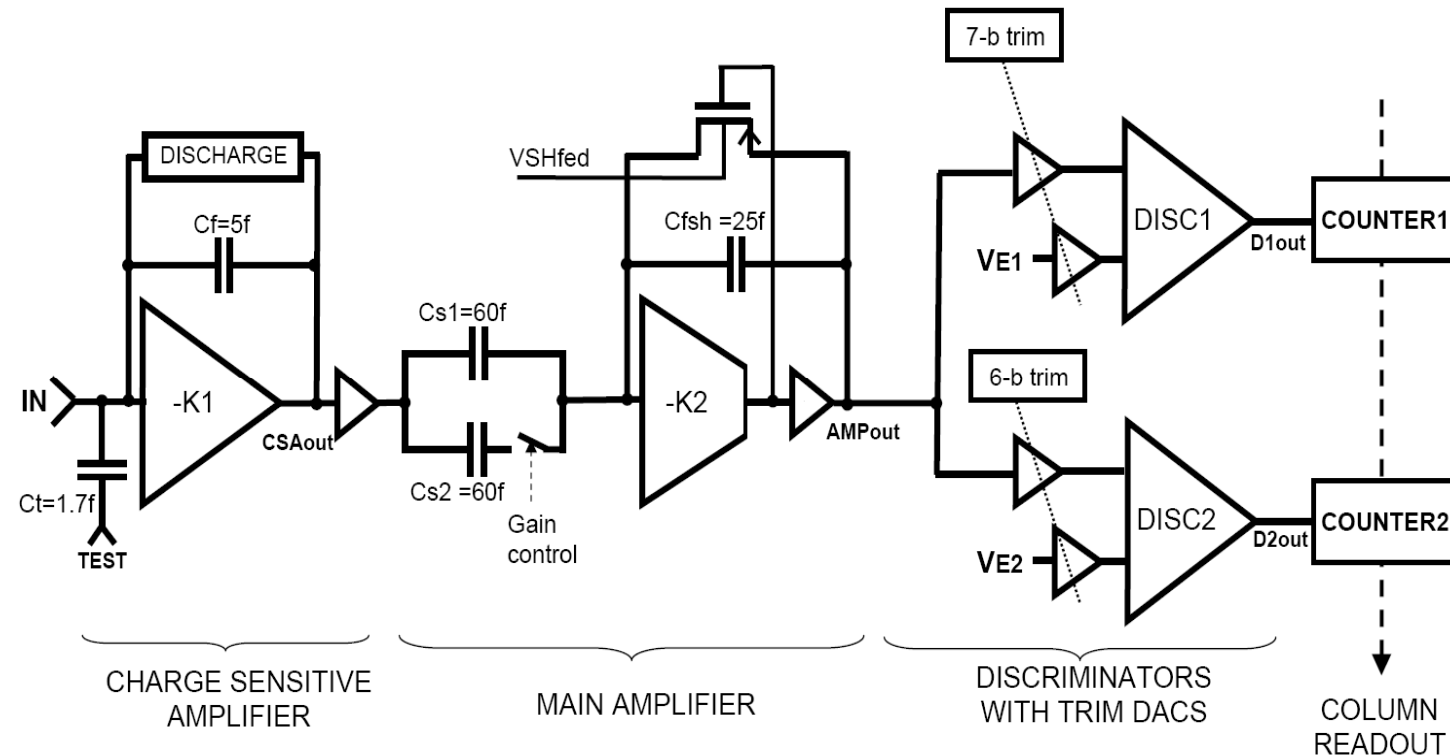
Architecture of PX90DC



Chip photo

1280 pixels (100x100 μm^2), CMOS TSMC process 90 nm

Single channel architecture



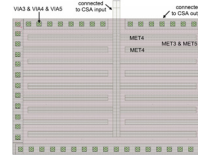
Comments:

- single ended CSA and shaper (AC coupling)
- noise minimization in CSA
- main amplifier with feedback bias
- offset correction

CSA core

Vddm = 0.8V
Vdda = 1.2V

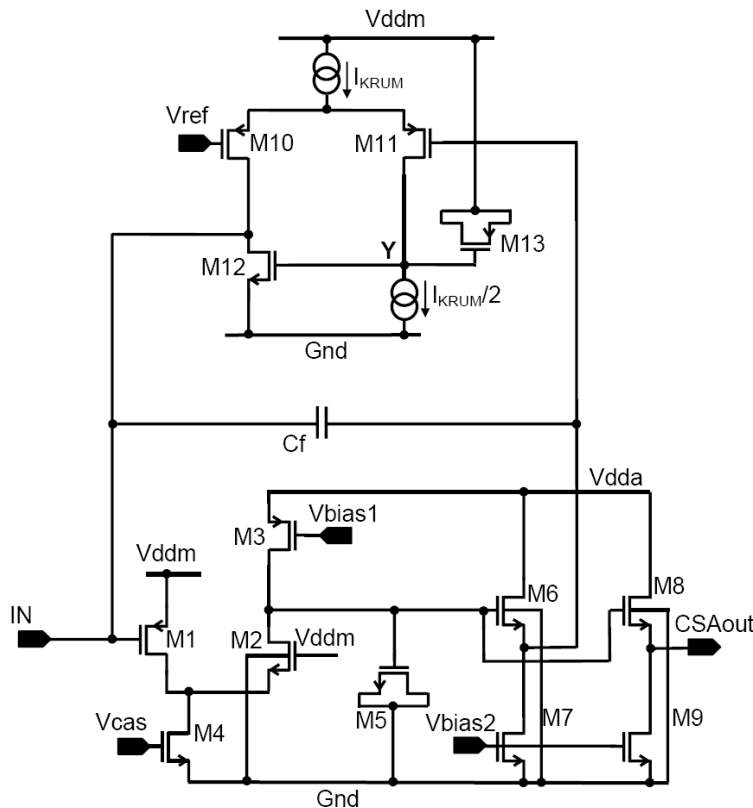
Cf = 5fF



$$I_F = \frac{I_{DS}}{2n\mu C_{ox}(W/L)\phi_T^2}$$

OPERATING POINT OF SELECTED TRANSISTORS IN CSA

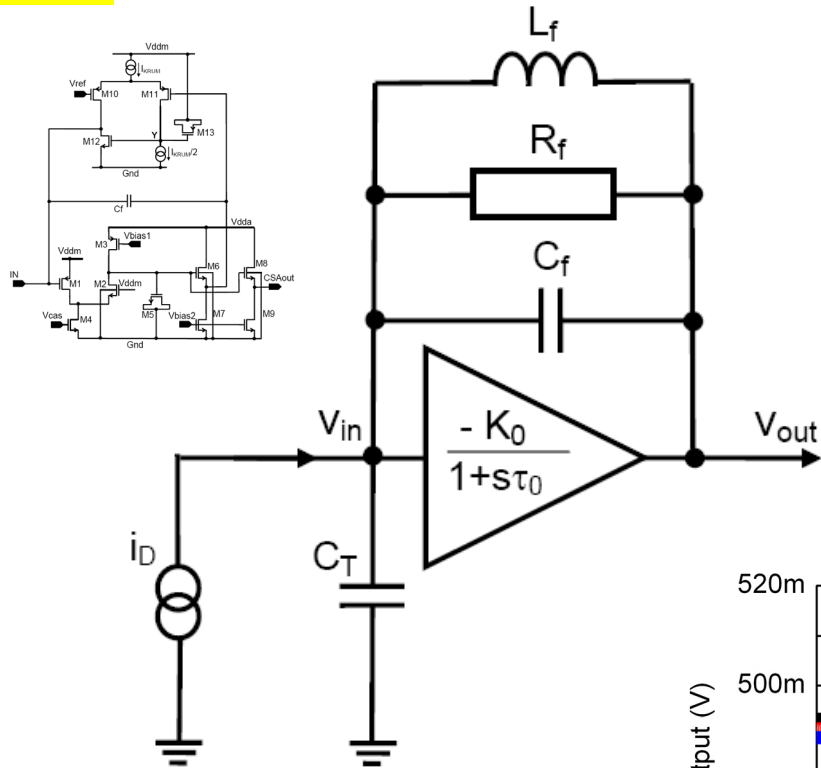
Device	W/L [μm/μm]	I _{DS} [μA]	g _m [μA/V]	g _{ds} [μA/V]	I _F
M1	20/0.2	5.06	124	3.73	0.273
M2	5/0.2	1.07	27.3	0.87	0.076
M3	2/3	1.07	11.1	0.19	8.67
M4	1.44/20	6.13	6.7	10.2	151



Noise performance .

$$\frac{dv_{core}^2}{df} \approx \frac{dv_1^2}{df} + \frac{(g_{ds1} + g_{ds4})^2}{g_{m1}^2} \frac{dv_2^2}{df} + \frac{g_{m3}^2}{g_{m1}^2} \frac{dv_3^2}{df} + \frac{g_{m4}^2}{g_{m1}^2} \frac{dv_4^2}{df}$$

Signal shaping at CSA output



$$H_1(s) = \frac{v_{out}}{i_D} \approx \frac{-sL_f}{As^3 + Bs^2 + Cs + 1}$$

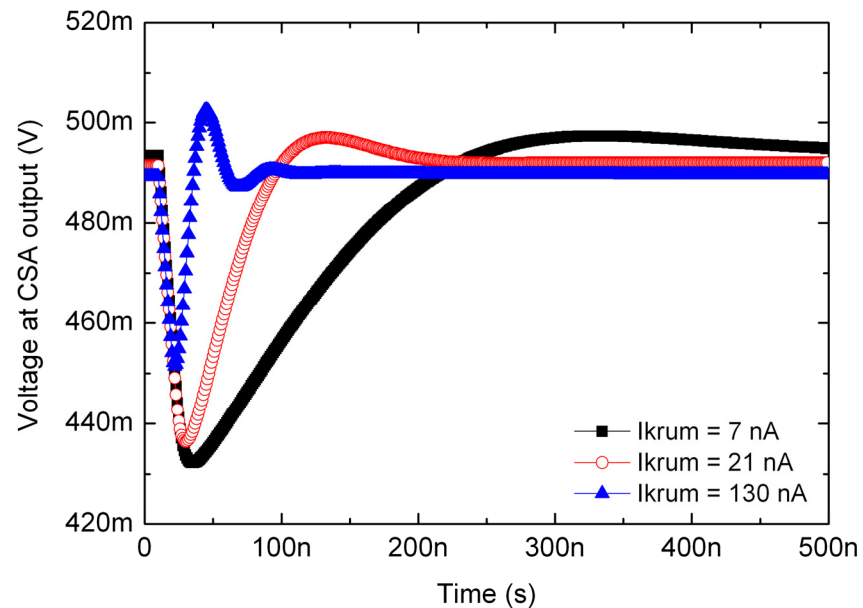
$$A = \frac{L_f(C_T + C_f)}{\omega_0 K_0}$$

$$B = L_f \left(C_f + \frac{1}{R_f \omega_0 K_0} + \frac{C_T}{K_0} \right)$$

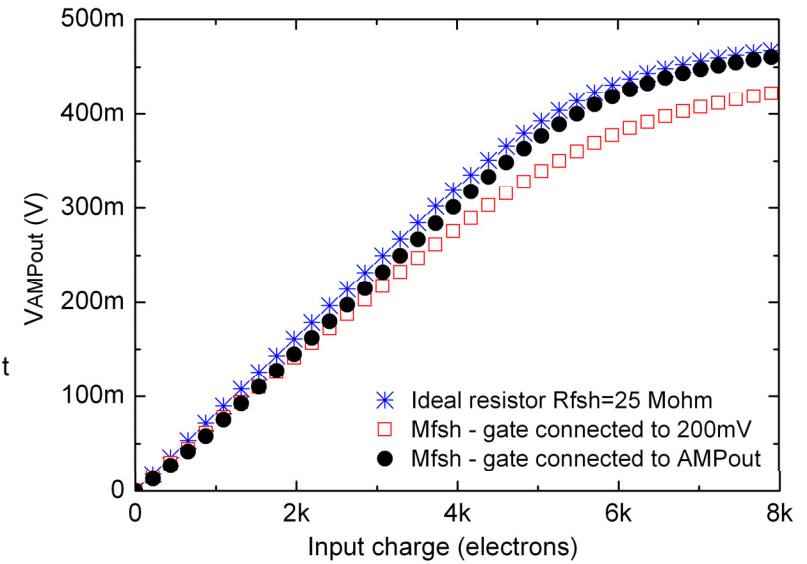
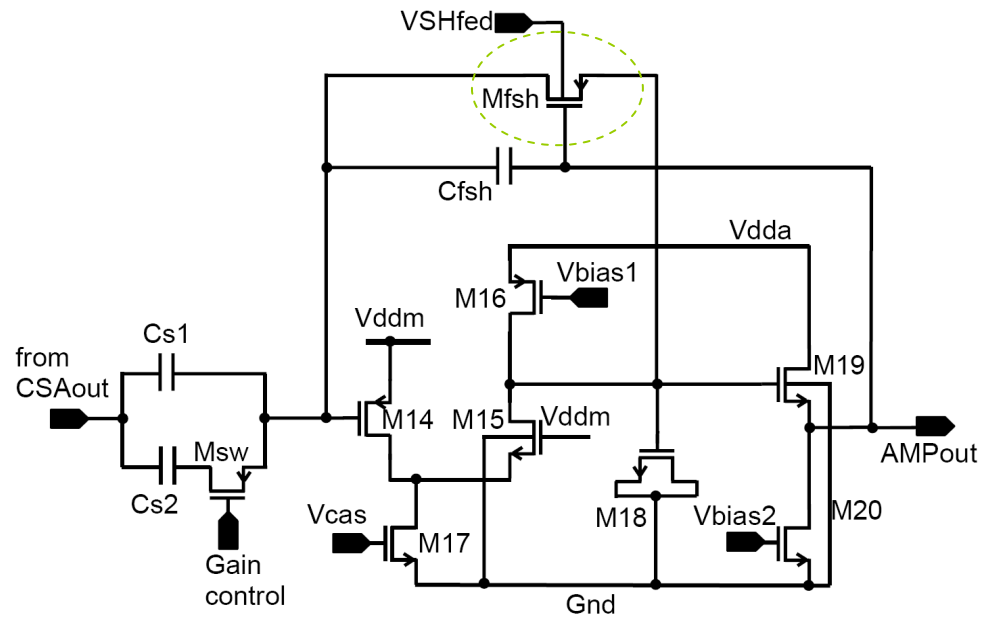
$$C = \frac{L_f}{R_f} + \frac{1}{\omega_0 K_0}$$

$$R_f \approx 2/g_{m10}$$

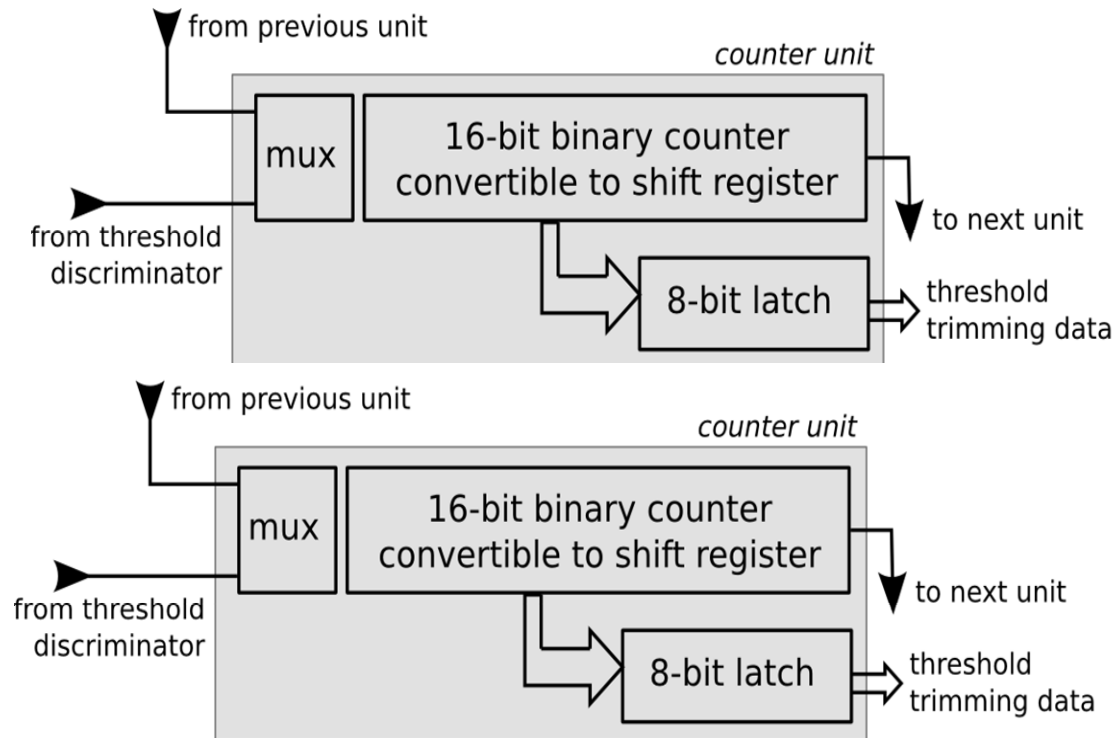
$$L_f = \frac{2C_{g13}}{g_{m10}g_{m12}}$$



Main amplifier

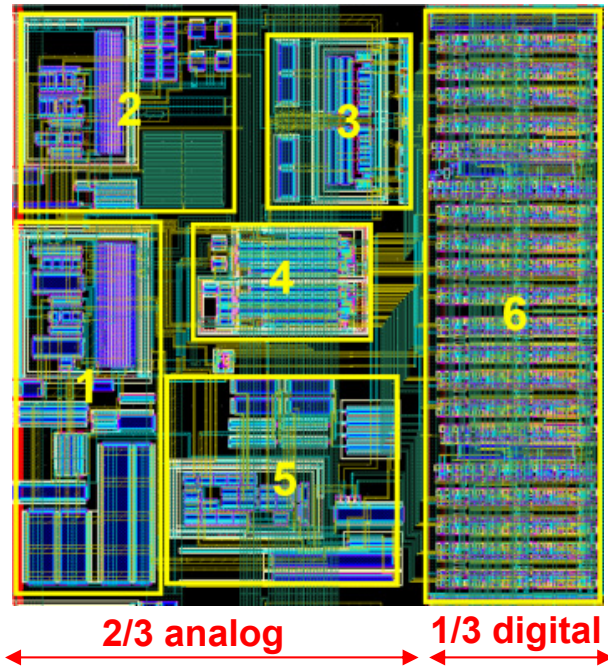


Digital part of pixel



Each unit contains a 16-bit binary counter which can be converted into a shift register. The units are grouped according to the thresholds, e.g. the units counting the low threshold discriminator pulses are connected together and the units counting the high threshold discriminators are connected together. This way the data for both thresholds can be read out independently.

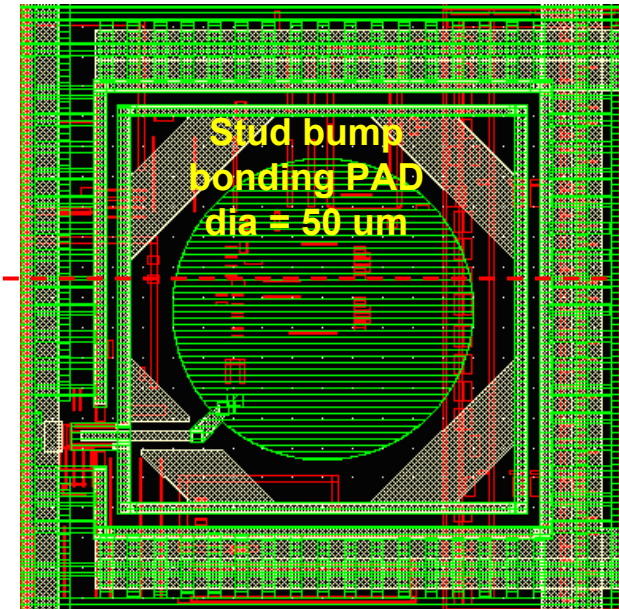
Layout of single pixel



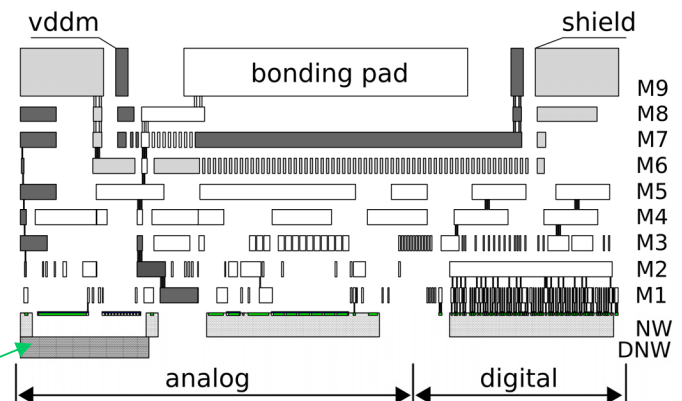
- Blocks in single pixel**
(MET4-MET9 are removed):
- 1 - CSA ,
 - 2 – main amplifier,
 - 3 - discriminators,
 - 4 - trim DACs,
 - 5 - reference blocks,
 - 6 - counters and registers

Input pad capacitance was reduced to 80 fF

NMOS transistors in Deep N-WELL



Cross section:



Tests, detector bonding

power consumption, functionality

The following tests were performed for FPDR90 IC:

- static and dynamic power consumption,
- functionality of the digital block,
- effective threshold spread and its correction,
- gain measurement and noise performance,
- crosstalk in continuous readout mode.
- high count rate tests,

Power supply voltage:

- analog part: 0.8V (CSA input) and 1.2V
- digital part: 1.2V (core) and 2.5V (LVDS)

Power consumption per pixel:
no coating: 42 uW/pixel

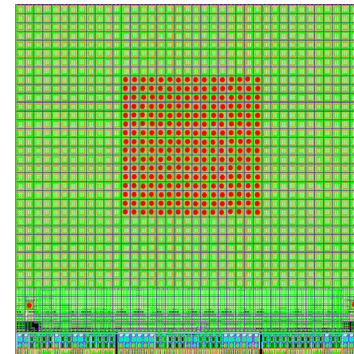
Functionality: OK.

LVDS input/output;
checked at that moment up to 200 MHz

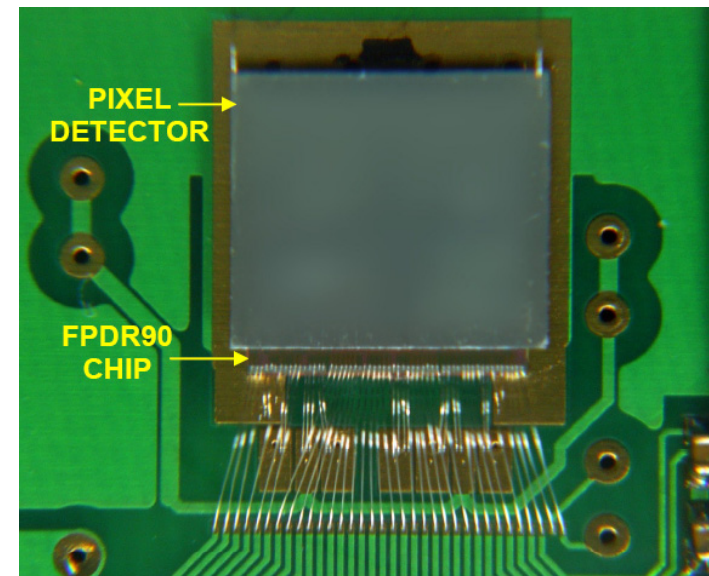
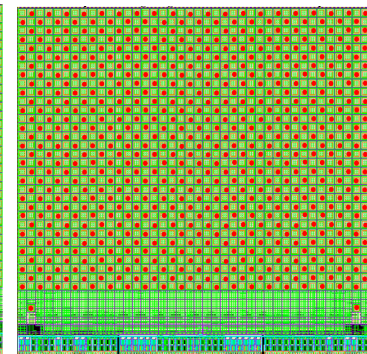
NI PXI-6562 200 MHz

Digital Waveform Generator/Analyzer.

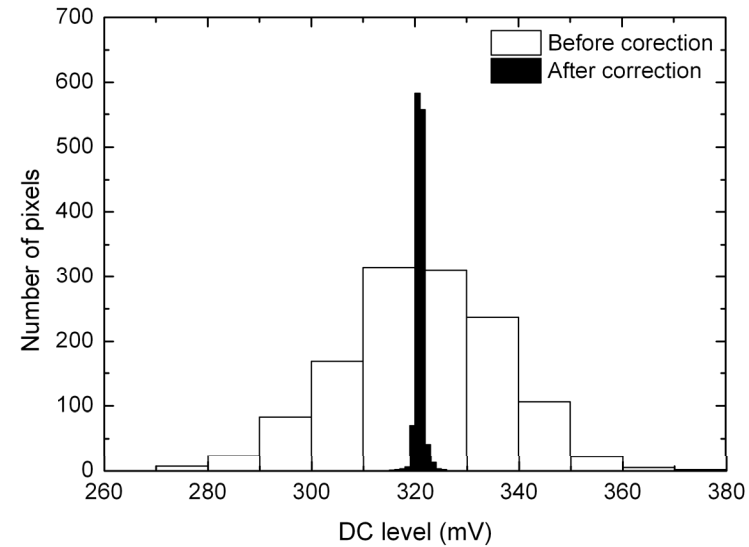
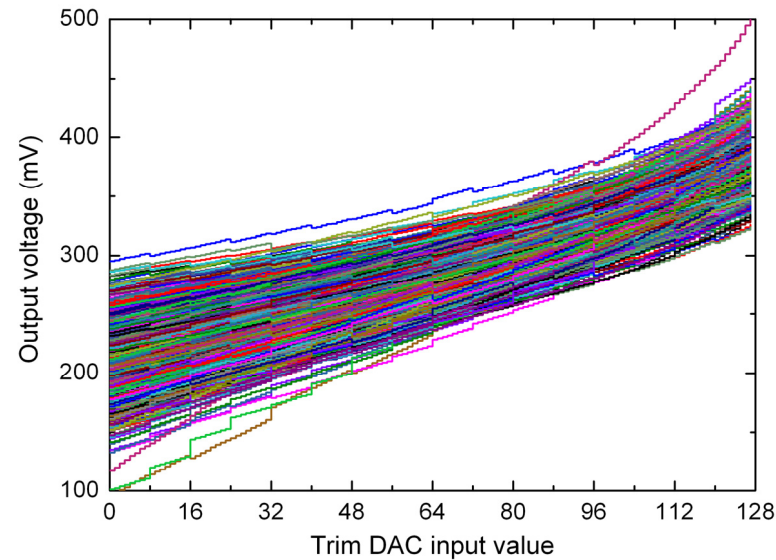
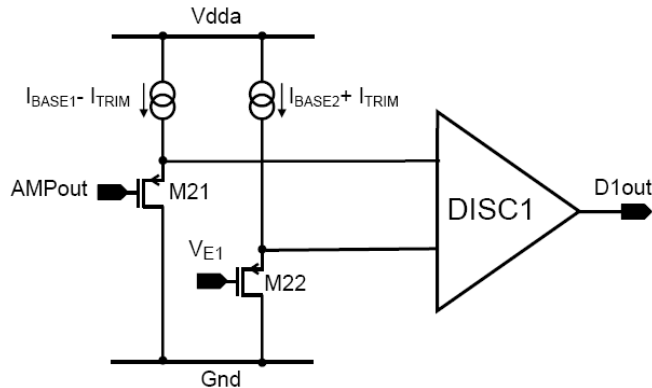
Pattern A



Pattern B



Trim DACs – offset correction



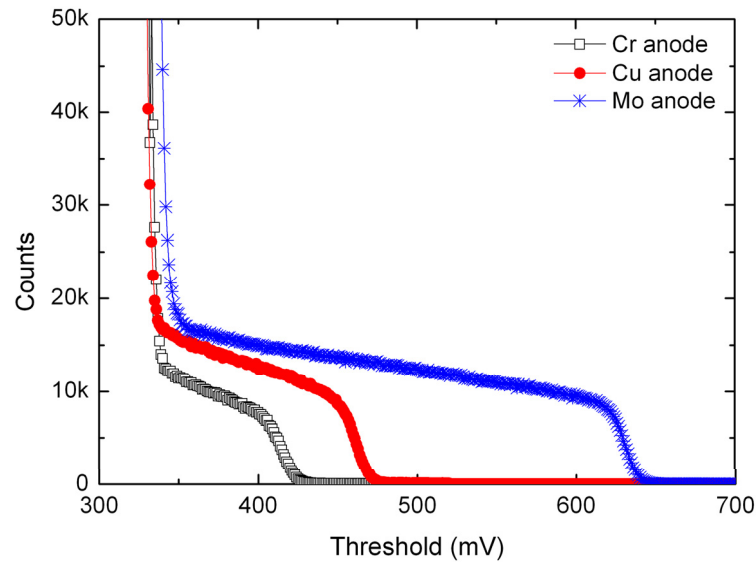
Results:

- before correction: $sd = 15 \text{ mV}$
- 7-bit trim: $sd = 0.76 \text{ mV}$
- 6-bit trim: $sd = 1.19 \text{ mV}$

Comments:

- changing trim DAC value does not change power consumption of PUC,
- range of trim DAC is controlled by external resistors

Measurement with X-ray tube

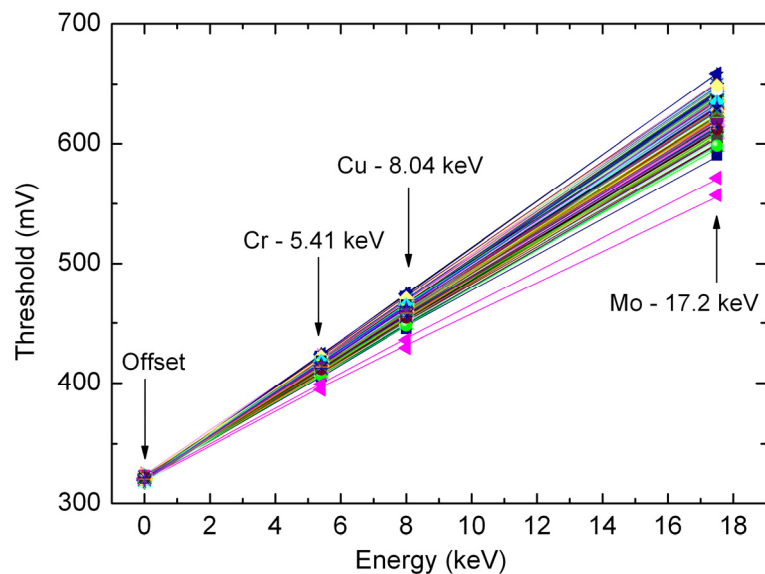


GAIN:

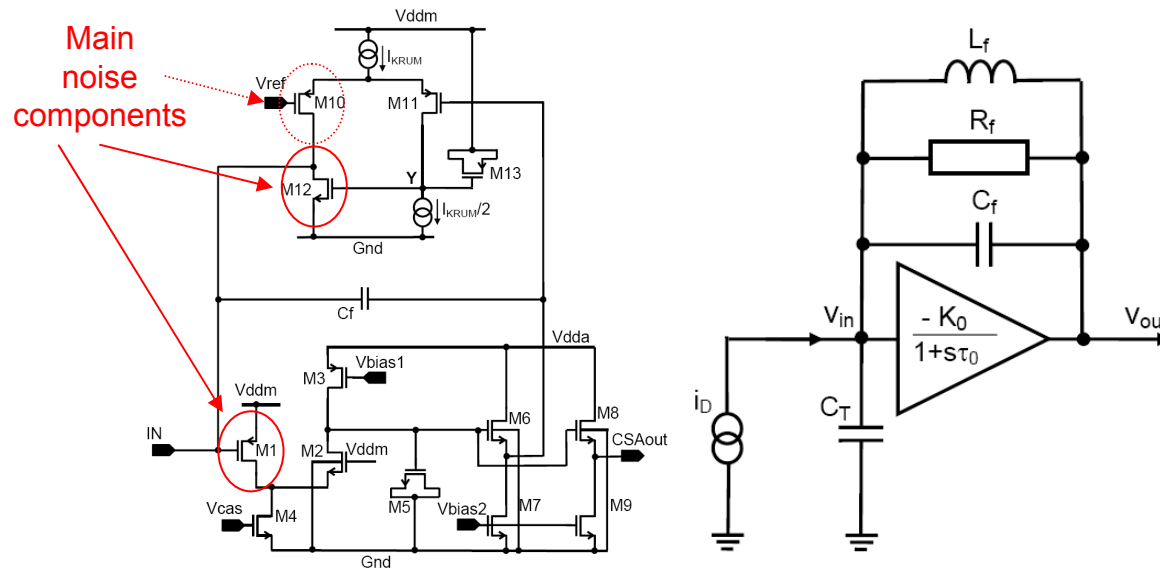
- high gain mode: **64 uV/el (sd = 2 uV/el)**
- high gain mode: **32 uV/el (sd = 1.2 uV/el)**

NOISE (high/low gain)

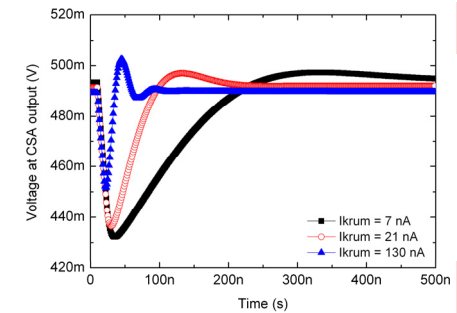
- pixel connected to the detector: **106/107 el rms.**
- pixel not connected to the detector: **91/95 el rms.**



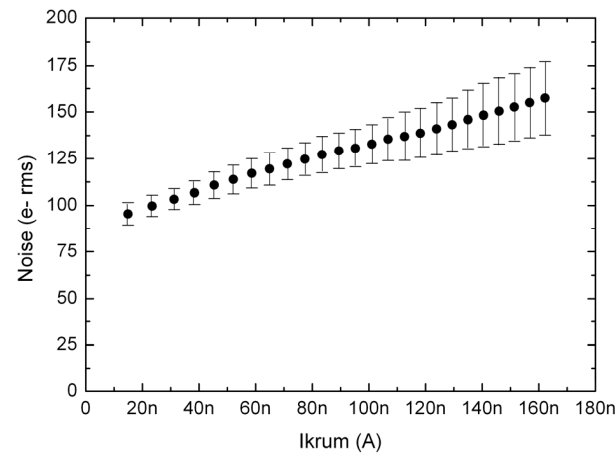
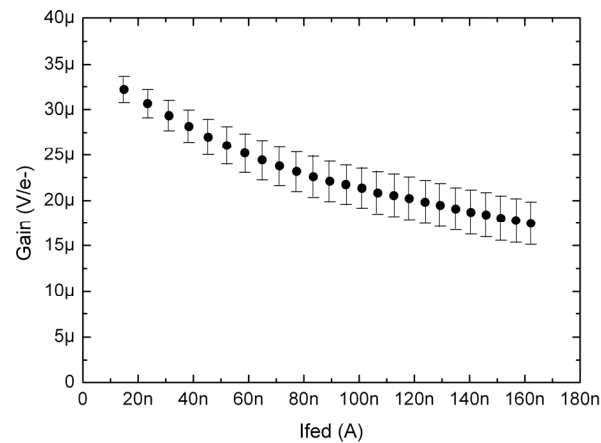
Ikrum current



CSA output – analytical formula



Measurements:



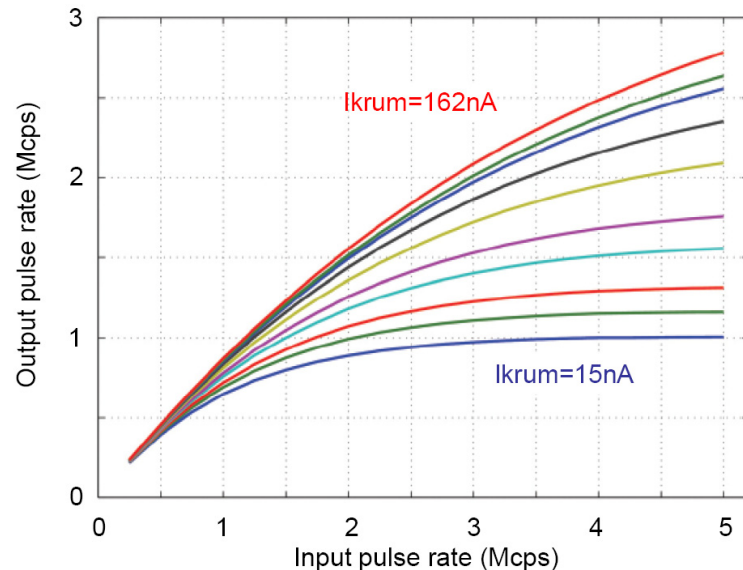
With stud-bonded detector

Low $I_{krum}=15n$
 32.2 $\mu V/e^-$ and 95 e^- rms

High $I_{krum}=162n$
 17.5 $\mu V/e^-$ and 157 e^- rms

Tests for high count rate performance (Cu X-ray tube)

X-ray tube operated at 30 kV applied voltage and the current was changed in the range from 10 mA up 300 mA and Al absorber

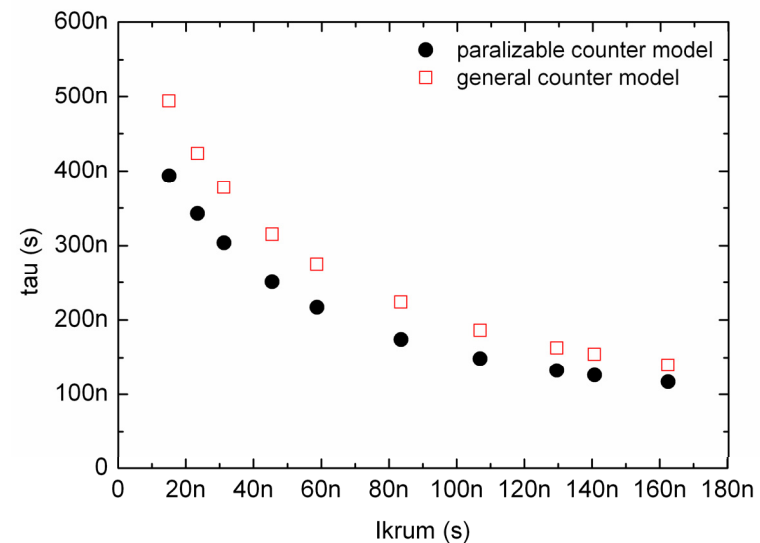


paralyzable counter model

$$m = n \exp(-n \tau_p)$$

generalized dead times model

$$m = \frac{\theta n}{\exp(\theta n \tau) + \theta - 1}$$



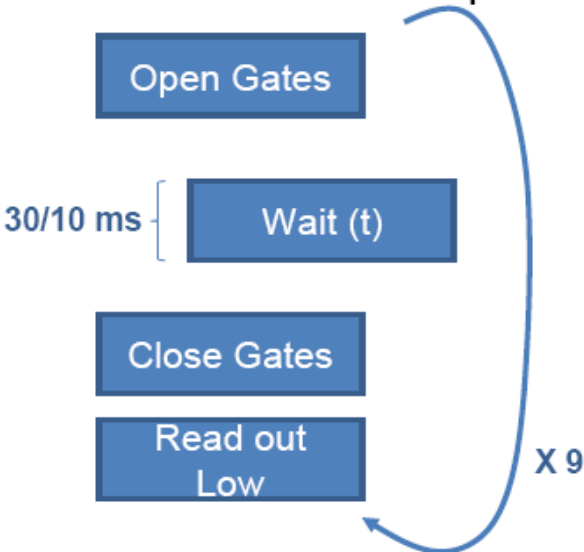
For the highest values of I_{Krum} current

- paralyzable counter model is $\tau_p = 117 \text{ ns}$
(with $sd = 44 \text{ ns}$)

- generalized dead times model is $\tau = 139 \text{ ns}$
(with $sd = 54 \text{ ns}$).

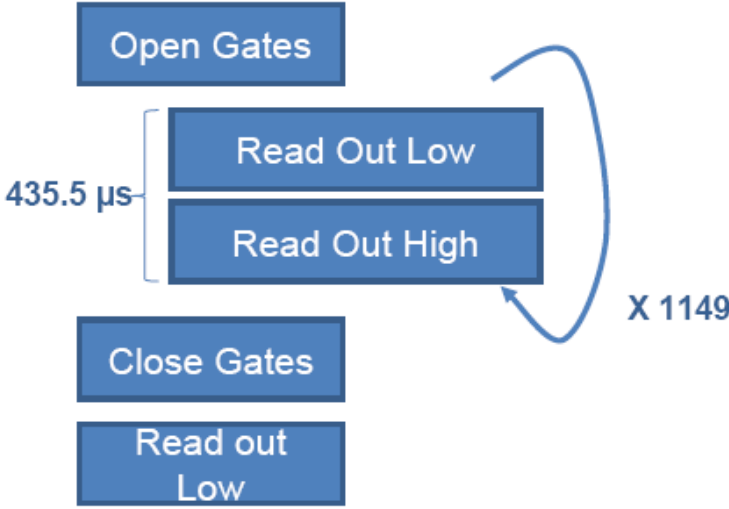
Tests for digital crosstalk in continuous mode of operation

Standard mode of operation

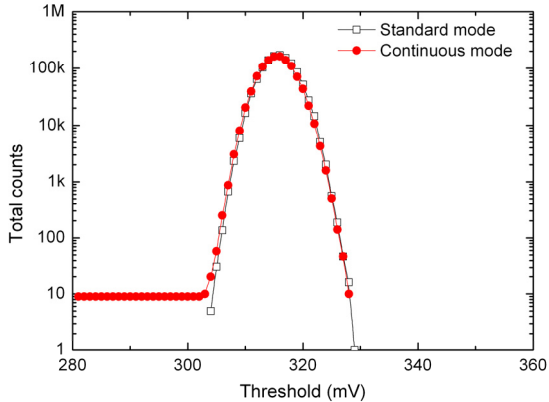
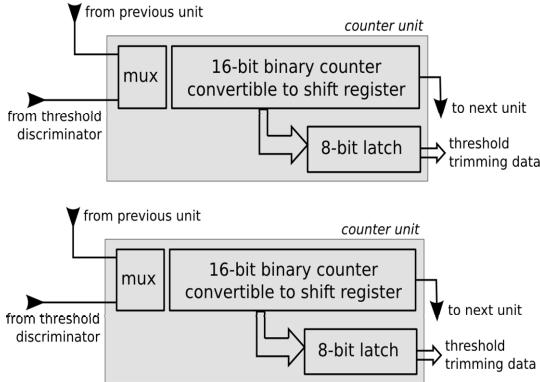


Total waiting time = 0.25 s
 Total waiting time = 8 x 30 ms + 1 x 10 ms

Continuous mode of operation



Total waiting time for High + Low = 0,5004 s
 Total waiting time for Low = 0.2502s



Summary

COMPARISON OF COUNTING PIXEL CHIPS IN SUBMICRON TECHNOLOGY

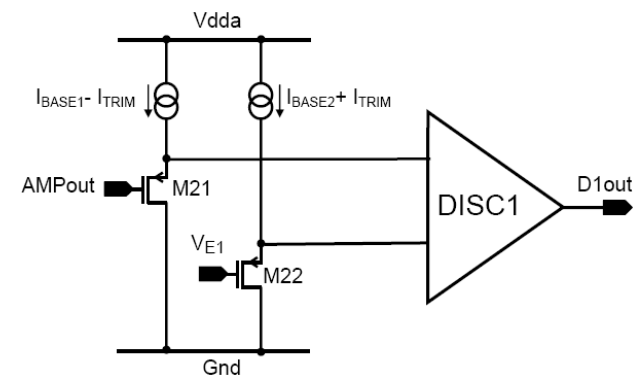
Chip	Medipix II	Pilatus 2	XPAD3S	Eiger	FPDR90 this work
Technology	250 nm	250 nm	250 nm	250 nm	90 nm
Chip area [mm ²]	16.1×14.1	17.5×10.5	17.4×10.4	19.3×20.1	4×4
Pixel matrix	256×256	60×97	80×120	256×256	40×32
Pixel size[μm ²]	55×55	172×172	130×130	75×75	100×100
Power per pixel [μW]	8*	10	40	8.8	42
Noise [e ⁻ rms]	141	123	127	180	106
Offset spread after correction [e ⁻ rms]	–	10	57	20	12
Min. dead time - paralyzable model [ns]	–	125	–**	–**	117
Double threshold	Yes	No	No***	No	Yes
Counters per pixel	1 × 15 bit	1 × 20 bit	1 × 12 bit	1 × 12 bit	2 × 16 bit
Continuous readout	No	No	Yes	Yes	Yes

* only analog part

** count rate in both cases is about a few Mcps/pixel,

***version XPAD3C has double threshold.

1. **Digital functionality / area is really good in 90 nm CMOS**
2. **Noise: 106 el rms**
3. **Effective offset correction – 12 el. rms**
4. **Ikrum control: $\tau_p = 117$ ns**
5. **Continuous readout: no digital crosstalk**
6. **Power reduction per pixel: resize the dimension of correction source follower (total power 42 uW → 22 uW)**



Acknowledgments: prof. P. Fischer for help during stud-bonding and Cadence Academic Network for helpful discussion. This work was supported by the Ministry of Science and Higher Education, Poland